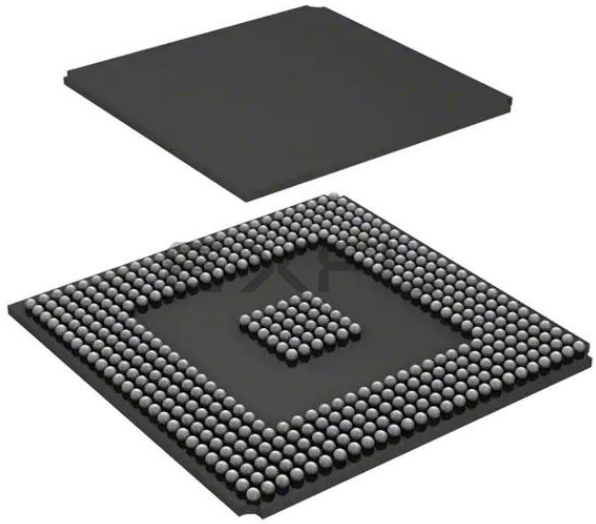

Welcome to E-XFL.COM

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	202752
Number of I/O	356
Number of Gates	1000000
Voltage - Supply	2.3V ~ 2.7V
Mounting Type	Surface Mount
Operating Temperature	-55°C ~ 125°C (TC)
Package / Case	456-BBGA
Supplier Device Package	456-PBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/apa1000-bgg456m

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ProASIC^PLUS Architecture

The proprietary ProASIC^PLUS architecture provides granularity comparable to gate arrays.

The ProASIC^PLUS device core consists of a Sea-of-Tiles (Figure 1-1). Each tile can be configured as a three-input logic function (e.g., NAND gate, D-Flip-Flop, etc.) by programming the appropriate Flash switch interconnections (Figure 1-2 and Figure 1-3 on page 1-3). Tiles and larger functions are connected with any of the four levels of routing hierarchy. Flash switches are distributed throughout the device to provide nonvolatile, reconfigurable interconnect programming. Flash switches are programmed to connect signal lines to the appropriate logic cell inputs and outputs. Dedicated high-performance lines are connected as needed for fast, low-skew global signal distribution throughout the core. Maximum core utilization is possible for virtually any design.

ProASIC^PLUS devices also contain embedded, two-port SRAM blocks with built-in FIFO/RAM control logic. Programming options include synchronous or asynchronous operation, two-port RAM configurations, user defined depth and width, and parity generation or checking. Please see the "Embedded Memory Configurations" section on page 1-23 for more information.

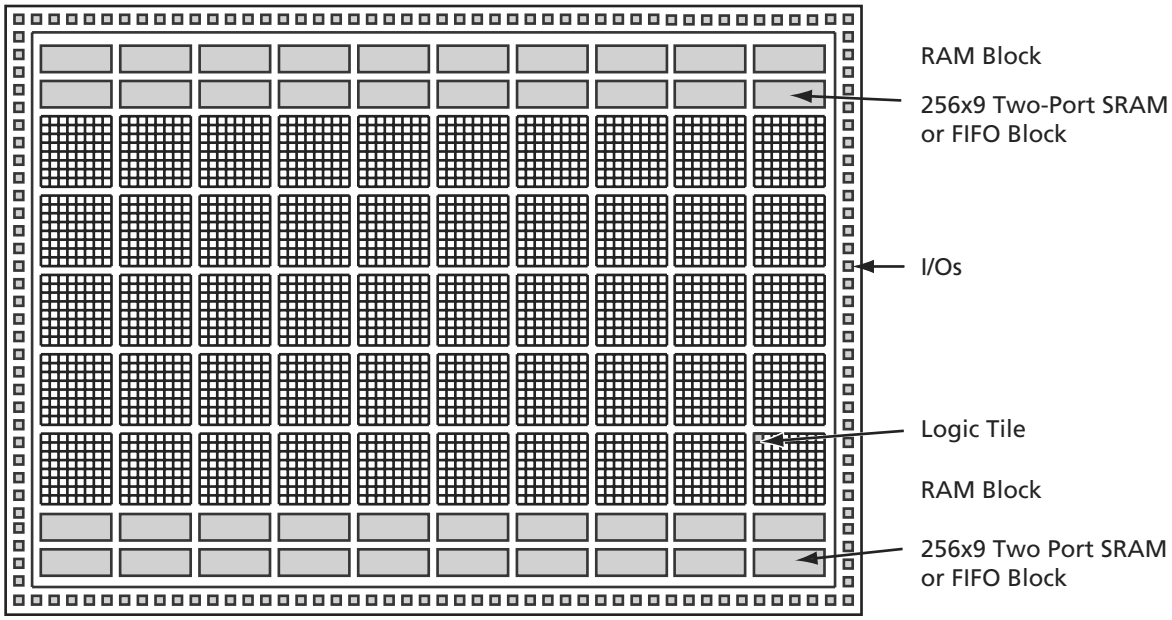


Figure 1-1 • **The ProASIC^PLUS Device Architecture**

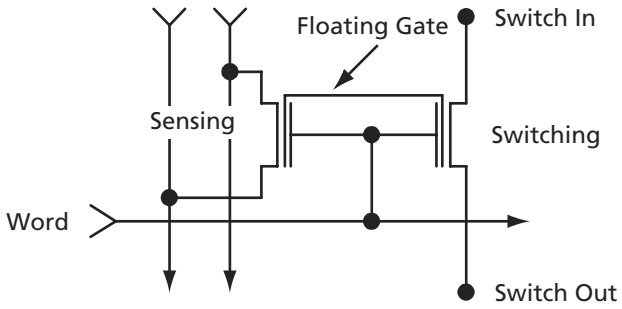


Figure 1-2 • **Flash Switch**

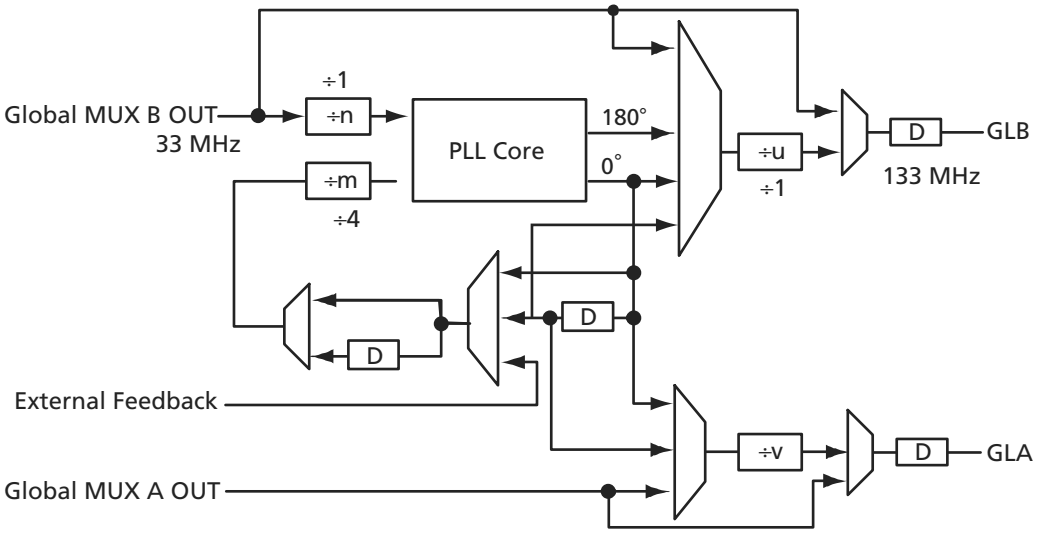


Figure 1-16 • **Using the PLL 33 MHz In, 133 MHz Out**

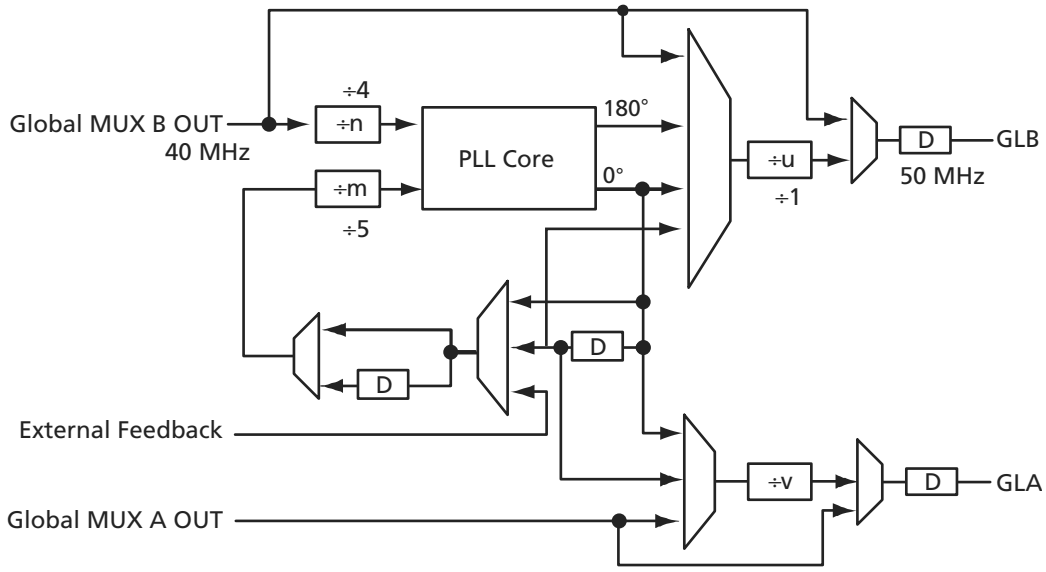


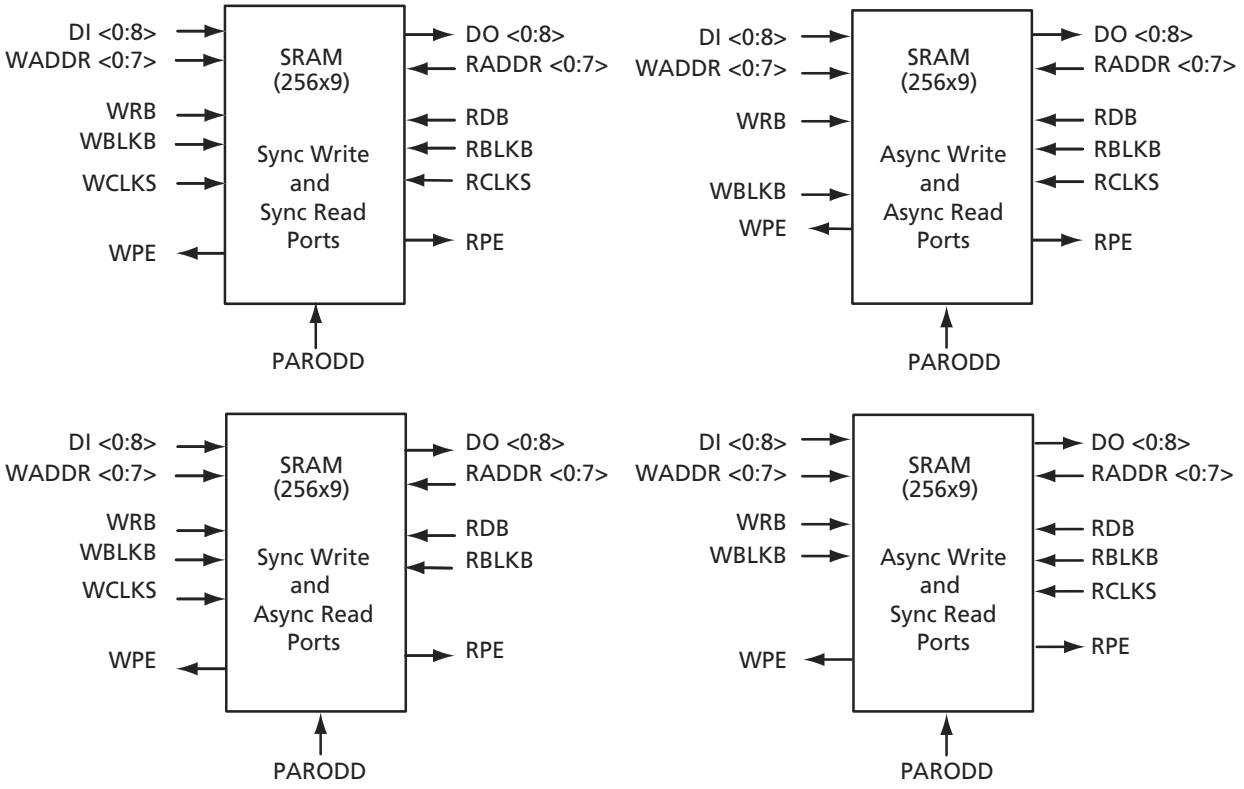
Figure 1-17 • **Using the PLL 40 MHz In, 50 MHz Out**

PLL I/O Constraints

PLL locking is guaranteed only when the following constraints are followed:

Table 1-10 • **PLL I/O Constraints**

	$T_J \leq$ –40°C		Value $T_J >$ –40°C
I/O Type	PLL locking is guaranteed only when using low drive strength and low slew rate I/O. PLL locking may be inconsistent when using high drive strength or high slew rate I/Os		No Constraints
SSO	APA300	Hermetic packages ≤ 8 SSO	With FIN ≤ 180 MHz and outputs switching simultaneously
		Plastic packages ≤ 16 SSO	
	APA600	Hermetic packages ≤ 16 SSO	
		Plastic packages ≤ 32 SSO	
	APA1000	Hermetic packages ≤ 16 SSO	
		Plastic packages ≤ 32 SSO	
	APA300	Hermetic packages ≤ 12 SSO	With FIN ≤ 50 MHz and half outputs switching on positive clock edge, half switching on the negative clock edge no less than 10nsec later
		Plastic packages ≤ 20 SSO	
	APA600	Hermetic packages ≤ 32 SSO	
		Plastic packages ≤ 64 SSO	
	APA1000	Hermetic packages ≤ 32 SSO	
		Plastic packages ≤ 64 SSO	



Note: *Each RAM block contains a multiplexer (called DMUX) for each output signal, increasing design efficiency. These DMUX cells do not consume any core logic tiles and connect directly to high-speed routing resources between the RAM blocks. They are used when RAM blocks are cascaded and are automatically inserted by the software tools.*

Figure 1-21 • **Example SRAM Block Diagrams**

Table 1-14 • **Memory Block SRAM Interface Signals**

SRAM Signal	Bits	In/Out	Description
WCLKS	1	In	Write clock used on synchronization on write side
RCLKS	1	In	Read clock used on synchronization on read side
RADDR<0:7>	8	In	Read address
RBLKB	1	In	Read block select (active Low)
RDB	1	In	Read pulse (active Low)
WADDR<0:7>	8	In	Write address
WBLKB	1	In	Write block select (active Low)
DI<0:8>	9	In	Input data bits <0:8>, <8> can be used for parity In
WRB	1	In	Write pulse (active Low)
DO<0:8>	9	Out	Output data bits <0:8>, <8> can be used for parity Out
RPE	1	Out	Read parity error (active High)
WPE	1	Out	Write parity error (active High)
PARODD	1	In	Selects Odd parity generation/detect when High, Even parity when Low

Note: *Not all signals shown are used in all modes.*

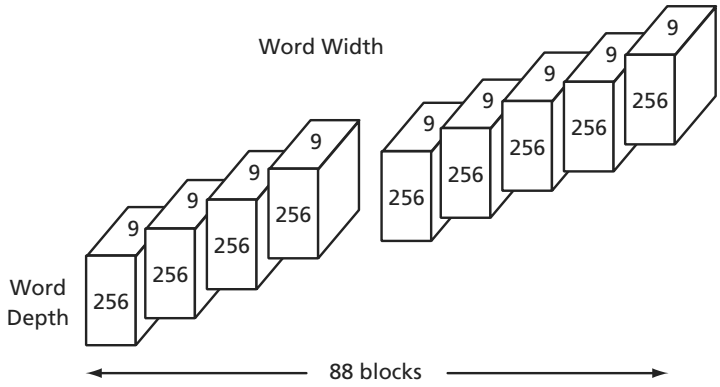


Figure 1-23 • **APA1000 Memory Block Architecture**

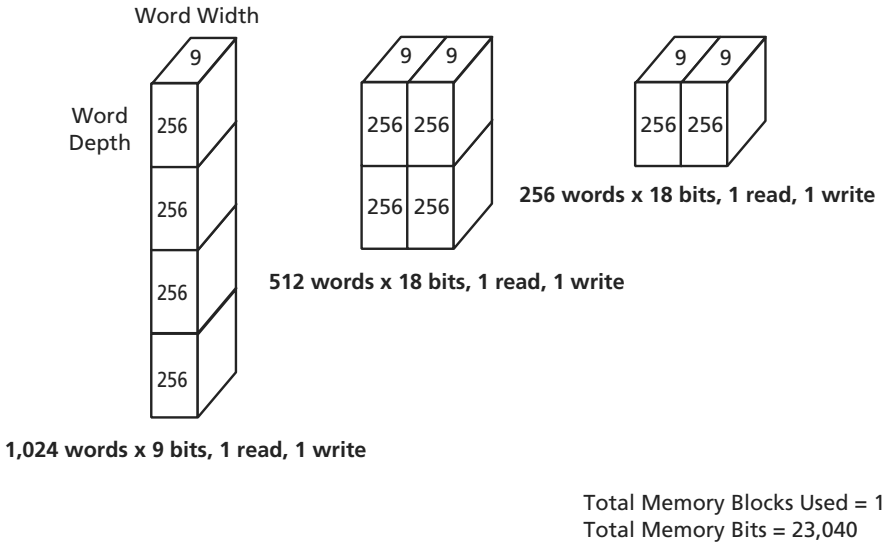


Figure 1-24 • **Example Showing Memory Arrays with Different Widths and Depths**

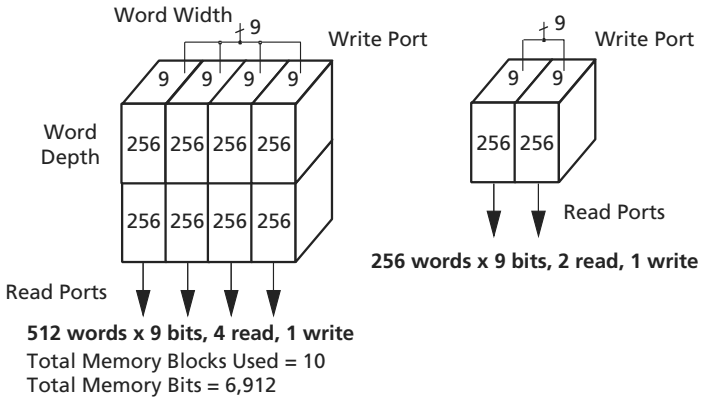


Figure 1-25 • **Multi-Port Memory Usage**

Design Environment

The ProASIC^PLUS family of FPGAs is fully supported by both Actel's Libero® Integrated Design Environment (IDE) and Designer FPGA Development software. Actel Libero IDE is an integrated design manager that seamlessly integrates design tools while guiding the user through the design flow, managing all design and log files, and passing necessary design data among tools. Additionally, Libero IDE allows users to integrate both schematic and HDL synthesis into a single flow and verify the entire design in a single environment (see Actel's website for more information about *Libero IDE*). Libero IDE includes Synplify® AE from Synplicity®, ViewDraw® AE from Mentor Graphics®, Model*Sim*® HDL Simulator from Mentor Graphics, WaveFormer Lite™ AE from SynaptiCAD®, PALACE™ AE Physical Synthesis from Magma, and Designer software from Actel.

PALACE is an effective tool when designing with ProASIC^PLUS. PALACE AE Physical Synthesis from Magma takes an EDIF netlist and optimizes the performance of ProASIC^PLUS devices through a physical placement-driven process, ensuring that timing closure is easily achieved.

Actel's Designer software is a place-and-route tool that provides a comprehensive suite of back-end support tools for FPGA development. The Designer software includes the following:

- Timer – a world-class integrated static timing analyzer and constraints editor that support timing-driven place-and-route
- NetlistViewer – a design netlist schematic viewer
- ChipPlanner – a graphical floorplanner viewer and editor
- SmartPower – allows the designer to quickly estimate the power consumption of a design
- PinEditor – a graphical application for editing pin assignments and I/O attributes
- I/O Attribute Editor – displays all assigned and unassigned I/O macros and their attributes in a spreadsheet format

With the Designer software, a user can lock the design pins before layout while minimally impacting the results of place-and-route. Additionally, Actel's back-annotation flow is compatible with all the major simulators. Another tool included in the Designer software is the SmartGen macro builder, which easily creates popular and commonly used logic functions for implementation into your schematic or HDL design.

Actel's Designer software is compatible with the most popular FPGA design entry and verification tools from EDA vendors, such as Mentor Graphics, Synplicity, Synopsys, and Cadence Design Systems. The Designer software is available for both the Windows and UNIX operating systems.

ISP

The user can generate *.bit or *.stp programming files from the Designer software and can use these files to program a device.

ProASIC^PLUS devices can be programmed in-system. For more information on ISP of ProASIC^PLUS devices, refer to the *In-System Programming ProASIC^PLUS Devices* and *Performing Internal In-System Programming Using Actel's ProASIC^PLUS Devices* application notes. Prior to being programmed for the first time, the ProASIC^PLUS device I/Os are in a tristate condition with the pull-up resistor option enabled.

Package Thermal Characteristics

The ProASIC^PLUS family is available in several package types with a range of pin counts. Actel has selected packages based on high pin count, reliability factors, and superior thermal characteristics.

Thermal resistance defines the ability of a package to conduct heat away from the silicon, through the package to the surrounding air. Junction-to-ambient thermal resistance is measured in degrees Celsius/Watt and is represented as Theta ja (Θ_{ja}). The lower the thermal resistance, the more efficiently a package will dissipate heat.

A package's maximum allowed power (P) is a function of maximum junction temperature (T_J), maximum ambient operating temperature (T_A), and junction-to-ambient thermal resistance Θ_{ja}. Maximum junction temperature is the maximum allowable temperature on the active surface of the IC and is 110° C. P is defined as:

$$P = \frac{T_J - T_A}{\Theta_{ja}}$$

EQ 1-4

Θ_{ja} is a function of the rate (in linear feet per minute (lfpm)) of airflow in contact with the package. When the estimated power consumption exceeds the maximum allowed power, other means of cooling, such as increasing the airflow rate, must be used. The maximum power dissipation allowed for a Military temperature device is specified as a function of Θ_{jc}. The absolute maximum junction temperature is 150°C.

The calculation of the absolute maximum power dissipation allowed for a Military temperature application is illustrated in the following example for a 456-pin PBGA package:

$$\text{Maximum Power Allowed} = \frac{\text{Max. junction temp. (°C)} - \text{Max. case temp. (°C)}}{\theta_{jc}(\text{°C/W})} = \frac{150\text{°C} - 125\text{°C}}{3.0\text{°C/W}} = 8.333\text{W}$$

EQ 1-5

Table 1-16 • **Package Thermal Characteristics**

Plastic Packages	Pin Count	θ_{jc}	θ_{ja} Still Air	θ_{ja} 1.0 m/s 200 ft./min.	θ_{ja} 2.5 m/s 500 ft./min.	Units
Thin Quad Flat Pack (TQFP)	100	14.0	33.5	27.4	25.0	°C/W
Thin Quad Flat Pack (TQFP)	144	11.0	33.5	28.0	25.7	°C/W
Plastic Quad Flat Pack (PQFP)[1]	208	8.0	26.1	22.5	20.8	°C/W
PQFP with Heat spreader[2]	208	3.8	16.2	13.3	11.9	°C/W
Plastic Ball Grid Array (PBGA)	456	3.0	15.6	12.5	11.6	°C/W
Fine Pitch Ball Grid Array (FBGA)	144	3.8	26.9	22.9	21.5	°C/W
Fine Pitch Ball Grid Array (FBGA)	256	3.8	26.6	22.8	21.5	°C/W
Fine Pitch Ball Grid Array (FBGA)[3]	484	3.2	18.0	14.7	13.6	°C/W
Fine Pitch Ball Grid Array (FBGA)[4]	484	3.2	20.5	17.0	15.9	°C/W
Fine Pitch Ball Grid Array (FBGA)	676	3.2	16.4	13.0	12.0	°C/W
Fine Pitch Ball Grid Array (FBGA)	896	2.4	13.6	10.4	9.4	°C/W
Fine Pitch Ball Grid Array (FBGA)	1152	1.8	12.0	8.9	7.9	°C/W
Ceramic Quad Flat Pack (CQFP)	208	2.0	22.0	19.8	18.0	°C/W
Ceramic Quad Flat Pack (CQFP)	352	2.0	17.9	16.1	14.7	°C/W
Ceramic Column Grid Array (CCGA/LGA)	624	6.5	8.9	8.5	8.0	°C/W

Notes:

1. *Valid for the following devices irrespective of temperature grade: APA075, APA150, and APA300*
2. *Valid for the following devices irrespective of temperature grade: APA450, APA600, APA750, and APA1000*
3. *Depopulated Array*
4. *Full array*

Calculating Typical Power Dissipation

ProASIC^PLUS device power is calculated with both a static and an active component. The active component is a function of both the number of tiles utilized and the system speed. Power dissipation can be calculated using the following formula:

Total Power Consumption—P_{total}

$P_{total} = P_{dc} + P_{ac}$

where:

P_{dc} = 7 mW for the APA075
8 mW for the APA150
11 mW for the APA300
12 mW for the APA450
12 mW for the APA600
13 mW for the APA750
19 mW for the APA1000
P_{dc} includes the static components of $P_{VDDP} + P_{VDD} + P_{AVDD}$

P_{ac} = $P_{clock} + P_{storage} + P_{logic} + P_{outputs} + P_{inputs} + P_{pll} + P_{memory}$

Global Clock Contribution—P_{clock}

P_{clock}, the clock component of power dissipation, is given by the piece-wise model:

for R < 15000 the model is: (P1 + (P2*R) - (P7*R2)) * Fs (lightly-loaded clock trees)

for R > 15000 the model is: (P10 + P11*R) * Fs (heavily-loaded clock trees)

where:

P1 = 100 µW/MHz is the basic power consumption of the clock tree per MHz of the clock

P2 = 1.3 µW/MHz is the incremental power consumption of the clock tree per storage tile – also per MHz of the clock

P7 = 0.00003 µW/MHz is a correction factor for partially-loaded clock trees

P10 = 6850 µW/MHz is the basic power consumption of the clock tree per MHz of the clock

P11 = 0.4 µW/MHz is the incremental power consumption of the clock tree per storage tile – also per MHz of the clock

R = the number of storage tiles clocked by this clock

Fs = the clock frequency

Storage-Tile Contribution—$P_{storage}$

$P_{storage}$, the storage-tile (Register) component of AC power dissipation, is given by

$P_{storage} = P5 * ms * Fs$

where:

P5 = 1.1 µW/MHz is the average power consumption of a storage tile per MHz of its output toggling rate. The maximum output toggling rate is Fs/2.

ms = the number of storage tiles (Register) switching during each Fs cycle

Fs = the clock frequency

The following is an APA750 example using a shift register design with 13,440 storage tiles (Register) and 0 logic tiles. This design has one clock at 10 MHz, and 24 outputs toggling at 5 MHz. We then calculate the various components as follows:

P_{clock}

Fs = 10 MHz

R = 13,440

=> $P_{clock} = (P1 + (P2*R) - (P7*R^2)) * Fs = 121.5$ mW

$P_{storage}$

ms = 13,440 (in a shift register 100% of storage tiles are toggling at each clock cycle and Fs = 10 MHz)

=> $P_{storage} = P5 * ms * Fs = 147.8$ mW

P_{logic}

mc = 0 (no logic tiles in this shift register)

=> $P_{logic} = 0$ mW

$P_{outputs}$

C_{load} = 40 pF

V_{DDP} = 3.3 V

p = 24

Fp = 5 MHz

=> $P_{outputs} = (P4 + (C_{load} * V_{DDP}^2)) * p * Fp = 91.4$ mW

P_{inputs}

q = 1

Fq = 10 MHz

=> $P_{inputs} = P8 * q * Fq = 0.3$ mW

P_{memory}

N_{memory} = 0 (no RAM/FIFO blocks in this shift register)

=> $P_{memory} = 0$ mW

P_{ac}

=> 361 mW

P_{total}

$P_{dc} + P_{ac} = 374$ mW (typical)

Operating Conditions

Standard and –F parts are the same unless otherwise noted. All –F parts are only available as commercial.

Table 1-17 • **Absolute Maximum Ratings***

Parameter	Condition	Minimum	Maximum	Units
Supply Voltage Core (V_{DD})		–0.3	3.0	V
Supply Voltage I/O Ring (V_{DDP})		–0.3	4.0	V
DC Input Voltage		–0.3	V_{DDP} + 0.3	V
PCI DC Input Voltage		–1.0	V_{DDP} + 1.0	V
PCI DC Input Clamp Current (absolute)	V_{IN} < –1 or V_{IN} = V_{DDP} + 1 V	10		mA
LVPECL Input Voltage		–0.3	V_{DDP} + 0.5	V
GND		0	0	V

Note: **Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. Devices should not be operated outside the Recommended Operating Conditions.*

Table 1-18 • **Programming, Storage, and Operating Limits**

			Storage Temperature		Operating
Product Grade	Programming Cycles (min.)	Program Retention (min.)	Min.	Max.	T_J Max. Junction Temperature
Commercial	500	20 years	–55°C	110°C	110°C
Industrial	500	20 years	–55°C	110°C	110°C
Military	100	Refer to Table 1-19 on page 1-35	–65°C	150°C	150°C
MIL-STD-883	100	Refer to Table 1-19 on page 1-35	–65°C	150°C	150°C

Performance Retention

For devices operated and stored at 110°C or less, the performance retention period is 20 years after programming. For devices operated and stored at temperatures greater than 110°C, refer to Table 1-19 on page 1-35 to determine the performance retention period. Actel does not guarantee performance if the performance retention period is exceeded. Designers can determine the performance retention period from the following table.

Evaluate the percentage of time spent at the highest temperature, then determine the next highest temperature to which the device will be exposed. In Table 1-19 on page 1-35, find the temperature profile that most closely matches the application.

Example – the ambient temperature of a system cycles between 100°C (25% of the time) and 50°C (75% of the time). No forced ventilation cooling system is in use. An APA600-PQ208M FPGA operates in the system, dissipating 1 W. The package thermal resistance (junction-to-ambient) in still air Θ_{ja} is 20°C/W, indicating that the junction temperature of the FPGA will be 120°C (25% of the time) and 70°C (75% of the time). The entry in Table 1-19 on page 1-35, which most closely matches the application, is 25% at 125°C with 75% at 110°C. Performance retention in this example is at least 16.0 years.

Note that exceeding the stated retention period may result in a performance degradation in the FPGA below the worst-case performance indicated in the Actel Timer. To ensure that performance does not degrade below the worst-case values in the Actel Timer, the FPGA must be reprogrammed within the performance retention period. In addition, note that performance retention is independent of whether or not the FPGA is operating. The retention period of a device in storage at a given temperature will be the same as the retention period of a device operating at that junction temperature.

Table 1-24 • **DC Electrical Specifications (V_{DDP} = 3.3 V ±0.3 V and V_{DD} = 2.5 V ±0.2 V) Applies to Military Temperature and MIL-STD-883B Temperature Only**

Symbol	Parameter	Conditions		Military/MIL-STD-883B[1] Min.	Typ.	Max.	Units
V_{OH}	Output High Voltage 3.3 V I/O, High Drive, High Slew (OB33PH) 3.3V I/O, High Drive, Normal/ Low Slew (OB33PN/OB33PL) 3.3 V I/O, Low Drive , High/ Normal/Low Slew (OB33LH/ OB33LN/OB33LL)	 I_{OH} = –8 mA I_{OH} = –16 mA I_{OH} = –3mA I_{OH} = –8mA I_{OH} = –3 mA I_{OH} = –8 mA		 0.9*V_{DDP} 2.4 0.9*V_{DDP} 2.4 0.9*V_{DDP} 2.4			V
V_{OL}	Output Low Voltage 3.3 V I/O, High Drive, High Slew (OB33PH) 3.3V I/O, High Drive, Normal/ Low Slew (OB33PN/OB33PL)) 3.3 V I/O, Low Drive, High/ Normal/Low Slew (OB33LH/ OB33LN/OB33LL)	 I_{OL} = 12 mA I_{OL} = 17 mA I_{OL} = 28 mA I_{OL} = 4 mA I_{OL} = 6 mA I_{OL} = 13 mA I_{OL} = 4 mA I_{OL} = 6 mA I_{OL} = 13 mA				 0.1V_{DDP} 0.4 0.7 0.1V_{DDP} 0.4 0.7 0.1V_{DDP} 0.4 0.7	V
V_{IH}[4]	Input High Voltage 3.3 V Schmitt Trigger Inputs 3.3 V LVTTL/LVCMOS 2.5 V Mode			1.6 2 1.7		V_{DDP} + 0.3 V_{DDP} + 0.3 V_{DDP} + 0.3	V
V_{IL}[5]	Input Low Voltage 3.3 V Schmitt Trigger Inputs 3.3 V LVTTL/LVCMOS 2.5 V Mode			–0.3 –0.3 –0.3		0.7 0.8 0.7	V
$R_{WEAKPULLUP}$	Weak Pull-up Resistance (IOB33U)	$V_{IN} \geq$ 1.5 V		7		43	kΩ
$R_{WEAKPULLUP}$	Weak Pull-up Resistance (IOB25U)	$V_{IN} \geq$ 1.5 V		7		43	kΩ
I_{IN}	Input Current	with pull up (V_{IN} = GND)		–300		–40	µA
		without pull up (V_{IN} = GND or V_{DD})		–10		10	µA
I_{DDQ}	Quiescent Supply Current (standby) Commercial	V_{IN} = GND[2] or V_{DD}	Std.		5.0	15	mA
			–F		5.0	25	mA

Notes:

1. *All process conditions. Military Temperature / MIL-STD-883 Class B: Junction Temperature: –55 to +125°C.*
2. *No pull-up resistor required.*
3. *This will not exceed 2 mA total per device.*
4. *During transitions, the input signal may overshoot to V_{DDP}+1.0 V for a limited time of no larger than 10% of the duty cycle.*
5. *During transitions, the input signal may undershoot to –1.0 V for a limited time of no larger than 10% of the duty cycle.*

Table 1-24 • **DC Electrical Specifications (V_{DDP} = 3.3 V ±0.3 V and V_{DD} = 2.5 V ±0.2 V) (Continued)**
Applies to Military Temperature and MIL-STD-883B Temperature Only

Symbol	Parameter	Conditions		Military/MIL-STD-883B[1] Min.	Typ.	Max.	Units
I_{DDQ}	Quiescent Supply Current (standby) Industrial	V_{IN} = GND[2] or V_{DD}	Std.		5.0	20	mA
I_{DDQ}	Quiescent Supply Current (standby) Military	V_{IN} = GND[2] or V_{DD}	Std.		5.0	25	mA
I_{OZ}	Tristate Output Leakage Current	V_{OH} = GND or V_{DD}	Std.	–10		10	µA
			–F[3]	–10		100	µA
I_{OSH}	Output Short Circuit Current High 3.3 V High Drive (OB33P) 3.3 V Low Drive (OB33L)	 V_{IN} = GND V_{IN} = GND		 –200 –100			
I_{OSL}	Output Short Circuit Current Low 3.3 V High Drive 3.3 V Low Drive	 V_{IN} = V_{DD} V_{IN} = V_{DD}				 200 100	
$C_{I/O}$	I/O Pad Capacitance					10	pF
C_{CLK}	Clock Input Pad Capacitance					10	pF

Notes:

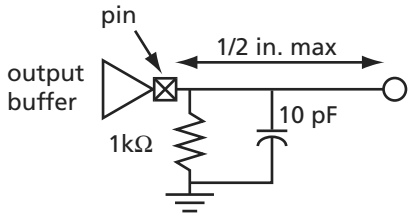
1. *All process conditions. Military Temperature / MIL-STD-883 Class B: Junction Temperature: –55 to +125°C.*
2. *No pull-up resistor required.*
3. *This will not exceed 2 mA total per device.*
4. *During transitions, the input signal may overshoot to V_{DDP} +1.0 V for a limited time of no larger than 10% of the duty cycle.*
5. *During transitions, the input signal may undershoot to –1.0 V for a limited time of no larger than 10% of the duty cycle.*

Table 1-26 • **AC Specifications (3.3 V PCI Revision 2.2 Operation)**

Symbol	Parameter	Condition	Commercial/Industrial/Military/MIL-STD- 883		Units
			Min.	Max.	
$I_{OH(AC)}$	Switching Current High	$0 < V_{OUT} \le 0.3V_{DDP}$*	$-12V_{DDP}$		mA
		$0.3V_{DDP} \le V_{OUT} < 0.9V_{DDP}$*	$(-17.1 + (V_{DDP} - V_{OUT}))$		mA
		$0.7V_{DDP} < V_{OUT} < V_{DDP}$*		See equation C – page 124 of the PCI Specification document rev. 2.2	
	(Test Point)	$V_{OUT} = 0.7V_{DDP}$*		$-32V_{DDP}$	mA
$I_{OL(AC)}$	Switching Current Low	$V_{DDP} > V_{OUT} \ge 0.6V_{DDP}$*	$16V_{DDP}$		mA
		$0.6V_{DDP} > V_{OUT} > 0.1V_{DDP}$ [1]	$(26.7V_{OUT})$		mA
		$0.18V_{DDP} > V_{OUT} > 0$*		See equation D – page 124 of the PCI Specification document rev. 2.2	
	(Test Point)	$V_{OUT} = 0.18V_{DDP}$		$38V_{DDP}$	mA
I_{CL}	Low Clamp Current	$-3 < V_{IN} \le -1$	$-25 + (V_{IN} + 1)/0.015$		mA
I_{CH}	High Clamp Current	$V_{DDP} + 4 > V_{IN} \ge V_{DDP} + 1$	$25 + (V_{IN} - V_{DDP} - 1)/0.015$		mA
$slew_R$	Output Rise Slew Rate	$0.2V_{DDP}$ to $0.6V_{DDP}$ load*	1	4	V/ns
$slew_F$	Output Fall Slew Rate	$0.6V_{DDP}$ to $0.2V_{DDP}$ load*	1	4	V/ns

Note: ** Refer to the PCI Specification document rev. 2.2.*

Pad Loading Applicable to the Rising Edge PCI



Pad Loading Applicable to the Falling Edge PCI

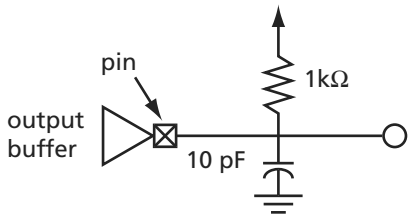


Table 1-37 • **Worst-Case Military Conditions**
V_{DDP} = 3.0V, V_{DD} = 2.3V, T_J = 125°C for Military/MIL-STD-883

Macro Type	Description	Max. t_{INYH}[1]	Max. t_{INYL}[2]	Units
		Std.	Std.	
IB33	3.3V, CMOS Input Levels[3], No Pull-up Resistor	0.5	0.6	ns
IB33S	3.3V, CMOS Input Levels[3], No Pull-up Resistor, Schmitt Trigger	0.6	0.8	ns

Notes:

1. *t_{INYH} = Input Pad-to-Y High*
2. *t_{INYL} = Input Pad-to-Y Low*
3. *LVTTL delays are the same as CMOS delays.*
4. *For LP Macros, V_{DDP}=2.3V for delays.*

Table 1-38 • **Worst-Case Military Conditions**
V_{DDP} = 2.3V, V_{DD} = 2.3V, T_J = 125°C for Military/MIL-STD-883

Macro Type	Description	Max. t_{INYH}[1]	Max. t_{INYL}[2]	Units
		Std.	Std.	
IB25LP	2.5V, CMOS Input Levels[3], Low Power	0.9	0.7	ns
IB25LPS	2.5V, CMOS Input Levels[3], Low Power, Schmitt Trigger	0.8	1.0	ns

Notes:

1. *t_{INYH} = Input Pad-to-Y High*
2. *t_{INYL} = Input Pad-to-Y Low*
3. *LVTTL delays are the same as CMOS delays.*
4. *For LP Macros, V_{DDP}=2.3V for delays.*

Table 1-50 • **JTAG Switching Characteristics**

Description	Symbol	Min	Max	Unit
Output delay from TCK falling to TDI, TMS	t_{TCKTDI}	–4	4	ns
TDO Setup time before TCK rising	t_{TDOTCK}	10		ns
TDO Hold time after TCK rising	t_{TCKTDO}	0		ns
TCK period	t_{TCK}	100 [2]	1,000	ns
RCK period	t_{RCK}	100	1,000	ns

Notes:

1. *For DC electrical specifications of the JTAG pins (TCK, TDI, TMS, TDO, TRST), refer to Table 1-22 on page 1-37 when V_{DDP} = 2.5 V and Table 1-24 on page 1-41 when V_{DDP} = 3.3 V.*
2. *If RCK is being used, there is no minimum on the TCK period.*

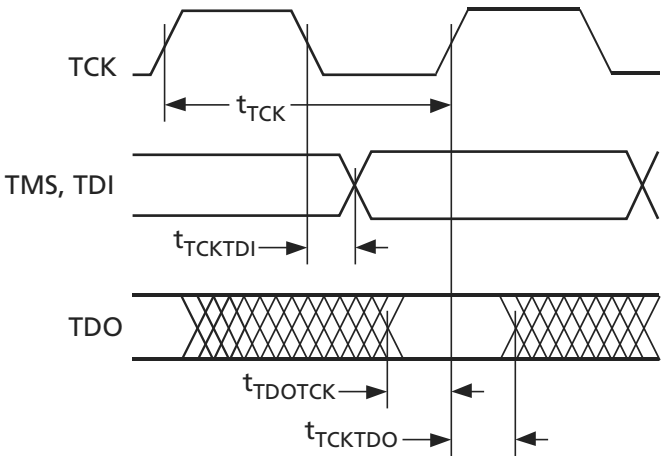


Figure 1-30 • **JTAG Operation Timing**

Embedded Memory Specifications

This section discusses ProASIC^PLUS SRAM/FIFO embedded memory and its interface signals, including timing diagrams that show the relationships of signals as they pertain to single embedded memory blocks (Table 1-51). Table 1-13 on page 1-24 shows basic SRAM and FIFO configurations. Simultaneous read and write to the same location must be done with care. On such accesses the DI bus is output to the DO bus. Refer to the *ProASIC^PLUS RAM and FIFO Blocks* application note for more information.

Enclosed Timing Diagrams—SRAM Mode:

- "Synchronous SRAM Read, Access Timed Output Strobe (Synchronous Transparent)" section on page 1-58
- "Synchronous SRAM Read, Pipeline Mode Outputs (Synchronous Pipelined)" section on page 1-59
- "Asynchronous SRAM Write" section on page 1-60
- "Asynchronous SRAM Read, Address Controlled, RDB=0" section on page 1-61
- "Asynchronous SRAM Read, RDB Controlled" section on page 1-62
- "Synchronous SRAM Write"
- Embedded Memory Specifications

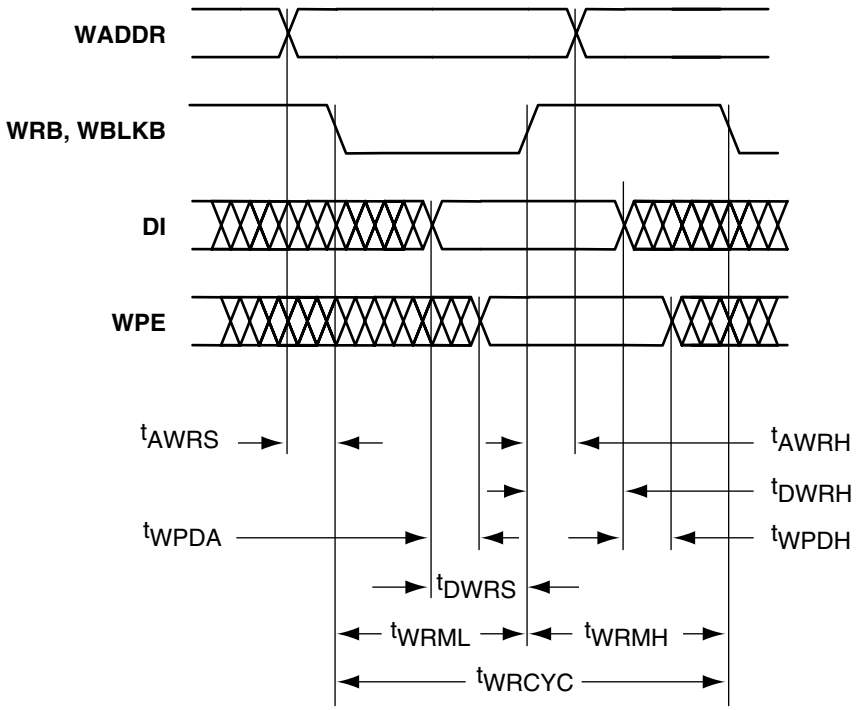
The difference between synchronous transparent and pipeline modes is the timing of all the output signals from the memory. In transparent mode, the outputs will change within the same clock cycle to reflect the data requested by the currently valid access to the memory. If clock cycles are short (high clock speed), the data requires most of the clock cycle to change to valid values (stable signals). Processing of this data in the same clock cycle is nearly impossible. Most designers add registers at all outputs of the memory to push the data processing into the next clock cycle. An entire clock cycle can then be used to process the data. To simplify use of this memory setup, suitable registers have been implemented as part of the memory primitive and are available to the user in the synchronous pipeline mode. In this mode, the output signals will change shortly after the second rising edge, following the initiation of the read access.

Table 1-51 • **Memory Block SRAM Interface Signals**

SRAM Signal	Bits	In/Out	Description
WCLKS	1	In	Write clock used on synchronization on write side
RCLKS	1	In	Read clock used on synchronization on read side
RADDR<0:7>	8	In	Read address
RBLKB	1	In	True read block select (active Low)
RDB	1	In	True read pulse (active Low)
WADDR<0:7>	8	In	Write address
WBLKB	1	In	Write block select (active Low)
DI<0:8>	9	In	Input data bits <0:8>, <8> can be used for parity In
WRB	1	In	Negative true write pulse
DO<0:8>	9	Out	Output data bits <0:8>, <8> can be used for parity Out
RPE	1	Out	Read parity error (active High)
WPE	1	Out	Write parity error (active High)
PARODD	1	In	Selects Odd parity generation/detect when high, Even when low

Note: *Not all signals shown are used in all modes.*

Asynchronous SRAM Write



Note: *The plot shows the normal operation status.*

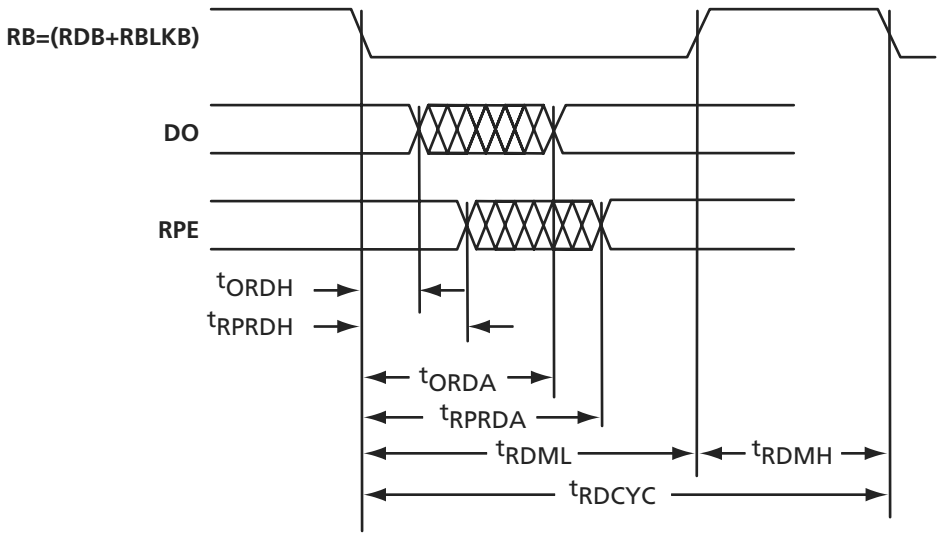
Figure 1-33 • **Asynchronous SRAM Write**

Table 1-54 • **T_J = 0°C to 110°C; V_{DD} = 2.3 V to 2.7 V for Commercial/industrial**
T_J = –55°C to 150°C, V_{DD} = 2.3 V to 2.7 V for Military/MIL-STD-883B

Symbol t_{xxx}	Description	Min.	Max.	Units	Notes
AWRH	WADDR hold from WB ↑	1.0		ns	
AWRS	WADDR setup to WB ↓	0.5		ns	
DWRH	DI hold from WB ↑	1.5		ns	
DWRS	DI setup to WB ↑	0.5		ns	PARGEN is inactive.
DWRS	DI setup to WB ↑	2.5		ns	PARGEN is active.
WPDA	WPE access from DI	3.0		ns	WPE is invalid, while PARGEN is active.
WPDH	WPE hold from DI		1.0	ns	
WRCYC	Cycle time	7.5		ns	
WRMH	WB high phase	3.0		ns	Inactive
WRML	WB low phase	3.0		ns	Active

Note: *All –F speed grade devices are 20% slower than the standard numbers.*

Asynchronous SRAM Read, RDB Controlled



Note: *The plot shows the normal operation status.*

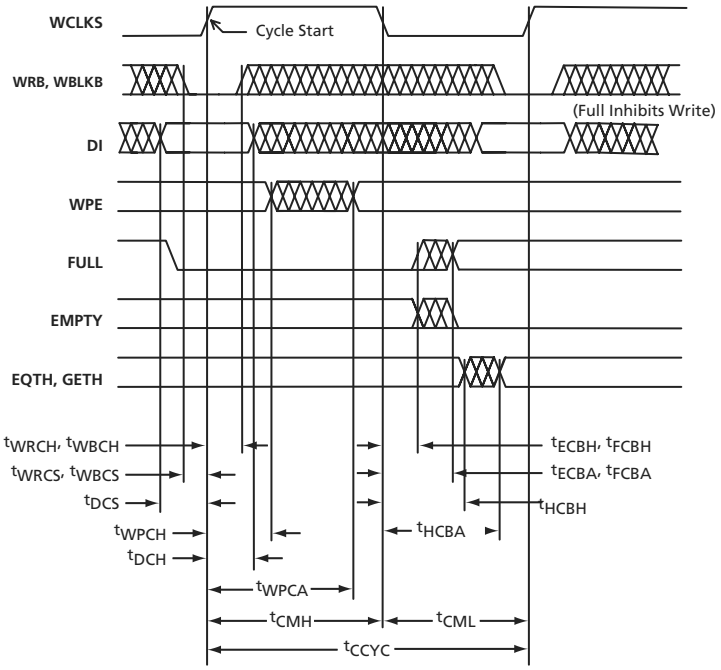
Figure 1-35 • **Asynchronous SRAM Read, RDB Controlled**

Table 1-56 • **T_J = 0°C to 110°C; V_{DD} = 2.3 V to 2.7 V for Commercial/industrial**
T_J = –55°C to 150°C, V_{DD} = 2.3 V to 2.7 V for Military/MIL-STD-883

Symbol t_{xxx}	Description	Min.	Max.	Units	Notes
ORDA	New DO access from RB ↓	7.5		ns	
ORDH	Old DO valid from RB ↓		3.0	ns	
RDCYC	Read cycle time	7.5		ns	
RDMH	RB high phase	3.0		ns	Inactive setup to new cycle
RDML	RB low phase	3.0		ns	Active
RPRDA	New RPE access from RB ↓	9.5		ns	
RPRDH	Old RPE valid from RB ↓		3.0	ns	

Note: *All –F speed grade devices are 20% slower than the standard numbers.*

Synchronous FIFO Write



Note: *The plot shows the normal operation status.*

Figure 1-47 • **Synchronous FIFO Write**

Table 1-67 • **T_J = 0°C to 110°C; V_{DD} = 2.3 V to 2.7 V for Commercial/industrial**
T_J = –55°C to 150°C, V_{DD} = 2.3 V to 2.7 V for Military/MIL-STD-883

Symbol t_{xxx}	Description	Min.	Max.	Units	Notes
CCYC	Cycle time	7.5		ns	
CMH	Clock high phase	3.0		ns	
CML	Clock low phase	3.0		ns	
DCH	DI hold from WCLKS ↑	0.5		ns	
DCS	DI setup to WCLKS ↑	1.0		ns	
FCBA	New FULL access from WCLKS ↓	3.0[1]		ns	
ECBA	EMPTY↓ access from WCLKS ↓	3.0[1]		ns	
ECBH, FCBH, HCBH	Old EMPTY, FULL, EQTH, & GETH valid hold time from WCLKS ↓		1.0	ns	Empty/full/thresh are invalid from the end of hold until the new access is complete
HCBA	EQTH or GETH access from WCLKS ↓	4.5		ns	
WPCA	New WPE access from WCLKS ↑	3.0		ns	WPE is invalid, while PARGEN is active
WPCH	Old WPE valid from WCLKS ↑		0.5	ns	
WRCH, WBCH	WRB & WBLKB hold from WCLKS ↑	0.5		ns	
WRCS, WBCS	WRB & WBLKB setup to WCLKS ↑	1.0		ns	

Notes:

1. *At fast cycles, ECBA and FCBA = MAX (7.5 ns – CMH), 3.0 ns.*
2. *All –F speed grade devices are 20% slower than the standard numbers.*