Microchip Technology - APA1000-PQG208M Datasheet

Welcome to **E-XFL.COM**

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	202752
Number of I/O	158
Number of Gates	1000000
Voltage - Supply	2.3V ~ 2.7V
Mounting Type	Surface Mount
Operating Temperature	-55°C ~ 125°C (TC)
Package / Case	208-BFQFP
Supplier Device Package	208-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/apa1000-pqg208m

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

General Description

The ProASIC$^{\underline{PLUS}}$ family of devices, Actel's second-generation Flash FPGAs, offers enhanced performance over Actel's ProASIC family. It combines the advantages of ASICs with the benefits of programmable devices through nonvolatile Flash technology. This enables engineers to create high-density systems using existing ASIC or FPGA design flows and tools. In addition, the ProASIC$^{\underline{PLUS}}$ family offers a unique clock conditioning circuit based on two on-board phase-locked loops (PLLs). The family offers up to one million system gates, supported with up to 198 kbits of two-port SRAM and up to 712 user I/Os, all providing 50 MHz PCI performance.

Advantages to the designer extend beyond performance. Unlike SRAM-based FPGAs, four levels of routing hierarchy simplify routing, while the use of Flash technology allows all functionality to be live at power-up. No external boot PROM is required to support device programming. While on-board security mechanisms prevent access to the program information, reprogramming can be performed in-system to support future design iterations and field upgrades. The device's architecture mitigates the complexity of ASIC migration at higher user volume. This makes ProASIC$^{\underline{PLUS}}$ a cost-effective solution for applications in the networking, communications, computing, and avionics markets.

The ProASIC$^{\underline{PLUS}}$ family achieves its nonvolatility and reprogrammability through an advanced Flash-based 0.22 μm LVCMOS process with four layers of metal. Standard CMOS design techniques are used to implement logic and control functions, including the PLLs and LVPECL inputs. This results in predictable performance compatible with gate arrays.

The ProASIC$^{\underline{PLUS}}$ architecture provides granularity comparable to gate arrays. The device core consists of a Sea-of-Tiles^{TM}. Each tile can be configured as a flip-flop, latch, or three-input/one-output logic function by programming the appropriate Flash switches. The combination of fine granularity, flexible routing resources, and abundant Flash switches allow 100% utilization and over 95% routability for highly congested designs. Tiles and larger functions are interconnected through a four-level routing hierarchy.

Embedded two-port SRAM blocks with built-in FIFO/RAM control logic can have user-defined depths and widths. Users can also select programming for synchronous or asynchronous operation, as well as parity generations or checking.

The unique clock conditioning circuitry in each device includes two clock conditioning blocks. Each block provides a PLL core, delay lines, phase shifts (0° and 180°), and clock multipliers/dividers, as well as the circuitry needed to provide bidirectional access to the PLL. The PLL block contains four programmable frequency dividers which allow the incoming clock signal to be divided by a wide range of factors from 1 to 64. The clock conditioning circuit also delays or advances the incoming reference clock up to 8 ns (in increments of 0.25 ns). The PLL can be configured internally or externally during operation without redesigning or reprogramming the part. In addition to the PLL, there are two LVPECL differential input pairs to accommodate high-speed clock and data inputs.

To support customer needs for more comprehensive, lower-cost, board-level testing, Actel's ProASIC$^{\underline{PLUS}}$ devices are fully compatible with IEEE Standard 1149.1 for test access port and boundary-scan test architecture. For more information concerning the Flash FPGA implementation, please refer to the "Boundary Scan (JTAG)" section on page 1-11.

ProASIC$^{\underline{PLUS}}$ devices are available in a variety of high-performance plastic packages. Those packages and the performance features discussed above are described in more detail in the following sections.

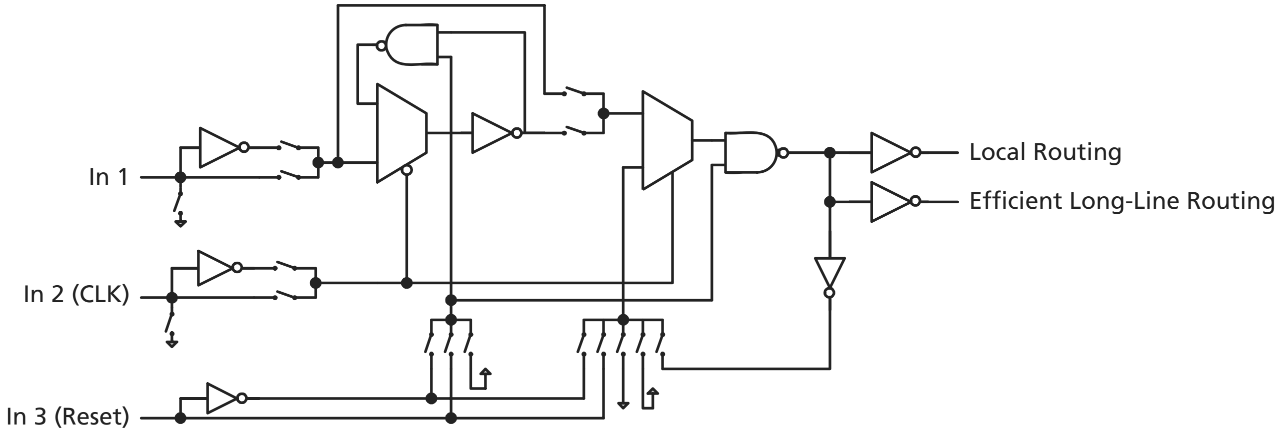


Figure 1-3 • **Core Logic Tile**

Live at Power-Up

The Actel Flash-based ProASIC$^{\underline{\text{PLUS}}}$ devices support Level 0 of the live at power-up (LAPU) classification standard. This feature helps in system component initialization, executing critical tasks before the processor wakes up, setting up and configuring memory blocks, clock generation, and bus activity management. The LAPU feature of Flash-based ProASIC$^{\underline{\text{PLUS}}}$ devices greatly simplifies total system design and reduces total system cost, often eliminating the need for Complex Programmable Logic Device (CPLD) and clock generation PLLs that are used for this purpose in a system. In addition, glitches and brownouts in system power will not corrupt the ProASIC$^{\underline{\text{PLUS}}}$ device's Flash configuration, and unlike SRAM-based FPGAs, the device will not have to be reloaded when system power is restored. This enables the reduction or complete removal of the configuration PROM, expensive voltage monitor, brownout detection, and clock generator devices from the PCB design. Flash-based ProASIC$^{\underline{\text{PLUS}}}$ devices simplify total system design, and reduce cost and design risk, while increasing system reliability and improving system initialization time.

Flash Switch

Unlike SRAM FPGAs, ProASIC$^{\underline{\text{PLUS}}}$ uses a live-on-power-up ISP Flash switch as its programming element.

In the ProASIC$^{\underline{\text{PLUS}}}$ Flash switch, two transistors share the floating gate, which stores the programming information. One is the sensing transistor, which is only used for writing and verification of the floating gate voltage. The other is the switching transistor. It can be used in the architecture to connect/separate routing nets or to configure logic. It is also used to erase the floating gate (Figure 1-2 on page 1-2).

Logic Tile

The logic tile cell (Figure 1-3) has three inputs (any or all of which can be inverted) and one output (which can connect to both ultra-fast local and efficient long-line routing resources). Any three-input, one-output logic function (except a three-input XOR) can be configured as one tile. The tile can be configured as a latch with clear or set or as a flip-flop with clear or set. Thus, the tiles can flexibly map logic and sequential gates of a design.

Routing Resources

The routing structure of ProASIC$^{\underline{PLUS}}$ devices is designed to provide high performance through a flexible four-level hierarchy of routing resources: ultra-fast local resources, efficient long-line resources, high-speed, very long-line resources, and high performance global networks.

The ultra-fast local resources are dedicated lines that allow the output of each tile to connect directly to every input of the eight surrounding tiles (Figure 1-4).

The efficient long-line resources provide routing for longer distances and higher fanout connections. These resources vary in length (spanning 1, 2, or 4 tiles), run both vertically and horizontally, and cover the entire ProASIC$^{\underline{PLUS}}$ device (Figure 1-5 on page 1-5). Each tile can drive signals onto the efficient long-line resources, which can in turn access every input of every tile. Active buffers are inserted automatically by routing software to limit the loading effects due to distance and fanout.

The high-speed, very long-line resources, which span the entire device with minimal delay, are used to route very long or very high fanout nets. (Figure 1-6 on page 1-6).

The high-performance global networks are low-skew, high fanout nets that are accessible from external pins or from internal logic (Figure 1-7 on page 1-7). These nets are typically used to distribute clocks, resets, and other high fanout nets requiring a minimum skew. The global networks are implemented as clock trees, and signals can be introduced at any junction. These can be employed hierarchically with signals accessing every input on all tiles.

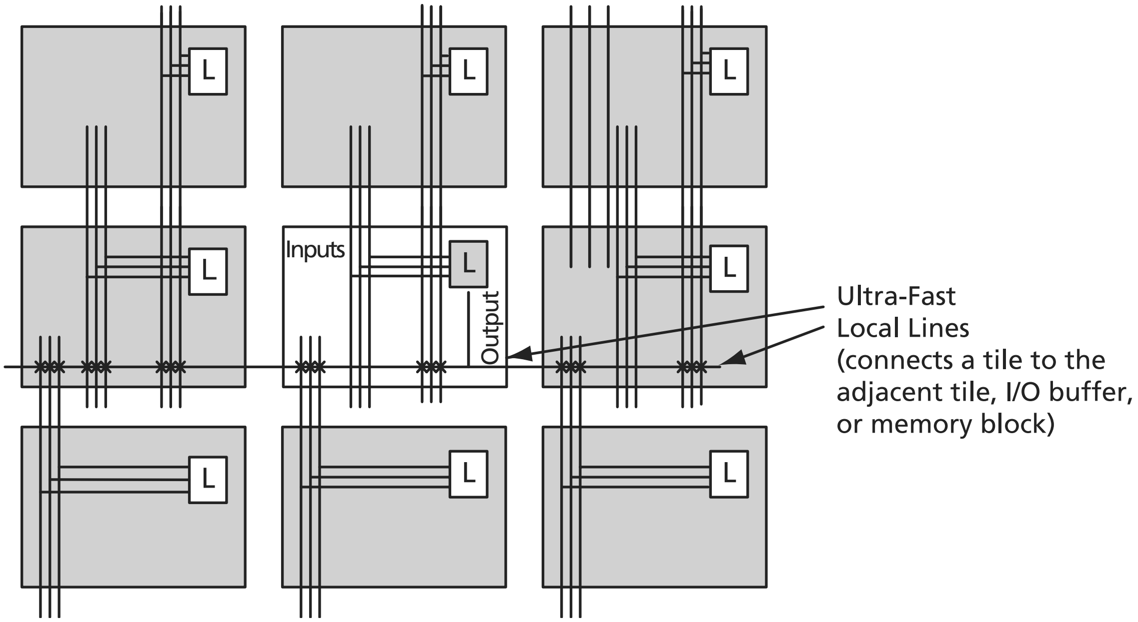
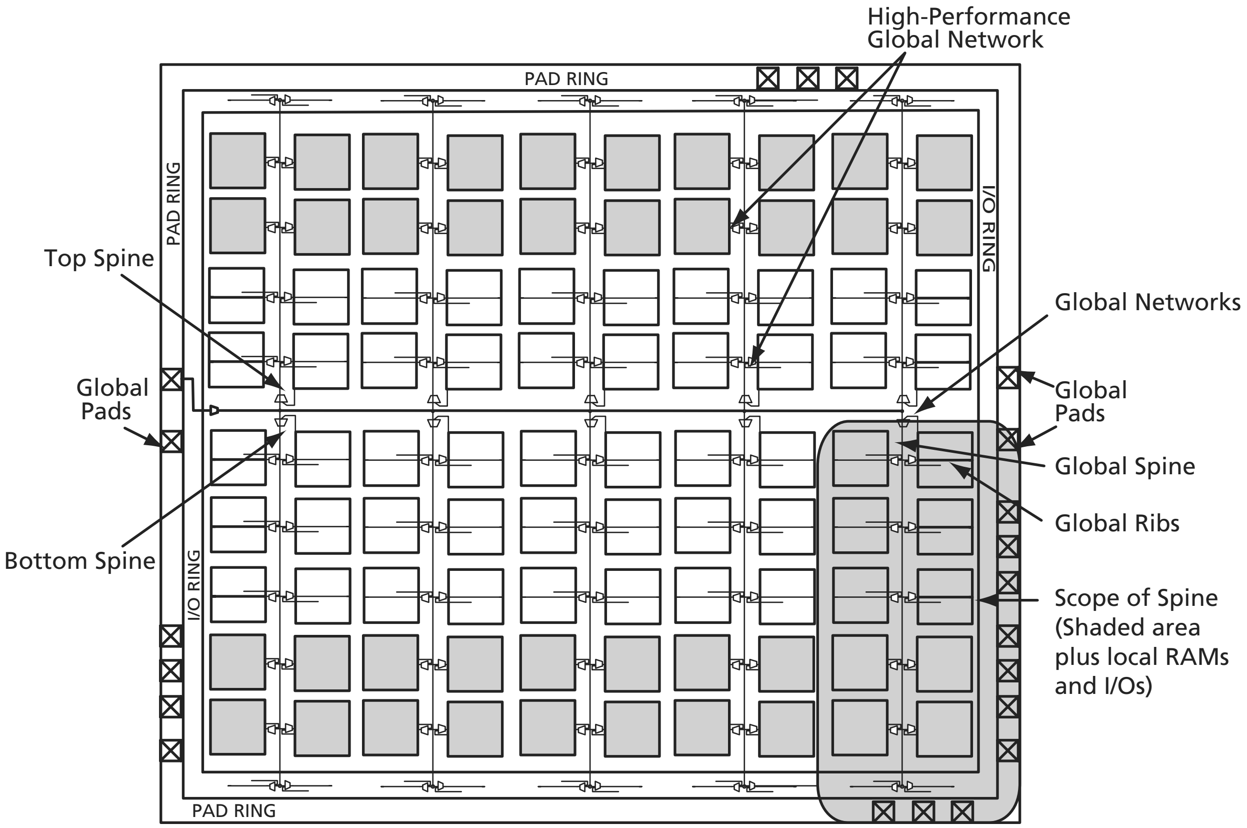


Figure 1-4 • **Ultra-Fast Local Resources**



Note: *This figure shows routing for only one global path.*

Figure 1-7 • **High-Performance Global Network**

Table 1-1 • **Clock Spines**

	APA075	**APA150**	**APA300**	**APA450**	**APA600**	**APA750**	**APA1000**
Global Clock Networks (Trees)	4	4	4	4	4	4	4
Clock Spines/Tree	6	8	8	12	14	16	22
Total Spines	24	32	32	48	56	64	88
Top or Bottom Spine Height (Tiles)	16	24	32	32	48	64	80
Tiles in Each Top or Bottom Spine	512	768	1,024	1,024	1,536	2,048	2,560
Total Tiles	3,072	6,144	8,192	12,288	21,504	32,768	56,320

Timing Control and Characteristics

ProASIC$^{\underline{PLUS}}$ Clock Management System

ProASIC$^{\underline{PLUS}}$ devices provide designers with very flexible clock conditioning capabilities. Each member of the ProASIC$^{\underline{PLUS}}$ family contains two phase-locked loop (PLL) blocks which perform the following functions:

- Clock Phase Adjustment via Programmable Delay (250 ps steps from –7 ns to +8 ns)
- Clock Skew Minimization
- Clock Frequency Synthesis

Each PLL has the following key features:

- Input Frequency Range (f_{IN}) = 1.5 to 180 MHz
- Feedback Frequency Range (f_{VCO}) = 24 to 180 MHz
- Output Frequency Range (f_{OUT}) = 8 to 180 MHz
- Output Phase Shift = 0 ° and 180 °
- Output Duty Cycle = 50%
- Low Output Jitter (max at 25°C)
  - f_{VCO} <10 MHz. Jitter ±1% or better
  - 10 MHz < f_{VCO} < 60 MHz. Jitter ±2% or better
  - f_{VCO} > 60 MHz. Jitter ±1% or better

Note: Jitter(ps) = Jitter(%)* period

For Example:

Jitter in picoseconds at 100 MHz = 0.01 * (1/100E6) = 100 ps

- Maximum Acquisition Time = 80 µs for f_{VCO} > 40 MHz
  = 30 µs for f_{VCO} < 40 MHz
- Low Power Consumption – 6.9 mW (max – analog supply) + 7.0µW/MHz (max – digital supply)

Physical Implementation

Each side of the chip contains a clock conditioning circuit based on a 180 MHz PLL block (Figure 1-14 on page 1-14). Two global multiplexed lines extend along each side of the chip to provide bidirectional access to the PLL on that side (neither MUX can be connected to the opposite side's PLL). Each global line has optional LVPECL input pads (described below). The global lines may be driven by either the LVPECL global input pad or the outputs from the PLL block, or both. Each global line can be driven by a different output from the PLL. Unused global pins can be configured as regular I/Os or left unconnected. They default to an input with pull-up. The two signals available to drive the global networks are as follows (Figure 1-15 on page 1-15, Table 1-7 on page 1-15, and Table 1-8 on page 1-16):

Global A (secondary clock)

- Output from Global MUX A
- Conditioned version of PLL output (f_{OUT}) – delayed or advanced
- Divided version of either of the above
- Further delayed version of either of the above (0.25 ns, 0.50 ns, or 4.00 ns delay)[1]

Global B

- Output from Global MUX B
- Delayed or advanced version of f_{OUT}
- Divided version of either of the above
- Further delayed version of either of the above (0.25 ns, 0.50 ns, or 4.00 ns delay)[2]

Functional Description

Each PLL block contains four programmable dividers as shown in Figure 1-14 on page 1-14. These allow frequency scaling of the input clock signal as follows:

- The n divider divides the input clock by integer factors from 1 to 32.
- The m divider in the feedback path allows multiplication of the input clock by integer factors ranging from 1 to 64.
- The two dividers together can implement any combination of multiplication and division resulting in a clock frequency between 24 and 180 MHz exiting the PLL core. This clock has a fixed 50% duty cycle.
- The output frequency of the PLL core is given by the formula EQ 1-1 (f_{REF} is the reference clock frequency):

$$f_{OUT} = f_{REF} * m/n \tag{EQ 1-1}$$

- The third and fourth dividers (u and v) permit the signals applied to the global network to each be further divided by integer factors ranging from 1 to 4.

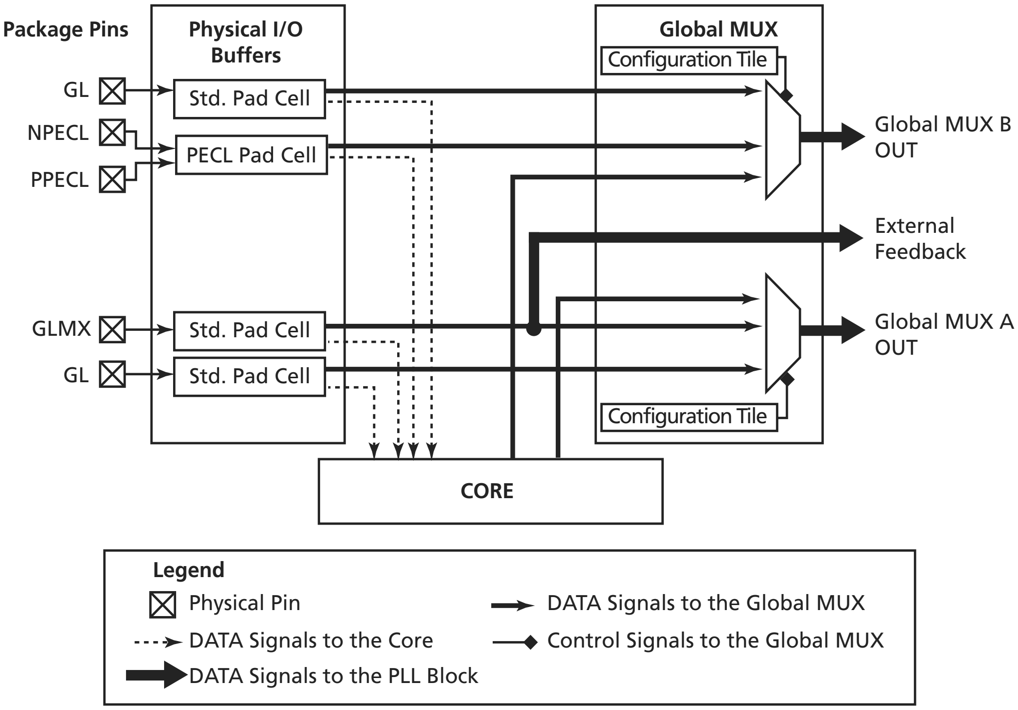
The implementations shown in EQ2 and EQ3 enable the user to define a wide range of frequency multiplier and divisors.

$$f_{GLB} = m/(n*u) \tag{EQ 1-2}$$

$$f_{GLA} = m/(n*v) \tag{EQ 1-3}$$

---

1. *This mode is available through the delay feature of the Global MUX driver.*



Note: *When a signal from an I/O tile is connected to the core, it cannot be connected to the Global MUX at the same time.*

Figure 1-15 • **Input Connectors to ProASIC^{PLUS} Clock Conditioning Circuitry**

Table 1-7 • **Clock-Conditioning Circuitry MUX Settings**

MUX	**Datapath**	**Comments**
FBSEL		
1	Internal Feedback	
2	Internal Feedback and Advance Clock Using FBDLY	–0.25 to –4 ns in 0.25 ns increments
3	External Feedback (EXTFB)	
XDLYSEL		
0	Feedback Unchanged	
1	Deskew feedback by advancing clock by system delay	Fixed delay of -2.95 ns
OBMUX	**GLB**	
0	Primary bypass, no divider	
1	Primary bypass, use divider	
2	Delay Clock Using FBDLY	+0.25 to +4 ns in 0.25 ns increments
4	Phase Shift Clock by 0°	
5	Reserved	
6	Phase Shift Clock by +180°	
7	Reserved	
OAMUX	**GLA**	
0	Secondary bypass, no divider	
1	Secondary bypass, use divider	
2	Delay Clock Using FBDLY	+0.25 to +4 ns in 0.25 ns increments
3	Phase Shift Clock by 0°	

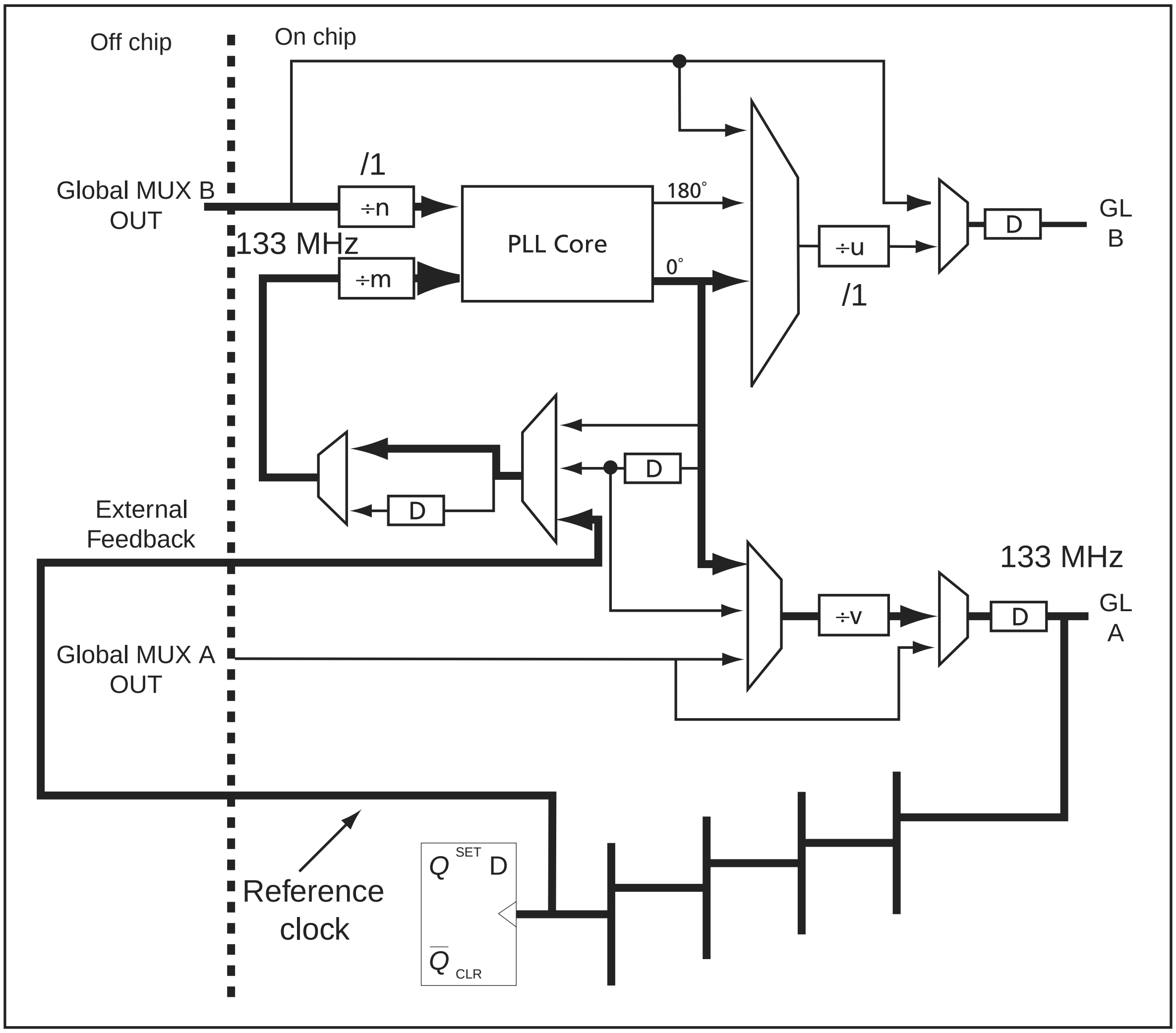


Figure 1-20 • **Using the PLL for Clock Deskewing**

User Security

ProASIC$^{\text{PLUS}}$ devices have FlashLock protection bits that, once programmed, block the entire programmed contents from being read externally. Please refer to Table 1-11 for details on the number of bits in the key for each device. If locked, the user can only reprogram the device employing the user-defined security key. This protects the device from being read back and duplicated. Since programmed data is stored in nonvolatile memory cells (actually very small capacitors) rather than in the wiring, physical deconstruction cannot be used to compromise data. This type of security breach is further discouraged by the placement of the memory cells beneath the four metal layers (whose removal cannot be accomplished without disturbing the charge in the capacitor). This is the highest security provided in the industry. For more information, refer to Actel's *Design Security in Nonvolatile Flash and Antifuse FPGAs* white paper.

Table 1-11 • **Flashlock Key Size by Device**

Device	Key Size
APA075	79 bits
APA150	79 bits
APA300	79 bits
APA450	119 bits
APA600	167 bits
APA750	191 bits
APA1000	263 bits

Embedded Memory Floorplan

The embedded memory is located across the top and bottom of the device in 256x9 blocks (Figure 1-1 on page 1-2). Depending on the device, up to 88 blocks are available to support a variety of memory configurations. Each block can be programmed as an independent memory array or combined (using dedicated memory routing resources) to form larger, more complex memory configurations. A single memory configuration could include blocks from both the top and bottom memory locations.

Embedded Memory Configurations

The embedded memory in the ProASIC$^{\text{PLUS}}$ family provides great configuration flexibility (Table 1-12). Each ProASIC$^{\text{PLUS}}$ block is designed and optimized as a two-port memory (one read, one write). This provides 198 kbits of two-port and/or single port memory in the APA1000 device.

Each memory block can be configured as FIFO or SRAM, with independent selection of synchronous or asynchronous read and write ports (Table 1-13). Additional characteristics include programmable flags as well as parity checking and generation. Figure 1-21 on page 1-25 and Figure 1-22 on page 1-26 show the block diagrams of the basic SRAM and FIFO blocks. Table 1-14 on page 1-25 and Table 1-15 on page 1-26 describe memory block SRAM and FIFO interface signals, respectively. A single memory block is designed to operate at up to 150 MHz (standard speed grade typical conditions). Each block is comprised of 256 9-bit words (one read port, one write port). The memory blocks may be cascaded in width and/or depth to create the desired memory organization. (Figure 1-23 on page 1-27). This provides optimal bit widths of 9 (one block), 18, 36, and 72, and optimal depths of 256, 512, 768, and 1,024. Refer to Actel's *SmartGen User's Guide* for more information.

Figure 1-24 on page 1-27 gives an example of optimal memory usage. Ten blocks with 23,040 bits have been used to generate three arrays of various widths and depths. Figure 1-25 on page 1-27 shows how RAM blocks can be used in parallel to create extra read ports. In this example, using only 10 of the 88 available blocks of the APA1000 yields an effective 6,912 bits of multiple port RAM. The Actel SmartGen software facilitates building wider and deeper memory configurations for optimal memory usage.

Table 1-12 • **ProASIC$^{\text{PLUS}}$ Memory Configurations by Device**

			Maximum Width		Maximum Depth	
Device	**Bottom**	**Top**	**D**	**W**	**D**	**W**
APA075	0	12	256	108	1,536	9
APA150	0	16	256	144	2,048	9
APA300	16	16	256	144	2,048	9
APA450	24	24	256	216	3,072	9
APA600	28	28	256	252	3,584	9

Logic-Tile Contribution—P_{logic}

P_{logic}, the logic-tile component of AC power dissipation, is given by

$P_{logic} = P3 * mc * Fs$

where:

P3 = 1.4 µW/MHz is the average power consumption of a logic tile per MHz of its output toggling rate. The maximum output toggling rate is Fs/2.
mc = the number of logic tiles switching during each Fs cycle
Fs = the clock frequency

I/O Output Buffer Contribution—$P_{outputs}$

$P_{outputs}$, the I/O component of AC power dissipation, is given by

$P_{outputs} = (P4 + (C_{load} * V_{DDP}^2)) * p * Fp$

where:

P4 = 326 µW/MHz is the intrinsic power consumption of an output pad normalized per MHz of the output frequency. This is the total I/O current V_{DDP}.
C_{load} = the output load
p = the number of outputs
Fp = the average output frequency

I/O Input Buffer's Buffer Contribution—P_{inputs}

The input’s component of AC power dissipation is given by

$P_{inputs} = P8 * q * Fq$

where:

P8 = 29 µW/MHz is the intrinsic power consumption of an input pad normalized per MHz of the input frequency.
q = the number of inputs
Fq = the average input frequency

PLL Contribution—P_{pll}

$P_{pll} = P9 * N_{pll}$

where:

P9 = 7.5 mW. This value has been estimated at maximum PLL clock frequency.
N_{Pll} = number of PLLs used

RAM Contribution—P_{memory}

Finally, P_{memory}, the memory component of AC power consumption, is given by

$P_{memory} = P6 * N_{memory} * F_{memory} * E_{memory}$

where:

P6 = 175 µW/MHz is the average power consumption of a memory block per MHz of the clock
N_{memory} = the number of RAM/FIFO blocks (1 block = 256 words * 9 bits)
F_{memory} = the clock frequency of the memory
E_{memory} = the average number of active blocks divided by the total number of blocks (N) of the memory.

- Typical values for E_{memory} would be 1/4 for a 1k x 8,9,16, 32 memory and 1/16 for a 4kx8, 9, 16, and 32 memory configuration
- In addition, an application-dependent component to E_{memory} can be considered. For example, for a 1kx8 memory configuration using only 1 cycle out of 2, $E_{memory} = 1/4*1/2 = 1/8$

Table 1-20 • **Recommended Maximum Operating Conditions Programming and PLL Supplies**

Parameter	Condition	Commercial/Industrial/Military/MIL-STD-883		Units
		Minimum	Maximum	
V_{PP}	During Programming	15.8	16.5	V
	Normal Operation[1]	0	16.5	V
V_{PN}	During Programming	–13.8	–13.2	V
	Normal Operation[2]	–13.8	0.5	V
I_{PP}	During Programming		25	mA
I_{PN}	During Programming		10	mA
AVDD		V_{DD}	V_{DD}	V
AGND		GND	GND	V

Notes:

1. *Please refer to the "VPP Programming Supply Pin" section on page 1-77 for more information.*
2. *Please refer to the "VPN Programming Supply Pin" section on page 1-77 for more information.*

Table 1-21 • **Recommended Operating Conditions**

Parameter	Symbol	Limits		
		Commercial	Industrial	Military/MIL-STD-883
DC Supply Voltage (2.5 V I/Os)	V_{DD} and V_{DDP}	2.5 V ± 0.2 V	2.5 V ± 0.2 V	2.5 V ± 0.2 V
DC Supply Voltage (3.3 V I/Os)	V_{DDP} V_{DD}	3.3 V ± 0.3 V 2.5 V ± 0.2 V	3.3 V ± 0.3 V 2.5 V ± 0.2 V	3.3 V ± 0.3 V 2.5 V ± 0.2 V
Operating Ambient Temperature Range	T_A, T_C	0°C to 70°C	–40°C to 85°C	–55°C (T_A) to 125°C (T_C)
Maximum Operating Junction Temperature	T_J	110°C	110°C	150°C

Note: *For I/O long-term reliability, external pull-up resistors cannot be used to increase output voltage above V_{DDP}.*

Table 1-23 • **DC Electrical Specifications (V_{DDP} = 3.3 V ±0.3 V and V_{DD} = 2.5 V ±0.2 V) (Continued)**
Applies to Commercial and Industrial Temperature Only

				Commercial/Industrial[1]			
Symbol	**Parameter**	**Conditions**		**Min.**	**Typ.**	**Max.**	**Units**
I_{OZ}	Tristate Output Leakage Current	V_{OH} = GND or V_{DD}	Std.	–10		10	µA
			–F[2, 4]	–10		100	µA
I_{OSH}	Output Short Circuit Current High						
	3.3 V High Drive (OB33P)	V_{IN} = GND		–200			
	3.3 V Low Drive (OB33L)	V_{IN} = GND		–100			
I_{OSL}	Output Short Circuit Current Low						
	3.3 V High Drive	V_{IN} = V_{DD}				200	
	3.3 V Low Drive	V_{IN} = V_{DD}				100	
$C_{I/O}$	I/O Pad Capacitance					10	pF
C_{CLK}	Clock Input Pad Capacitance					10	pF

Notes:

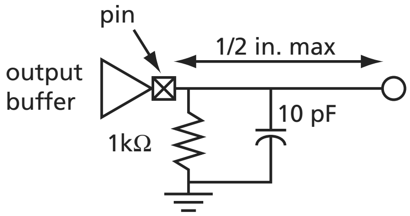
1. *All process conditions. Commercial/Industrial: Junction Temperature: –40 to +110°C.*
2. *All –F parts are only available as commercial.*
3. *No pull-up resistor required.*
4. *This will not exceed 2 mA total per device.*
5. *During transitions, the input signal may overshoot to V_{DDP} +1.0 V for a limited time of no larger than 10% of the duty cycle.*
6. *During transitions, the input signal may undershoot to –1.0 V for a limited time of no larger than 10% of the duty cycle.*

Table 1-26 • **AC Specifications (3.3 V PCI Revision 2.2 Operation)**

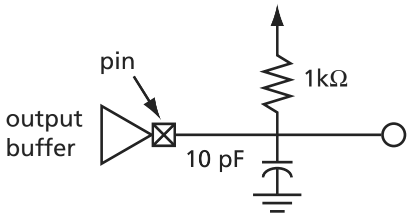
Symbol	**Parameter**	**Condition**	**Commercial/Industrial/Military/MIL-STD- 883**		**Units**
			Min.	**Max.**	
$I_{OH(AC)}$	Switching Current High	$0 < V_{OUT} \leq 0.3V_{DDP}$*	$-12V_{DDP}$		mA
		$0.3V_{DDP} \leq V_{OUT} < 0.9V_{DDP}$*	$(-17.1 + (V_{DDP} - V_{OUT}))$		mA
		$0.7V_{DDP} < V_{OUT} < V_{DDP}$*		See equation C – page 124 of the PCI Specification document rev. 2.2	
	(Test Point)	$V_{OUT} = 0.7V_{DDP}$*		$-32V_{DDP}$	mA
$I_{OL(AC)}$	Switching Current Low	$V_{DDP} > V_{OUT} \geq 0.6V_{DDP}$*	$16V_{DDP}$		mA
		$0.6V_{DDP} > V_{OUT} > 0.1V_{DDP}$ [1]	$(26.7V_{OUT})$		mA
		$0.18V_{DDP} > V_{OUT} > 0$*		See equation D – page 124 of the PCI Specification document rev. 2.2	
	(Test Point)	$V_{OUT} = 0.18V_{DDP}$		$38V_{DDP}$	mA
I_{CL}	Low Clamp Current	$-3 < V_{IN} \leq -1$	$-25 + (V_{IN} + 1)/0.015$		mA
I_{CH}	High Clamp Current	$V_{DDP} + 4 > V_{IN} \geq V_{DDP} + 1$	$25 + (V_{IN} - V_{DDP} - 1)/0.015$		mA
$slew_R$	Output Rise Slew Rate	$0.2V_{DDP}$ to $0.6V_{DDP}$ load*	1	4	V/ns
$slew_F$	Output Fall Slew Rate	$0.6V_{DDP}$ to $0.2V_{DDP}$ load*	1	4	V/ns

Note: ** Refer to the PCI Specification document rev. 2.2.*

Pad Loading Applicable to the Rising Edge PCI



Pad Loading Applicable to the Falling Edge PCI



Input Buffer Delays

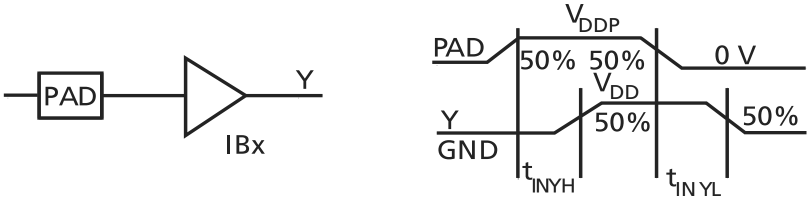


Figure 1-28 • **Input Buffer Delays**

Table 1-35 • **Worst-Case Commercial Conditions**
V_{DDP} = 3.0 V, V_{DD} = 2.3 V, T_J = 70°C

		Max. t_{INYH}[1]		**Max. t_{INYL}[2]**		
Macro Type	**Description**	**Std.**	**–F**	**Std.**	**–F**	**Units**
IB33	3.3 V, CMOS Input Levels[3], No Pull-up Resistor	0.4	0.5	0.6	0.7	ns
IB33S	3.3 V, CMOS Input Levels[3], No Pull-up Resistor, Schmitt Trigger	0.6	0.7	0.8	0.9	ns

Notes:

1. *t_{INYH} = Input Pad-to-Y High*
2. *t_{INYL} = Input Pad-to-Y Low*
3. *LVTTL delays are the same as CMOS delays.*
4. *For LP Macros, V_{DDP}=2.3 V for delays.*
5. *All –F parts are only available as commercial.*

Table 1-36 • **Worst-Case Commercial Conditions**
V_{DDP} = 2.3 V, V_{DD} = 2.3 V, T_J = 70°C

		Max. t_{INYH}[1]		**Max. t_{INYL}[2]**		
Macro Type	**Description**	**Std.**	**–F**	**Std.**	**–F**	**Units**
IB25LP	2.5 V, CMOS Input Levels[3], Low Power	0.9	1.1	0.6	0.8	ns
IB25LPS	2.5 V, CMOS Input Levels[3], Low Power, Schmitt Trigger	0.7	0.9	0.9	1.1	ns

Notes:

1. *t_{INYH} = Input Pad-to-Y High*
2. *t_{INYL} = Input Pad-to-Y Low*
3. *LVTTL delays are the same as CMOS delays.*
4. *For LP Macros, V_{DDP}=2.3 V for delays.*
5. *All –F parts are only available as commercial.*

Table 1-41 • **Worst-Case Military Conditions**
V_{DDP} = 3.0V, V_{DD} = 2.3V, T_J = 125°C for Military/MIL-STD-883

Macro Type	Description	Max. t_{INYH}[1]	Max. t_{INYL}[2]
		Std.	Std.
GL33	3.3V, CMOS Input Levels[3], No Pull-up Resistor	1.1	1.1
GL33S	3.3V, CMOS Input Levels[3], No Pull-up Resistor, Schmitt Trigger	1.1	1.1
PECL	PPECL Input Levels	1.1	1.1

Notes:

1. *t_{INYH} = Input Pad-to-Y High*
2. *t_{INYL} = Input Pad-to-Y Low*
3. *LVTTL delays are the same as CMOS delays.*
4. *For LP Macros, V_{DDP}=2.3V for delays.*

Table 1-42 • **Worst-Case Military Conditions**
V_{DDP} = 2.3V, V_{DD} = 2.3V, T_J = 125°C for Military/MIL-STD-883

Macro Type	Description	Max. t_{INYH}[1]	Max. t_{INYL}[2]
		Std.	Std.
GL25LP	2.5V, CMOS Input Levels[3], Low Power	1.0	1.1
GL25LPS	2.5V, CMOS Input Levels[3], Low Power, Schmitt Trigger	1.4	1.0

Notes:

1. *t_{INYH} = Input Pad-to-Y High*
2. *t_{INYL} = Input Pad-to-Y Low*
3. *LVTTL delays are the same as CMOS delays.*
4. *For LP Macros, V_{DDP}=2.3V for delays.*

Embedded Memory Specifications

This section discusses ProASIC^{PLUS} SRAM/FIFO embedded memory and its interface signals, including timing diagrams that show the relationships of signals as they pertain to single embedded memory blocks (Table 1-51). Table 1-13 on page 1-24 shows basic SRAM and FIFO configurations. Simultaneous read and write to the same location must be done with care. On such accesses the DI bus is output to the DO bus. Refer to the *ProASIC^{PLUS} RAM and FIFO Blocks* application note for more information.

Enclosed Timing Diagrams—SRAM Mode:

- "Synchronous SRAM Read, Access Timed Output Strobe (Synchronous Transparent)" section on page 1-58
- "Synchronous SRAM Read, Pipeline Mode Outputs (Synchronous Pipelined)" section on page 1-59
- "Asynchronous SRAM Write" section on page 1-60
- "Asynchronous SRAM Read, Address Controlled, RDB=0" section on page 1-61
- "Asynchronous SRAM Read, RDB Controlled" section on page 1-62
- "Synchronous SRAM Write"
- Embedded Memory Specifications

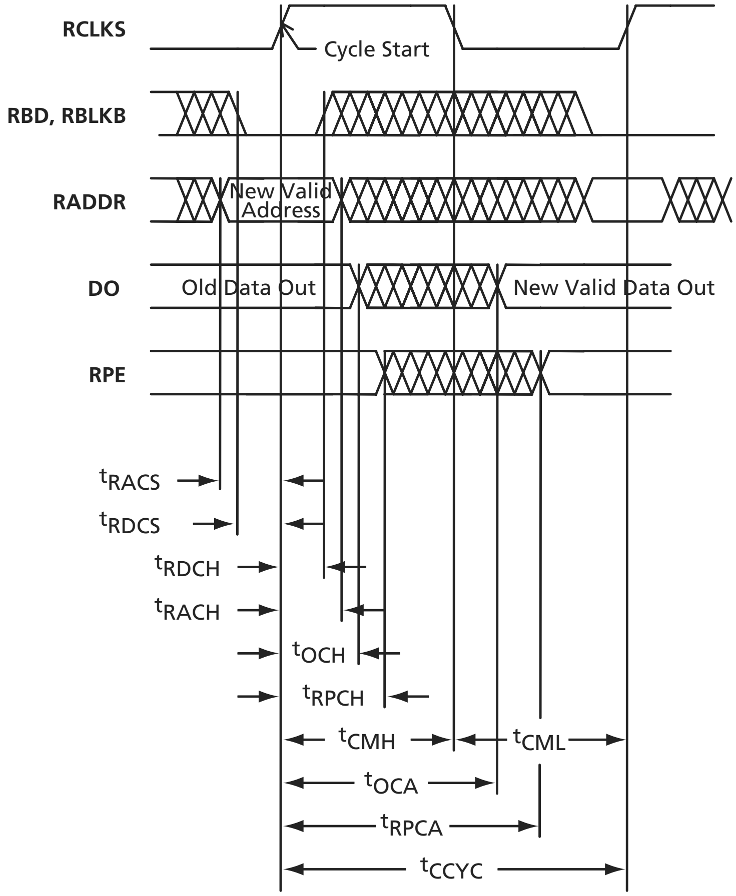
The difference between synchronous transparent and pipeline modes is the timing of all the output signals from the memory. In transparent mode, the outputs will change within the same clock cycle to reflect the data requested by the currently valid access to the memory. If clock cycles are short (high clock speed), the data requires most of the clock cycle to change to valid values (stable signals). Processing of this data in the same clock cycle is nearly impossible. Most designers add registers at all outputs of the memory to push the data processing into the next clock cycle. An entire clock cycle can then be used to process the data. To simplify use of this memory setup, suitable registers have been implemented as part of the memory primitive and are available to the user in the synchronous pipeline mode. In this mode, the output signals will change shortly after the second rising edge, following the initiation of the read access.

Table 1-51 • **Memory Block SRAM Interface Signals**

SRAM Signal	Bits	In/Out	Description
WCLKS	1	In	Write clock used on synchronization on write side
RCLKS	1	In	Read clock used on synchronization on read side
RADDR<0:7>	8	In	Read address
RBLKB	1	In	True read block select (active Low)
RDB	1	In	True read pulse (active Low)
WADDR<0:7>	8	In	Write address
WBLKB	1	In	Write block select (active Low)
DI<0:8>	9	In	Input data bits <0:8>, <8> can be used for parity In
WRB	1	In	Negative true write pulse
DO<0:8>	9	Out	Output data bits <0:8>, <8> can be used for parity Out
RPE	1	Out	Read parity error (active High)
WPE	1	Out	Write parity error (active High)
PARODD	1	In	Selects Odd parity generation/detect when high, Even when low

Note: *Not all signals shown are used in all modes.*

Synchronous SRAM Read, Access Timed Output Strobe (Synchronous Transparent)



Note: *The plot shows the normal operation status.*

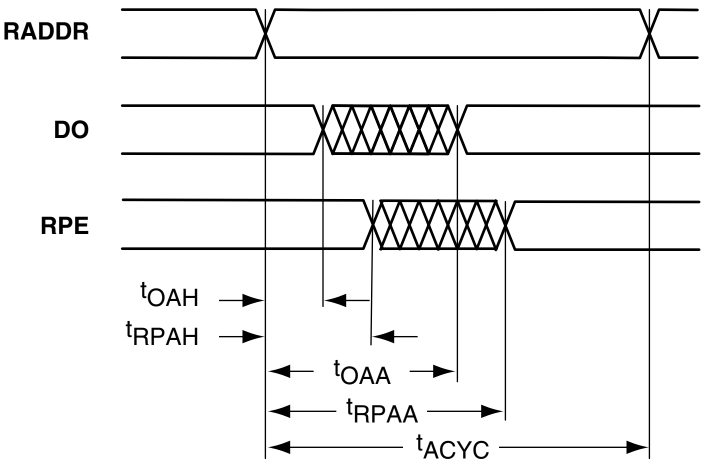
Figure 1-31 • **Synchronous SRAM Read, Access Timed Output Strobe (Synchronous Transparent)**

Table 1-52 • **T_J = 0°C to 110°C; V_{DD} = 2.3 V to 2.7 V for Commercial/industrial**
T_J = –55°C to 150°C, V_{DD} = 2.3 V to 2.7 V for Military/MIL-STD-883

Symbol t_{xxx}	Description	Min.	Max.	Units	Notes
CCYC	Cycle time	7.5		ns	
CMH	Clock high phase	3.0		ns	
CML	Clock low phase	3.0		ns	
OCA	New DO access from RCLKS ↑	7.5		ns	
OCH	Old DO valid from RCLKS ↑		3.0	ns	
RACH	RADDR hold from RCLKS ↑	0.5		ns	
RACS	RADDR setup to RCLKS ↑	1.0		ns	
RDCH	RDB hold from RCLKS ↑	0.5		ns	
RDCS	RDB setup to RCLKS ↑	1.0		ns	
RPCA	New RPE access from RCLKS ↑	9.5		ns	
RPCH	Old RPE valid from RCLKS ↑		3.0	ns	

Note: *All –F speed grade devices are 20% slower than the standard numbers.*

Asynchronous SRAM Read, Address Controlled, RDB=0



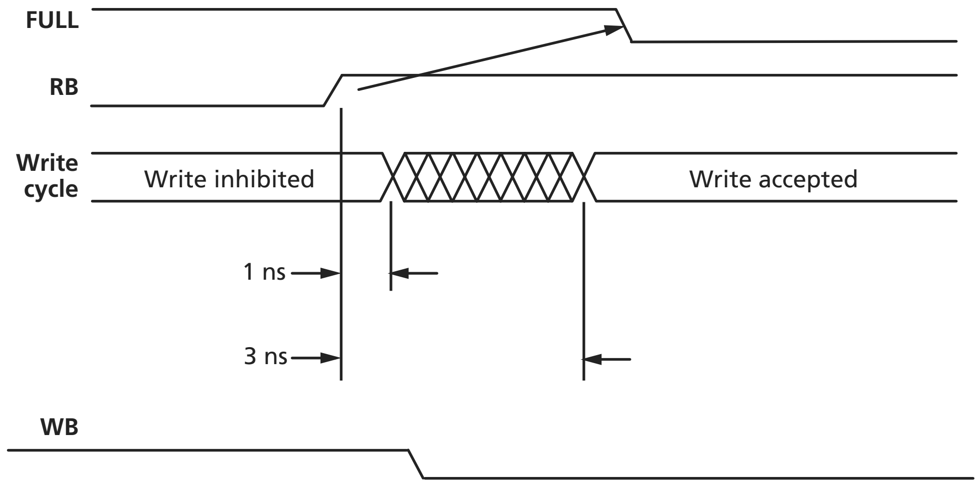
Note: *The plot shows the normal operation status.*

Figure 1-34 • **Asynchronous SRAM Read, Address Controlled, RDB=0**

Table 1-55 • **T_J = 0°C to 110°C; V_{DD} = 2.3 V to 2.7 V for Commercial/industrial**
T_J = –55°C to 150°C, V_{DD} = 2.3 V to 2.7 V for Military/MIL-STD-883B

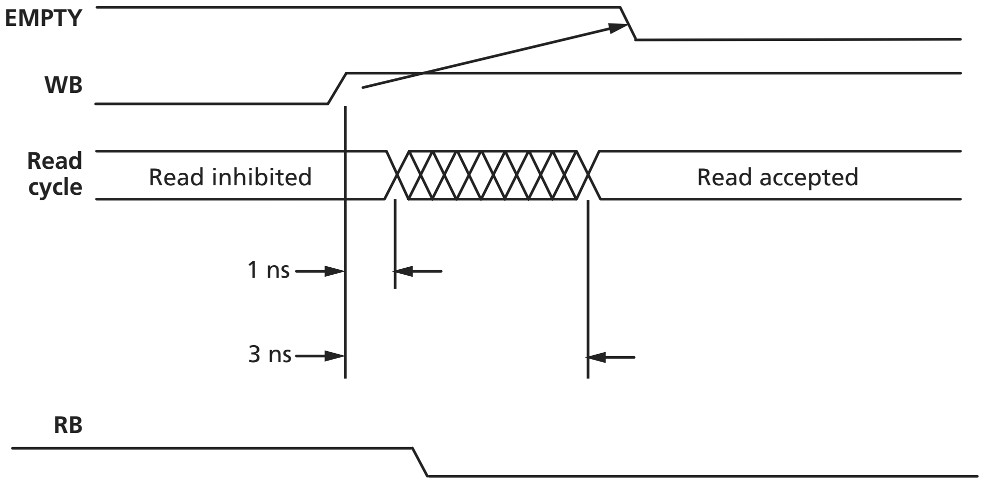
Symbol t_{xxx}	Description	Min.	Max.	Units	Notes
ACYC	Read cycle time	7.5		ns	
OAA	New DO access from RADDR stable	7.5		ns	
OAH	Old DO hold from RADDR stable		3.0	ns	
RPAA	New RPE access from RADDR stable	10.0		ns	
RPAH	Old RPE hold from RADDR stable		3.0	ns	

Note: *All –F speed grade devices are 20% slower than the standard numbers.*



Note: *All –F speed grade devices are 20% slower than the standard numbers.*

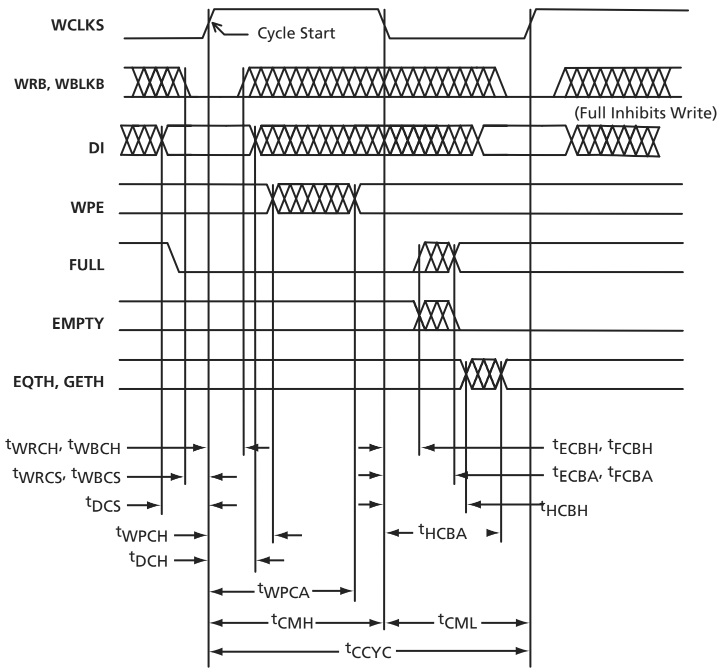
Figure 1-41 • **Write Timing Diagram**



Note: *All –F speed grade devices are 20% slower than the standard numbers.*

Figure 1-42 • **Read Timing Diagram**

Synchronous FIFO Write



Note: *The plot shows the normal operation status.*

Figure 1-47 • **Synchronous FIFO Write**

Table 1-67 • **T_J = 0°C to 110°C; V_{DD} = 2.3 V to 2.7 V for Commercial/industrial**
T_J = –55°C to 150°C, V_{DD} = 2.3 V to 2.7 V for Military/MIL-STD-883

Symbol t_{xxx}	**Description**	**Min.**	**Max.**	**Units**	**Notes**
CCYC	Cycle time	7.5		ns	
CMH	Clock high phase	3.0		ns	
CML	Clock low phase	3.0		ns	
DCH	DI hold from WCLKS ↑	0.5		ns	
DCS	DI setup to WCLKS ↑	1.0		ns	
FCBA	New FULL access from WCLKS ↓	3.0[1]		ns	
ECBA	EMPTY↓ access from WCLKS ↓	3.0[1]		ns	
ECBH, FCBH, HCBH	Old EMPTY, FULL, EQTH, & GETH valid hold time from WCLKS ↓		1.0	ns	Empty/full/thresh are invalid from the end of hold until the new access is complete
HCBA	EQTH or GETH access from WCLKS ↓	4.5		ns	
WPCA	New WPE access from WCLKS ↑	3.0		ns	WPE is invalid, while PARGEN is active
WPCH	Old WPE valid from WCLKS ↑		0.5	ns	
WRCH, WBCH	WRB & WBLKB hold from WCLKS ↑	0.5		ns	
WRCS, WBCS	WRB & WBLKB setup to WCLKS ↑	1.0		ns	

Notes:

1. *At fast cycles, ECBA and FCBA = MAX (7.5 ns – CMH), 3.0 ns.*
2. *All –F speed grade devices are 20% slower than the standard numbers.*

V_{PP} **Programming Supply Pin**

This pin may be connected to any voltage between GND and 16.5 V during normal operation, or it can be left unconnected.[2] For information on using this pin during programming, see the *In-System Programming ProASIC$^{\underline{PLUS}}$ Devices* application note. Actel recommends floating the pin or connecting it to V_{DDP}.

V_{PN} **Programming Supply Pin**

This pin may be connected to any voltage between 0.5V and –13.8 V during normal operation, or it can be left unconnected.[3] For information on using this pin during programming, see the *In-System Programming ProASIC$^{\underline{PLUS}}$ Devices* application note. Actel recommends floating the pin or connecting it to GND.

Recommended Design Practice for V_{PN}/V_{PP}

ProASIC$^{\underline{PLUS}}$ Devices – APA450, APA600, APA750, APA1000

Bypass capacitors are required from V_{PP} to GND and V_{PN} to GND for all ProASIC$^{\underline{PLUS}}$ devices during programming. During the erase cycle, ProASIC$^{\underline{PLUS}}$ devices may have current surges on the V_{PP} and V_{PN} power supplies. The only way to maintain the integrity of the power distribution to the ProASIC$^{\underline{PLUS}}$ device during these current surges is to counteract the inductance of the finite length conductors that distribute the power to the device. This can be accomplished by providing sufficient bypass capacitance between the V_{PP} and V_{PN} pins and GND (using the shortest paths possible). Without sufficient bypass capacitance to counteract the inductance, the V_{PP} and V_{PN} pins may incur a voltage spike beyond the voltage that the device can withstand. This issue applies to all programming configurations.

The solution prevents spikes from damaging the ProASIC$^{\underline{PLUS}}$ devices. Bypass capacitors are required for the V_{PP} and V_{PN} pads. Use a 0.01 µF to 0.1 µF ceramic capacitor with a 25 V or greater rating. To filter low-frequency noise (decoupling), use a 4.7 µF (low ESR, <1 <Ω, tantalum, 25 V or greater rating) capacitor. The capacitors should be located as close to the device pins as possible (within 2.5 cm is desirable). The smaller, high-frequency capacitor should be placed closer to the device pins than the larger low-frequency capacitor. The same dual-capacitor circuit should be used on both the V_{PP} and V_{PN} pins (Figure 1-49).

ProASIC$^{\underline{PLUS}}$ Devices – APA075, APA150, APA300

These devices do not require bypass capacitors on the V_{PP} and V_{PN} pins as long as the total combined distance of the programming cable and the trace length on the board is less than or equal to 30 inches. Note: For trace lengths greater than 30 inches, use the bypass capacitor recommendations in the previous section.

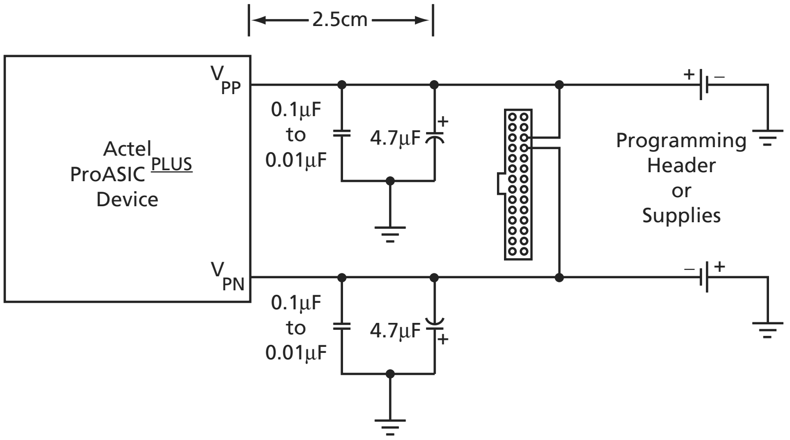


Figure 1-49 • **ProASIC$^{\underline{PLUS}}$ V_{PP} and V_{PN} Capacitor Requirements**

---

[2] *There is a nominal 40 kΩ pull-up resistor on V_{PP}*

[3] *There is a nominal 40 kΩ pull-down resistor on V_{PN}.*