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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	73728
Number of I/O	158
Number of Gates	300000
Voltage - Supply	2.3V ~ 2.7V
Mounting Type	Surface Mount
Operating Temperature	-55°C ~ 125°C (TC)
Package / Case	208-BFCQFP with Tie Bar
Supplier Device Package	208-CQFP (75x75)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/apa300-cq208m

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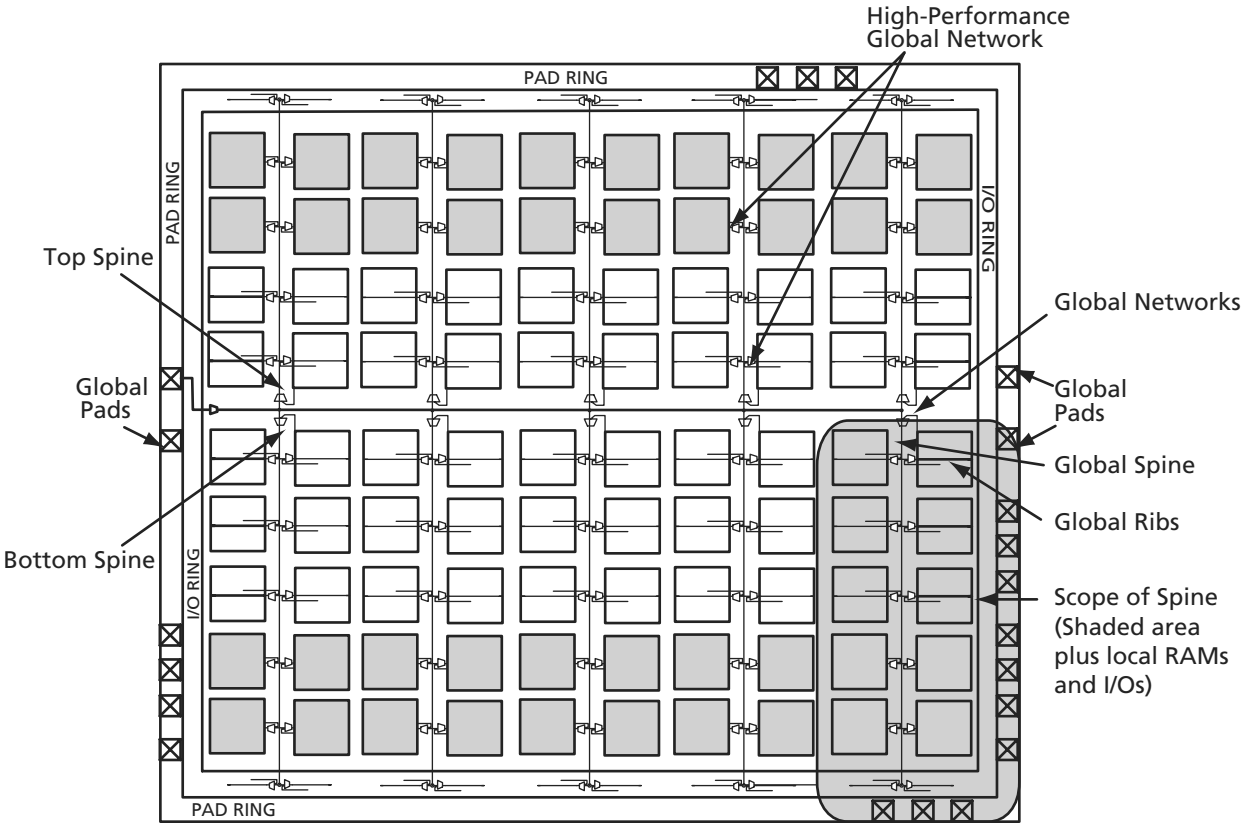


Note: *This figure shows routing for only one global path.*

Figure 1-7 • **High-Performance Global Network**

Table 1-1 • **Clock Spines**

	APA075	APA150	APA300	APA450	APA600	APA750	APA1000
Global Clock Networks (Trees)	4	4	4	4	4	4	4
Clock Spines/Tree	6	8	8	12	14	16	22
Total Spines	24	32	32	48	56	64	88
Top or Bottom Spine Height (Tiles)	16	24	32	32	48	64	80
Tiles in Each Top or Bottom Spine	512	768	1,024	1,024	1,536	2,048	2,560
Total Tiles	3,072	6,144	8,192	12,288	21,504	32,768	56,320

Boundary Scan (JTAG)

ProASIC^PLUS devices are compatible with IEEE Standard 1149.1, which defines a set of hardware architecture and mechanisms for cost-effective, board-level testing. The basic ProASIC^PLUS boundary-scan logic circuit is composed of the TAP (test access port), TAP controller, test data registers, and instruction register (Figure 1-12). This circuit supports all mandatory IEEE 1149.1 instructions (EXTEST, SAMPLE/PRELOAD and BYPASS) and the optional IDCODE instruction (Table 1-6).

Each test section is accessed through the TAP, which has five associated pins: TCK (test clock input), TDI and TDO (test data input and output), TMS (test mode selector) and TRST (test reset input). TMS, TDI and TRST are equipped with pull-up resistors to ensure proper operation when no input data is supplied to them. These pins are dedicated for boundary-scan test usage. Actel recommends that a nominal 20 kΩ pull-up resistor is added to TDO and TCK pins.

The TAP controller is a four-bit state machine (16 states) that operates as shown in Figure 1-13 on page 1-12. The '1's and '0's represent the values that must be present at TMS at a rising edge of TCK for the given state transition to occur. IR and DR indicate that the instruction register or the data register is operating in that state.

ProASIC^PLUS devices have to be programmed at least once for complete boundary-scan functionality to be available. Prior to being programmed, EXTEST is not available. If boundary-scan functionality is required prior to programming, refer to online technical support on the Actel website and search for ProASIC^PLUS BSDL.

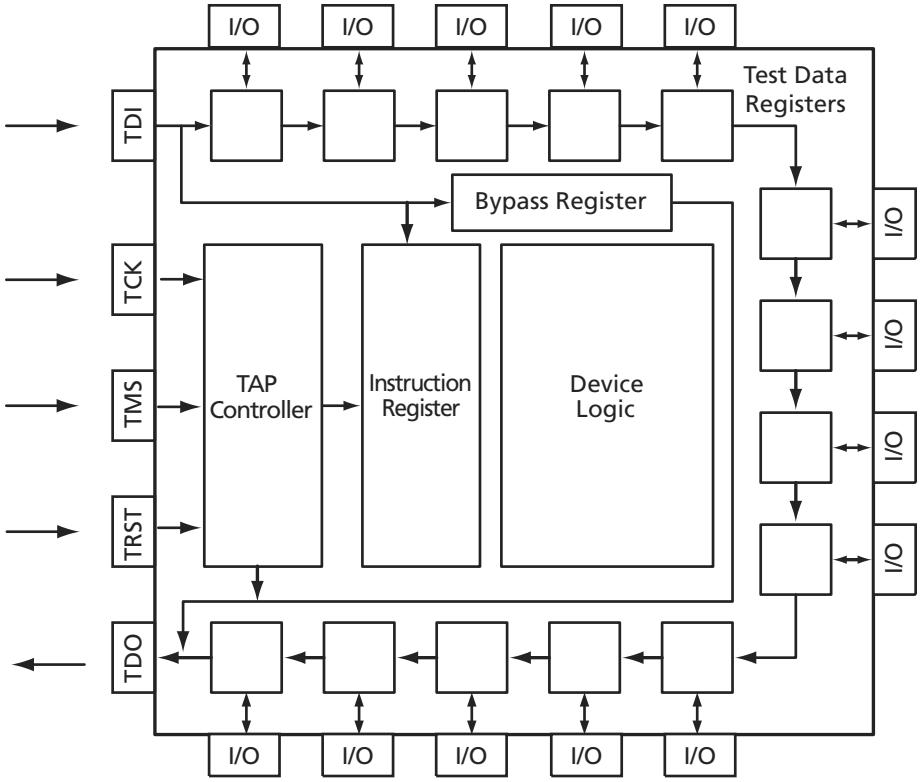


Figure 1-12 • **ProASIC^PLUS JTAG Boundary Scan Test Logic Circuit**

Table 1-6 • **Boundary-Scan Opcodes**

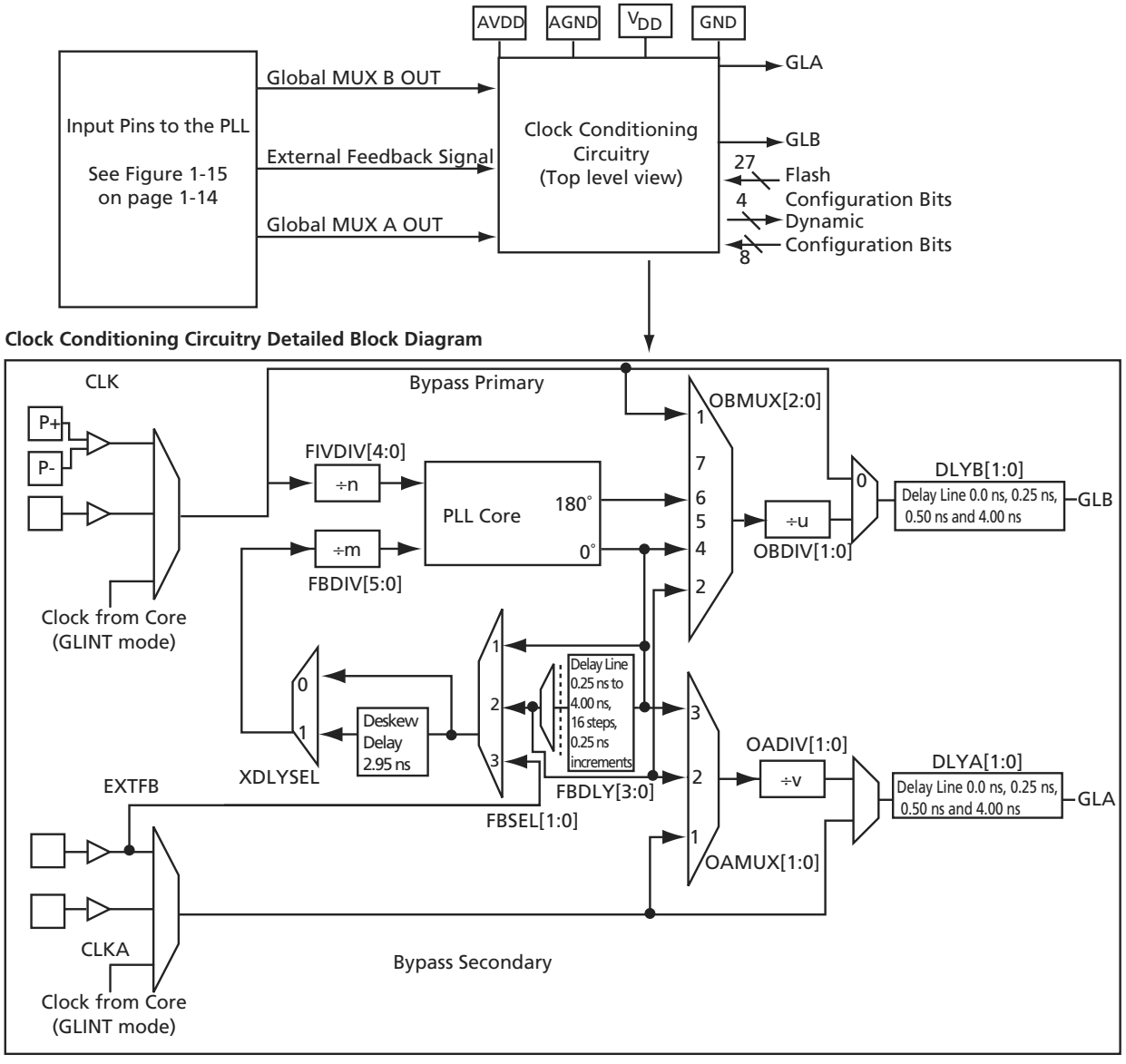
	Hex Opcode
EXTEST	00
SAMPLE/PRELOAD	01
IDCODE	0F

Table 1-6 • **Boundary-Scan Opcodes**

	Hex Opcode
CLAMP	05
BYPASS	FF

enable the user to define a wide range of frequency multipliers and divisors. The clock conditioning circuit can advance or delay the clock up to 8 ns (in increments of 0.25 ns) relative to the positive edge of the incoming reference clock. The system also allows for the selection of output frequency clock phases of 0° and 180°.

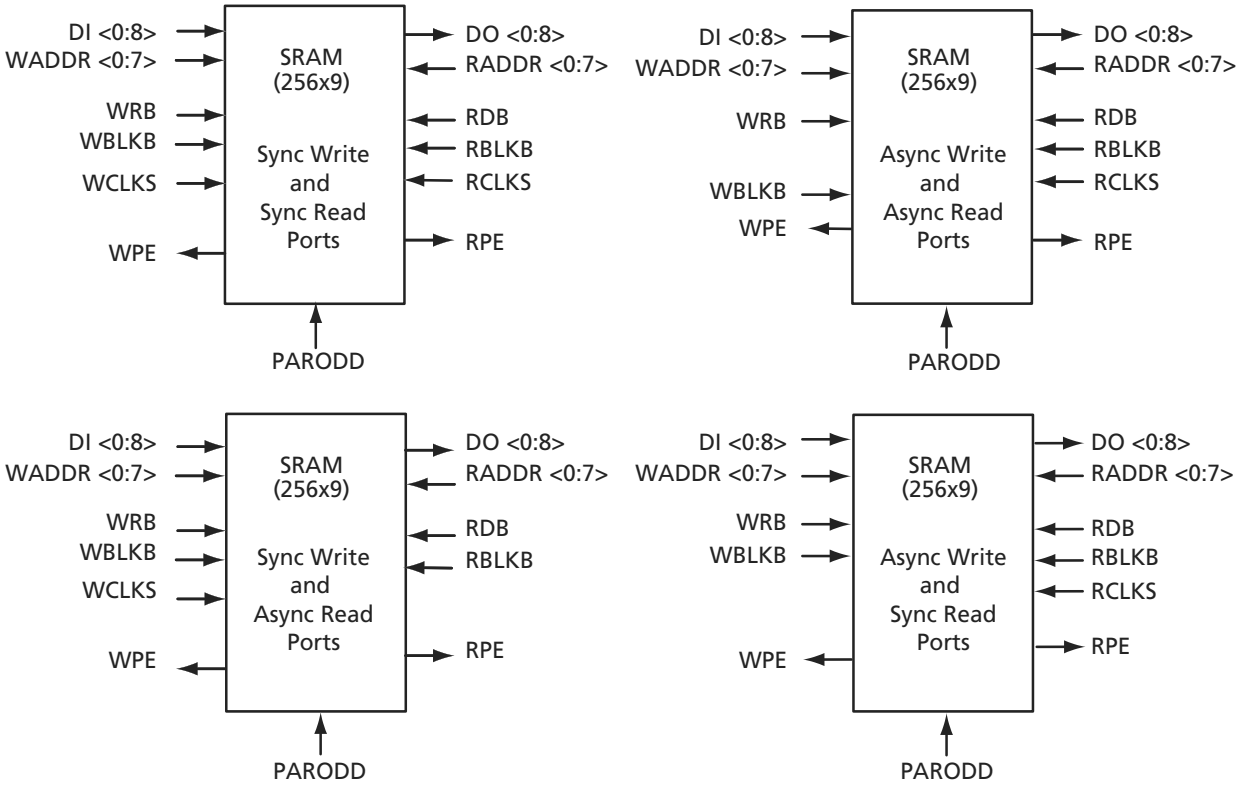
Prior to the application of signals to the rib drivers, they pass through programmable delay units, one per global network. These units permit the delaying of global signals relative to other signals to assist in the control of input set-up times. Not all possible combinations of input and output modes can be used. The degrees of freedom available in the bidirectional global pad system and in the clock conditioning circuit have been restricted. This avoids unnecessary and unwieldy design kit and software work.



Notes:

1. *FBDLY is a programmable delay line from 0 to 4 ns in 250 ps increments.*
2. *DLYA and DLYB are programmable delay lines, each with selectable values 0 ps, 250 ps, 500 ps, and 4 ns.*
3. *OBDIV will also divide the phase-shift since it takes place after the PLL Core.*

Figure 1-14 • **PLL Block – Top-Level View and Detailed PLL Block Diagram**



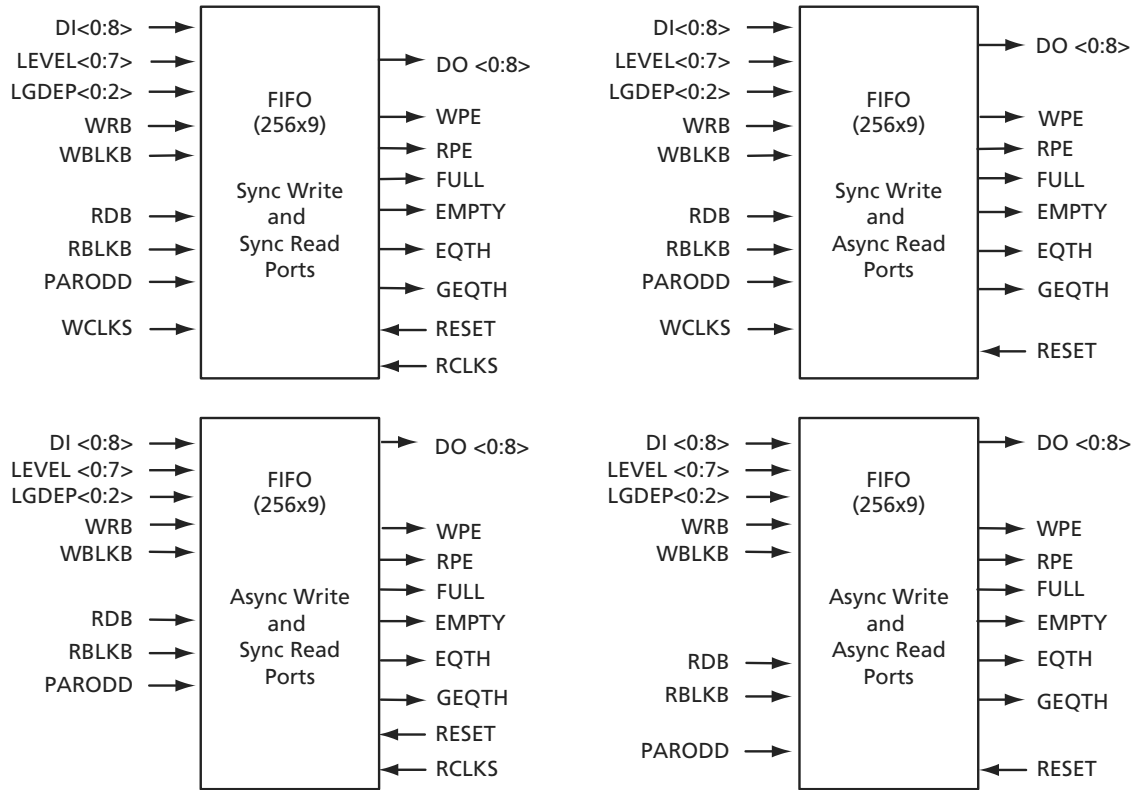
Note: *Each RAM block contains a multiplexer (called DMUX) for each output signal, increasing design efficiency. These DMUX cells do not consume any core logic tiles and connect directly to high-speed routing resources between the RAM blocks. They are used when RAM blocks are cascaded and are automatically inserted by the software tools.*

Figure 1-21 • **Example SRAM Block Diagrams**

Table 1-14 • **Memory Block SRAM Interface Signals**

SRAM Signal	Bits	In/Out	Description
WCLKS	1	In	Write clock used on synchronization on write side
RCLKS	1	In	Read clock used on synchronization on read side
RADDR<0:7>	8	In	Read address
RBLKB	1	In	Read block select (active Low)
RDB	1	In	Read pulse (active Low)
WADDR<0:7>	8	In	Write address
WBLKB	1	In	Write block select (active Low)
DI<0:8>	9	In	Input data bits <0:8>, <8> can be used for parity In
WRB	1	In	Write pulse (active Low)
DO<0:8>	9	Out	Output data bits <0:8>, <8> can be used for parity Out
RPE	1	Out	Read parity error (active High)
WPE	1	Out	Write parity error (active High)
PARODD	1	In	Selects Odd parity generation/detect when High, Even parity when Low

Note: *Not all signals shown are used in all modes.*



Note: *Each RAM block contains a multiplexer (called DMUX) for each output signal, increasing design efficiency. These DMUX cells do not consume any core logic tiles and connect directly to high-speed routing resources between the RAM blocks. They are used when RAM blocks are cascaded and are automatically inserted by the software tools.*

Figure 1-22 • **Basic FIFO Block Diagrams**

Table 1-15 • **Memory Block FIFO Interface Signals**

FIFO Signal	Bits	In/Out	Description
WCLKS	1	In	Write clock used for synchronization on write side
RCLKS	1	In	Read clock used for synchronization on read side
LEVEL <0:7>	8	In	Direct configuration implements static flag logic
RBLKB	1	In	Read block select (active Low)
RDB	1	In	Read pulse (active Low)
RESET	1	In	Reset for FIFO pointers (active Low)
WBLKB	1	In	Write block select (active Low)
DI<0:8>	9	In	Input data bits <0:8>, <8> will be generated parity if PARGEN is true
WRB	1	In	Write pulse (active Low)
FULL, EMPTY	2	Out	FIFO flags. FULL prevents write and EMPTY prevents read
EQTH, GEQTH	2	Out	EQTH is true when the FIFO holds the number of words specified by the LEVEL signal. GEQTH is true when the FIFO holds (LEVEL) words or more
DO<0:8>	9	Out	Output data bits <0:8>. <8> will be parity output if PARGEN is true.
RPE	1	Out	Read parity error (active High)
WPE	1	Out	Write parity error (active High)
LGDEP <0:2>	3	In	Configures DEPTH of the FIFO to $2^{(LGDEP+1)}$
PARODD	1	In	Parity generation/detect – Even when Low, Odd when High

Logic-Tile Contribution—P_{logic}

P_{logic}, the logic-tile component of AC power dissipation, is given by

$$P_{logic} = P3 * mc * Fs$$

where:

- P3 = 1.4 µW/MHz is the average power consumption of a logic tile per MHz of its output toggling rate. The maximum output toggling rate is Fs/2.
- mc = the number of logic tiles switching during each Fs cycle
- Fs = the clock frequency

I/O Output Buffer Contribution—$P_{outputs}$

$P_{outputs}$, the I/O component of AC power dissipation, is given by

$$P_{outputs} = (P4 + (C_{load} * V_{DDP}^2)) * p * Fp$$

where:

- P4 = 326 µW/MHz is the intrinsic power consumption of an output pad normalized per MHz of the output frequency. This is the total I/O current V_{DDP}.
- C_{load} = the output load
- p = the number of outputs
- Fp = the average output frequency

I/O Input Buffer's Buffer Contribution—P_{inputs}

The input's component of AC power dissipation is given by

$$P_{inputs} = P8 * q * Fq$$

where:

- P8 = 29 µW/MHz is the intrinsic power consumption of an input pad normalized per MHz of the input frequency.
- q = the number of inputs
- Fq = the average input frequency

PLL Contribution—P_{pll}

$$P_{pll} = P9 * N_{pll}$$

where:

- P9 = 7.5 mW. This value has been estimated at maximum PLL clock frequency.
- N_{PII} = number of PLLs used

RAM Contribution—P_{memory}

Finally, P_{memory}, the memory component of AC power consumption, is given by

$$P_{memory} = P6 * N_{memory} * F_{memory} * E_{memory}$$

where:

- P6 = 175 µW/MHz is the average power consumption of a memory block per MHz of the clock
- N_{memory} = the number of RAM/FIFO blocks (1 block = 256 words * 9 bits)
- F_{memory} = the clock frequency of the memory
- E_{memory} = the average number of active blocks divided by the total number of blocks (N) of the memory.
  - Typical values for E_{memory} would be 1/4 for a 1k x 8,9,16, 32 memory and 1/16 for a 4kx8, 9, 16, and 32 memory configuration
  - In addition, an application-dependent component to E_{memory} can be considered. For example, for a 1kx8 memory configuration using only 1 cycle out of 2, E_{memory} = 1/4*1/2 = 1/8

Table 1-20 • **Recommended Maximum Operating Conditions Programming and PLL Supplies**

Parameter	Condition	Commercial/Industrial/Military/MIL-STD-883		Units
		Minimum	Maximum	
V_{PP}	During Programming	15.8	16.5	V
	Normal Operation[1]	0	16.5	V
V_{PN}	During Programming	–13.8	–13.2	V
	Normal Operation[2]	–13.8	0.5	V
I_{PP}	During Programming		25	mA
I_{PN}	During Programming		10	mA
AVDD		V_{DD}	V_{DD}	V
AGND		GND	GND	V

Notes:
1. *Please refer to the "VPP Programming Supply Pin" section on page 1-77 for more information.*
2. *Please refer to the "VPN Programming Supply Pin" section on page 1-77 for more information.*

Table 1-21 • **Recommended Operating Conditions**

Parameter	Symbol	Limits		
		Commercial	Industrial	Military/MIL-STD-883
DC Supply Voltage (2.5 V I/Os)	V_{DD} and V_{DDP}	2.5 V ± 0.2 V	2.5 V ± 0.2 V	2.5 V ± 0.2 V
DC Supply Voltage (3.3 V I/Os)	V_{DDP} V_{DD}	3.3 V ± 0.3 V 2.5 V ± 0.2 V	3.3 V ± 0.3 V 2.5 V ± 0.2 V	3.3 V ± 0.3 V 2.5 V ± 0.2 V
Operating Ambient Temperature Range	T_A, T_C	0°C to 70°C	–40°C to 85°C	–55°C (T_A) to 125°C (T_C)
Maximum Operating Junction Temperature	T_J	110°C	110°C	150°C

Note: *For I/O long-term reliability, external pull-up resistors cannot be used to increase output voltage above V_{DDP}.*

Table 1-22 • **DC Electrical Specifications (V_{DDP} = 2.5 V ±0.2V) (Continued)**

Symbol	Parameter	Conditions	Commercial/Industrial/ Military/MIL-STD-883[1, 2]			
			Min.	Typ.	Max.	Units
I_{OSH}	Output Short Circuit Current High High Drive (OB25LPH) Low Drive (OB25LPL)	 $V_{IN} = V_{SS}$ $V_{IN} = V_{SS}$	 –120 –100			mA
I_{OSL}	Output Short Circuit Current Low High Drive (OB25LPH) Low Drive (OB25LPL)	 $V_{IN} = V_{DDP}$ $V_{IN} = V_{DDP}$			 100 30	mA
$C_{I/O}$	I/O Pad Capacitance				10	pF
C_{CLK}	Clock Input Pad Capacitance				10	pF

Notes:

1. *All process conditions. Commercial/Industrial: Junction Temperature: –40 to +110°C.*
2. *All process conditions. Military: Junction Temperature: –55 to +150°C.*
3. *All –F parts are available only as commercial.*
4. *No pull-up resistor.*
5. *This will not exceed 2 mA total per device.*
6. *During transitions, the input signal may overshoot to V_{DDP} +1.0V for a limited time of no larger than 10% of the duty cycle.*
7. *During transitions, the input signal may undershoot to -1.0V for a limited time of no larger than 10% of the duty cycle.*

Table 1-23 • **DC Electrical Specifications (V_{DDP} = 3.3 V ±0.3 V and V_{DD} = 2.5 V ±0.2 V) (Continued)**
Applies to Commercial and Industrial Temperature Only

Symbol	Parameter	Conditions		Commercial/Industrial[1] Min.	Typ.	Max.	Units
I_{OZ}	Tristate Output Leakage Current	V_{OH} = GND or V_{DD}	Std.	–10		10	µA
			–F[2, 4]	–10		100	µA
I_{OSH}	Output Short Circuit Current High 3.3 V High Drive (OB33P) 3.3 V Low Drive (OB33L)	 V_{IN} = GND V_{IN} = GND		 –200 –100			
I_{OSL}	Output Short Circuit Current Low 3.3 V High Drive 3.3 V Low Drive	 V_{IN} = V_{DD} V_{IN} = V_{DD}				 200 100	
$C_{I/O}$	I/O Pad Capacitance					10	pF
C_{CLK}	Clock Input Pad Capacitance					10	pF

Notes:

1. *All process conditions. Commercial/Industrial: Junction Temperature: –40 to +110°C.*
2. *All –F parts are only available as commercial.*
3. *No pull-up resistor required.*
4. *This will not exceed 2 mA total per device.*
5. *During transitions, the input signal may overshoot to V_{DDP} +1.0 V for a limited time of no larger than 10% of the duty cycle.*
6. *During transitions, the input signal may undershoot to –1.0 V for a limited time of no larger than 10% of the duty cycle.*

Table 1-25 • **DC Specifications (3.3 V PCI Operation)[1]**

Symbol	Parameter	Condition		Commercial/ Industrial[2,3]		Military/MIL-STD- 883[2,3]		Units
				Min.	Max.	Min.	Max.	
V_{DD}	Supply Voltage for Core			2.3	2.7	2.3	2.7	V
V_{DDP}	Supply Voltage for I/O Ring			3.0	3.6	3.0	3.6	V
V_{IH}	Input High Voltage			$0.5V_{DDP}$	V_{DDP} + 0.5	$0.5V_{DDP}$	V_{DDP} + 0.5	V
V_{IL}	Input Low Voltage			–0.5	$0.3V_{DDP}$	–0.5	$0.3V_{DDP}$	V
I_{IPU}	Input Pull-up Voltage[4]			$0.7V_{DDP}$		$0.7V_{DDP}$		V
I_{IL}	Input Leakage Current[5]	$0 < V_{IN} < V_{DDP}$	Std.	–10	10	–50	50	µA
			–F[3, 6]	–10	100			µA
V_{OH}	Output High Voltage	I_{OUT} = –500 µA		$0.9V_{DDP}$		$0.9V_{DDP}$		V
V_{OL}	Output Low Voltage	I_{OUT} = 1500 µA			$0.1V_{DDP}$		$0.1V_{DDP}$	V
C_{IN}	Input Pin Capacitance (except CLK)				10		10	pF
C_{CLK}	CLK Pin Capacitance			5	12	5	12	pF

Notes:

1. *For PCI operation, use GL33, OTB33PH, OB33PH, IOB33PH, IB33, or IB33S macro library cell only.*
2. *All process conditions. Junction Temperature: –40 to +110°C for Commercial and Industrial devices and –55 to +125°C for Military.*
3. *All –F parts are available as commercial only.*
4. *This specification is guaranteed by design. It is the minimum voltage to which pull-up resistors are calculated to pull a floated network. Designers with applications sensitive to static power utilization should ensure that the input buffer is conducting minimum current at this input voltage.*
5. *Input leakage currents include hi-Z output leakage for all bidirectional buffers with tristate outputs.*
6. *The sum of the leakage currents for all inputs shall not exceed 2mA per device.*

Tristate Buffer Delays

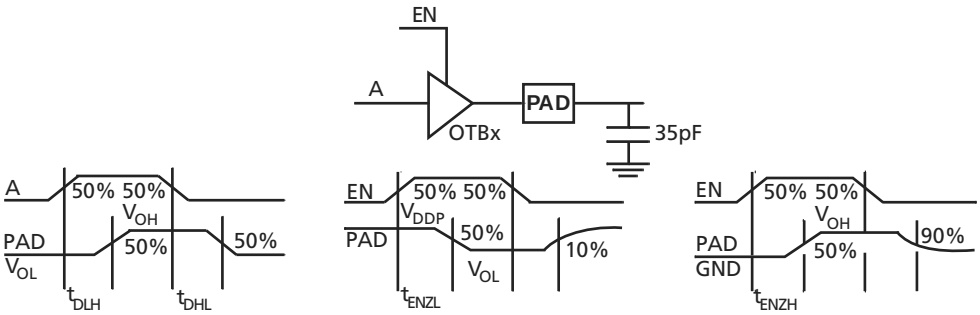


Figure 1-26 • **Tristate Buffer Delays**

Table 1-27 • **Worst-Case Commercial Conditions**
V_{DDP} = 3.0 V, V_{DD} = 2.3 V, 35 pF load, T_J = 70°C

Macro Type	Description	Max t_{DLH}[1]		Max t_{DHL}[2]		Max t_{ENZH}[3]		Max t_{ENZL}[4]		Units
		Std.	–F	Std.	–F	Std.	–F	Std.	–F	
OTB33PH	3.3 V, PCI Output Current, High Slew Rate	2.0	2.4	2.2	2.6	2.2	2.6	2.0	2.4	ns
OTB33PN	3.3 V, High Output Current, Nominal Slew Rate	2.2	2.6	2.9	3.5	2.4	2.9	2.1	2.5	ns
OTB33PL	3.3 V, High Output Current, Low Slew Rate	2.5	3.0	3.2	3.9	2.7	3.3	2.8	3.4	ns
OTB33LH	3.3 V, Low Output Current, High Slew Rate	2.6	3.1	4.0	4.8	2.8	3.4	3.0	3.6	ns
OTB33LN	3.3 V, Low Output Current, Nominal Slew Rate	2.9	3.5	4.3	5.2	3.2	3.8	4.1	4.9	ns
OTB33LL	3.3 V, Low Output Current, Low Slew Rate	3.0	3.6	5.6	6.7	3.3	3.9	5.5	6.6	ns

Notes:

1. *t_{DLH}=Data-to-Pad High*
2. *t_{DHL}=Data-to-Pad Low*
3. *t_{ENZH}=Enable-to-Pad, Z to High*
4. *t_{ENZL} = Enable-to-Pad, Z to Low*
5. *All –F parts are only available as commercial.*

Table 1-28 • **Worst-Case Commercial Conditions**
V_{DDP} = 2.3 V, V_{DD} = 2.3 V, 35 pF load, T_J = 70°C

Macro Type	Description	Max t_{DLH}[1]		Max t_{DHL}[2]		Max t_{ENZH}[3]		Max t_{ENZL}[4]		Units
		Std.	–F	Std.	–F	Std.	–F	Std.	–F	
OTB25LPHH	2.5 V, Low Power, High Output Current, High Slew Rate[5]	2.0	2.4	2.1	2.5	2.3	2.7	2.0	2.4	ns
OTB25LPHN	2.5 V, Low Power, High Output Current, Nominal Slew Rate[5]	2.4	2.9	3.0	3.6	2.7	3.2	2.1	2.5	ns
OTB25LPHL	2.5 V, Low Power, High Output Current, Low Slew Rate[5]	2.9	3.5	3.2	3.8	3.1	3.8	2.7	3.2	ns
OTB25LPLH	2.5 V, Low Power, Low Output Current, High Slew Rate[5]	2.7	3.3	4.6	5.5	3.0	3.6	2.6	3.1	ns

Notes:

1. *t_{DLH}=Data-to-Pad High*
2. *t_{DHL}=Data-to-Pad Low*
3. *t_{ENZH}=Enable-to-Pad, Z to High*
4. *t_{ENZL} = Enable-to-Pad, Z to Low*
5. *Low power I/O work with V_{DDP}=2.5 V ±10% only. V_{DDP}=2.3 V for delays.*
6. *All –F parts are only available as commercial.*

Table 1-37 • **Worst-Case Military Conditions**
V_{DDP} = 3.0V, V_{DD} = 2.3V, T_J = 125°C for Military/MIL-STD-883

Macro Type	Description	Max. t_{INYH}[1]	Max. t_{INYL}[2]	Units
		Std.	Std.	
IB33	3.3V, CMOS Input Levels[3], No Pull-up Resistor	0.5	0.6	ns
IB33S	3.3V, CMOS Input Levels[3], No Pull-up Resistor, Schmitt Trigger	0.6	0.8	ns

Notes:

1. *t_{INYH} = Input Pad-to-Y High*
2. *t_{INYL} = Input Pad-to-Y Low*
3. *LVTTL delays are the same as CMOS delays.*
4. *For LP Macros, V_{DDP}=2.3V for delays.*

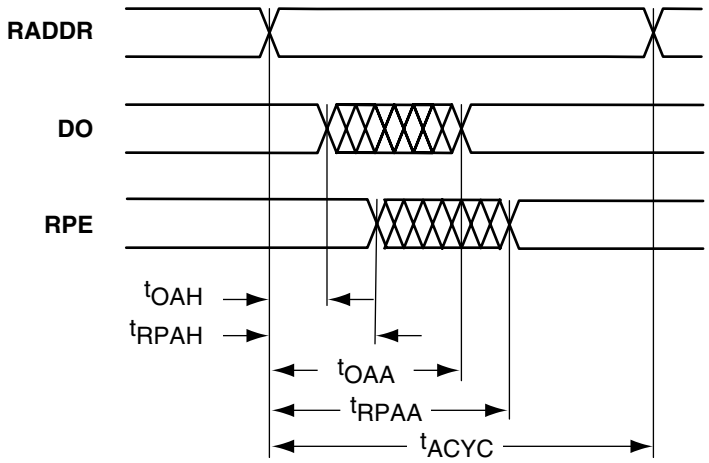
Table 1-38 • **Worst-Case Military Conditions**
V_{DDP} = 2.3V, V_{DD} = 2.3V, T_J = 125°C for Military/MIL-STD-883

Macro Type	Description	Max. t_{INYH}[1]	Max. t_{INYL}[2]	Units
		Std.	Std.	
IB25LP	2.5V, CMOS Input Levels[3], Low Power	0.9	0.7	ns
IB25LPS	2.5V, CMOS Input Levels[3], Low Power, Schmitt Trigger	0.8	1.0	ns

Notes:

1. *t_{INYH} = Input Pad-to-Y High*
2. *t_{INYL} = Input Pad-to-Y Low*
3. *LVTTL delays are the same as CMOS delays.*
4. *For LP Macros, V_{DDP}=2.3V for delays.*

Asynchronous SRAM Read, Address Controlled, RDB=0



Note: *The plot shows the normal operation status.*

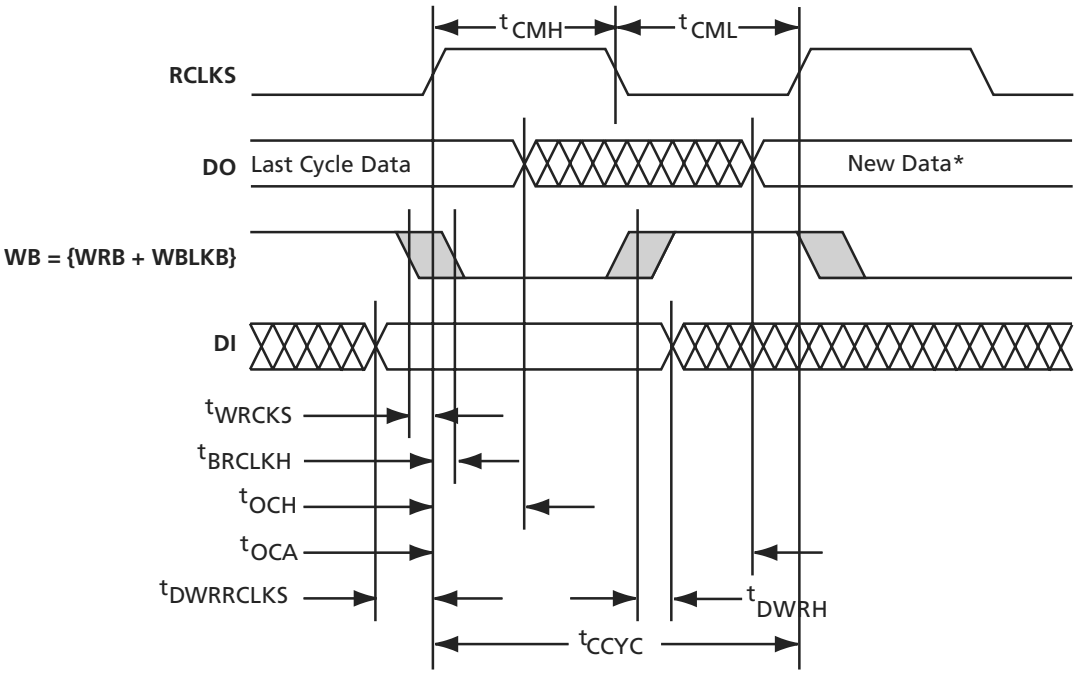
Figure 1-34 • **Asynchronous SRAM Read, Address Controlled, RDB=0**

Table 1-55 • **T_J = 0°C to 110°C; V_{DD} = 2.3 V to 2.7 V for Commercial/industrial**
T_J = –55°C to 150°C, V_{DD} = 2.3 V to 2.7 V for Military/MIL-STD-883B

Symbol t_{xxx}	Description	Min.	Max.	Units	Notes
ACYC	Read cycle time	7.5		ns	
OAA	New DO access from RADDR stable	7.5		ns	
OAH	Old DO hold from RADDR stable		3.0	ns	
RPAA	New RPE access from RADDR stable	10.0		ns	
RPAH	Old RPE hold from RADDR stable		3.0	ns	

Note: *All –F speed grade devices are 20% slower than the standard numbers.*

Asynchronous Write and Synchronous Read to the Same Location



* New data is read if WB ↓ occurs before setup time.
The stored data is read if WB ↓ occurs after hold time.

Note: *The plot shows the normal operation status.*

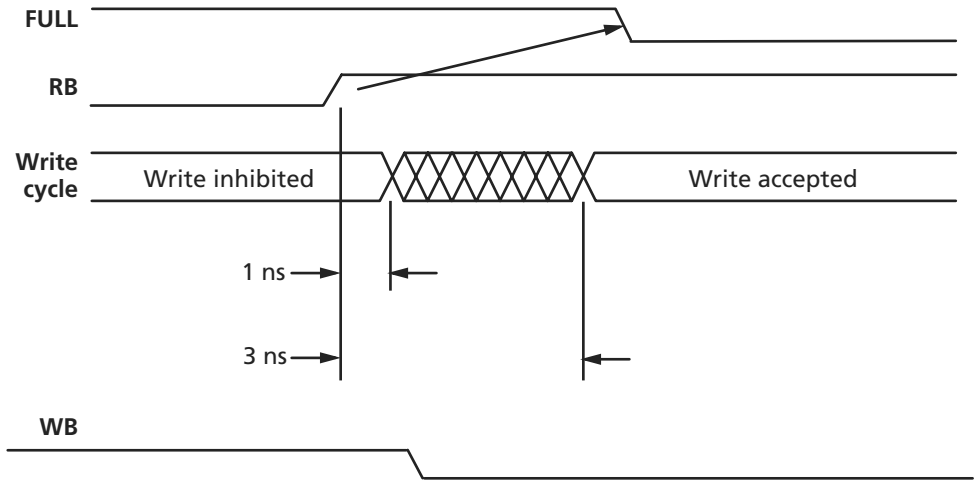
Figure 1-38 • **Asynchronous Write and Synchronous Read to the Same Location**

Table 1-59 • **T_J = 0°C to 110°C; V_{DD} = 2.3 V to 2.7 V for Commercial/industrial**
T_J = –55°C to 150°C, V_{DD} = 2.3 V to 2.7 V for Military/MIL-STD-883

Symbol t_{xxx}	Description	Min.	Max.	Units	Notes
CCYC	Cycle time	7.5		ns	
CMH	Clock high phase	3.0		ns	
CML	Clock low phase	3.0		ns	
WBRCLKS	WB ↓ to RCLKS ↑ setup time	–0.1		ns	
WBRCLKH	WB ↓ to RCLKS ↑ hold time		7.0	ns	
OCH	Old DO valid from RCLKS ↑		3.0	ns	OCA/OCH displayed for Access Timed Output
OCA	New DO valid from RCLKS ↑	7.5		ns	
DWRRCLKS	DI to RCLKS ↑ setup time	0		ns	
DWRH	DI to WB ↑ hold time		1.5	ns	

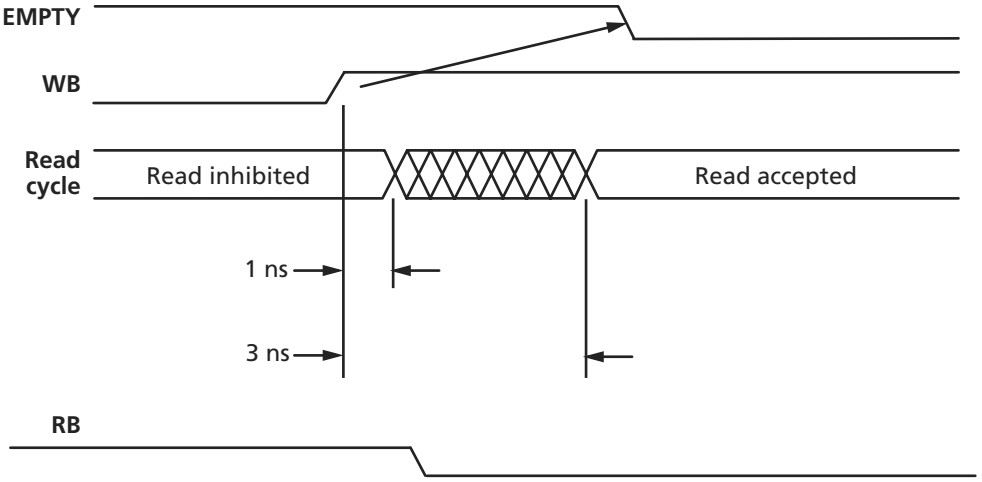
Notes:

1. *This behavior is valid for Access Timed Output and Pipelined Mode Output. The table shows the timings of an Access Timed Output.*
2. *In asynchronous write and synchronous read access to the same location, the new write data will be read out if the active write signal edge occurs before or at the same time as the active read clock edge. If WB changes to low after hold time, the data will be read.*
3. *A setup or hold time violation will result in unknown output data.*
4. *All –F speed grade devices are 20% slower than the standard numbers.*



Note: *All –F speed grade devices are 20% slower than the standard numbers.*

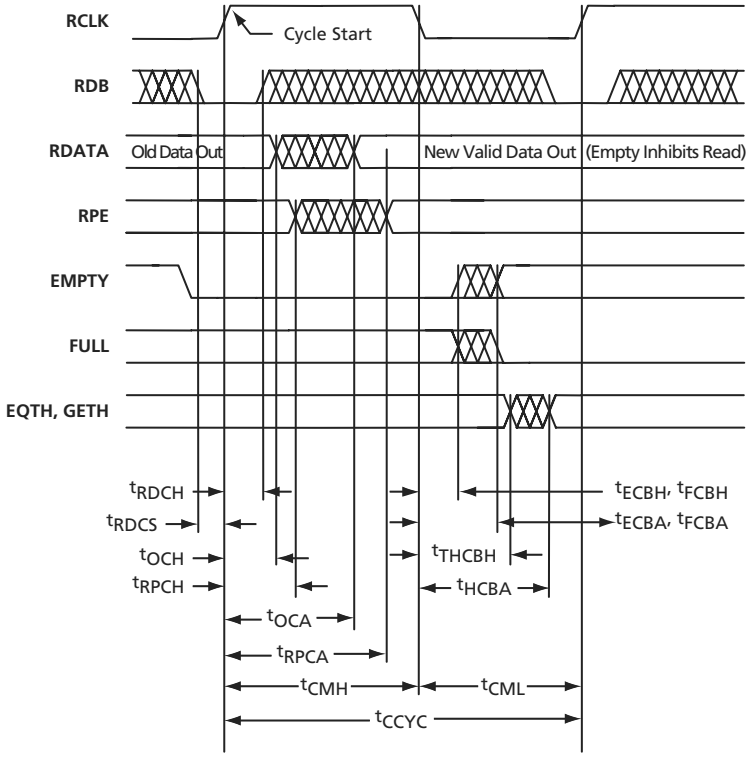
Figure 1-41 • **Write Timing Diagram**



Note: *All –F speed grade devices are 20% slower than the standard numbers.*

Figure 1-42 • **Read Timing Diagram**

Synchronous FIFO Read, Access Timed Output Strobe (Synchronous Transparent)



Note: *The plot shows the normal operation status.*

Figure 1-45 • **Synchronous FIFO Read, Access Timed Output Strobe (Synchronous Transparent)**

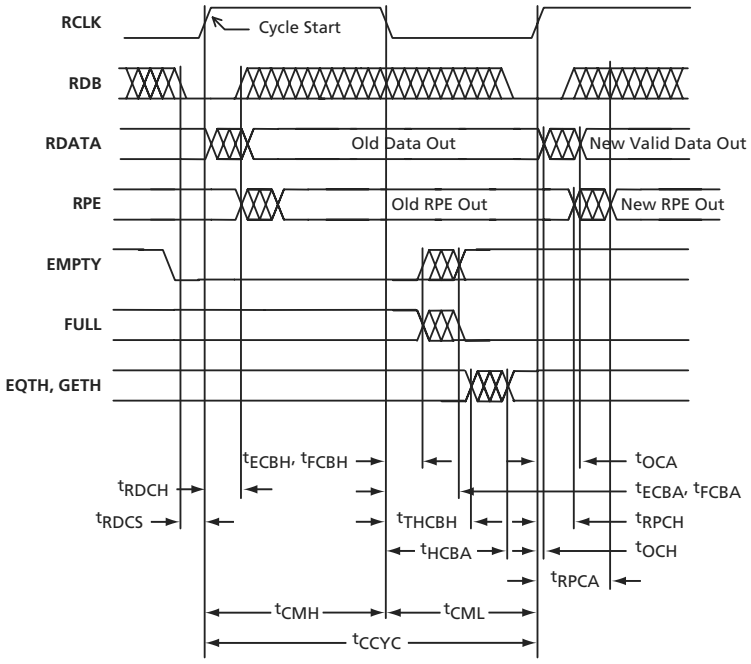
Table 1-65 • **T_J = 0°C to 110°C; V_{DD} = 2.3 V to 2.7 V for Commercial/industrial**
T_J = –55°C to 150°C, V_{DD} = 2.3 V to 2.7 V for Military/MIL-STD-883

Symbol t_{xxx}	Description	Min.	Max.	Units	Notes
CCYC	Cycle time	7.5		ns	
CMH	Clock high phase	3.0		ns	
CML	Clock low phase	3.0		ns	
ECBA	New EMPTY access from RCLKS ↓	3.0[1]		ns	
FCBA	FULL ↓ access from RCLKS ↓	3.0[1]		ns	
ECBH, FCBH, THCBH	Old EMPTY, FULL, EQTH, & GETH valid hold time from RCLKS ↓		1.0	ns	Empty/full/thresh are invalid from the end of hold until the new access is complete
OCA	New DO access from RCLKS ↑	7.5		ns	
OCH	Old DO valid from RCLKS ↑		3.0	ns	
RDCH	RDB hold from RCLKS ↑	0.5		ns	
RDCS	RDB setup to RCLKS ↑	1.0		ns	
RPCA	New RPE access from RCLKS ↑	9.5		ns	
RPCH	Old RPE valid from RCLKS ↑		3.0	ns	
HCBA	EQTH or GETH access from RCLKS ↓	4.5		ns	

Notes:

1. *At fast cycles, ECBA and FCBA = MAX (7.5 ns – CMH), 3.0 ns.*
2. *All –F speed grade devices are 20% slower than the standard numbers.*

Synchronous FIFO Read, Pipeline Mode Outputs (Synchronous Pipelined)



Note: *The plot shows the normal operation status.*

Figure 1-46 • **Synchronous FIFO Read, Pipeline Mode Outputs (Synchronous Pipelined)**

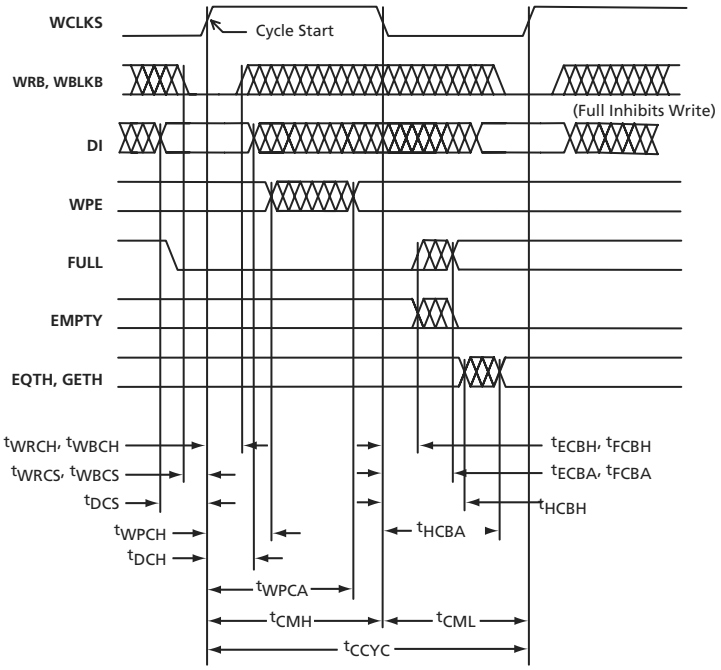
Table 1-66 • **T_J = 0°C to 110°C; V_{DD} = 2.3 V to 2.7 V for Commercial/industrial**
T_J = –55°C to 150°C, V_{DD} = 2.3 V to 2.7 V for Military/MIL-STD-883

Symbol t_{xxx}	Description	Min.	Max.	Units	Notes
CCYC	Cycle time	7.5		ns	
CMH	Clock high phase	3.0		ns	
CML	Clock low phase	3.0		ns	
ECBA	New EMPTY access from RCLKS ↓	3.0[1]		ns	
FCBA	FULL ↓ access from RCLKS ↓	3.0[1]		ns	
ECBH, FCBH, THCBH	Old EMPTY, FULL, EQTH, & GETH valid hold time from RCLKS ↓		1.0	ns	Empty/full/thresh are invalid from the end of hold until the new access is complete
OCA	New DO access from RCLKS ↑	2.0		ns	
OCH	Old DO valid from RCLKS ↑		0.75	ns	
RDCH	RDB hold from RCLKS ↑	0.5		ns	
RDCS	RDB setup to RCLKS ↑	1.0		ns	
RPCA	New RPE access from RCLKS ↑	4.0		ns	
RPCH	Old RPE valid from RCLKS ↑		1.0	ns	
HCBA	EQTH or GETH access from RCLKS ↓	4.5		ns	

Notes:

1. *At fast cycles, ECBA and FCBA = MAX (7.5 ns – CMS), 3.0 ns.*
2. *All –F speed grade devices are 20% slower than the standard numbers.*

Synchronous FIFO Write



Note: *The plot shows the normal operation status.*

Figure 1-47 • **Synchronous FIFO Write**

Table 1-67 • **T_J = 0°C to 110°C; V_{DD} = 2.3 V to 2.7 V for Commercial/industrial**
T_J = –55°C to 150°C, V_{DD} = 2.3 V to 2.7 V for Military/MIL-STD-883

Symbol t_{xxx}	Description	Min.	Max.	Units	Notes
CCYC	Cycle time	7.5		ns	
CMH	Clock high phase	3.0		ns	
CML	Clock low phase	3.0		ns	
DCH	DI hold from WCLKS ↑	0.5		ns	
DCS	DI setup to WCLKS ↑	1.0		ns	
FCBA	New FULL access from WCLKS ↓	3.0[1]		ns	
ECBA	EMPTY↓ access from WCLKS ↓	3.0[1]		ns	
ECBH, FCBH, HCBH	Old EMPTY, FULL, EQTH, & GETH valid hold time from WCLKS ↓		1.0	ns	Empty/full/thresh are invalid from the end of hold until the new access is complete
HCBA	EQTH or GETH access from WCLKS ↓	4.5		ns	
WPCA	New WPE access from WCLKS ↑	3.0		ns	WPE is invalid, while PARGEN is active
WPCH	Old WPE valid from WCLKS ↑		0.5	ns	
WRCH, WBCH	WRB & WBLKB hold from WCLKS ↑	0.5		ns	
WRCS, WBCS	WRB & WBLKB setup to WCLKS ↑	1.0		ns	

Notes:

1. *At fast cycles, ECBA and FCBA = MAX (7.5 ns – CMH), 3.0 ns.*
2. *All –F speed grade devices are 20% slower than the standard numbers.*

Pin Description

User Pins

I/O **User Input/Output**

The I/O pin functions as an input, output, tristate, or bidirectional buffer. Input and output signal levels are compatible with standard LVTTL and LVCMOS specifications. Unused I/O pins are configured as inputs with pull-up resistors.

NC **No Connect**

To maintain compatibility with other Actel ProASIC^{PLUS} products, it is recommended that this pin not be connected to the circuitry on the board.

GL **Global Pin**

Low skew input pin for clock or other global signals. This pin can be configured with an internal pull-up resistor. When it is not connected to the global network or the clock conditioning circuit, it can be configured and used as a normal I/O.

GLMX **Global Multiplexing Pin**

Low skew input pin for clock or other global signals. This pin can be used in one of two special ways (refer to Actel's *Using ProASIC^{PLUS} Clock Conditioning Circuits*).

When the external feedback option is selected for the PLL block, this pin is routed as the external feedback source to the clock conditioning circuit.

In applications where two different signals access the same global net at different times through the use of GLMXx and GLMXLx macros, this pin will be fixed as one of the source pins.

This pin can be configured with an internal pull-up resistor. When it is not connected to the global network or the clock conditioning circuit, it can be configured and used as any normal I/O. If not used, the GLMXx pin will be configured as an input with pull-up.

Dedicated Pins

GND **Ground**

Common ground supply voltage.

V_{DD} **Logic Array Power Supply Pin**

2.5 V supply voltage.

V_{DDP} **I/O Pad Power Supply Pin**

2.5 V or 3.3 V supply voltage.

TMS **Test Mode Select**

The TMS pin controls the use of boundary-scan circuitry. This pin has an internal pull-up resistor.

TCK **Test Clock**

Clock input pin for boundary scan (maximum 10 MHz). Actel recommends adding a nominal 20 kΩ pull-up resistor to this pin.

TDI **Test Data In**

Serial input for boundary scan. A dedicated pull-up resistor is included to pull this pin high when not being driven.

TDO **Test Data Out**

Serial output for boundary scan. Actel recommends adding a nominal 20kΩ pull-up resistor to this pin.

TRST **Test Reset Input**

Asynchronous, active-low input pin for resetting boundary-scan circuitry. This pin has an internal pull-up resistor. For more information, please refer to *Power-up Behavior of ProASIC^{PLUS} Devices* application note.

Special Function Pins

RCK **Running Clock**

A free running clock is needed during programming if the programmer cannot guarantee that TCK will be uninterrupted. If not used, this pin has an internal pull-up and can be left floating.

NPECL **User Negative Input**

Provides high speed clock or data signals to the PLL block. If unused, leave the pin unconnected.

PPECL **User Positive Input**

Provides high speed clock or data signals to the PLL block. If unused, leave the pin unconnected.

AVDD **PLL Power Supply**

Analog V_{DD} should be V_{DD} (core voltage) 2.5 V (nominal) and be decoupled from GND with suitable decoupling capacitors to reduce noise. For more information, refer to Actel's *Using ProASIC^{PLUS} Clock Conditioning Circuits* application note. If the clock conditioning circuitry is not used in a design, AVDD can either be left floating or tied to 2.5 V.

AGND **PLL Power Ground**

The analog ground can be connected to the system ground. For more information, refer to Actel's *Using ProASIC^{PLUS} Clock Conditioning Circuits* application note. If the PLLs or clock conditioning circuitry are not used in a design, AGND should be tied to GND.