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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	73728
Number of I/O	186
Number of Gates	300000
Voltage - Supply	2.3V ~ 2.7V
Mounting Type	Surface Mount
Operating Temperature	-55°C ~ 125°C (TC)
Package / Case	256-LBGA
Supplier Device Package	256-FPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/apa300-fg256m

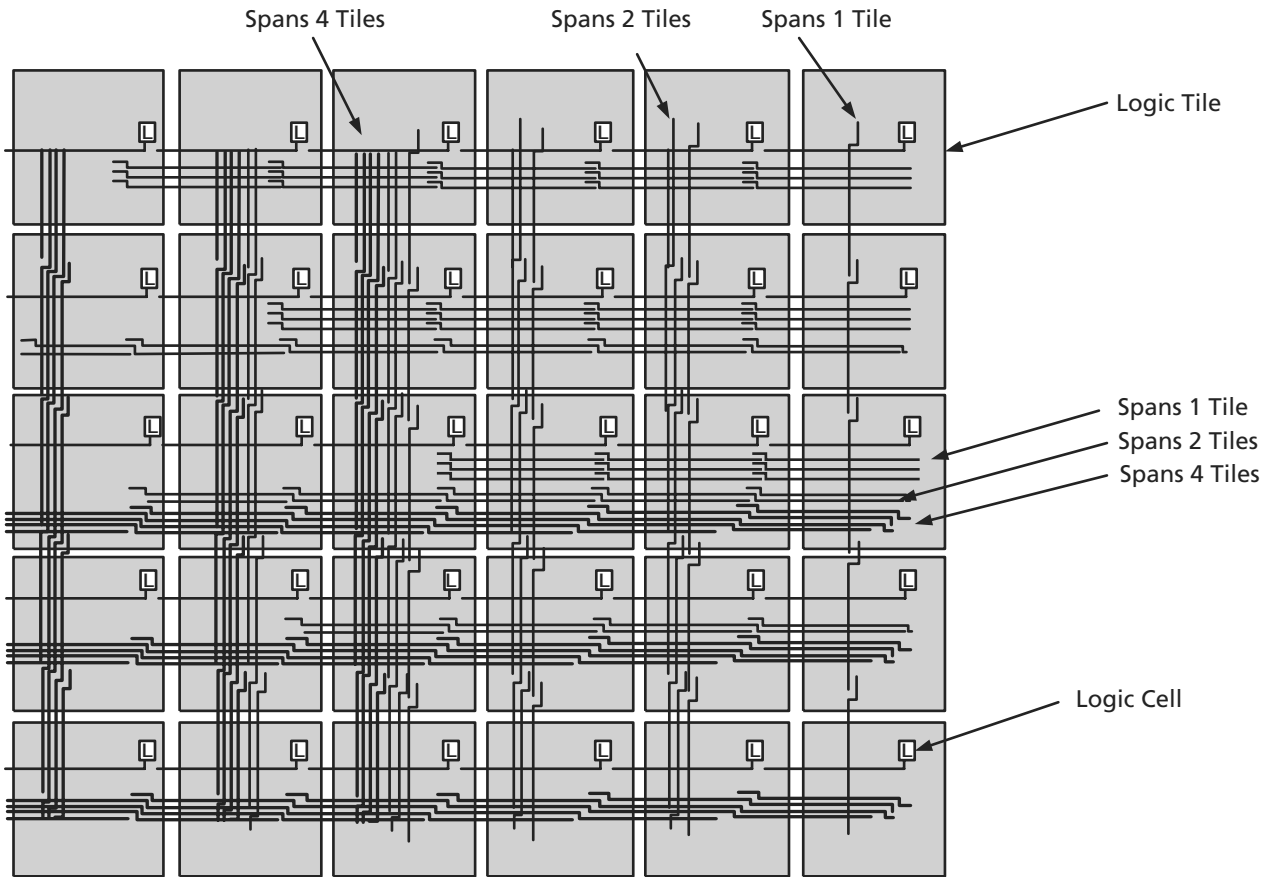
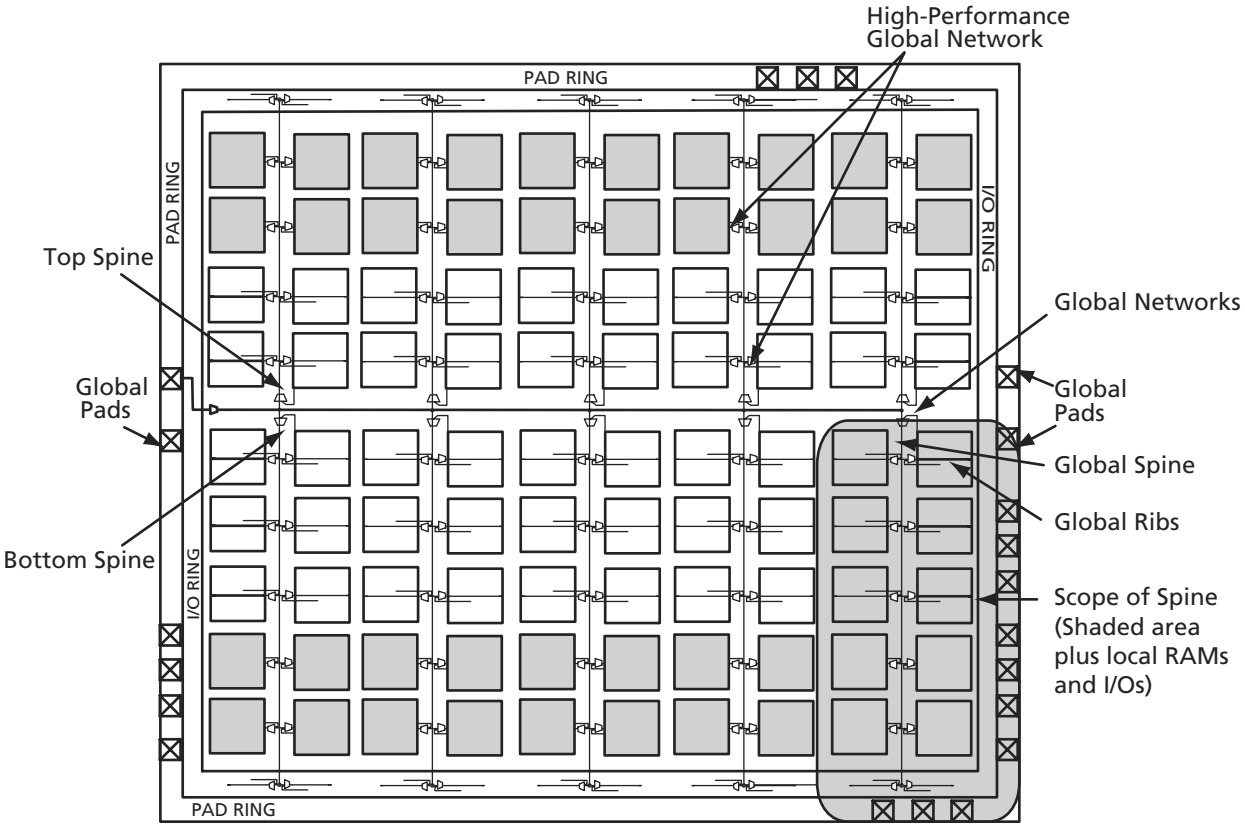


Figure 1-5 • **Efficient Long-Line Resources**



Note: *This figure shows routing for only one global path.*

Figure 1-7 • **High-Performance Global Network**

Table 1-1 • **Clock Spines**

	APA075	APA150	APA300	APA450	APA600	APA750	APA1000
Global Clock Networks (Trees)	4	4	4	4	4	4	4
Clock Spines/Tree	6	8	8	12	14	16	22
Total Spines	24	32	32	48	56	64	88
Top or Bottom Spine Height (Tiles)	16	24	32	32	48	64	80
Tiles in Each Top or Bottom Spine	512	768	1,024	1,024	1,536	2,048	2,560
Total Tiles	3,072	6,144	8,192	12,288	21,504	32,768	56,320

The TAP controller receives two control inputs (TMS and TCK) and generates control and clock signals for the rest of the test logic architecture. On power-up, the TAP controller enters the Test-Logic-Reset state. To guarantee a reset of the controller from any of the possible states, TMS must remain high for five TCK cycles. The TRST pin may also be used to asynchronously place the TAP controller in the Test-Logic-Reset state.

ProASIC^PLUS devices support three types of test data registers: bypass, device identification, and boundary scan. The bypass register is selected when no other register needs to be accessed in a device. This speeds up test data transfer to other devices in a test data path. The 32-bit device identification register is a shift register with four fields (lowest significant byte (LSB), ID number, part number and version). The boundary-scan register observes and controls the state of each I/O pin.

Each I/O cell has three boundary-scan register cells, each with a serial-in, serial-out, parallel-in, and parallel-out pin. The serial pins are used to serially connect all the boundary-scan register cells in a device into a boundary-scan register chain, which starts at the TDI pin and ends at the TDO pin. The parallel ports are connected to the internal core logic tile and the input, output, and control ports of an I/O buffer to capture and load data into the register to control or observe the logic state of each I/O.

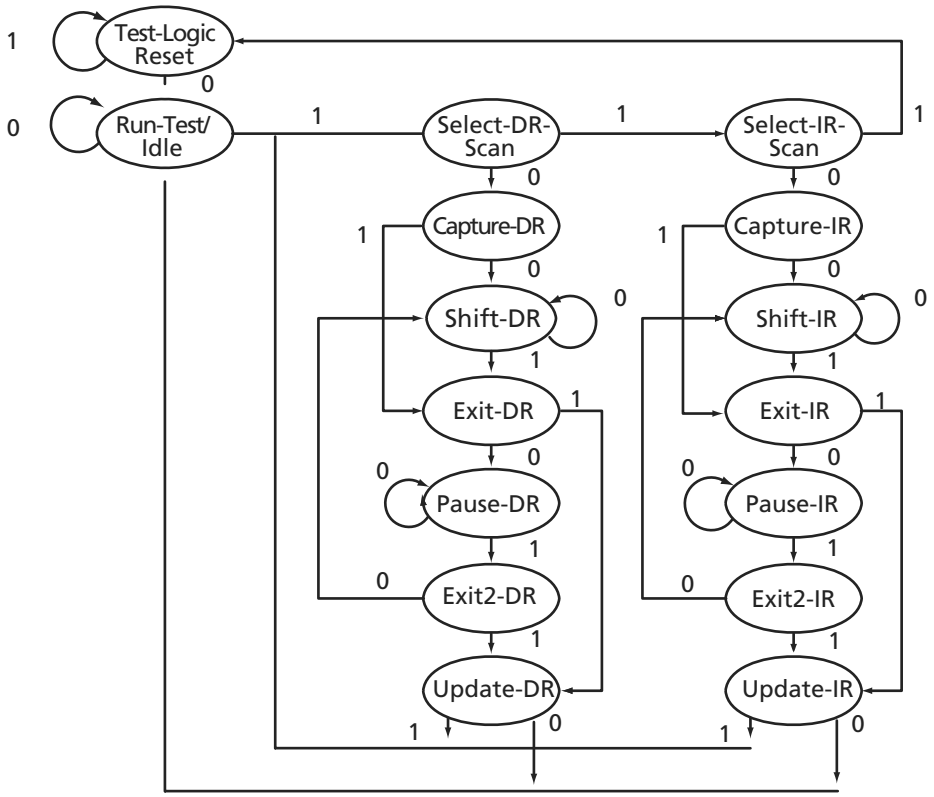


Figure 1-13 • **TAP Controller State Diagram**

Timing Control and Characteristics

ProASIC^PLUS Clock Management System

ProASIC^PLUS devices provide designers with very flexible clock conditioning capabilities. Each member of the ProASIC^PLUS family contains two phase-locked loop (PLL) blocks which perform the following functions:

- Clock Phase Adjustment via Programmable Delay (250 ps steps from –7 ns to +8 ns)
- Clock Skew Minimization
- Clock Frequency Synthesis

Each PLL has the following key features:

- Input Frequency Range (f_{IN}) = 1.5 to 180 MHz
- Feedback Frequency Range (f_{VCO}) = 24 to 180 MHz
- Output Frequency Range (f_{OUT}) = 8 to 180 MHz
- Output Phase Shift = 0 ° and 180 °
- Output Duty Cycle = 50%
- Low Output Jitter (max at 25°C)
  - f_{VCO} <10 MHz. Jitter ±1% or better
  - 10 MHz < f_{VCO} < 60 MHz. Jitter ±2% or better
  - f_{VCO} > 60 MHz. Jitter ±1% or better

Note: Jitter(ps) = Jitter(%)* period

For Example:

Jitter in picoseconds at 100 MHz = 0.01 * (1/100E6) = 100 ps

- Maximum Acquisition Time = 80 µs for f_{VCO} > 40 MHz
  = 30 µs for f_{VCO} < 40 MHz
- Low Power Consumption – 6.9 mW (max – analog supply) + 7.0µW/MHz (max – digital supply)

Physical Implementation

Each side of the chip contains a clock conditioning circuit based on a 180 MHz PLL block (Figure 1-14 on page 1-14). Two global multiplexed lines extend along each side of the chip to provide bidirectional access to the PLL on that side (neither MUX can be connected to the opposite side's PLL). Each global line has optional LVPECL input pads (described below). The global lines may be driven by either the LVPECL global input pad or the outputs from the PLL block, or both. Each global line can be driven by a different output from the PLL. Unused global pins can be configured as regular I/Os or left unconnected. They default to an input with pull-up. The two signals available to drive the global networks are as follows (Figure 1-15 on page 1-15, Table 1-7 on page 1-15, and Table 1-8 on page 1-16):

Global A (secondary clock)

- Output from Global MUX A
- Conditioned version of PLL output (f_{OUT}) – delayed or advanced
- Divided version of either of the above
- Further delayed version of either of the above (0.25 ns, 0.50 ns, or 4.00 ns delay)[1]

Global B

- Output from Global MUX B
- Delayed or advanced version of f_{OUT}
- Divided version of either of the above
- Further delayed version of either of the above (0.25 ns, 0.50 ns, or 4.00 ns delay)[2]

Functional Description

Each PLL block contains four programmable dividers as shown in Figure 1-14 on page 1-14. These allow frequency scaling of the input clock signal as follows:

- The n divider divides the input clock by integer factors from 1 to 32.
- The m divider in the feedback path allows multiplication of the input clock by integer factors ranging from 1 to 64.
- The two dividers together can implement any combination of multiplication and division resulting in a clock frequency between 24 and 180 MHz exiting the PLL core. This clock has a fixed 50% duty cycle.
- The output frequency of the PLL core is given by the formula EQ 1-1 (f_{REF} is the reference clock frequency):

$$f_{OUT} = f_{REF} * m/n \quad \textit{EQ 1-1}$$

- The third and fourth dividers (u and v) permit the signals applied to the global network to each be further divided by integer factors ranging from 1 to 4.

The implementations shown in EQ2 and EQ3 enable the user to define a wide range of frequency multiplier and divisors.

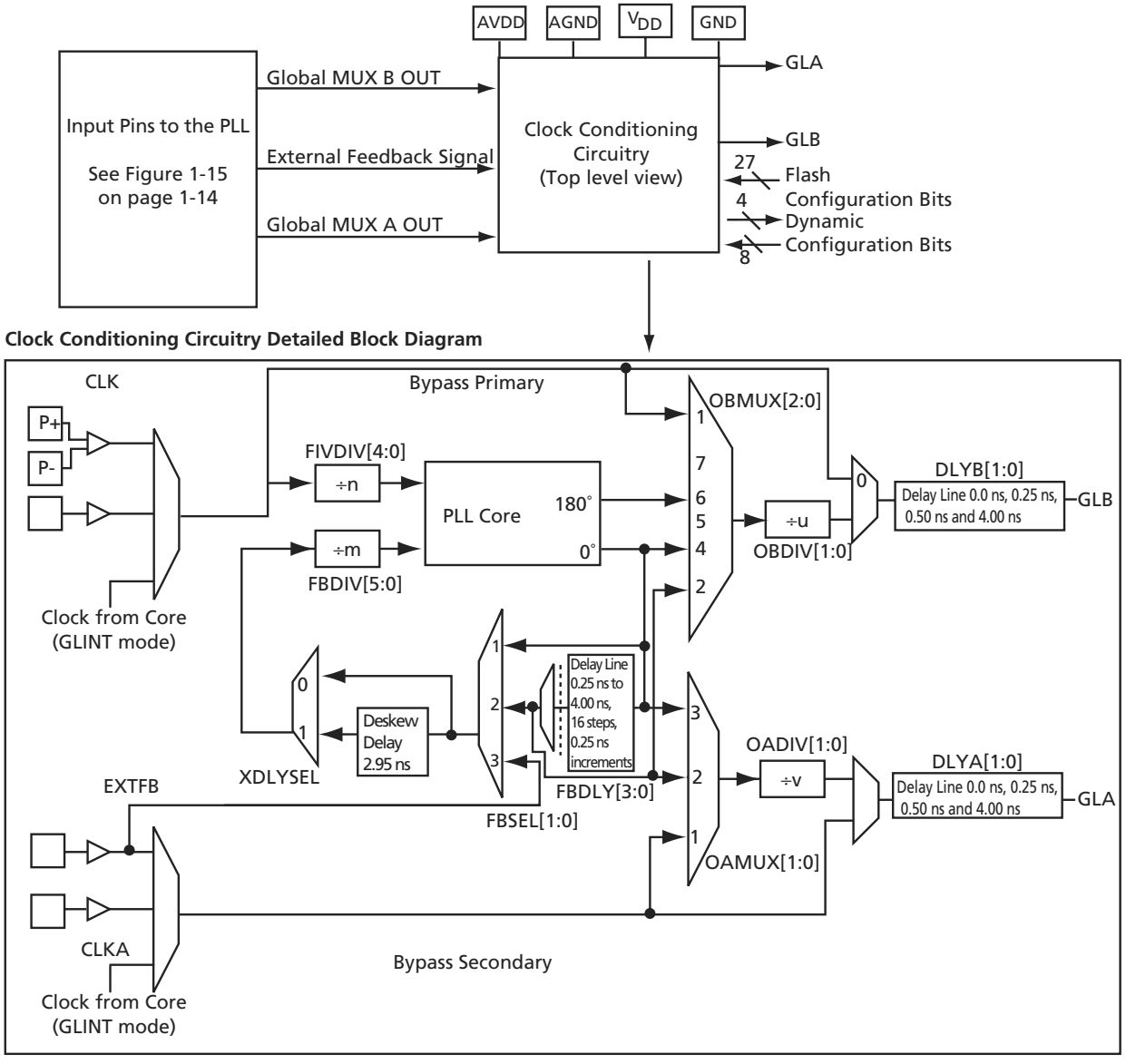
$$f_{GLB} = m/(n*u) \quad \textit{EQ 1-2}$$

$$f_{GLA} = m/(n*v) \quad \textit{EQ 1-3}$$

1. This mode is available through the delay feature of the Global MUX driver.

enable the user to define a wide range of frequency multipliers and divisors. The clock conditioning circuit can advance or delay the clock up to 8 ns (in increments of 0.25 ns) relative to the positive edge of the incoming reference clock. The system also allows for the selection of output frequency clock phases of 0° and 180°.

Prior to the application of signals to the rib drivers, they pass through programmable delay units, one per global network. These units permit the delaying of global signals relative to other signals to assist in the control of input set-up times. Not all possible combinations of input and output modes can be used. The degrees of freedom available in the bidirectional global pad system and in the clock conditioning circuit have been restricted. This avoids unnecessary and unwieldy design kit and software work.



Notes:

1. *FBDLY is a programmable delay line from 0 to 4 ns in 250 ps increments.*
2. *DLYA and DLYB are programmable delay lines, each with selectable values 0 ps, 250 ps, 500 ps, and 4 ns.*
3. *OBDIV will also divide the phase-shift since it takes place after the PLL Core.*

Figure 1-14 • **PLL Block – Top-Level View and Detailed PLL Block Diagram**

Table 1-8 • **Clock-Conditioning Circuitry Delay-Line Settings**

Delay Line	Delay Value (ns)
DLYB	
0	0
1	+0.25
2	+0.50
3	+4.0
DLYA	
0	0
1	+0.25
2	+0.50
3	+4.0

Lock Signal

An active-high Lock signal (added via the SmartGen PLL development tool) indicates that the PLL has locked to the incoming clock signal. The PLL will acquire and maintain lock even when there is jitter on the incoming clock signal. The PLL will maintain lock with an input jitter up to 5% of the input period, with a maximum of 5 ns. Users can employ the Lock signal as a soft reset of the logic driven by GLB and/or GLA. Note if F_{IN} is not within specified frequencies, then both the F_{OUT} and lock signal are indeterminate.

PLL Configuration Options

The PLL can be configured during design (via Flash-configuration bits set in the programming bitstream) or dynamically during device operation, thus eliminating the need to reprogram the device. The dynamic configuration bits are loaded into a serial-in/parallel-out shift register provided in the clock conditioning circuit. The shift register can be accessed either from user logic within the device or via the JTAG port. Another option is internal dynamic configuration via user-designed hardware. Refer to Actel's *ProASIC^PLUS PLL Dynamic Reconfiguration Using JTAG* application note for more information.

For information on the clock conditioning circuit, refer to Actel's *Using ProASIC^PLUS Clock Conditioning Circuits* application note.

Sample Implementations

Frequency Synthesis

Figure 1-16 on page 1-17 illustrates an example where the PLL is used to multiply a 33 MHz external clock up to 133 MHz. Figure 1-17 on page 1-17 uses two dividers to synthesize a 50 MHz output clock from a 40 MHz input reference clock. The input frequency of 40 MHz is multiplied by five and divided by four, giving an output clock (GLB) frequency of 50 MHz. When dividers are used, a given ratio can be generated in multiple ways, allowing the user to stay within the operating frequency ranges of the PLL. For example, in this case the input divider could have been two and the output divider also two, giving us a division of the input frequency by four to go with the feedback loop division (effective multiplication) by five.

Adjustable Clock Delay

Figure 1-18 on page 1-18 illustrates the delay of the input clock by employing one of the adjustable delay lines. This is easily done in ProASIC^PLUS by bypassing the PLL core entirely and using the output delay line. Notice also that the output clock can be effectively advanced relative to the input clock by using the delay line in the feedback path. This is shown in Figure 1-19 on page 1-18.

Clock Skew Minimization

Figure 1-20 on page 1-19 indicates how feedback from the clock network can be used to create minimal skew between the distributed clock network and the input clock. The input clock is fed to the reference clock input of the PLL. The output clock (GLA) feeds a clock network. The feedback input to the PLL uses a clock input delayed by a routing network. The PLL then adjusts the phase of the input clock to match the delayed clock, thus providing nearly zero effective skew between the two clocks. Refer to Actel's *Using ProASIC^PLUS Clock Conditioning Circuits* application note for more information.

Table 1-12 • **ProASIC^PLUS Memory Configurations by Device**

Device	Bottom	Top	Maximum Width		Maximum Depth	
			D	W	D	W
APA750	32	32	256	288	4,096	9
APA1000	44	44	256	396	5,632	9

Table 1-13 • **Basic Memory Configurations**

Type	Write Access	Read Access	Parity	Library Cell Name
RAM	Asynchronous	Asynchronous	Checked	RAM256x9AA
RAM	Asynchronous	Asynchronous	Generated	RAM256x9AAP
RAM	Asynchronous	Synchronous Transparent	Checked	RAM256x9AST
RAM	Asynchronous	Synchronous Transparent	Generated	RAM256x9ASTP
RAM	Asynchronous	Synchronous Pipelined	Checked	RAM256x9ASR
RAM	Asynchronous	Synchronous Pipelined	Generated	RAM256x9ASRP
RAM	Synchronous	Asynchronous	Checked	RAM256x9SA
RAM	Synchronous	Asynchronous	Generated	RAM256xSAP
RAM	Synchronous	Synchronous Transparent	Checked	RAM256x9SST
RAM	Synchronous	Synchronous Transparent	Generated	RAM256x9SSTP
RAM	Synchronous	Synchronous Pipelined	Checked	RAM256x9SSR
RAM	Synchronous	Synchronous Pipelined	Generated	RAM256x9SSRP
FIFO	Asynchronous	Asynchronous	Checked	FIFO256x9AA
FIFO	Asynchronous	Asynchronous	Generated	FIFO256x9AAP
FIFO	Asynchronous	Synchronous Transparent	Checked	FIFO256x9AST
FIFO	Asynchronous	Synchronous Transparent	Generated	FIFO256x9ASTP
FIFO	Asynchronous	Synchronous Pipelined	Checked	FIFO256x9ASR
FIFO	Asynchronous	Synchronous Pipelined	Generated	FIFO256x9ASRP
FIFO	Synchronous	Asynchronous	Checked	FIFO256x9SA
FIFO	Synchronous	Asynchronous	Generated	FIFO256x9SAP
FIFO	Synchronous	Synchronous Transparent	Checked	FIFO256x9SST
FIFO	Synchronous	Synchronous Transparent	Generated	FIFO256x9SSTP
FIFO	Synchronous	Synchronous Pipelined	Checked	FIFO256x9SSR
FIFO	Synchronous	Synchronous Pipelined	Generated	FIFO256x9SSRP

Operating Conditions

Standard and –F parts are the same unless otherwise noted. All –F parts are only available as commercial.

Table 1-17 • **Absolute Maximum Ratings***

Parameter	Condition	Minimum	Maximum	Units
Supply Voltage Core (V_{DD})		–0.3	3.0	V
Supply Voltage I/O Ring (V_{DDP})		–0.3	4.0	V
DC Input Voltage		–0.3	V_{DDP} + 0.3	V
PCI DC Input Voltage		–1.0	V_{DDP} + 1.0	V
PCI DC Input Clamp Current (absolute)	V_{IN} < –1 or V_{IN} = V_{DDP} + 1 V	10		mA
LVPECL Input Voltage		–0.3	V_{DDP} + 0.5	V
GND		0	0	V

Note: **Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. Devices should not be operated outside the Recommended Operating Conditions.*

Table 1-18 • **Programming, Storage, and Operating Limits**

			Storage Temperature		Operating
Product Grade	Programming Cycles (min.)	Program Retention (min.)	Min.	Max.	T_J Max. Junction Temperature
Commercial	500	20 years	–55°C	110°C	110°C
Industrial	500	20 years	–55°C	110°C	110°C
Military	100	Refer to Table 1-19 on page 1-35	–65°C	150°C	150°C
MIL-STD-883	100	Refer to Table 1-19 on page 1-35	–65°C	150°C	150°C

Performance Retention

For devices operated and stored at 110°C or less, the performance retention period is 20 years after programming. For devices operated and stored at temperatures greater than 110°C, refer to Table 1-19 on page 1-35 to determine the performance retention period. Actel does not guarantee performance if the performance retention period is exceeded. Designers can determine the performance retention period from the following table.

Evaluate the percentage of time spent at the highest temperature, then determine the next highest temperature to which the device will be exposed. In Table 1-19 on page 1-35, find the temperature profile that most closely matches the application.

Example – the ambient temperature of a system cycles between 100°C (25% of the time) and 50°C (75% of the time). No forced ventilation cooling system is in use. An APA600-PQ208M FPGA operates in the system, dissipating 1 W. The package thermal resistance (junction-to-ambient) in still air Θ_{ja} is 20°C/W, indicating that the junction temperature of the FPGA will be 120°C (25% of the time) and 70°C (75% of the time). The entry in Table 1-19 on page 1-35, which most closely matches the application, is 25% at 125°C with 75% at 110°C. Performance retention in this example is at least 16.0 years.

Note that exceeding the stated retention period may result in a performance degradation in the FPGA below the worst-case performance indicated in the Actel Timer. To ensure that performance does not degrade below the worst-case values in the Actel Timer, the FPGA must be reprogrammed within the performance retention period. In addition, note that performance retention is independent of whether or not the FPGA is operating. The retention period of a device in storage at a given temperature will be the same as the retention period of a device operating at that junction temperature.

Table 1-22 • **DC Electrical Specifications (V_{DDP} = 2.5 V ±0.2V)**

Symbol	Parameter	Conditions		Commercial/Industrial/ Military/MIL-STD-883[1, 2] Min.	Typ.	Max.	Units
V_{OH}	Output High Voltage						
	High Drive (OB25LPH)	I_{OH} = –6 mA		2.1			
		I_{OH} = –12 mA		2.0			
		I_{OH} = –24 mA		1.7			V
	Low Drive (OB25LPL)	I_{OH} = –3 mA		2.1			
		I_{OH} = –6 mA		1.9			
		I_{OH} = –8 mA		1.7			
V_{OL}	Output Low Voltage						
	High Drive (OB25LPH)	I_{OL} = 8 mA				0.2	
		I_{OL} = 15 mA				0.4	
		I_{OL} = 24 mA				0.7	V
	Low Drive (OB25LPL)	I_{OL} = 4 mA				0.2	
		I_{OL} = 8 mA				0.4	
		I_{OL} = 15 mA				0.7	
V_{IH}[6]	Input High Voltage			1.7		V_{DDP} + 0.3	V
V_{IL}[7]	Input Low Voltage			–0.3		0.7	V
$R_{WEAKPULLUP}$	Weak Pull-up Resistance (OTB25LPU)	$V_{IN} \geq$ 1.25 V		6		56	kΩ
HYST	Input Hysteresis Schmitt	See Table 1-4 on page 1-9		0.3	0.35	0.45	V
I_{IN}	Input Current	with pull up (V_{IN} = GND)		–240		– 20	µA
		without pull up (V_{IN} = GND or V_{DD})		–10		10	µA
I_{DDQ}	Quiescent Supply Current (standby) Commercial	V_{IN} = GND[4] or V_{DD}	Std.		5.0	15	mA
			–F[3]		5.0	25	mA
I_{DDQ}	Quiescent Supply Current (standby) Industrial	V_{IN} = GND[4] or V_{DD}	Std.		5.0	20	mA
I_{DDQ}	Quiescent Supply Current (standby) Military/MIL-STD-883	V_{IN} = GND[4] or V_{DD}	Std.		5.0	25	mA
I_{OZ}	Tristate Output Leakage Current	V_{OH} = GND or V_{DD}	Std.	–10		10	µA
			–F[3, 5]	–10		100	µA

Notes:

1. *All process conditions. Commercial/Industrial: Junction Temperature: –40 to +110°C.*
2. *All process conditions. Military: Junction Temperature: –55 to +150°C.*
3. *All –F parts are available only as commercial.*
4. *No pull-up resistor.*
5. *This will not exceed 2 mA total per device.*
6. *During transitions, the input signal may overshoot to V_{DDP} +1.0V for a limited time of no larger than 10% of the duty cycle.*
7. *During transitions, the input signal may undershoot to -1.0V for a limited time of no larger than 10% of the duty cycle.*

Table 1-33 • **Worst-Case Military Conditions**
V_{DDP} = 3.0V, V_{DD} = 2.3V, 35 pF load, T_J = 125°C for Military/MIL-STD-883

Macro Type	Description	Max. t_{DLH}[1] Std.	Max. t_{DHL}[2] Std.	Units
OB33PH	3.3V, PCI Output Current, High Slew Rate	2.1	2.3	ns
OB33PN	3.3V, High Output Current, Nominal Slew Rate	2.5	3.2	ns
OB33PL	3.3V, High Output Current, Low Slew Rate	2.7	3.5	ns
OB33LH	3.3V, Low Output Current, High Slew Rate	2.7	4.3	ns
OB33LN	3.3V, Low Output Current, Nominal Slew Rate	3.3	4.7	ns
OB33LL	3.3V, Low Output Current, Low Slew Rate	3.3	6.1	ns

Notes:

1. *t_{DLH} = Data-to-Pad High*
2. *t_{DHL} = Data-to-Pad Low*

Table 1-34 • **Worst-Case Military Conditions**
V_{DDP} = 2.3 V, V_{DD} = 2.3V, 35 pF load, T_J = 125°C for Military/MIL-STD-883

Macro Type	Description	Max. t_{DLH}[1] Std.	Max. t_{DHL}[2] Std.	Units
OB25LPHH	2.5V, Low Power, High Output Current, High Slew Rate[3]	2.3	2.4	ns
OB25LPHN	2.5V, Low Power, High Output Current, Nominal Slew Rate[3]	2.7	3.3	ns
OB25LPHL	2.5V, Low Power, High Output Current, Low Slew Rate[3]	3.2	3.5	ns
OB25LPLH	2.5V, Low Power, Low Output Current, High Slew Rate[3]	3.0	5.0	ns
OB25LPLN	2.5V, Low Power, Low Output Current, Nominal Slew Rate[3]	3.9	4.6	ns
OB25LPLL	2.5V, Low Power, Low Output Current, Low Slew Rate[3]	4.3	5.7	ns

Notes:

1. *t_{DLH} = Data-to-Pad High*
2. *t_{DHL} = Data-to-Pad Low*
3. *Low power I/O work with V_{DDP}=2.5V ±10% only. V_{DDP}=2.3V for delays.*

Input Buffer Delays

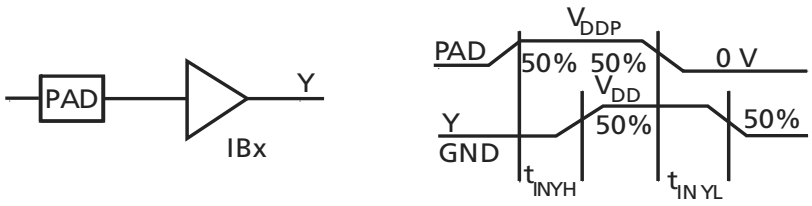


Figure 1-28 • **Input Buffer Delays**

Table 1-35 • **Worst-Case Commercial Conditions**
V_{DDP} = 3.0 V, V_{DD} = 2.3 V, T_J = 70°C

Macro Type	Description	Max. t_{INYH}[1]		Max. t_{INYL}[2]		Units
		Std.	–F	Std.	–F	
IB33	3.3 V, CMOS Input Levels[3], No Pull-up Resistor	0.4	0.5	0.6	0.7	ns
IB33S	3.3 V, CMOS Input Levels[3], No Pull-up Resistor, Schmitt Trigger	0.6	0.7	0.8	0.9	ns

Notes:

1. *t_{INYH} = Input Pad-to-Y High*
2. *t_{INYL} = Input Pad-to-Y Low*
3. *LVTTL delays are the same as CMOS delays.*
4. *For LP Macros, V_{DDP}=2.3 V for delays.*
5. *All –F parts are only available as commercial.*

Table 1-36 • **Worst-Case Commercial Conditions**
V_{DDP} = 2.3 V, V_{DD} = 2.3 V, T_J = 70°C

Macro Type	Description	Max. t_{INYH}[1]		Max. t_{INYL}[2]		Units
		Std.	–F	Std.	–F	
IB25LP	2.5 V, CMOS Input Levels[3], Low Power	0.9	1.1	0.6	0.8	ns
IB25LPS	2.5 V, CMOS Input Levels[3], Low Power, Schmitt Trigger	0.7	0.9	0.9	1.1	ns

Notes:

1. *t_{INYH} = Input Pad-to-Y High*
2. *t_{INYL} = Input Pad-to-Y Low*
3. *LVTTL delays are the same as CMOS delays.*
4. *For LP Macros, V_{DDP}=2.3 V for delays.*
5. *All –F parts are only available as commercial.*

Table 1-37 • **Worst-Case Military Conditions**
V_{DDP} = 3.0V, V_{DD} = 2.3V, T_J = 125°C for Military/MIL-STD-883

Macro Type	Description	Max. t_{INYH}[1]	Max. t_{INYL}[2]	Units
		Std.	Std.	
IB33	3.3V, CMOS Input Levels[3], No Pull-up Resistor	0.5	0.6	ns
IB33S	3.3V, CMOS Input Levels[3], No Pull-up Resistor, Schmitt Trigger	0.6	0.8	ns

Notes:

1. *t_{INYH} = Input Pad-to-Y High*
2. *t_{INYL} = Input Pad-to-Y Low*
3. *LVTTL delays are the same as CMOS delays.*
4. *For LP Macros, V_{DDP}=2.3V for delays.*

Table 1-38 • **Worst-Case Military Conditions**
V_{DDP} = 2.3V, V_{DD} = 2.3V, T_J = 125°C for Military/MIL-STD-883

Macro Type	Description	Max. t_{INYH}[1]	Max. t_{INYL}[2]	Units
		Std.	Std.	
IB25LP	2.5V, CMOS Input Levels[3], Low Power	0.9	0.7	ns
IB25LPS	2.5V, CMOS Input Levels[3], Low Power, Schmitt Trigger	0.8	1.0	ns

Notes:

1. *t_{INYH} = Input Pad-to-Y High*
2. *t_{INYL} = Input Pad-to-Y Low*
3. *LVTTL delays are the same as CMOS delays.*
4. *For LP Macros, V_{DDP}=2.3V for delays.*

Table 1-50 • **JTAG Switching Characteristics**

Description	Symbol	Min	Max	Unit
Output delay from TCK falling to TDI, TMS	t_{TCKTDI}	–4	4	ns
TDO Setup time before TCK rising	t_{TDOTCK}	10		ns
TDO Hold time after TCK rising	t_{TCKTDO}	0		ns
TCK period	t_{TCK}	100 [2]	1,000	ns
RCK period	t_{RCK}	100	1,000	ns

Notes:

1. *For DC electrical specifications of the JTAG pins (TCK, TDI, TMS, TDO, TRST), refer to Table 1-22 on page 1-37 when V_{DDP} = 2.5 V and Table 1-24 on page 1-41 when V_{DDP} = 3.3 V.*
2. *If RCK is being used, there is no minimum on the TCK period.*

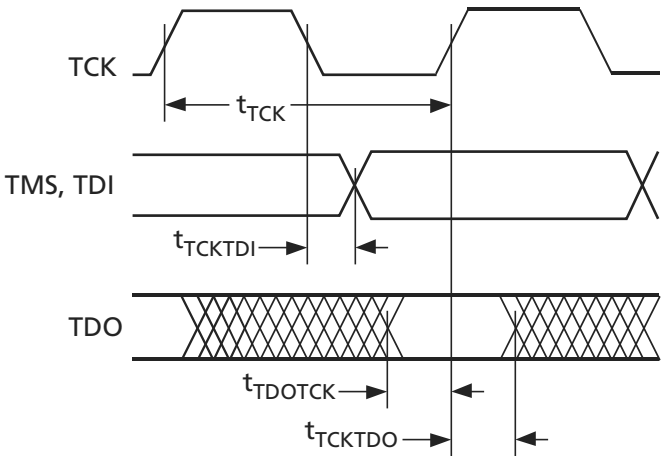
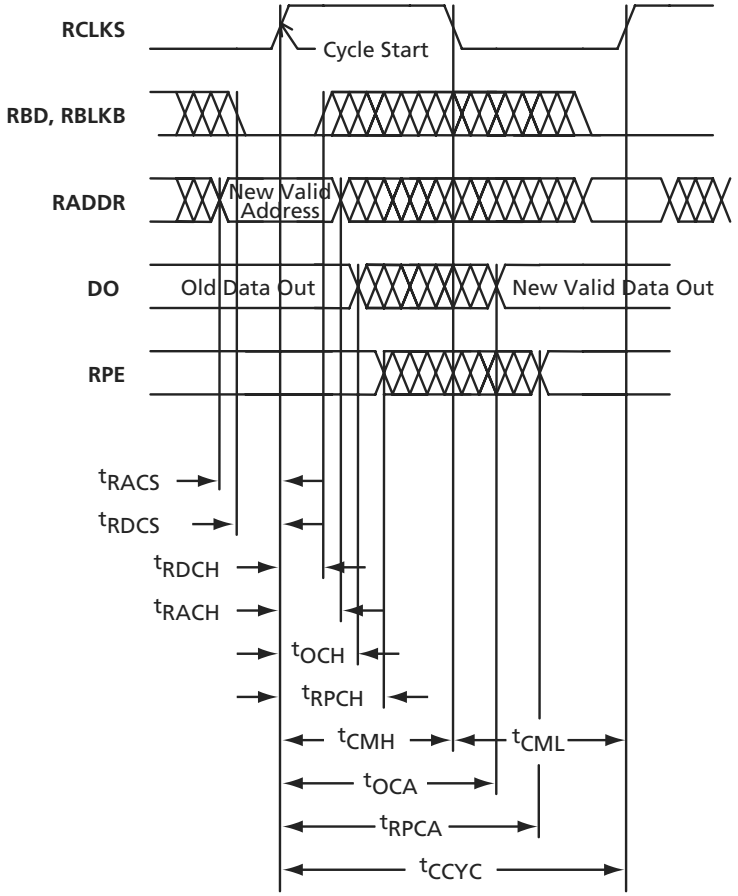


Figure 1-30 • **JTAG Operation Timing**

Synchronous SRAM Read, Access Timed Output Strobe (Synchronous Transparent)



Note: *The plot shows the normal operation status.*

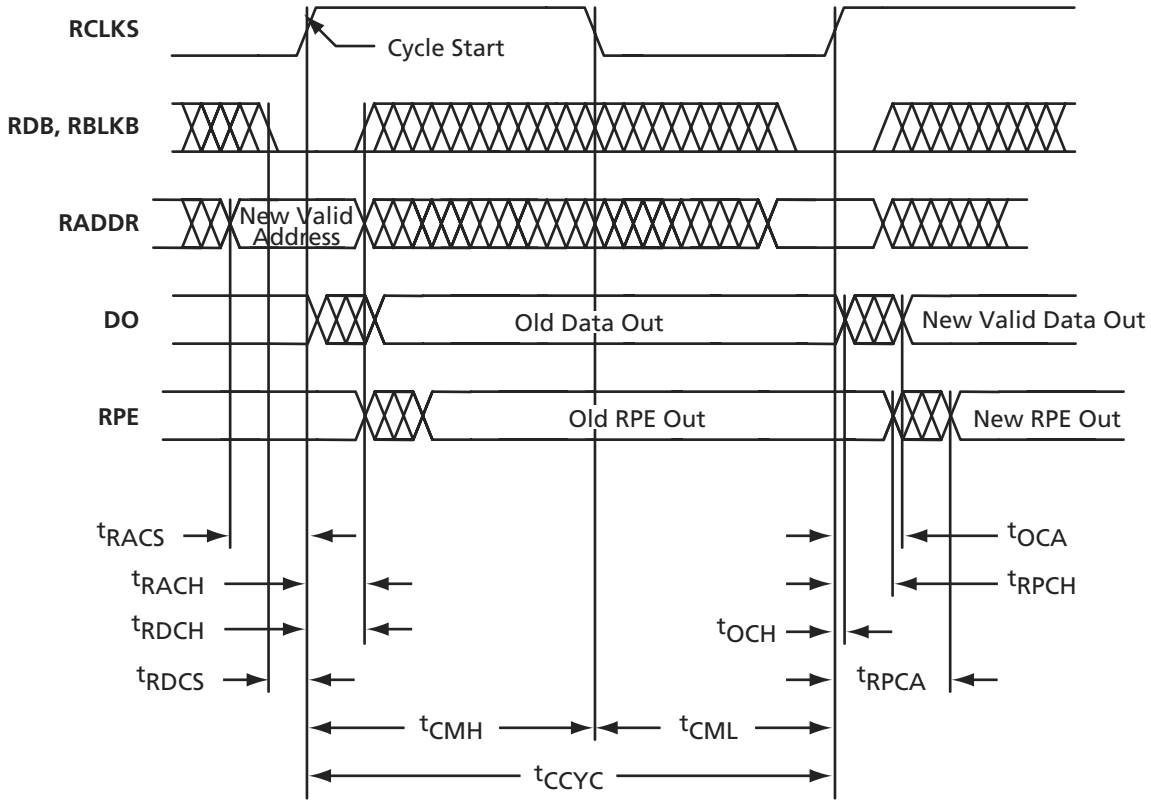
Figure 1-31 • **Synchronous SRAM Read, Access Timed Output Strobe (Synchronous Transparent)**

Table 1-52 • **T_J = 0°C to 110°C; V_{DD} = 2.3 V to 2.7 V for Commercial/industrial**
T_J = –55°C to 150°C, V_{DD} = 2.3 V to 2.7 V for Military/MIL-STD-883

Symbol t_{xxx}	Description	Min.	Max.	Units	Notes
CCYC	Cycle time	7.5		ns	
CMH	Clock high phase	3.0		ns	
CML	Clock low phase	3.0		ns	
OCA	New DO access from RCLKS ↑	7.5		ns	
OCH	Old DO valid from RCLKS ↑		3.0	ns	
RACH	RADDR hold from RCLKS ↑	0.5		ns	
RACS	RADDR setup to RCLKS ↑	1.0		ns	
RDCH	RDB hold from RCLKS ↑	0.5		ns	
RDCS	RDB setup to RCLKS ↑	1.0		ns	
RPCA	New RPE access from RCLKS ↑	9.5		ns	
RPCH	Old RPE valid from RCLKS ↑		3.0	ns	

Note: *All –F speed grade devices are 20% slower than the standard numbers.*

Synchronous SRAM Read, Pipeline Mode Outputs (Synchronous Pipelined)



Note: *The plot shows the normal operation status.*

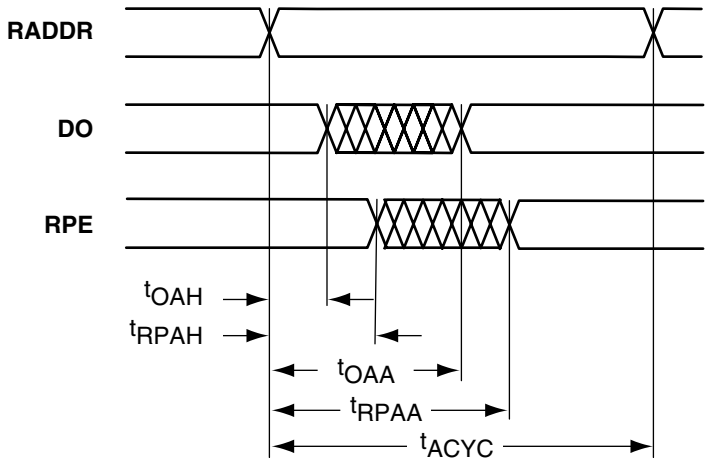
Figure 1-32 • **Synchronous SRAM Read, Pipeline Mode Outputs (Synchronous Pipelined)**

Table 1-53 • **T_J = 0°C to 110°C; V_{DD} = 2.3 V to 2.7 V for Commercial/industrial**
T_J = 0°C to 150°C, V_{DD} = 2.3 V to 2.7 V for Military/MIL-STD-883

Symbol t_{xxx}	Description	Min.	Max.	Units	Notes
CCYC	Cycle time	7.5		ns	
CMH	Clock high phase	3.0		ns	
CML	Clock low phase	3.0		ns	
OCA	New DO access from RCLKS ↑	2.0		ns	
OCH	Old DO valid from RCLKS ↑		0.75	ns	
RACH	RADDR hold from RCLKS ↑	0.5		ns	
RACS	RADDR setup to RCLKS ↑	1.0		ns	
RDCH	RDB hold from RCLKS ↑	0.5		ns	
RDCS	RDB setup to RCLKS ↑	1.0		ns	
RPCA	New RPE access from RCLKS ↑	4.0		ns	
RPCH	Old RPE valid from RCLKS ↑		1.0	ns	

Note: *All –F speed grade devices are 20% slower than the standard numbers.*

Asynchronous SRAM Read, Address Controlled, RDB=0



Note: *The plot shows the normal operation status.*

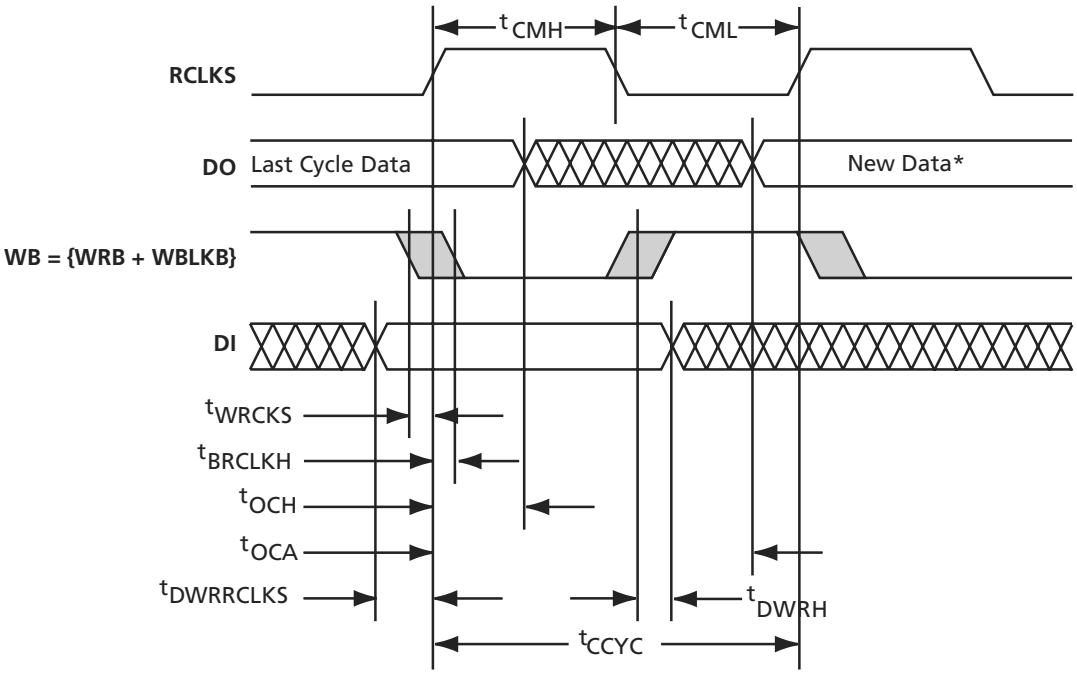
Figure 1-34 • **Asynchronous SRAM Read, Address Controlled, RDB=0**

Table 1-55 • **T_J = 0°C to 110°C; V_{DD} = 2.3 V to 2.7 V for Commercial/industrial**
T_J = –55°C to 150°C, V_{DD} = 2.3 V to 2.7 V for Military/MIL-STD-883B

Symbol t_{xxx}	Description	Min.	Max.	Units	Notes
ACYC	Read cycle time	7.5		ns	
OAA	New DO access from RADDR stable	7.5		ns	
OAH	Old DO hold from RADDR stable		3.0	ns	
RPAA	New RPE access from RADDR stable	10.0		ns	
RPAH	Old RPE hold from RADDR stable		3.0	ns	

Note: *All –F speed grade devices are 20% slower than the standard numbers.*

Asynchronous Write and Synchronous Read to the Same Location



* New data is read if WB ↓ occurs before setup time.
The stored data is read if WB ↓ occurs after hold time.

Note: *The plot shows the normal operation status.*

Figure 1-38 • **Asynchronous Write and Synchronous Read to the Same Location**

Table 1-59 • **T_J = 0°C to 110°C; V_{DD} = 2.3 V to 2.7 V for Commercial/industrial**
T_J = –55°C to 150°C, V_{DD} = 2.3 V to 2.7 V for Military/MIL-STD-883

Symbol t_{xxx}	Description	Min.	Max.	Units	Notes
CCYC	Cycle time	7.5		ns	
CMH	Clock high phase	3.0		ns	
CML	Clock low phase	3.0		ns	
WBRCLKS	WB ↓ to RCLKS ↑ setup time	–0.1		ns	
WBRCLKH	WB ↓ to RCLKS ↑ hold time		7.0	ns	
OCH	Old DO valid from RCLKS ↑		3.0	ns	OCA/OCH displayed for Access Timed Output
OCA	New DO valid from RCLKS ↑	7.5		ns	
DWRRCLKS	DI to RCLKS ↑ setup time	0		ns	
DWRH	DI to WB ↑ hold time		1.5	ns	

Notes:

1. *This behavior is valid for Access Timed Output and Pipelined Mode Output. The table shows the timings of an Access Timed Output.*
2. *In asynchronous write and synchronous read access to the same location, the new write data will be read out if the active write signal edge occurs before or at the same time as the active read clock edge. If WB changes to low after hold time, the data will be read.*
3. *A setup or hold time violation will result in unknown output data.*
4. *All –F speed grade devices are 20% slower than the standard numbers.*

Asynchronous FIFO Full and Empty Transitions

The asynchronous FIFO accepts writes and reads while not full or not empty. When the FIFO is full, all writes are inhibited. Conversely, when the FIFO is empty, all reads are inhibited. A problem is created if the FIFO is written to during the transition from full to not full, or read during the transition from empty to not empty. The exact time at which the write or read operation changes from inhibited to accepted after the read (write) signal which causes the transition from full or empty to not full or not empty is indeterminate. For slow cycles, this indeterminate period starts 1 ns after the RB (WB) transition, which deactivates full or not empty and ends 3 ns after the RB (WB) transition. For fast cycles, the indeterminate period ends 3 ns (7.5 ns – RDL (WRL)) after the RB (WB) transition, whichever is later (Table 1-1 on page 1-7).

The timing diagram for write is shown in Figure 1-38 on page 1-65. The timing diagram for read is shown in Figure 1-39 on page 1-66. For basic SRAM configurations, see Table 1-14 on page 1-25. When reset is asserted, the empty flag will be asserted, the counters will reset, the outputs go to zero, but the internal RAM is not erased.

Enclosed Timing Diagrams – FIFO Mode:

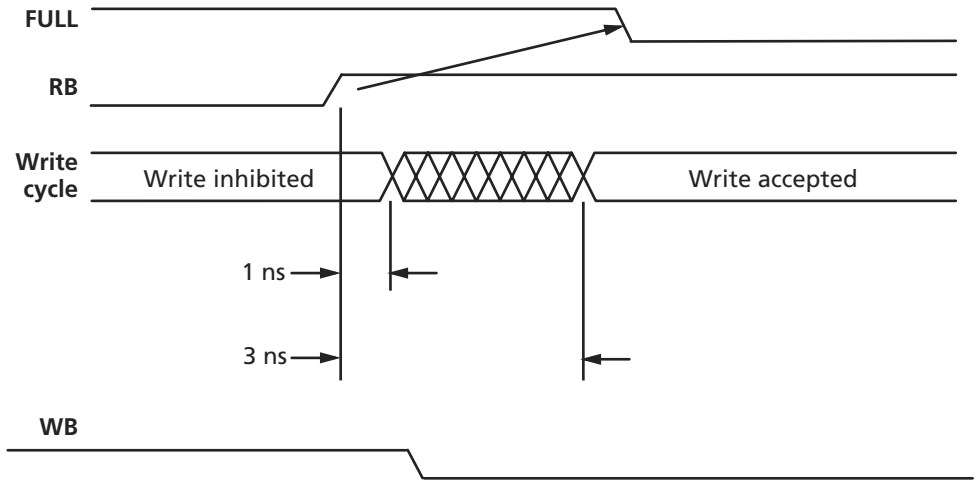
The following timing diagrams apply only to single cell; they are not applicable to cascaded cells. For more information, refer to the *ProASIC^PLUS RAM/FIFO Blocks* application note.

- "Asynchronous FIFO Read" section on page 1-70
- "Asynchronous FIFO Write" section on page 1-71
- "Synchronous FIFO Read, Access Timed Output Strobe (Synchronous Transparent)" section on page 1-72
- "Synchronous FIFO Read, Pipeline Mode Outputs (Synchronous Pipelined)" section on page 1-73
- "Synchronous FIFO Write" section on page 1-74
- "FIFO Reset" section on page 1-75

Table 1-62 • **Memory Block FIFO Interface Signals**

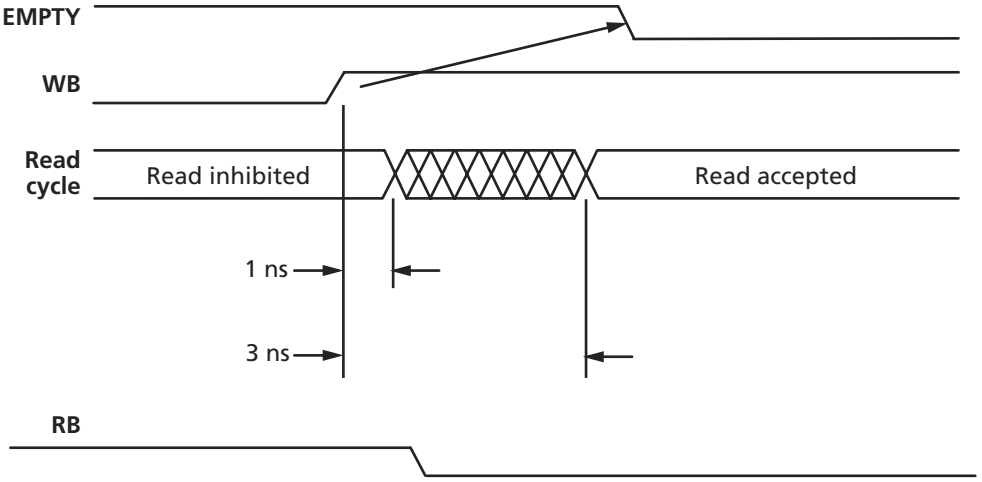
FIFO Signal	Bits	In/Out	Description
WCLKS	1	In	Write clock used for synchronization on write side
RCLKS	1	In	Read clock used for synchronization on read side
LEVEL <0:7>*	8	In	Direct configuration implements static flag logic
RBLKB	1	In	Read block select (active Low)
RDB	1	In	Read pulse (active Low)
RESET	1	In	Reset for FIFO pointers (active Low)
WBLKB	1	In	Write block select (active Low)
DI<0:8>	9	In	Input data bits <0:8>, <8> will be generated if PARGEN is true
WRB	1	In	Write pulse (active Low)
FULL, EMPTY	2	Out	FIFO flags. FULL prevents write and EMPTY prevents read
EQTH, GEQTH*	2	Out	EQTH is true when the FIFO holds the number of words specified by the LEVEL signal. GEQTH is true when the FIFO holds (LEVEL) words or more
DO<0:8>	9	Out	Output data bits <0:8>
RPE	1	Out	Read parity error (active High)
WPE	1	Out	Write parity error (active High)
LGDEP <0:2>	3	In	Configures DEPTH of the FIFO to $2^{(LGDEP+1)}$
PARODD	1	In	Selects Odd parity generation/detect when high, Even when low

Note: **LEVEL is always eight bits (0000.0000, 0000.0001). That means for values of DEPTH greater than 256, not all values will be possible, e.g. for DEPTH=512, the LEVEL can only have the values 2, 4, . . ., 512. The LEVEL signal circuit will generate signals that indicate whether the FIFO is exactly filled to the value of LEVEL (EQTH) or filled equal or higher (GEQTH) than the specified LEVEL. Since counting starts at 0, EQTH will become true when the FIFO holds (LEVEL+1) words for 512-bit FIFOs.*



Note: *All –F speed grade devices are 20% slower than the standard numbers.*

Figure 1-41 • **Write Timing Diagram**



Note: *All –F speed grade devices are 20% slower than the standard numbers.*

Figure 1-42 • **Read Timing Diagram**

Pin Description

User Pins

I/O **User Input/Output**

The I/O pin functions as an input, output, tristate, or bidirectional buffer. Input and output signal levels are compatible with standard LVTTL and LVCMOS specifications. Unused I/O pins are configured as inputs with pull-up resistors.

NC **No Connect**

To maintain compatibility with other Actel ProASIC^{PLUS} products, it is recommended that this pin not be connected to the circuitry on the board.

GL **Global Pin**

Low skew input pin for clock or other global signals. This pin can be configured with an internal pull-up resistor. When it is not connected to the global network or the clock conditioning circuit, it can be configured and used as a normal I/O.

GLMX **Global Multiplexing Pin**

Low skew input pin for clock or other global signals. This pin can be used in one of two special ways (refer to Actel's *Using ProASIC^{PLUS} Clock Conditioning Circuits*).

When the external feedback option is selected for the PLL block, this pin is routed as the external feedback source to the clock conditioning circuit.

In applications where two different signals access the same global net at different times through the use of GLMXx and GLMXLx macros, this pin will be fixed as one of the source pins.

This pin can be configured with an internal pull-up resistor. When it is not connected to the global network or the clock conditioning circuit, it can be configured and used as any normal I/O. If not used, the GLMXx pin will be configured as an input with pull-up.

Dedicated Pins

GND **Ground**

Common ground supply voltage.

V_{DD} **Logic Array Power Supply Pin**

2.5 V supply voltage.

V_{DDP} **I/O Pad Power Supply Pin**

2.5 V or 3.3 V supply voltage.

TMS **Test Mode Select**

The TMS pin controls the use of boundary-scan circuitry. This pin has an internal pull-up resistor.

TCK **Test Clock**

Clock input pin for boundary scan (maximum 10 MHz). Actel recommends adding a nominal 20 kΩ pull-up resistor to this pin.

TDI **Test Data In**

Serial input for boundary scan. A dedicated pull-up resistor is included to pull this pin high when not being driven.

TDO **Test Data Out**

Serial output for boundary scan. Actel recommends adding a nominal 20kΩ pull-up resistor to this pin.

TRST **Test Reset Input**

Asynchronous, active-low input pin for resetting boundary-scan circuitry. This pin has an internal pull-up resistor. For more information, please refer to *Power-up Behavior of ProASIC^{PLUS} Devices* application note.

Special Function Pins

RCK **Running Clock**

A free running clock is needed during programming if the programmer cannot guarantee that TCK will be uninterrupted. If not used, this pin has an internal pull-up and can be left floating.

NPECL **User Negative Input**

Provides high speed clock or data signals to the PLL block. If unused, leave the pin unconnected.

PPECL **User Positive Input**

Provides high speed clock or data signals to the PLL block. If unused, leave the pin unconnected.

AVDD **PLL Power Supply**

Analog V_{DD} should be V_{DD} (core voltage) 2.5 V (nominal) and be decoupled from GND with suitable decoupling capacitors to reduce noise. For more information, refer to Actel's *Using ProASIC^{PLUS} Clock Conditioning Circuits* application note. If the clock conditioning circuitry is not used in a design, AVDD can either be left floating or tied to 2.5 V.

AGND **PLL Power Ground**

The analog ground can be connected to the system ground. For more information, refer to Actel's *Using ProASIC^{PLUS} Clock Conditioning Circuits* application note. If the PLLs or clock conditioning circuitry are not used in a design, AGND should be tied to GND.