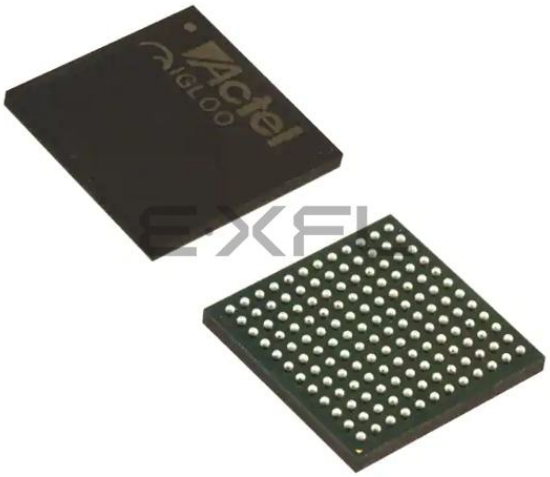

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	73728
Number of I/O	100
Number of Gates	300000
Voltage - Supply	2.3V ~ 2.7V
Mounting Type	Surface Mount
Operating Temperature	-55°C ~ 125°C (TC)
Package / Case	144-LBGA
Supplier Device Package	144-FPBGA (13x13)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/apa300-fgg144m

Routing Resources

The routing structure of ProASIC^PLUS devices is designed to provide high performance through a flexible four-level hierarchy of routing resources: ultra-fast local resources, efficient long-line resources, high-speed, very long-line resources, and high performance global networks.

The ultra-fast local resources are dedicated lines that allow the output of each tile to connect directly to every input of the eight surrounding tiles (Figure 1-4).

The efficient long-line resources provide routing for longer distances and higher fanout connections. These resources vary in length (spanning 1, 2, or 4 tiles), run both vertically and horizontally, and cover the entire ProASIC^PLUS device (Figure 1-5 on page 1-5). Each tile can drive signals onto the efficient long-line resources, which can in turn access every input of every tile. Active buffers are inserted automatically by routing software to limit the loading effects due to distance and fanout.

The high-speed, very long-line resources, which span the entire device with minimal delay, are used to route very long or very high fanout nets. (Figure 1-6 on page 1-6).

The high-performance global networks are low-skew, high fanout nets that are accessible from external pins or from internal logic (Figure 1-7 on page 1-7). These nets are typically used to distribute clocks, resets, and other high fanout nets requiring a minimum skew. The global networks are implemented as clock trees, and signals can be introduced at any junction. These can be employed hierarchically with signals accessing every input on all tiles.

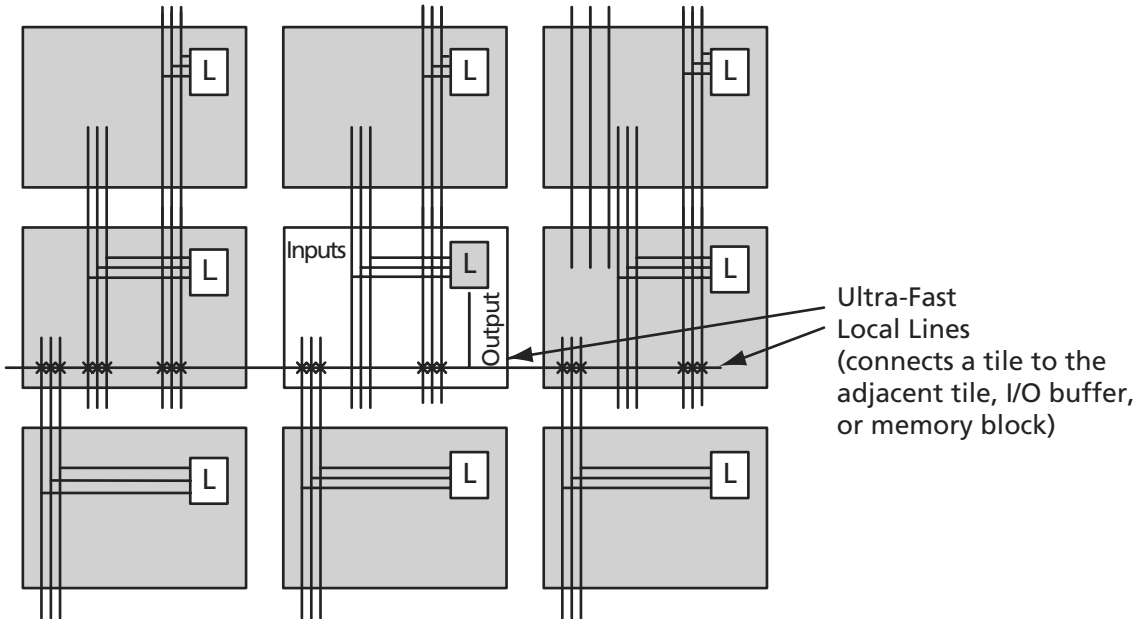
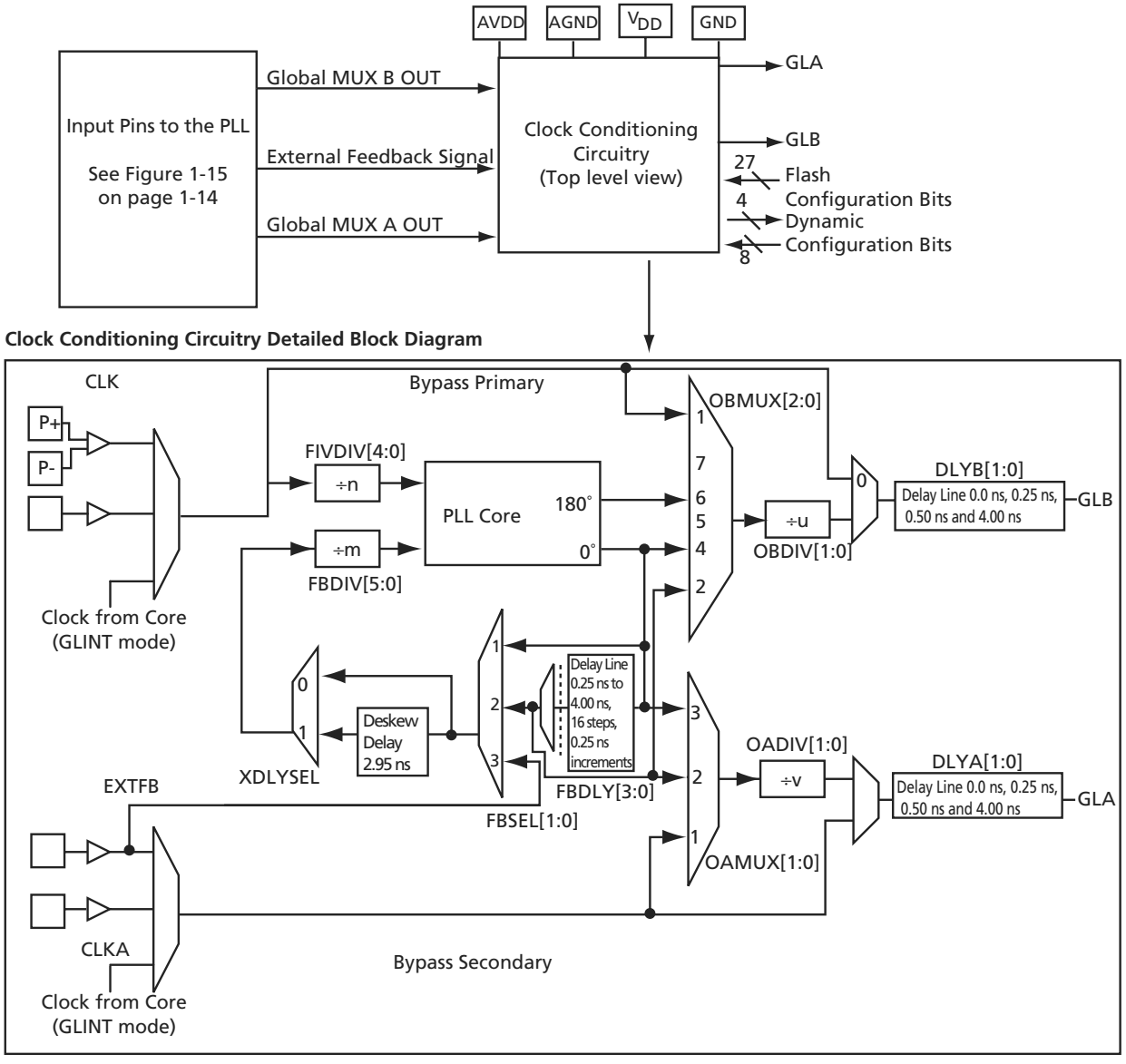


Figure 1-4 • **Ultra-Fast Local Resources**

enable the user to define a wide range of frequency multipliers and divisors. The clock conditioning circuit can advance or delay the clock up to 8 ns (in increments of 0.25 ns) relative to the positive edge of the incoming reference clock. The system also allows for the selection of output frequency clock phases of 0° and 180°.

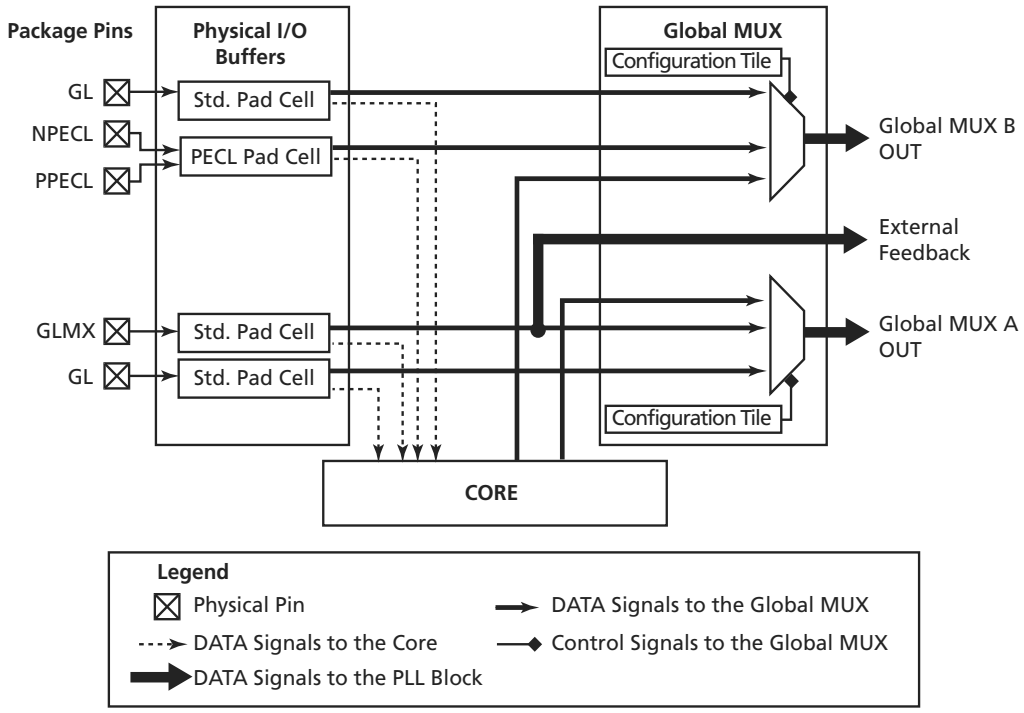
Prior to the application of signals to the rib drivers, they pass through programmable delay units, one per global network. These units permit the delaying of global signals relative to other signals to assist in the control of input set-up times. Not all possible combinations of input and output modes can be used. The degrees of freedom available in the bidirectional global pad system and in the clock conditioning circuit have been restricted. This avoids unnecessary and unwieldy design kit and software work.



Notes:

1. *FBDLY is a programmable delay line from 0 to 4 ns in 250 ps increments.*
2. *DLYA and DLYB are programmable delay lines, each with selectable values 0 ps, 250 ps, 500 ps, and 4 ns.*
3. *OBDIV will also divide the phase-shift since it takes place after the PLL Core.*

Figure 1-14 • **PLL Block – Top-Level View and Detailed PLL Block Diagram**



Note: *When a signal from an I/O tile is connected to the core, it cannot be connected to the Global MUX at the same time.*

Figure 1-15 • **Input Connectors to ProASIC^PLUS Clock Conditioning Circuitry**

Table 1-7 • **Clock-Conditioning Circuitry MUX Settings**

MUX	Datapath	Comments
FBSEL		
1	Internal Feedback	
2	Internal Feedback and Advance Clock Using FBDLY	–0.25 to –4 ns in 0.25 ns increments
3	External Feedback (EXTFB)	
XDLYSEL		
0	Feedback Unchanged	
1	Deskew feedback by advancing clock by system delay	Fixed delay of -2.95 ns
OBMUX	**GLB**	
0	Primary bypass, no divider	
1	Primary bypass, use divider	
2	Delay Clock Using FBDLY	+0.25 to +4 ns in 0.25 ns increments
4	Phase Shift Clock by 0°	
5	Reserved	
6	Phase Shift Clock by +180°	
7	Reserved	
OAMUX	**GLA**	
0	Secondary bypass, no divider	
1	Secondary bypass, use divider	
2	Delay Clock Using FBDLY	+0.25 to +4 ns in 0.25 ns increments
3	Phase Shift Clock by 0°	

Logic Tile Timing Characteristics

Timing characteristics for ProASIC^PLUS devices fall into three categories: family dependent, device dependent, and design dependent. The input and output buffer characteristics are common to all ProASIC^PLUS family members. Internal routing delays are device dependent. Design dependency means that actual delays are not determined until after placement and routing of the user's design are complete. Delay values may then be determined by using the Timer utility or by performing simulation with post-layout delays.

Critical Nets and Typical Nets

Propagation delays are expressed only for typical nets, which are used for initial design performance evaluation. Critical net delays can then be applied to the most timing-critical paths. Critical nets are determined by net property assignment prior to place-and-route. Refer to the Actel *Designer User's Guide* or online help for details on using constraints.

Timing Derating

Since ProASIC^PLUS devices are manufactured with a CMOS process, device performance will vary with temperature, voltage, and process. Minimum timing parameters reflect maximum operating voltage, minimum operating temperature, and optimal process variations. Maximum timing parameters reflect minimum operating voltage, maximum operating temperature, and worst-case process variations (within process specifications). The derating factors shown in Table 1-9 should be applied to all timing data contained within this datasheet.

All timing numbers listed in this datasheet represent sample timing characteristics of ProASIC^PLUS devices. Actual timing delay values are design-specific and can be derived from the Timer tool in Actel's Designer software after place-and-route.

Table 1-9 • **Temperature and Voltage Derating Factors (Normalized to Worst-Case Commercial, T_J = 70°C, V_{DD} = 2.3 V)**

	–55°C	–40°C	0°C	25°C	70°C	85°C	110°C	125°C	135°C	150°C
2.3 V	0.84	0.86	0.91	0.94	1.00	1.02	1.05	1.13	1.18	1.27
2.5 V	0.81	0.82	0.87	0.90	0.95	0.98	1.01	1.09	1.13	1.21
2.7 V	0.77	0.79	0.83	0.86	0.91	0.93	0.96	1.04	1.08	1.16

Notes:

1. *The user can set the junction temperature in Designer software to be any integer value in the range of –55°C to 175°C.*
2. *The user can set the core voltage in Designer software to be any value between 1.4 V and 1.6 V.*

User Security

ProASIC^PLUS devices have FlashLock protection bits that, once programmed, block the entire programmed contents from being read externally. Please refer to Table 1-11 for details on the number of bits in the key for each device. If locked, the user can only reprogram the device employing the user-defined security key. This protects the device from being read back and duplicated. Since programmed data is stored in nonvolatile memory cells (actually very small capacitors) rather than in the wiring, physical deconstruction cannot be used to compromise data. This type of security breach is further discouraged by the placement of the memory cells beneath the four metal layers (whose removal cannot be accomplished without disturbing the charge in the capacitor). This is the highest security provided in the industry. For more information, refer to Actel's *Design Security in Nonvolatile Flash and Antifuse FPGAs* white paper.

Table 1-11 • **Flashlock Key Size by Device**

Device	Key Size
APA075	79 bits
APA150	79 bits
APA300	79 bits
APA450	119 bits
APA600	167 bits
APA750	191 bits
APA1000	263 bits

Embedded Memory Floorplan

The embedded memory is located across the top and bottom of the device in 256x9 blocks (Figure 1-1 on page 1-2). Depending on the device, up to 88 blocks are available to support a variety of memory configurations. Each block can be programmed as an independent memory array or combined (using dedicated memory routing resources) to form larger, more complex memory configurations. A single memory configuration could include blocks from both the top and bottom memory locations.

Embedded Memory Configurations

The embedded memory in the ProASIC^PLUS family provides great configuration flexibility (Table 1-12). Each ProASIC^PLUS block is designed and optimized as a two-port memory (one read, one write). This provides 198 kbits of two-port and/or single port memory in the APA1000 device.

Each memory block can be configured as FIFO or SRAM, with independent selection of synchronous or asynchronous read and write ports (Table 1-13). Additional characteristics include programmable flags as well as parity checking and generation. Figure 1-21 on page 1-25 and Figure 1-22 on page 1-26 show the block diagrams of the basic SRAM and FIFO blocks. Table 1-14 on page 1-25 and Table 1-15 on page 1-26 describe memory block SRAM and FIFO interface signals, respectively. A single memory block is designed to operate at up to 150 MHz (standard speed grade typical conditions). Each block is comprised of 256 9-bit words (one read port, one write port). The memory blocks may be cascaded in width and/or depth to create the desired memory organization. (Figure 1-23 on page 1-27). This provides optimal bit widths of 9 (one block), 18, 36, and 72, and optimal depths of 256, 512, 768, and 1,024. Refer to Actel's *SmartGen User's Guide* for more information.

Figure 1-24 on page 1-27 gives an example of optimal memory usage. Ten blocks with 23,040 bits have been used to generate three arrays of various widths and depths. Figure 1-25 on page 1-27 shows how RAM blocks can be used in parallel to create extra read ports. In this example, using only 10 of the 88 available blocks of the APA1000 yields an effective 6,912 bits of multiple port RAM. The Actel SmartGen software facilitates building wider and deeper memory configurations for optimal memory usage.

Table 1-12 • **ProASIC^PLUS Memory Configurations by Device**

Device	Bottom	Top	Maximum Width		Maximum Depth	
			D	W	D	W
APA075	0	12	256	108	1,536	9
APA150	0	16	256	144	2,048	9
APA300	16	16	256	144	2,048	9
APA450	24	24	256	216	3,072	9
APA600	28	28	256	252	3,584	9

Table 1-19 • **Military Temperature Grade Product Performance Retention**

Minimum Time at T_J 110°C or below	Minimum Time at T_J 125°C or below	Minimum Time at T_J 135°C or below	Minimum Time at T_J 150°C or below	Minimum Performance Retention (Years)
100%				20.0
90%	10%			18.2
75%	25%			16
90%		10%		15.4
50%	50%			13.3
90%			10%	11.8
75%		25%		11.4
	100%			10
	90%	10%		9.1
50%		50%		8
	75%	25%		8
	90%		10%	7.7
75%			25%	7.3
	50%	50%		6.7
	75%		25%	5.7
		100%		5
		90%	10%	4.5
50%			50%	4.4
	50%		50%	4
		75%	25%	4
		50%	50%	3.3
			100%	2.5

Table 1-23 • **DC Electrical Specifications (V_{DDP} = 3.3 V ±0.3 V and V_{DD} = 2.5 V ±0.2 V) Applies to Commercial and Industrial Temperature Only**

Symbol	Parameter	Conditions		Commercial/Industrial[1] Min.	Typ.	Max.	Units
V_{OH}	Output High Voltage 3.3 V I/O, High Drive (OB33P) 3.3 V I/O, Low Drive (OB33L)	 I_{OH} = –14 mA I_{OH} = –24 mA I_{OH} = –6 mA I_{OH} = –12 mA		 0.9*V_{DDP} 2.4 0.9*V_{DDP} 2.4			V
V_{OL}	Output Low Voltage 3.3 V I/O, High Drive (OB33P) 3.3 V I/O, Low Drive (OB33L)	 I_{OL} = 15 mA I_{OL} = 20 mA I_{OL} = 28 mA I_{OL} = 7 mA I_{OL} = 10 mA I_{OL} = 15 mA				 0.1V_{DDP} 0.4 0.7 0.1V_{DDP} 0.4 0.7	V
V_{IH}[5]	Input High Voltage 3.3 V Schmitt Trigger Inputs 3.3 V LVTTL/LVCMOS 2.5 V Mode			 1.6 2 1.7		 V_{DDP} + 0.3 V_{DDP} + 0.3 V_{DDP} + 0.3	V
V_{IL}[6]	Input Low Voltage 3.3 V Schmitt Trigger Inputs 3.3 V LVTTL/LVCMOS 2.5 V Mode			 –0.3 –0.3 –0.3		 0.8 0.8 0.7	V
$R_{WEAKPULLUP}$	Weak Pull-up Resistance (IOB33U)	$V_{IN} \geq$ 1.5 V		7		43	kΩ
$R_{WEAKPULLUP}$	Weak Pull-up Resistance (IOB25U)	$V_{IN} \geq$ 1.5 V		7		43	kΩ
I_{IN}	Input Current	with pull up (V_{IN} = GND)		–300		–40	µA
		without pull up (V_{IN} = GND or V_{DD})		–10		10	µA
I_{DDQ}	Quiescent Supply Current (standby) Commercial	V_{IN} = GND[3] or V_{DD}	Std.		5.0	15	mA
			–F[2]		5.0	25	mA
I_{DDQ}	Quiescent Supply Current (standby) Industrial	V_{IN} = GND[3] or V_{DD}	Std.		5.0	20	mA
I_{DDQ}	Quiescent Supply Current (standby) Military	V_{IN} = GND[3] or V_{DD}	Std.		5.0	25	mA

Notes:

1. *All process conditions. Commercial/Industrial: Junction Temperature: –40 to +110°C.*
2. *All –F parts are only available as commercial.*
3. *No pull-up resistor required.*
4. *This will not exceed 2 mA total per device.*
5. *During transitions, the input signal may overshoot to V_{DDP} +1.0 V for a limited time of no larger than 10% of the duty cycle.*
6. *During transitions, the input signal may undershoot to –1.0 V for a limited time of no larger than 10% of the duty cycle.*

Table 1-23 • **DC Electrical Specifications (V_{DDP} = 3.3 V ±0.3 V and V_{DD} = 2.5 V ±0.2 V) (Continued)**
Applies to Commercial and Industrial Temperature Only

Symbol	Parameter	Conditions		Commercial/Industrial[1] Min.	Typ.	Max.	Units
I_{OZ}	Tristate Output Leakage Current	V_{OH} = GND or V_{DD}	Std.	–10		10	µA
			–F[2, 4]	–10		100	µA
I_{OSH}	Output Short Circuit Current High 3.3 V High Drive (OB33P) 3.3 V Low Drive (OB33L)	 V_{IN} = GND V_{IN} = GND		 –200 –100			
I_{OSL}	Output Short Circuit Current Low 3.3 V High Drive 3.3 V Low Drive	 V_{IN} = V_{DD} V_{IN} = V_{DD}				 200 100	
$C_{I/O}$	I/O Pad Capacitance					10	pF
C_{CLK}	Clock Input Pad Capacitance					10	pF

Notes:

1. *All process conditions. Commercial/Industrial: Junction Temperature: –40 to +110°C.*
2. *All –F parts are only available as commercial.*
3. *No pull-up resistor required.*
4. *This will not exceed 2 mA total per device.*
5. *During transitions, the input signal may overshoot to V_{DDP} +1.0 V for a limited time of no larger than 10% of the duty cycle.*
6. *During transitions, the input signal may undershoot to –1.0 V for a limited time of no larger than 10% of the duty cycle.*

Table 1-24 • **DC Electrical Specifications (V_{DDP} = 3.3 V ±0.3 V and V_{DD} = 2.5 V ±0.2 V) Applies to Military Temperature and MIL-STD-883B Temperature Only**

Symbol	Parameter	Conditions		Military/MIL-STD-883B[1] Min.	Typ.	Max.	Units
V_{OH}	Output High Voltage 3.3 V I/O, High Drive, High Slew (OB33PH) 3.3V I/O, High Drive, Normal/ Low Slew (OB33PN/OB33PL) 3.3 V I/O, Low Drive , High/ Normal/Low Slew (OB33LH/ OB33LN/OB33LL)	 I_{OH} = –8 mA I_{OH} = –16 mA I_{OH} = –3mA I_{OH} = –8mA I_{OH} = –3 mA I_{OH} = –8 mA		 0.9*V_{DDP} 2.4 0.9*V_{DDP} 2.4 0.9*V_{DDP} 2.4			V
V_{OL}	Output Low Voltage 3.3 V I/O, High Drive, High Slew (OB33PH) 3.3V I/O, High Drive, Normal/ Low Slew (OB33PN/OB33PL)) 3.3 V I/O, Low Drive, High/ Normal/Low Slew (OB33LH/ OB33LN/OB33LL)	 I_{OL} = 12 mA I_{OL} = 17 mA I_{OL} = 28 mA I_{OL} = 4 mA I_{OL} = 6 mA I_{OL} = 13 mA I_{OL} = 4 mA I_{OL} = 6 mA I_{OL} = 13 mA				 0.1V_{DDP} 0.4 0.7 0.1V_{DDP} 0.4 0.7 0.1V_{DDP} 0.4 0.7	V
V_{IH}[4]	Input High Voltage 3.3 V Schmitt Trigger Inputs 3.3 V LVTTL/LVCMOS 2.5 V Mode			1.6 2 1.7		V_{DDP} + 0.3 V_{DDP} + 0.3 V_{DDP} + 0.3	V
V_{IL}[5]	Input Low Voltage 3.3 V Schmitt Trigger Inputs 3.3 V LVTTL/LVCMOS 2.5 V Mode			–0.3 –0.3 –0.3		0.7 0.8 0.7	V
$R_{WEAKPULLUP}$	Weak Pull-up Resistance (IOB33U)	$V_{IN} \geq$ 1.5 V		7		43	kΩ
$R_{WEAKPULLUP}$	Weak Pull-up Resistance (IOB25U)	$V_{IN} \geq$ 1.5 V		7		43	kΩ
I_{IN}	Input Current	with pull up (V_{IN} = GND)		–300		–40	µA
		without pull up (V_{IN} = GND or V_{DD})		–10		10	µA
I_{DDQ}	Quiescent Supply Current (standby) Commercial	V_{IN} = GND[2] or V_{DD}	Std.		5.0	15	mA
			–F		5.0	25	mA

Notes:

1. *All process conditions. Military Temperature / MIL-STD-883 Class B: Junction Temperature: –55 to +125°C.*
2. *No pull-up resistor required.*
3. *This will not exceed 2 mA total per device.*
4. *During transitions, the input signal may overshoot to V_{DDP}+1.0 V for a limited time of no larger than 10% of the duty cycle.*
5. *During transitions, the input signal may undershoot to –1.0 V for a limited time of no larger than 10% of the duty cycle.*

Table 1-24 • **DC Electrical Specifications (V_{DDP} = 3.3 V ±0.3 V and V_{DD} = 2.5 V ±0.2 V) (Continued)**
Applies to Military Temperature and MIL-STD-883B Temperature Only

Symbol	Parameter	Conditions		Military/MIL-STD-883B[1] Min.	Typ.	Max.	Units
I_{DDQ}	Quiescent Supply Current (standby) Industrial	V_{IN} = GND[2] or V_{DD}	Std.		5.0	20	mA
I_{DDQ}	Quiescent Supply Current (standby) Military	V_{IN} = GND[2] or V_{DD}	Std.		5.0	25	mA
I_{OZ}	Tristate Output Leakage Current	V_{OH} = GND or V_{DD}	Std.	–10		10	µA
			–F[3]	–10		100	µA
I_{OSH}	Output Short Circuit Current High 3.3 V High Drive (OB33P) 3.3 V Low Drive (OB33L)	 V_{IN} = GND V_{IN} = GND		 –200 –100			
I_{OSL}	Output Short Circuit Current Low 3.3 V High Drive 3.3 V Low Drive	 V_{IN} = V_{DD} V_{IN} = V_{DD}				 200 100	
$C_{I/O}$	I/O Pad Capacitance					10	pF
C_{CLK}	Clock Input Pad Capacitance					10	pF

Notes:

1. *All process conditions. Military Temperature / MIL-STD-883 Class B: Junction Temperature: –55 to +125°C.*
2. *No pull-up resistor required.*
3. *This will not exceed 2 mA total per device.*
4. *During transitions, the input signal may overshoot to V_{DDP} +1.0 V for a limited time of no larger than 10% of the duty cycle.*
5. *During transitions, the input signal may undershoot to –1.0 V for a limited time of no larger than 10% of the duty cycle.*

Input Buffer Delays

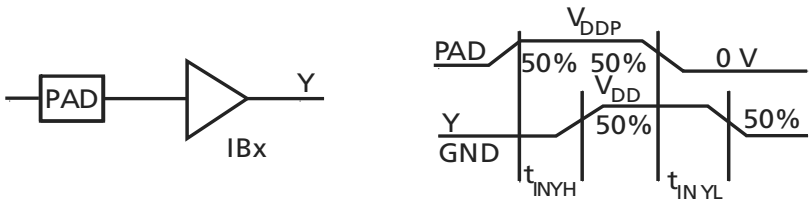


Figure 1-28 • **Input Buffer Delays**

Table 1-35 • **Worst-Case Commercial Conditions**
V_{DDP} = 3.0 V, V_{DD} = 2.3 V, T_J = 70°C

Macro Type	Description	Max. t_{INYH}[1]		Max. t_{INYL}[2]		Units
		Std.	–F	Std.	–F	
IB33	3.3 V, CMOS Input Levels[3], No Pull-up Resistor	0.4	0.5	0.6	0.7	ns
IB33S	3.3 V, CMOS Input Levels[3], No Pull-up Resistor, Schmitt Trigger	0.6	0.7	0.8	0.9	ns

Notes:

1. *t_{INYH} = Input Pad-to-Y High*
2. *t_{INYL} = Input Pad-to-Y Low*
3. *LVTTL delays are the same as CMOS delays.*
4. *For LP Macros, V_{DDP}=2.3 V for delays.*
5. *All –F parts are only available as commercial.*

Table 1-36 • **Worst-Case Commercial Conditions**
V_{DDP} = 2.3 V, V_{DD} = 2.3 V, T_J = 70°C

Macro Type	Description	Max. t_{INYH}[1]		Max. t_{INYL}[2]		Units
		Std.	–F	Std.	–F	
IB25LP	2.5 V, CMOS Input Levels[3], Low Power	0.9	1.1	0.6	0.8	ns
IB25LPS	2.5 V, CMOS Input Levels[3], Low Power, Schmitt Trigger	0.7	0.9	0.9	1.1	ns

Notes:

1. *t_{INYH} = Input Pad-to-Y High*
2. *t_{INYL} = Input Pad-to-Y Low*
3. *LVTTL delays are the same as CMOS delays.*
4. *For LP Macros, V_{DDP}=2.3 V for delays.*
5. *All –F parts are only available as commercial.*

Table 1-37 • **Worst-Case Military Conditions**
V_{DDP} = 3.0V, V_{DD} = 2.3V, T_J = 125°C for Military/MIL-STD-883

Macro Type	Description	Max. t_{INYH}[1]	Max. t_{INYL}[2]	Units
		Std.	Std.	
IB33	3.3V, CMOS Input Levels[3], No Pull-up Resistor	0.5	0.6	ns
IB33S	3.3V, CMOS Input Levels[3], No Pull-up Resistor, Schmitt Trigger	0.6	0.8	ns

Notes:

1. *t_{INYH} = Input Pad-to-Y High*
2. *t_{INYL} = Input Pad-to-Y Low*
3. *LVTTL delays are the same as CMOS delays.*
4. *For LP Macros, V_{DDP}=2.3V for delays.*

Table 1-38 • **Worst-Case Military Conditions**
V_{DDP} = 2.3V, V_{DD} = 2.3V, T_J = 125°C for Military/MIL-STD-883

Macro Type	Description	Max. t_{INYH}[1]	Max. t_{INYL}[2]	Units
		Std.	Std.	
IB25LP	2.5V, CMOS Input Levels[3], Low Power	0.9	0.7	ns
IB25LPS	2.5V, CMOS Input Levels[3], Low Power, Schmitt Trigger	0.8	1.0	ns

Notes:

1. *t_{INYH} = Input Pad-to-Y High*
2. *t_{INYL} = Input Pad-to-Y Low*
3. *LVTTL delays are the same as CMOS delays.*
4. *For LP Macros, V_{DDP}=2.3V for delays.*

Table 1-41 • **Worst-Case Military Conditions**
V_{DDP} = 3.0V, V_{DD} = 2.3V, T_J = 125°C for Military/MIL-STD-883

Macro Type	Description	Max. t_{INYH}[1]	Max. t_{INYL}[2]
		Std.	Std.
GL33	3.3V, CMOS Input Levels[3], No Pull-up Resistor	1.1	1.1
GL33S	3.3V, CMOS Input Levels[3], No Pull-up Resistor, Schmitt Trigger	1.1	1.1
PECL	PPECL Input Levels	1.1	1.1

Notes:

1. *t_{INYH} = Input Pad-to-Y High*
2. *t_{INYL} = Input Pad-to-Y Low*
3. *LVTTL delays are the same as CMOS delays.*
4. *For LP Macros, V_{DDP}=2.3V for delays.*

Table 1-42 • **Worst-Case Military Conditions**
V_{DDP} = 2.3V, V_{DD} = 2.3V, T_J = 125°C for Military/MIL-STD-883

Macro Type	Description	Max. t_{INYH}[1]	Max. t_{INYL}[2]
		Std.	Std.
GL25LP	2.5V, CMOS Input Levels[3], Low Power	1.0	1.1
GL25LPS	2.5V, CMOS Input Levels[3], Low Power, Schmitt Trigger	1.4	1.0

Notes:

1. *t_{INYH} = Input Pad-to-Y High*
2. *t_{INYL} = Input Pad-to-Y Low*
3. *LVTTL delays are the same as CMOS delays.*
4. *For LP Macros, V_{DDP}=2.3V for delays.*

Module Delays

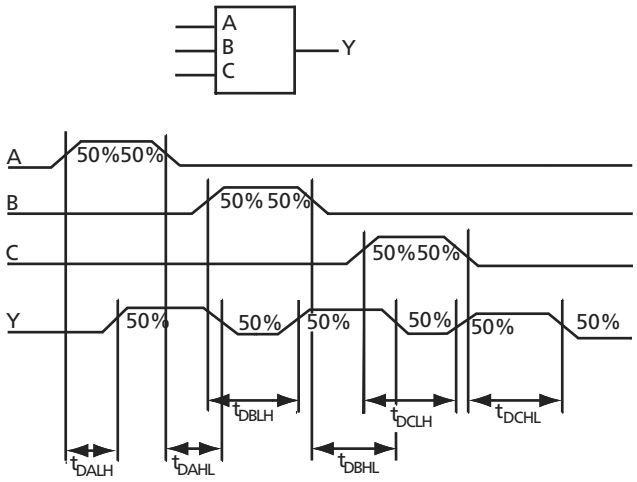


Figure 1-29 • **Module Delays**

Sample Macrocell Library Listing

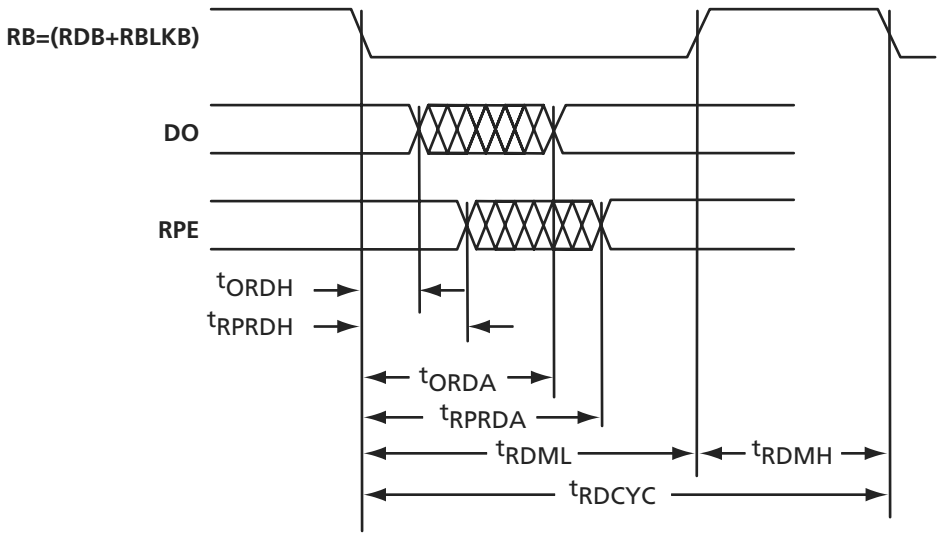
Table 1-47 • **Worst-Case Military Conditions[1]**
V_{DD} = 2.3 V, T_J = 70° C, T_J = 70°C, T_J = 125°C for Military/MIL-STD-883

Cell Name	Description		Std.		–F[2]		
			Max	Min	Max	Min	Units
NAND2	2-Input NAND		0.5		0.6		ns
AND2	2-Input AND		0.7		0.8		ns
NOR3	3-Input NOR		0.8		1.0		ns
MUX2L	2-1 MUX with Active Low Select		0.5		0.6		ns
OA21	2-Input OR into a 2-Input AND		0.8		1.0		ns
XOR2	2-Input Exclusive OR		0.6		0.8		ns
LDL	Active Low Latch (LH/HL)						ns
	CLK-Q	LH[3]	0.9		1.1		
		HL[3]	0.8		0.9		ns
	t_{setup}			0.7		0.8	ns
	t_{hold}			0.1		0.2	ns
DFFL	Negative Edge-Triggered D-type Flip-Flop (LH/HL)						ns
	CLK-Q	LH[3]	0.9		1.1		
		HL[3]	0.8		1.0		ns
	t_{setup}			0.6		0.7	ns
	t_{hold}			0.0		0.0	ns

Notes:

1. *Intrinsic delays have a variable component, coupled to the input slope of the signal. These numbers assume an input slope typical of local interconnect.*
2. *All –F parts are only available as commercial.*
3. *LH and HL refer to the Q transitions from Low to High and High to Low, respectively.*

Asynchronous SRAM Read, RDB Controlled



Note: *The plot shows the normal operation status.*

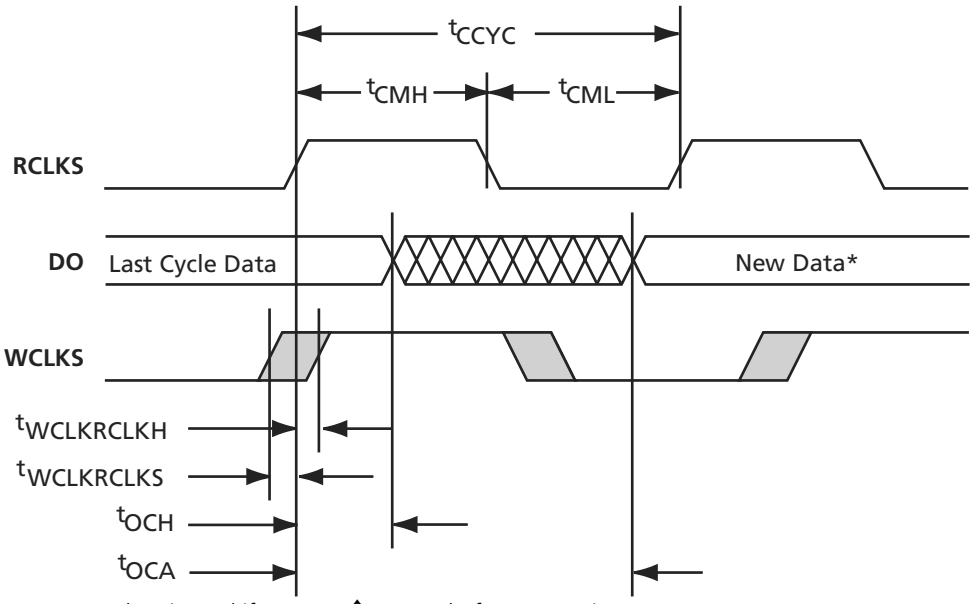
Figure 1-35 • **Asynchronous SRAM Read, RDB Controlled**

Table 1-56 • **T_J = 0°C to 110°C; V_{DD} = 2.3 V to 2.7 V for Commercial/industrial**
T_J = –55°C to 150°C, V_{DD} = 2.3 V to 2.7 V for Military/MIL-STD-883

Symbol t_{xxx}	Description	Min.	Max.	Units	Notes
ORDA	New DO access from RB ↓	7.5		ns	
ORDH	Old DO valid from RB ↓		3.0	ns	
RDCYC	Read cycle time	7.5		ns	
RDMH	RB high phase	3.0		ns	Inactive setup to new cycle
RDML	RB low phase	3.0		ns	Active
RPRDA	New RPE access from RB ↓	9.5		ns	
RPRDH	Old RPE valid from RB ↓		3.0	ns	

Note: *All –F speed grade devices are 20% slower than the standard numbers.*

Synchronous Write and Read to the Same Location



Note: *The plot shows the normal operation status.*

Figure 1-37 • **Synchronous Write and Read to the Same Location**

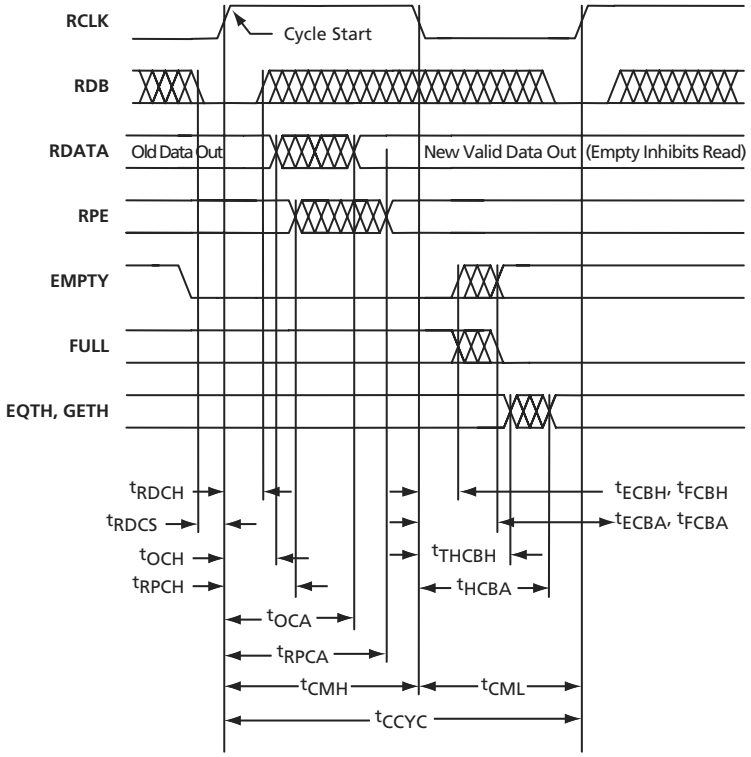
Table 1-58 • **T_J = 0°C to 110°C; V_{DD} = 2.3 V to 2.7 V for Commercial/industrial**
T_J = –55°C to 150°C, V_{DD} = 2.3 V to 2.7 V for Military/MIL-STD-883

Symbol t_{xxx}	Description	Min.	Max.	Units	Notes
CCYC	Cycle time	7.5		ns	
CMH	Clock high phase	3.0		ns	
CML	Clock low phase	3.0		ns	
WCLKRCLKS	WCLKS ↑ to RCLKS ↑ setup time	– 0.1		ns	
WCLKRCLKH	WCLKS ↑ to RCLKS ↑ hold time		7.0	ns	
OCH	Old DO valid from RCLKS ↑		3.0	ns	OCA/OCH displayed for Access Timed Output
OCA	New DO valid from RCLKS ↑	7.5		ns	

Notes:

1. *This behavior is valid for Access Timed Output and Pipelined Mode Output. The table shows the timings of an Access Timed Output.*
2. *During synchronous write and synchronous read access to the same location, the new write data will be read out if the active write clock edge occurs before or at the same time as the active read clock edge. The negative setup time insures this behavior for WCLKS and RCLKS driven by the same design signal.*
3. *If WCLKS changes after the hold time, the data will be read.*
4. *A setup or hold time violation will result in unknown output data.*
5. *All –F speed grade devices are 20% slower than the standard numbers.*

Synchronous FIFO Read, Access Timed Output Strobe (Synchronous Transparent)



Note: *The plot shows the normal operation status.*

Figure 1-45 • **Synchronous FIFO Read, Access Timed Output Strobe (Synchronous Transparent)**

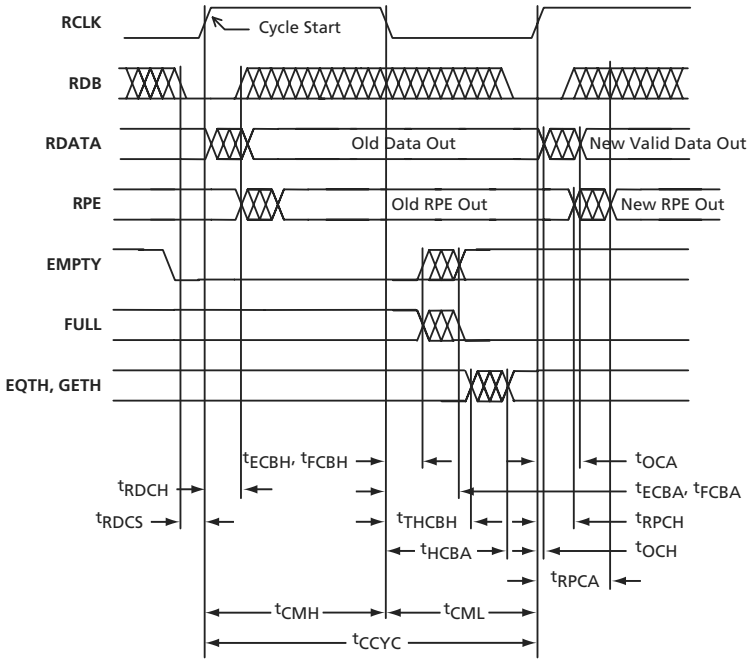
Table 1-65 • **T_J = 0°C to 110°C; V_{DD} = 2.3 V to 2.7 V for Commercial/industrial**
T_J = –55°C to 150°C, V_{DD} = 2.3 V to 2.7 V for Military/MIL-STD-883

Symbol t_{xxx}	Description	Min.	Max.	Units	Notes
CCYC	Cycle time	7.5		ns	
CMH	Clock high phase	3.0		ns	
CML	Clock low phase	3.0		ns	
ECBA	New EMPTY access from RCLKS ↓	3.0[1]		ns	
FCBA	FULL ↓ access from RCLKS ↓	3.0[1]		ns	
ECBH, FCBH, THCBH	Old EMPTY, FULL, EQTH, & GETH valid hold time from RCLKS ↓		1.0	ns	Empty/full/thresh are invalid from the end of hold until the new access is complete
OCA	New DO access from RCLKS ↑	7.5		ns	
OCH	Old DO valid from RCLKS ↑		3.0	ns	
RDCH	RDB hold from RCLKS ↑	0.5		ns	
RDCS	RDB setup to RCLKS ↑	1.0		ns	
RPCA	New RPE access from RCLKS ↑	9.5		ns	
RPCH	Old RPE valid from RCLKS ↑		3.0	ns	
HCBA	EQTH or GETH access from RCLKS ↓	4.5		ns	

Notes:

1. *At fast cycles, ECBA and FCBA = MAX (7.5 ns – CMH), 3.0 ns.*
2. *All –F speed grade devices are 20% slower than the standard numbers.*

Synchronous FIFO Read, Pipeline Mode Outputs (Synchronous Pipelined)



Note: *The plot shows the normal operation status.*

Figure 1-46 • **Synchronous FIFO Read, Pipeline Mode Outputs (Synchronous Pipelined)**

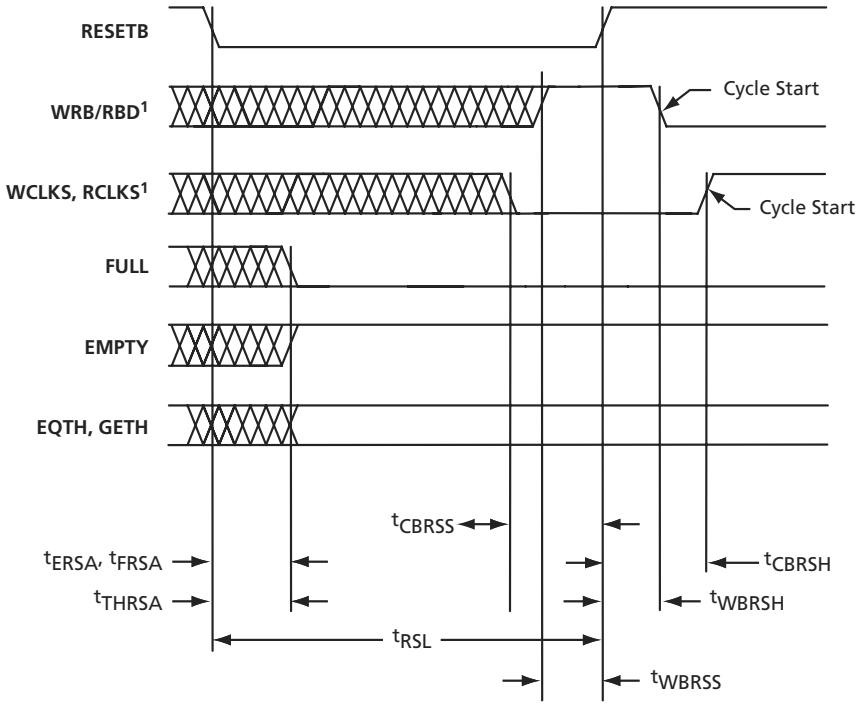
Table 1-66 • **T_J = 0°C to 110°C; V_{DD} = 2.3 V to 2.7 V for Commercial/industrial**
T_J = –55°C to 150°C, V_{DD} = 2.3 V to 2.7 V for Military/MIL-STD-883

Symbol t_{xxx}	Description	Min.	Max.	Units	Notes
CCYC	Cycle time	7.5		ns	
CMH	Clock high phase	3.0		ns	
CML	Clock low phase	3.0		ns	
ECBA	New EMPTY access from RCLKS ↓	3.0[1]		ns	
FCBA	FULL ↓ access from RCLKS ↓	3.0[1]		ns	
ECBH, FCBH, THCBH	Old EMPTY, FULL, EQTH, & GETH valid hold time from RCLKS ↓		1.0	ns	Empty/full/thresh are invalid from the end of hold until the new access is complete
OCA	New DO access from RCLKS ↑	2.0		ns	
OCH	Old DO valid from RCLKS ↑		0.75	ns	
RDCH	RDB hold from RCLKS ↑	0.5		ns	
RDCS	RDB setup to RCLKS ↑	1.0		ns	
RPCA	New RPE access from RCLKS ↑	4.0		ns	
RPCH	Old RPE valid from RCLKS ↑		1.0	ns	
HCBA	EQTH or GETH access from RCLKS ↓	4.5		ns	

Notes:

1. *At fast cycles, ECBA and FCBA = MAX (7.5 ns – CMS), 3.0 ns.*
2. *All –F speed grade devices are 20% slower than the standard numbers.*

FIFO Reset



Notes:

1. During reset, either the enables (WRB and RBD) OR the clocks (WCLKS and RCKLS) must be low.

2. The plot shows the normal operation status.

Figure 1-48 • **FIFO Reset**

Table 1-68 • **T_J = 0°C to 110°C; V_{DD} = 2.3 V to 2.7 V for Commercial/industrial**
T_J = –55°C to 150°C, V_{DD} = 2.3 V to 2.7 V for Military/MIL-STD-883

Symbol t_{xxx}	Description	Min.	Max.	Units	Notes
CBRSH[1]	WCLKS or RCLKS ↑ hold from RESETB ↑	1.5		ns	Synchronous mode only
CBRSS[1]	WCLKS or RCLKS ↓ setup to RESETB ↑	1.5		ns	Synchronous mode only
ERSA	New EMPTY ↑ access from RESETB ↓	3.0		ns	
FRSA	FULL ↓ access from RESETB ↓	3.0		ns	
RSL	RESETB low phase	7.5		ns	
THRSA	EQTH or GETH access from RESETB ↓	4.5		ns	
WBRSH[1]	WB ↓ hold from RESETB ↑	1.5		ns	Asynchronous mode only
WBRSS[1]	WB ↑ setup to RESETB ↑	1.5		ns	Asynchronous mode only

Notes:

1. During rest, the enables (WRB and RBD) must be high OR the clocks (WCLKS and RCKLS) must be low.

2. All –F speed grade devices are 20% slower than the standard numbers.