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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	73728
Number of I/O	158
Number of Gates	300000
Voltage - Supply	2.3V ~ 2.7V
Mounting Type	Surface Mount
Operating Temperature	-55°C ~ 125°C (TC)
Package / Case	208-BFQFP
Supplier Device Package	208-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/apa300-pq208m

Temperature Grade Offerings

Package	APA075	APA150	APA300	APA450	APA600	APA750	APA1000
TQ100	C, I	C, I					
TQ144	C, I						
PQ208	C, I	C, I	C, I, M	C, I	C, I, M	C, I	C, I, M
BG456		C, I	C, I, M	C, I	C, I, M	C, I	C, I, M
FG144	C, I	C, I	C, I, M	C, I			
FG256		C, I	C, I, M	C, I	C, I, M		
FG484				C, I	C, I, M		
FG676					C, I, M	C, I	
FG896						C, I	C, I, M
FG1152							C, I
CQ208			M, B		M, B		M, B
CQ352			M, B		M, B		M, B
CG624					M, B		M, B

Note: *C = Commercial*
I = Industrial
M = Military
B = MIL-STD-883

Speed Grade and Temperature Matrix

	–F	Std.
C	✓	✓
I		✓
M, B		✓

Note: *C = Commercial*
I = Industrial
M = Military
B = MIL-STD-883

General Description

The ProASIC^PLUS family of devices, Actel's second-generation Flash FPGAs, offers enhanced performance over Actel's ProASIC family. It combines the advantages of ASICs with the benefits of programmable devices through nonvolatile Flash technology. This enables engineers to create high-density systems using existing ASIC or FPGA design flows and tools. In addition, the ProASIC^PLUS family offers a unique clock conditioning circuit based on two on-board phase-locked loops (PLLs). The family offers up to one million system gates, supported with up to 198 kbits of two-port SRAM and up to 712 user I/Os, all providing 50 MHz PCI performance.

Advantages to the designer extend beyond performance. Unlike SRAM-based FPGAs, four levels of routing hierarchy simplify routing, while the use of Flash technology allows all functionality to be live at power-up. No external boot PROM is required to support device programming. While on-board security mechanisms prevent access to the program information, reprogramming can be performed in-system to support future design iterations and field upgrades. The device's architecture mitigates the complexity of ASIC migration at higher user volume. This makes ProASIC^PLUS a cost-effective solution for applications in the networking, communications, computing, and avionics markets.

The ProASIC^PLUS family achieves its nonvolatility and reprogrammability through an advanced Flash-based 0.22 µm LVCMOS process with four layers of metal. Standard CMOS design techniques are used to implement logic and control functions, including the PLLs and LVPECL inputs. This results in predictable performance compatible with gate arrays.

The ProASIC^PLUS architecture provides granularity comparable to gate arrays. The device core consists of a Sea-of-Tiles™. Each tile can be configured as a flip-flop, latch, or three-input/one-output logic function by programming the appropriate Flash switches. The combination of fine granularity, flexible routing resources, and abundant Flash switches allow 100% utilization and over 95% routability for highly congested designs. Tiles and larger functions are interconnected through a four-level routing hierarchy.

Embedded two-port SRAM blocks with built-in FIFO/RAM control logic can have user-defined depths and widths. Users can also select programming for synchronous or asynchronous operation, as well as parity generations or checking.

The unique clock conditioning circuitry in each device includes two clock conditioning blocks. Each block provides a PLL core, delay lines, phase shifts (0° and 180°), and clock multipliers/dividers, as well as the circuitry needed to provide bidirectional access to the PLL. The PLL block contains four programmable frequency dividers which allow the incoming clock signal to be divided by a wide range of factors from 1 to 64. The clock conditioning circuit also delays or advances the incoming reference clock up to 8 ns (in increments of 0.25 ns). The PLL can be configured internally or externally during operation without redesigning or reprogramming the part. In addition to the PLL, there are two LVPECL differential input pairs to accommodate high-speed clock and data inputs.

To support customer needs for more comprehensive, lower-cost, board-level testing, Actel's ProASIC^PLUS devices are fully compatible with IEEE Standard 1149.1 for test access port and boundary-scan test architecture. For more information concerning the Flash FPGA implementation, please refer to the "Boundary Scan (JTAG)" section on page 1-11.

ProASIC^PLUS devices are available in a variety of high-performance plastic packages. Those packages and the performance features discussed above are described in more detail in the following sections.

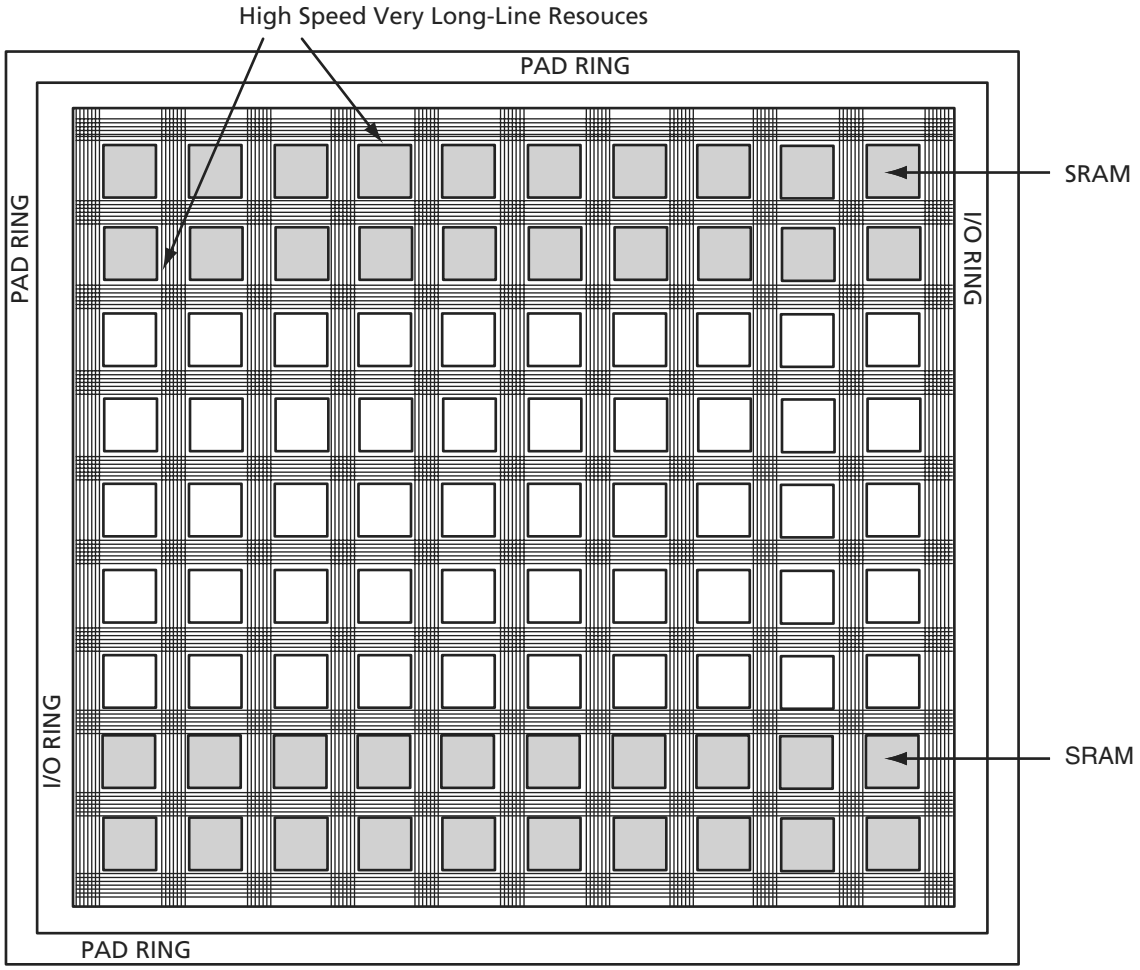


Figure 1-6 • **High-Speed, Very Long-Line Resources**

Clock Resources

The ProASIC^PLUS family offers powerful and flexible control of circuit timing through the use of analog circuitry. Each chip has two clock conditioning blocks containing a phase-locked loop (PLL) core, delay lines, phase shifter (0° and 180°), clock multiplier/dividers, and all the circuitry needed for the selection and interconnection of inputs to the global network (thus providing bidirectional access to the PLL). This permits the PLL block to drive inputs and/or outputs via the two global lines on each side of the chip (four total lines). This circuitry is discussed in more detail in the "ProASICPLUS Clock Management System" section on page 1-13.

Clock Trees

One of the main architectural benefits of ProASIC^PLUS is the set of power- and delay-friendly global networks. ProASIC^PLUS offers four global trees. Each of these trees is based on a network of spines and ribs that reach all the tiles in their regions (Figure 1-7 on page 1-7). This flexible clock tree architecture allows users to map up to 88 different internal/external clocks in an APA1000 device. Details on the clock spines and various numbers of the family are given in Table 1-1 on page 1-7.

The flexible use of the ProASIC^PLUS clock spine allows the designer to cope with several design requirements. Users implementing clock-resource intensive applications can easily route external or gated internal clocks using global routing spines. Users can also drastically reduce delay penalties and save buffering resources by mapping critical high fanout nets to spines. For design hints on using these features, refer to Actel's *Efficient Use of ProASIC Clock Trees* application note.

Array Coordinates

During many place-and-route operations in Actel's Designer software tool, it is possible to set constraints that require array coordinates.

Table 1-2 is provided as a reference. The array coordinates are measured from the lower left (0,0). They can be used in region constraints for specific groups of core cells, I/Os, and RAM blocks. Wild cards are also allowed.

I/O and cell coordinates are used for placement constraints. Two coordinate systems are needed because there is not a one-to-one correspondence between I/O cells and core cells. In addition, the I/O coordinate system changes depending on the die/package combination.

Core cell coordinates start at the lower left corner (represented as (1,1)) or at (1,5) if memory blocks are present at the bottom. Memory coordinates use the same system and are indicated in Table 1-2. The memory coordinates for an APA1000 are illustrated in Figure 1-8. For more information on how to use constraints, see the *Designer User's Guide* or online help for ProASIC^PLUS software tools.

Table 1-2 • **Array Coordinates**

	Logic Tile				Memory Rows		All	
	Min.		Max.		Bottom	Top		
Device	**x**	**y**	**x**	**y**	**y**	**y**	**Min.**	**Max.**
APA075	1	1	96	32	–	(33,33) or (33, 35)	0,0	97, 37
APA150	1	1	128	48	–	(49,49) or (49, 51)	0,0	129, 53
APA300	1	5	128	68	(1,1) or (1,3)	(69,69) or (69, 71)	0,0	129, 73
APA450	1	5	192	68	(1,1) or (1,3)	(69,69) or (69, 71)	0,0	193, 73
APA600	1	5	224	100	(1,1) or (1,3)	(101,101) or (101, 103)	0,0	225, 105
APA750	1	5	256	132	(1,1) or (1,3)	(133,133) or (133, 135)	0,0	257, 137
APA1000	1	5	352	164	(1,1) or (1,3)	(165,165) or (165, 167)	0,0	353, 169

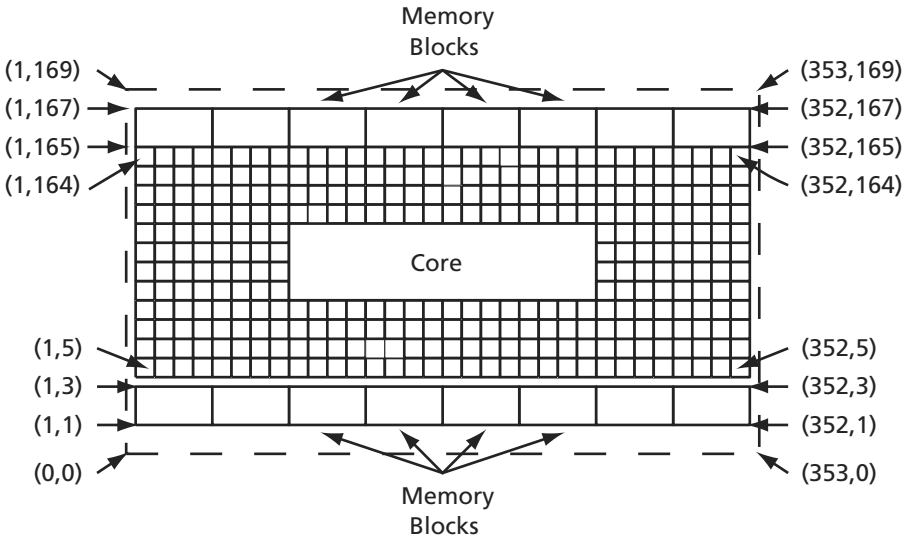


Figure 1-8 • **Core Cell Coordinates for the APA1000**

Boundary Scan (JTAG)

ProASIC^PLUS devices are compatible with IEEE Standard 1149.1, which defines a set of hardware architecture and mechanisms for cost-effective, board-level testing. The basic ProASIC^PLUS boundary-scan logic circuit is composed of the TAP (test access port), TAP controller, test data registers, and instruction register (Figure 1-12). This circuit supports all mandatory IEEE 1149.1 instructions (EXTEST, SAMPLE/PRELOAD and BYPASS) and the optional IDCODE instruction (Table 1-6).

Each test section is accessed through the TAP, which has five associated pins: TCK (test clock input), TDI and TDO (test data input and output), TMS (test mode selector) and TRST (test reset input). TMS, TDI and TRST are equipped with pull-up resistors to ensure proper operation when no input data is supplied to them. These pins are dedicated for boundary-scan test usage. Actel recommends that a nominal 20 kΩ pull-up resistor is added to TDO and TCK pins.

The TAP controller is a four-bit state machine (16 states) that operates as shown in Figure 1-13 on page 1-12. The '1's and '0's represent the values that must be present at TMS at a rising edge of TCK for the given state transition to occur. IR and DR indicate that the instruction register or the data register is operating in that state.

ProASIC^PLUS devices have to be programmed at least once for complete boundary-scan functionality to be available. Prior to being programmed, EXTEST is not available. If boundary-scan functionality is required prior to programming, refer to online technical support on the Actel website and search for ProASIC^PLUS BSDL.

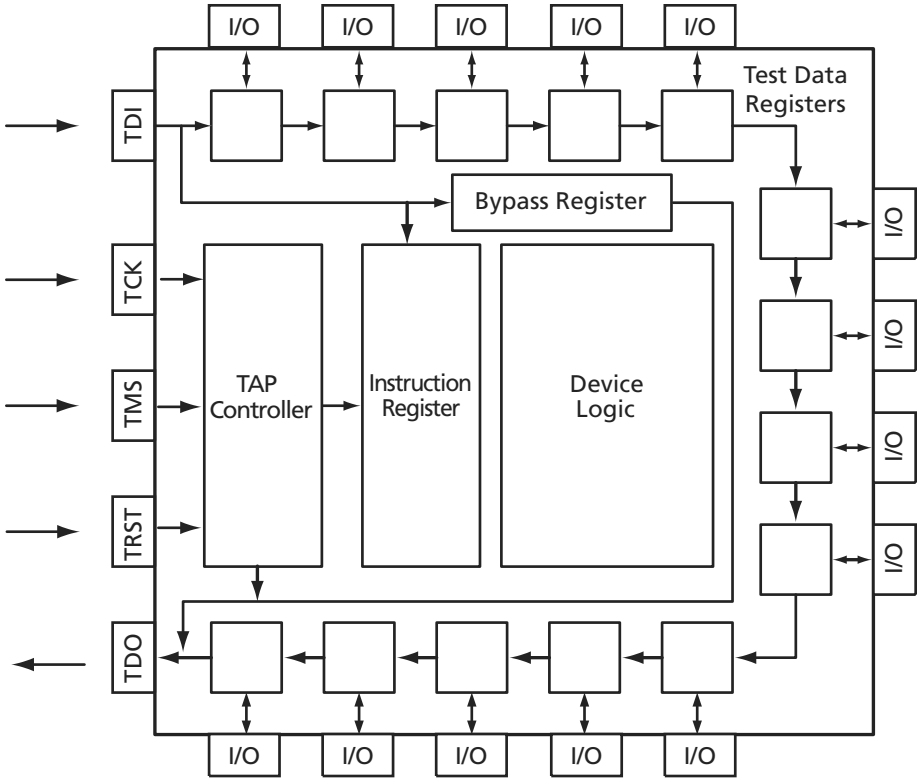


Figure 1-12 • **ProASIC^PLUS JTAG Boundary Scan Test Logic Circuit**

Table 1-6 • **Boundary-Scan Opcodes**

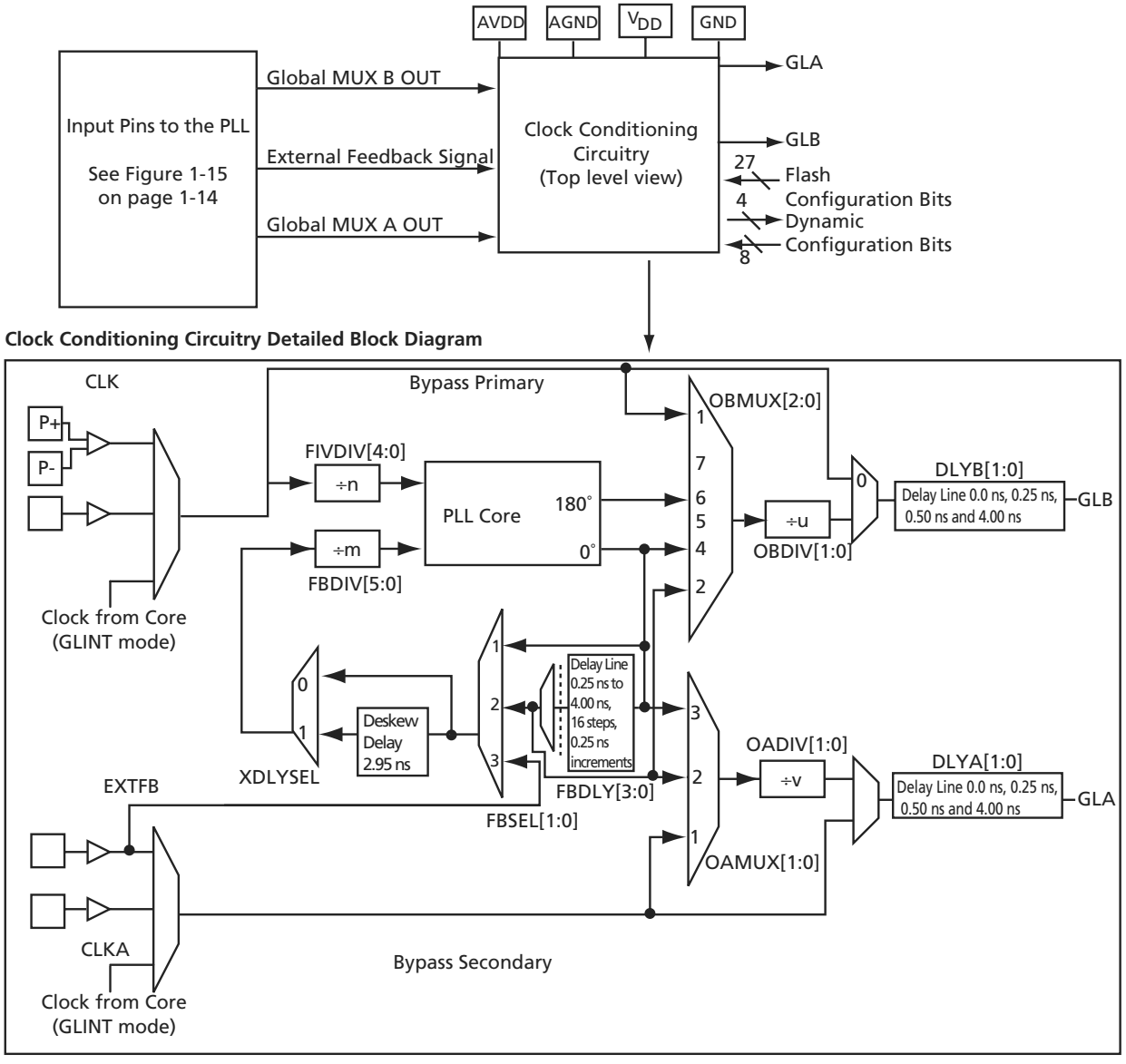
	Hex Opcode
EXTEST	00
SAMPLE/PRELOAD	01
IDCODE	0F

Table 1-6 • **Boundary-Scan Opcodes**

	Hex Opcode
CLAMP	05
BYPASS	FF

enable the user to define a wide range of frequency multipliers and divisors. The clock conditioning circuit can advance or delay the clock up to 8 ns (in increments of 0.25 ns) relative to the positive edge of the incoming reference clock. The system also allows for the selection of output frequency clock phases of 0° and 180°.

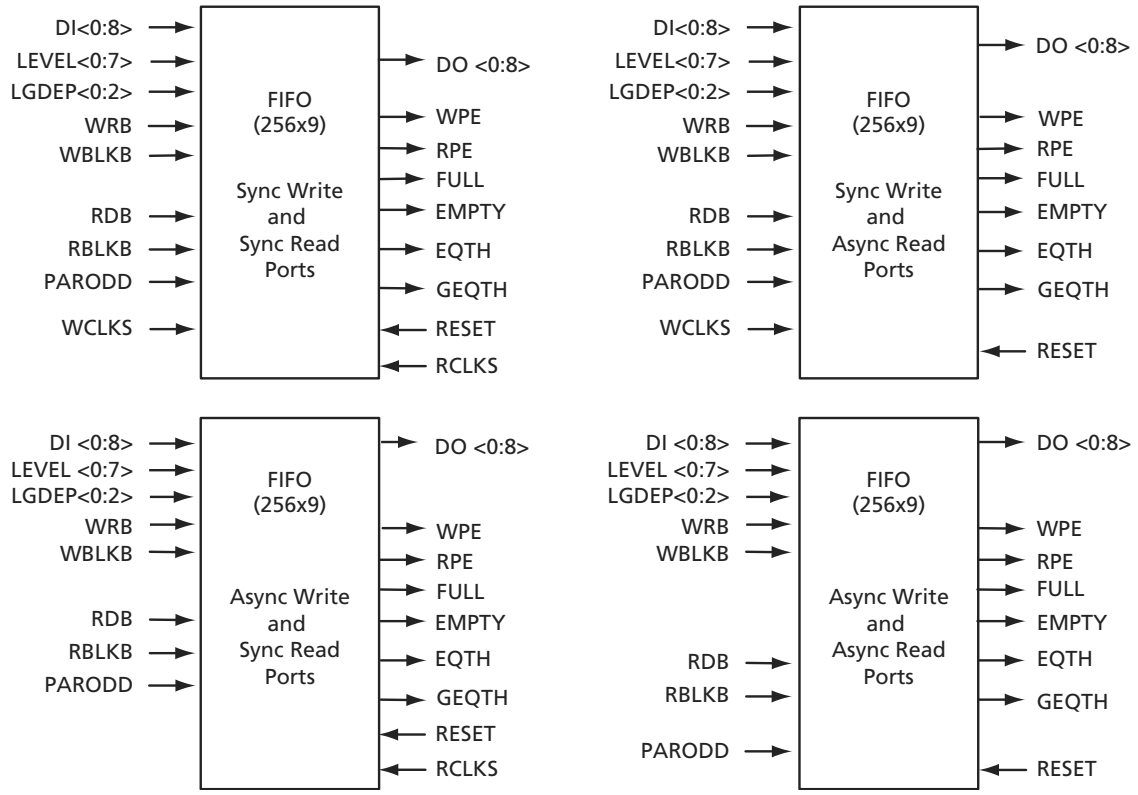
Prior to the application of signals to the rib drivers, they pass through programmable delay units, one per global network. These units permit the delaying of global signals relative to other signals to assist in the control of input set-up times. Not all possible combinations of input and output modes can be used. The degrees of freedom available in the bidirectional global pad system and in the clock conditioning circuit have been restricted. This avoids unnecessary and unwieldy design kit and software work.



Notes:

1. *FBDLY is a programmable delay line from 0 to 4 ns in 250 ps increments.*
2. *DLYA and DLYB are programmable delay lines, each with selectable values 0 ps, 250 ps, 500 ps, and 4 ns.*
3. *OBDIV will also divide the phase-shift since it takes place after the PLL Core.*

Figure 1-14 • **PLL Block – Top-Level View and Detailed PLL Block Diagram**



Note: *Each RAM block contains a multiplexer (called DMUX) for each output signal, increasing design efficiency. These DMUX cells do not consume any core logic tiles and connect directly to high-speed routing resources between the RAM blocks. They are used when RAM blocks are cascaded and are automatically inserted by the software tools.*

Figure 1-22 • **Basic FIFO Block Diagrams**

Table 1-15 • **Memory Block FIFO Interface Signals**

FIFO Signal	Bits	In/Out	Description
WCLKS	1	In	Write clock used for synchronization on write side
RCLKS	1	In	Read clock used for synchronization on read side
LEVEL <0:7>	8	In	Direct configuration implements static flag logic
RBLKB	1	In	Read block select (active Low)
RDB	1	In	Read pulse (active Low)
RESET	1	In	Reset for FIFO pointers (active Low)
WBLKB	1	In	Write block select (active Low)
DI<0:8>	9	In	Input data bits <0:8>, <8> will be generated parity if PARGEN is true
WRB	1	In	Write pulse (active Low)
FULL, EMPTY	2	Out	FIFO flags. FULL prevents write and EMPTY prevents read
EQTH, GEQTH	2	Out	EQTH is true when the FIFO holds the number of words specified by the LEVEL signal. GEQTH is true when the FIFO holds (LEVEL) words or more
DO<0:8>	9	Out	Output data bits <0:8>. <8> will be parity output if PARGEN is true.
RPE	1	Out	Read parity error (active High)
WPE	1	Out	Write parity error (active High)
LGDEP <0:2>	3	In	Configures DEPTH of the FIFO to $2^{(LGDEP+1)}$
PARODD	1	In	Parity generation/detect – Even when Low, Odd when High

Package Thermal Characteristics

The ProASIC^PLUS family is available in several package types with a range of pin counts. Actel has selected packages based on high pin count, reliability factors, and superior thermal characteristics.

Thermal resistance defines the ability of a package to conduct heat away from the silicon, through the package to the surrounding air. Junction-to-ambient thermal resistance is measured in degrees Celsius/Watt and is represented as Theta ja (Θ_{ja}). The lower the thermal resistance, the more efficiently a package will dissipate heat.

A package's maximum allowed power (P) is a function of maximum junction temperature (T_J), maximum ambient operating temperature (T_A), and junction-to-ambient thermal resistance Θ_{ja}. Maximum junction temperature is the maximum allowable temperature on the active surface of the IC and is 110° C. P is defined as:

$$P = \frac{T_J - T_A}{\Theta_{ja}}$$

EQ 1-4

Θ_{ja} is a function of the rate (in linear feet per minute (lfpm)) of airflow in contact with the package. When the estimated power consumption exceeds the maximum allowed power, other means of cooling, such as increasing the airflow rate, must be used. The maximum power dissipation allowed for a Military temperature device is specified as a function of Θ_{jc}. The absolute maximum junction temperature is 150°C.

The calculation of the absolute maximum power dissipation allowed for a Military temperature application is illustrated in the following example for a 456-pin PBGA package:

$$\text{Maximum Power Allowed} = \frac{\text{Max. junction temp. (°C)} - \text{Max. case temp. (°C)}}{\theta_{jc}(\text{°C/W})} = \frac{150\text{°C} - 125\text{°C}}{3.0\text{°C/W}} = 8.333\text{W}$$

EQ 1-5

Table 1-16 • **Package Thermal Characteristics**

Plastic Packages	Pin Count	θ_{jc}	θ_{ja} Still Air	θ_{ja} 1.0 m/s 200 ft./min.	θ_{ja} 2.5 m/s 500 ft./min.	Units
Thin Quad Flat Pack (TQFP)	100	14.0	33.5	27.4	25.0	°C/W
Thin Quad Flat Pack (TQFP)	144	11.0	33.5	28.0	25.7	°C/W
Plastic Quad Flat Pack (PQFP)[1]	208	8.0	26.1	22.5	20.8	°C/W
PQFP with Heat spreader[2]	208	3.8	16.2	13.3	11.9	°C/W
Plastic Ball Grid Array (PBGA)	456	3.0	15.6	12.5	11.6	°C/W
Fine Pitch Ball Grid Array (FBGA)	144	3.8	26.9	22.9	21.5	°C/W
Fine Pitch Ball Grid Array (FBGA)	256	3.8	26.6	22.8	21.5	°C/W
Fine Pitch Ball Grid Array (FBGA)[3]	484	3.2	18.0	14.7	13.6	°C/W
Fine Pitch Ball Grid Array (FBGA)[4]	484	3.2	20.5	17.0	15.9	°C/W
Fine Pitch Ball Grid Array (FBGA)	676	3.2	16.4	13.0	12.0	°C/W
Fine Pitch Ball Grid Array (FBGA)	896	2.4	13.6	10.4	9.4	°C/W
Fine Pitch Ball Grid Array (FBGA)	1152	1.8	12.0	8.9	7.9	°C/W
Ceramic Quad Flat Pack (CQFP)	208	2.0	22.0	19.8	18.0	°C/W
Ceramic Quad Flat Pack (CQFP)	352	2.0	17.9	16.1	14.7	°C/W
Ceramic Column Grid Array (CCGA/LGA)	624	6.5	8.9	8.5	8.0	°C/W

Notes:

1. *Valid for the following devices irrespective of temperature grade: APA075, APA150, and APA300*
2. *Valid for the following devices irrespective of temperature grade: APA450, APA600, APA750, and APA1000*
3. *Depopulated Array*
4. *Full array*

Logic-Tile Contribution—P_{logic}

P_{logic}, the logic-tile component of AC power dissipation, is given by

$$P_{logic} = P3 * mc * Fs$$

where:

- P3 = 1.4 µW/MHz is the average power consumption of a logic tile per MHz of its output toggling rate. The maximum output toggling rate is Fs/2.
- mc = the number of logic tiles switching during each Fs cycle
- Fs = the clock frequency

I/O Output Buffer Contribution—$P_{outputs}$

$P_{outputs}$, the I/O component of AC power dissipation, is given by

$$P_{outputs} = (P4 + (C_{load} * V_{DDP}^2)) * p * Fp$$

where:

- P4 = 326 µW/MHz is the intrinsic power consumption of an output pad normalized per MHz of the output frequency. This is the total I/O current V_{DDP}.
- C_{load} = the output load
- p = the number of outputs
- Fp = the average output frequency

I/O Input Buffer's Buffer Contribution—P_{inputs}

The input's component of AC power dissipation is given by

$$P_{inputs} = P8 * q * Fq$$

where:

- P8 = 29 µW/MHz is the intrinsic power consumption of an input pad normalized per MHz of the input frequency.
- q = the number of inputs
- Fq = the average input frequency

PLL Contribution—P_{pll}

$$P_{pll} = P9 * N_{pll}$$

where:

- P9 = 7.5 mW. This value has been estimated at maximum PLL clock frequency.
- N_{PII} = number of PLLs used

RAM Contribution—P_{memory}

Finally, P_{memory}, the memory component of AC power consumption, is given by

$$P_{memory} = P6 * N_{memory} * F_{memory} * E_{memory}$$

where:

- P6 = 175 µW/MHz is the average power consumption of a memory block per MHz of the clock
- N_{memory} = the number of RAM/FIFO blocks (1 block = 256 words * 9 bits)
- F_{memory} = the clock frequency of the memory
- E_{memory} = the average number of active blocks divided by the total number of blocks (N) of the memory.
  - Typical values for E_{memory} would be 1/4 for a 1k x 8,9,16, 32 memory and 1/16 for a 4kx8, 9, 16, and 32 memory configuration
  - In addition, an application-dependent component to E_{memory} can be considered. For example, for a 1kx8 memory configuration using only 1 cycle out of 2, E_{memory} = 1/4*1/2 = 1/8

The following is an APA750 example using a shift register design with 13,440 storage tiles (Register) and 0 logic tiles. This design has one clock at 10 MHz, and 24 outputs toggling at 5 MHz. We then calculate the various components as follows:

P_{clock}

Fs = 10 MHz

R = 13,440

=> $P_{clock} = (P1 + (P2*R) - (P7*R^2)) * Fs = 121.5$ mW

$P_{storage}$

ms = 13,440 (in a shift register 100% of storage tiles are toggling at each clock cycle and Fs = 10 MHz)

=> $P_{storage} = P5 * ms * Fs = 147.8$ mW

P_{logic}

mc = 0 (no logic tiles in this shift register)

=> $P_{logic} = 0$ mW

$P_{outputs}$

C_{load} = 40 pF

V_{DDP} = 3.3 V

p = 24

Fp = 5 MHz

=> $P_{outputs} = (P4 + (C_{load} * V_{DDP}^2)) * p * Fp = 91.4$ mW

P_{inputs}

q = 1

Fq = 10 MHz

=> $P_{inputs} = P8 * q * Fq = 0.3$ mW

P_{memory}

N_{memory} = 0 (no RAM/FIFO blocks in this shift register)

=> $P_{memory} = 0$ mW

P_{ac}

=> 361 mW

P_{total}

$P_{dc} + P_{ac} = 374$ mW (typical)

Operating Conditions

Standard and –F parts are the same unless otherwise noted. All –F parts are only available as commercial.

Table 1-17 • **Absolute Maximum Ratings***

Parameter	Condition	Minimum	Maximum	Units
Supply Voltage Core (V_{DD})		–0.3	3.0	V
Supply Voltage I/O Ring (V_{DDP})		–0.3	4.0	V
DC Input Voltage		–0.3	V_{DDP} + 0.3	V
PCI DC Input Voltage		–1.0	V_{DDP} + 1.0	V
PCI DC Input Clamp Current (absolute)	V_{IN} < –1 or V_{IN} = V_{DDP} + 1 V	10		mA
LVPECL Input Voltage		–0.3	V_{DDP} + 0.5	V
GND		0	0	V

Note: **Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. Devices should not be operated outside the Recommended Operating Conditions.*

Table 1-18 • **Programming, Storage, and Operating Limits**

			Storage Temperature		Operating
Product Grade	Programming Cycles (min.)	Program Retention (min.)	Min.	Max.	T_J Max. Junction Temperature
Commercial	500	20 years	–55°C	110°C	110°C
Industrial	500	20 years	–55°C	110°C	110°C
Military	100	Refer to Table 1-19 on page 1-35	–65°C	150°C	150°C
MIL-STD-883	100	Refer to Table 1-19 on page 1-35	–65°C	150°C	150°C

Performance Retention

For devices operated and stored at 110°C or less, the performance retention period is 20 years after programming. For devices operated and stored at temperatures greater than 110°C, refer to Table 1-19 on page 1-35 to determine the performance retention period. Actel does not guarantee performance if the performance retention period is exceeded. Designers can determine the performance retention period from the following table.

Evaluate the percentage of time spent at the highest temperature, then determine the next highest temperature to which the device will be exposed. In Table 1-19 on page 1-35, find the temperature profile that most closely matches the application.

Example – the ambient temperature of a system cycles between 100°C (25% of the time) and 50°C (75% of the time). No forced ventilation cooling system is in use. An APA600-PQ208M FPGA operates in the system, dissipating 1 W. The package thermal resistance (junction-to-ambient) in still air Θ_{ja} is 20°C/W, indicating that the junction temperature of the FPGA will be 120°C (25% of the time) and 70°C (75% of the time). The entry in Table 1-19 on page 1-35, which most closely matches the application, is 25% at 125°C with 75% at 110°C. Performance retention in this example is at least 16.0 years.

Note that exceeding the stated retention period may result in a performance degradation in the FPGA below the worst-case performance indicated in the Actel Timer. To ensure that performance does not degrade below the worst-case values in the Actel Timer, the FPGA must be reprogrammed within the performance retention period. In addition, note that performance retention is independent of whether or not the FPGA is operating. The retention period of a device in storage at a given temperature will be the same as the retention period of a device operating at that junction temperature.

Table 1-19 • **Military Temperature Grade Product Performance Retention**

Minimum Time at T_J 110°C or below	Minimum Time at T_J 125°C or below	Minimum Time at T_J 135°C or below	Minimum Time at T_J 150°C or below	Minimum Performance Retention (Years)
100%				20.0
90%	10%			18.2
75%	25%			16
90%		10%		15.4
50%	50%			13.3
90%			10%	11.8
75%		25%		11.4
	100%			10
	90%	10%		9.1
50%		50%		8
	75%	25%		8
	90%		10%	7.7
75%			25%	7.3
	50%	50%		6.7
	75%		25%	5.7
		100%		5
		90%	10%	4.5
50%			50%	4.4
	50%		50%	4
		75%	25%	4
		50%	50%	3.3
			100%	2.5

Table 1-23 • **DC Electrical Specifications (V_{DDP} = 3.3 V ±0.3 V and V_{DD} = 2.5 V ±0.2 V) Applies to Commercial and Industrial Temperature Only**

Symbol	Parameter	Conditions		Commercial/Industrial[1] Min.	Typ.	Max.	Units
V_{OH}	Output High Voltage 3.3 V I/O, High Drive (OB33P) 3.3 V I/O, Low Drive (OB33L)	 I_{OH} = –14 mA I_{OH} = –24 mA I_{OH} = –6 mA I_{OH} = –12 mA		 0.9*V_{DDP} 2.4 0.9*V_{DDP} 2.4			V
V_{OL}	Output Low Voltage 3.3 V I/O, High Drive (OB33P) 3.3 V I/O, Low Drive (OB33L)	 I_{OL} = 15 mA I_{OL} = 20 mA I_{OL} = 28 mA I_{OL} = 7 mA I_{OL} = 10 mA I_{OL} = 15 mA				 0.1V_{DDP} 0.4 0.7 0.1V_{DDP} 0.4 0.7	V
V_{IH}[5]	Input High Voltage 3.3 V Schmitt Trigger Inputs 3.3 V LVTTL/LVCMOS 2.5 V Mode			 1.6 2 1.7		 V_{DDP} + 0.3 V_{DDP} + 0.3 V_{DDP} + 0.3	V
V_{IL}[6]	Input Low Voltage 3.3 V Schmitt Trigger Inputs 3.3 V LVTTL/LVCMOS 2.5 V Mode			 –0.3 –0.3 –0.3		 0.8 0.8 0.7	V
$R_{WEAKPULLUP}$	Weak Pull-up Resistance (IOB33U)	$V_{IN} \geq$ 1.5 V		7		43	kΩ
$R_{WEAKPULLUP}$	Weak Pull-up Resistance (IOB25U)	$V_{IN} \geq$ 1.5 V		7		43	kΩ
I_{IN}	Input Current	with pull up (V_{IN} = GND)		–300		–40	µA
		without pull up (V_{IN} = GND or V_{DD})		–10		10	µA
I_{DDQ}	Quiescent Supply Current (standby) Commercial	V_{IN} = GND[3] or V_{DD}	Std.		5.0	15	mA
			–F[2]		5.0	25	mA
I_{DDQ}	Quiescent Supply Current (standby) Industrial	V_{IN} = GND[3] or V_{DD}	Std.		5.0	20	mA
I_{DDQ}	Quiescent Supply Current (standby) Military	V_{IN} = GND[3] or V_{DD}	Std.		5.0	25	mA

Notes:

1. *All process conditions. Commercial/Industrial: Junction Temperature: –40 to +110°C.*
2. *All –F parts are only available as commercial.*
3. *No pull-up resistor required.*
4. *This will not exceed 2 mA total per device.*
5. *During transitions, the input signal may overshoot to V_{DDP} +1.0 V for a limited time of no larger than 10% of the duty cycle.*
6. *During transitions, the input signal may undershoot to –1.0 V for a limited time of no larger than 10% of the duty cycle.*

Table 1-37 • **Worst-Case Military Conditions**
V_{DDP} = 3.0V, V_{DD} = 2.3V, T_J = 125°C for Military/MIL-STD-883

Macro Type	Description	Max. t_{INYH}[1]	Max. t_{INYL}[2]	Units
		Std.	Std.	
IB33	3.3V, CMOS Input Levels[3], No Pull-up Resistor	0.5	0.6	ns
IB33S	3.3V, CMOS Input Levels[3], No Pull-up Resistor, Schmitt Trigger	0.6	0.8	ns

Notes:

1. *t_{INYH} = Input Pad-to-Y High*
2. *t_{INYL} = Input Pad-to-Y Low*
3. *LVTTL delays are the same as CMOS delays.*
4. *For LP Macros, V_{DDP}=2.3V for delays.*

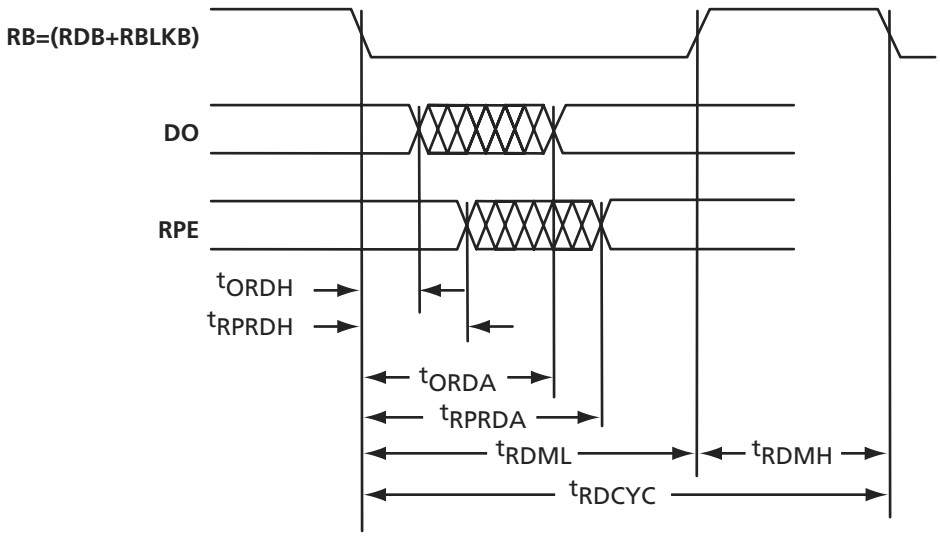
Table 1-38 • **Worst-Case Military Conditions**
V_{DDP} = 2.3V, V_{DD} = 2.3V, T_J = 125°C for Military/MIL-STD-883

Macro Type	Description	Max. t_{INYH}[1]	Max. t_{INYL}[2]	Units
		Std.	Std.	
IB25LP	2.5V, CMOS Input Levels[3], Low Power	0.9	0.7	ns
IB25LPS	2.5V, CMOS Input Levels[3], Low Power, Schmitt Trigger	0.8	1.0	ns

Notes:

1. *t_{INYH} = Input Pad-to-Y High*
2. *t_{INYL} = Input Pad-to-Y Low*
3. *LVTTL delays are the same as CMOS delays.*
4. *For LP Macros, V_{DDP}=2.3V for delays.*

Asynchronous SRAM Read, RDB Controlled



Note: *The plot shows the normal operation status.*

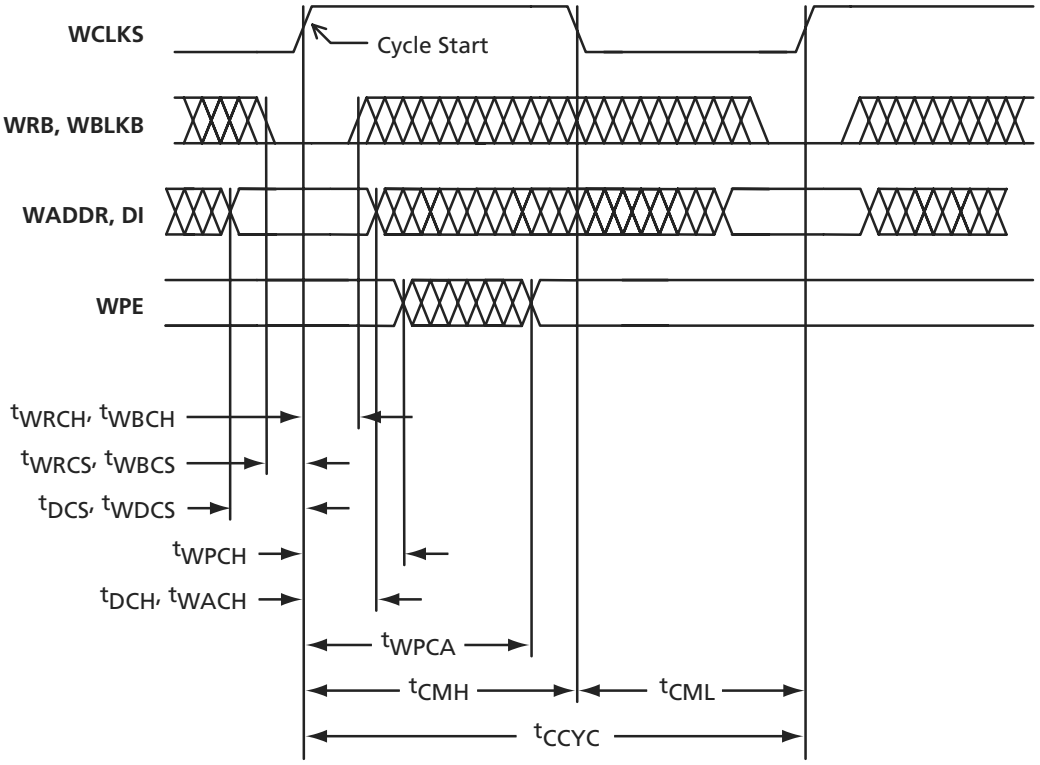
Figure 1-35 • **Asynchronous SRAM Read, RDB Controlled**

Table 1-56 • **T_J = 0°C to 110°C; V_{DD} = 2.3 V to 2.7 V for Commercial/industrial**
T_J = –55°C to 150°C, V_{DD} = 2.3 V to 2.7 V for Military/MIL-STD-883

Symbol t_{xxx}	Description	Min.	Max.	Units	Notes
ORDA	New DO access from RB ↓	7.5		ns	
ORDH	Old DO valid from RB ↓		3.0	ns	
RDCYC	Read cycle time	7.5		ns	
RDMH	RB high phase	3.0		ns	Inactive setup to new cycle
RDML	RB low phase	3.0		ns	Active
RPRDA	New RPE access from RB ↓	9.5		ns	
RPRDH	Old RPE valid from RB ↓		3.0	ns	

Note: *All –F speed grade devices are 20% slower than the standard numbers.*

Synchronous SRAM Write



Note: *The plot shows the normal operation status.*

Figure 1-36 • **Synchronous SRAM Write**

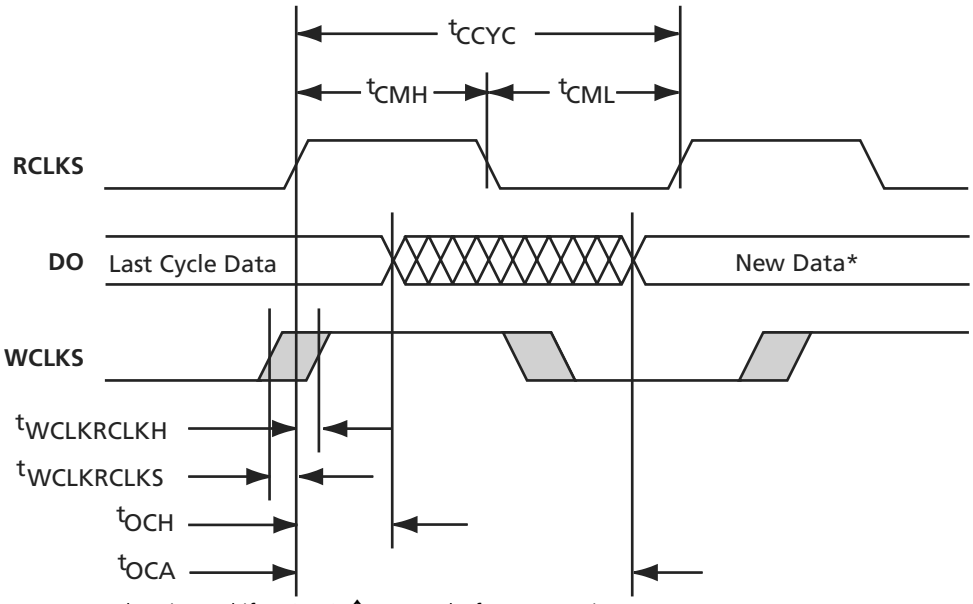
Table 1-57 • **T_J = 0°C to 110°C; V_{DD} = 2.3 V to 2.7 V for Commercial/industrial**
T_J = –55°C to 150°C, V_{DD} = 2.3 V to 2.7 V for Military/MIL-STD-883

Symbol t_{xxx}	Description	Min.	Max.	Units	Notes
CCYC	Cycle time	7.5		ns	
CMH	Clock high phase	3.0		ns	
CML	Clock low phase	3.0		ns	
DCH	DI hold from WCLKS ↑	0.5		ns	
DCS	DI setup to WCLKS ↑	1.0		ns	
WACH	WADDR hold from WCLKS ↑	0.5		ns	
WDCS	WADDR setup to WCLKS ↑	1.0		ns	
WPCA	New WPE access from WCLKS ↑	3.0		ns	WPE is invalid while PARGEN is active
WPCH	Old WPE valid from WCLKS ↑		0.5	ns	
WRCH, WBCH	WRB & WBLKB hold from WCLKS ↑	0.5		ns	
WRCS, WBCS	WRB & WBLKB setup to WCLKS ↑	1.0		ns	

Notes:

1. *On simultaneous read and write accesses to the same location, DI is output to DO.*
2. *All –F speed grade devices are 20% slower than the standard numbers.*

Synchronous Write and Read to the Same Location



Note: *The plot shows the normal operation status.*

Figure 1-37 • **Synchronous Write and Read to the Same Location**

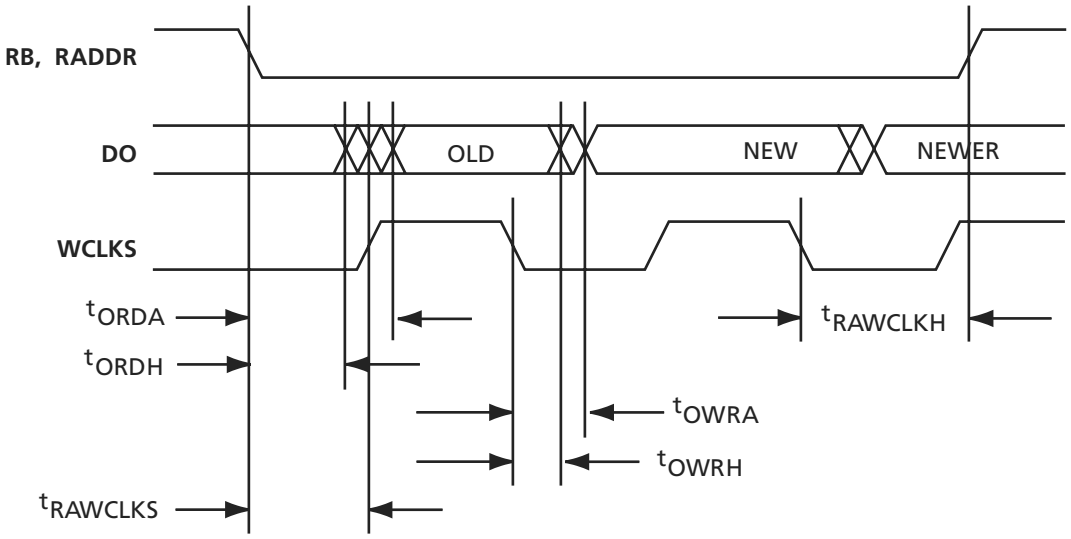
Table 1-58 • **T_J = 0°C to 110°C; V_{DD} = 2.3 V to 2.7 V for Commercial/industrial**
T_J = –55°C to 150°C, V_{DD} = 2.3 V to 2.7 V for Military/MIL-STD-883

Symbol t_{xxx}	Description	Min.	Max.	Units	Notes
CCYC	Cycle time	7.5		ns	
CMH	Clock high phase	3.0		ns	
CML	Clock low phase	3.0		ns	
WCLKRCLKS	WCLKS ↑ to RCLKS ↑ setup time	– 0.1		ns	
WCLKRCLKH	WCLKS ↑ to RCLKS ↑ hold time		7.0	ns	
OCH	Old DO valid from RCLKS ↑		3.0	ns	OCA/OCH displayed for Access Timed Output
OCA	New DO valid from RCLKS ↑	7.5		ns	

Notes:

1. *This behavior is valid for Access Timed Output and Pipelined Mode Output. The table shows the timings of an Access Timed Output.*
2. *During synchronous write and synchronous read access to the same location, the new write data will be read out if the active write clock edge occurs before or at the same time as the active read clock edge. The negative setup time insures this behavior for WCLKS and RCLKS driven by the same design signal.*
3. *If WCLKS changes after the hold time, the data will be read.*
4. *A setup or hold time violation will result in unknown output data.*
5. *All –F speed grade devices are 20% slower than the standard numbers.*

Synchronous Write and Asynchronous Read to the Same Location



Note: *The plot shows the normal operation status.*

Figure 1-40 • **Synchronous Write and Asynchronous Read to the Same Location**

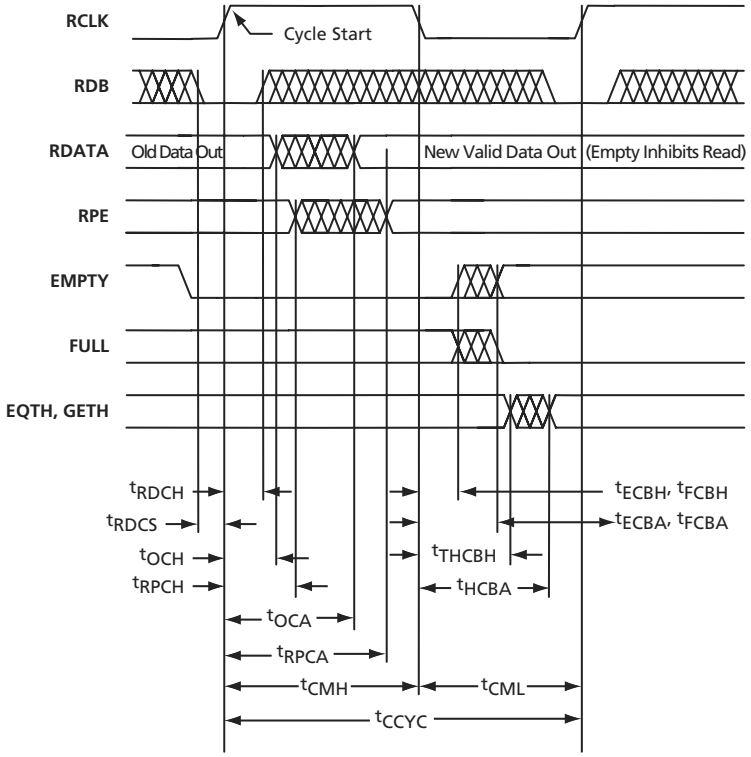
Table 1-61 • **T_J = 0°C to 110°C; V_{DD} = 2.3 V to 2.7 V for Commercial/industrial**
T_J = –55°C to 150°C, V_{DD} = 2.3 V to 2.7 V for Military/MIL-STD-883

Symbol t_{xxx}	Description	Min.	Max.	Units	Notes
ORDA	New DO access from RB ↓	7.5		ns	
ORDH	Old DO valid from RB ↓		3.0	ns	
OWRA	New DO access from WCLKS ↓	3.0		ns	
OWRH	Old DO valid from WCLKS ↓		0.5	ns	
RAWCLKS	RB ↓ or RADDR from WCLKS ↑	5.0		ns	
RAWCLKH	RB ↑ or RADDR from WCLKS ↓	5.0		ns	

Notes:

1. *During an asynchronous read cycle, each write operation (synchronous or asynchronous) to the same location will automatically trigger a read operation which updates the read data.*
2. *Violation of RAWCLKS will disturb access to OLD data.*
3. *Violation of RAWCLKH will disturb access to NEWER data.*
4. *All –F speed grade devices are 20% slower than the standard numbers.*

Synchronous FIFO Read, Access Timed Output Strobe (Synchronous Transparent)



Note: *The plot shows the normal operation status.*

Figure 1-45 • **Synchronous FIFO Read, Access Timed Output Strobe (Synchronous Transparent)**

Table 1-65 • **T_J = 0°C to 110°C; V_{DD} = 2.3 V to 2.7 V for Commercial/industrial**
T_J = –55°C to 150°C, V_{DD} = 2.3 V to 2.7 V for Military/MIL-STD-883

Symbol t_{xxx}	Description	Min.	Max.	Units	Notes
CCYC	Cycle time	7.5		ns	
CMH	Clock high phase	3.0		ns	
CML	Clock low phase	3.0		ns	
ECBA	New EMPTY access from RCLKS ↓	3.0[1]		ns	
FCBA	FULL ↓ access from RCLKS ↓	3.0[1]		ns	
ECBH, FCBH, THCBH	Old EMPTY, FULL, EQTH, & GETH valid hold time from RCLKS ↓		1.0	ns	Empty/full/thresh are invalid from the end of hold until the new access is complete
OCA	New DO access from RCLKS ↑	7.5		ns	
OCH	Old DO valid from RCLKS ↑		3.0	ns	
RDCH	RDB hold from RCLKS ↑	0.5		ns	
RDCS	RDB setup to RCLKS ↑	1.0		ns	
RPCA	New RPE access from RCLKS ↑	9.5		ns	
RPCH	Old RPE valid from RCLKS ↑		3.0	ns	
HCBA	EQTH or GETH access from RCLKS ↓	4.5		ns	

Notes:

1. *At fast cycles, ECBA and FCBA = MAX (7.5 ns – CMH), 3.0 ns.*
2. *All –F speed grade devices are 20% slower than the standard numbers.*

V_{PP} Programming Supply Pin

This pin may be connected to any voltage between GND and 16.5 V during normal operation, or it can be left unconnected.[2] For information on using this pin during programming, see the *In-System Programming ProASIC^PLUS Devices* application note. Actel recommends floating the pin or connecting it to V_{DDP}.

V_{PN} Programming Supply Pin

This pin may be connected to any voltage between 0.5V and –13.8 V during normal operation, or it can be left unconnected.[3] For information on using this pin during programming, see the *In-System Programming ProASIC^PLUS Devices* application note. Actel recommends floating the pin or connecting it to GND.

Recommended Design Practice for V_{PN}/V_{PP}

ProASIC^PLUS Devices – APA450, APA600, APA750, APA1000

Bypass capacitors are required from V_{PP} to GND and V_{PN} to GND for all ProASIC^PLUS devices during programming. During the erase cycle, ProASIC^PLUS devices may have current surges on the V_{PP} and V_{PN} power supplies. The only way to maintain the integrity of the power distribution to the ProASIC^PLUS device during these current surges is to counteract the inductance of the finite length conductors that distribute the power to the device. This can be accomplished by providing sufficient bypass capacitance between the V_{PP} and V_{PN} pins and GND (using the shortest paths possible). Without sufficient bypass capacitance to counteract the inductance, the V_{PP} and V_{PN} pins may incur a voltage spike beyond the voltage that the device can withstand. This issue applies to all programming configurations.

The solution prevents spikes from damaging the ProASIC^PLUS devices. Bypass capacitors are required for the V_{PP} and V_{PN} pads. Use a 0.01 µF to 0.1 µF ceramic capacitor with a 25 V or greater rating. To filter low-frequency noise (decoupling), use a 4.7 µF (low ESR, <1 <Ω, tantalum, 25 V or greater rating) capacitor. The capacitors should be located as close to the device pins as possible (within 2.5 cm is desirable). The smaller, high-frequency capacitor should be placed closer to the device pins than the larger low-frequency capacitor. The same dual-capacitor circuit should be used on both the V_{PP} and V_{PN} pins (Figure 1-49).

ProASIC^PLUS Devices – APA075, APA150, APA300

These devices do not require bypass capacitors on the V_{PP} and V_{PN} pins as long as the total combined distance of the programming cable and the trace length on the board is less than or equal to 30 inches. Note: For trace lengths greater than 30 inches, use the bypass capacitor recommendations in the previous section.

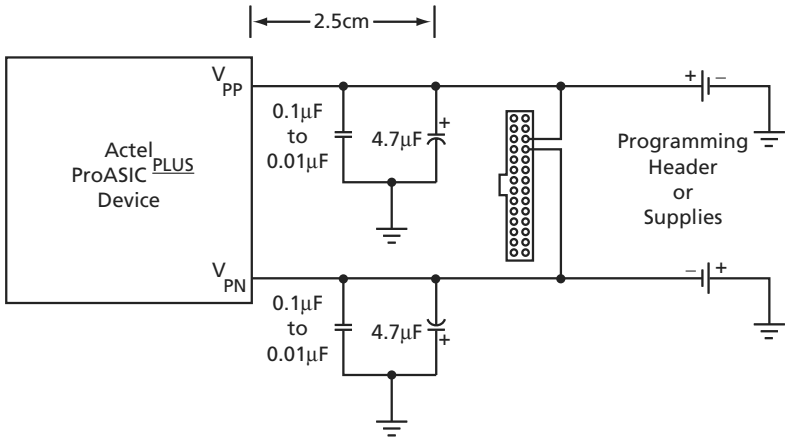


Figure 1-49 • **ProASIC^PLUS V_{PP} and V_{PN} Capacitor Requirements**

2. *There is a nominal 40 kΩ pull-up resistor on V_{PP}*
3. *There is a nominal 40 kΩ pull-down resistor on V_{PN}.*