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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	73728
Number of I/O	158
Number of Gates	300000
Voltage - Supply	2.3V ~ 2.7V
Mounting Type	Surface Mount
Operating Temperature	-55°C ~ 125°C (TC)
Package / Case	208-BFQFP
Supplier Device Package	208-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/apa300-pqg208m

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General Description

The ProASIC^PLUS family of devices, Actel's second-generation Flash FPGAs, offers enhanced performance over Actel's ProASIC family. It combines the advantages of ASICs with the benefits of programmable devices through nonvolatile Flash technology. This enables engineers to create high-density systems using existing ASIC or FPGA design flows and tools. In addition, the ProASIC^PLUS family offers a unique clock conditioning circuit based on two on-board phase-locked loops (PLLs). The family offers up to one million system gates, supported with up to 198 kbits of two-port SRAM and up to 712 user I/Os, all providing 50 MHz PCI performance.

Advantages to the designer extend beyond performance. Unlike SRAM-based FPGAs, four levels of routing hierarchy simplify routing, while the use of Flash technology allows all functionality to be live at power-up. No external boot PROM is required to support device programming. While on-board security mechanisms prevent access to the program information, reprogramming can be performed in-system to support future design iterations and field upgrades. The device's architecture mitigates the complexity of ASIC migration at higher user volume. This makes ProASIC^PLUS a cost-effective solution for applications in the networking, communications, computing, and avionics markets.

The ProASIC^PLUS family achieves its nonvolatility and reprogrammability through an advanced Flash-based 0.22 µm LVCMOS process with four layers of metal. Standard CMOS design techniques are used to implement logic and control functions, including the PLLs and LVPECL inputs. This results in predictable performance compatible with gate arrays.

The ProASIC^PLUS architecture provides granularity comparable to gate arrays. The device core consists of a Sea-of-Tiles™. Each tile can be configured as a flip-flop, latch, or three-input/one-output logic function by programming the appropriate Flash switches. The combination of fine granularity, flexible routing resources, and abundant Flash switches allow 100% utilization and over 95% routability for highly congested designs. Tiles and larger functions are interconnected through a four-level routing hierarchy.

Embedded two-port SRAM blocks with built-in FIFO/RAM control logic can have user-defined depths and widths. Users can also select programming for synchronous or asynchronous operation, as well as parity generations or checking.

The unique clock conditioning circuitry in each device includes two clock conditioning blocks. Each block provides a PLL core, delay lines, phase shifts (0° and 180°), and clock multipliers/dividers, as well as the circuitry needed to provide bidirectional access to the PLL. The PLL block contains four programmable frequency dividers which allow the incoming clock signal to be divided by a wide range of factors from 1 to 64. The clock conditioning circuit also delays or advances the incoming reference clock up to 8 ns (in increments of 0.25 ns). The PLL can be configured internally or externally during operation without redesigning or reprogramming the part. In addition to the PLL, there are two LVPECL differential input pairs to accommodate high-speed clock and data inputs.

To support customer needs for more comprehensive, lower-cost, board-level testing, Actel's ProASIC^PLUS devices are fully compatible with IEEE Standard 1149.1 for test access port and boundary-scan test architecture. For more information concerning the Flash FPGA implementation, please refer to the "Boundary Scan (JTAG)" section on page 1-11.

ProASIC^PLUS devices are available in a variety of high-performance plastic packages. Those packages and the performance features discussed above are described in more detail in the following sections.

Routing Resources

The routing structure of ProASIC^PLUS devices is designed to provide high performance through a flexible four-level hierarchy of routing resources: ultra-fast local resources, efficient long-line resources, high-speed, very long-line resources, and high performance global networks.

The ultra-fast local resources are dedicated lines that allow the output of each tile to connect directly to every input of the eight surrounding tiles (Figure 1-4).

The efficient long-line resources provide routing for longer distances and higher fanout connections. These resources vary in length (spanning 1, 2, or 4 tiles), run both vertically and horizontally, and cover the entire ProASIC^PLUS device (Figure 1-5 on page 1-5). Each tile can drive signals onto the efficient long-line resources, which can in turn access every input of every tile. Active buffers are inserted automatically by routing software to limit the loading effects due to distance and fanout.

The high-speed, very long-line resources, which span the entire device with minimal delay, are used to route very long or very high fanout nets. (Figure 1-6 on page 1-6).

The high-performance global networks are low-skew, high fanout nets that are accessible from external pins or from internal logic (Figure 1-7 on page 1-7). These nets are typically used to distribute clocks, resets, and other high fanout nets requiring a minimum skew. The global networks are implemented as clock trees, and signals can be introduced at any junction. These can be employed hierarchically with signals accessing every input on all tiles.

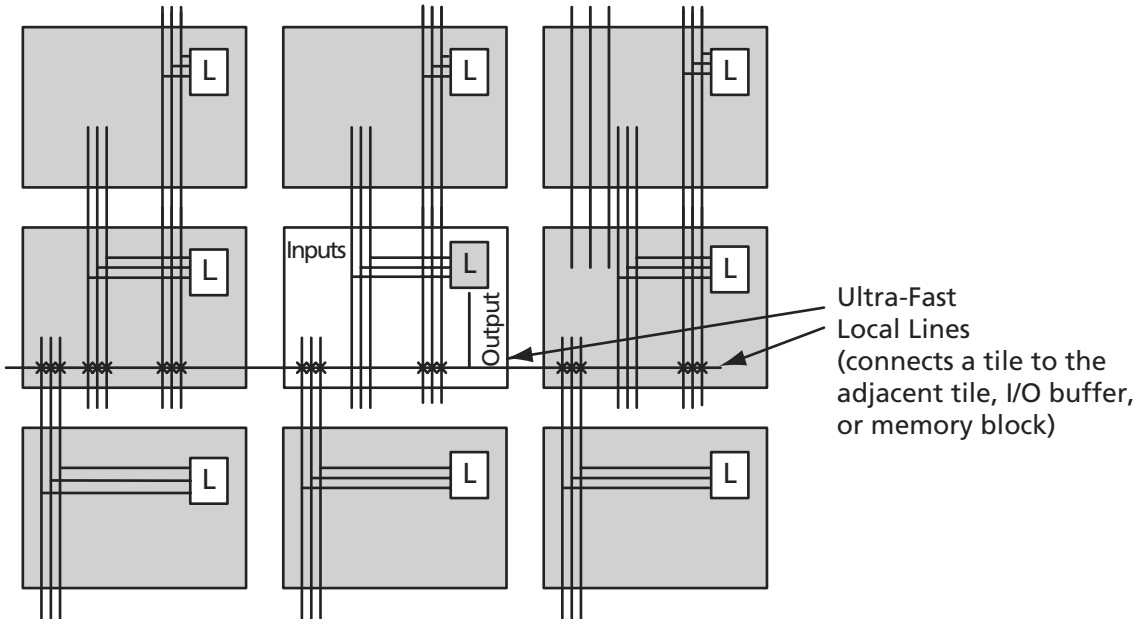


Figure 1-4 • **Ultra-Fast Local Resources**

Array Coordinates

During many place-and-route operations in Actel's Designer software tool, it is possible to set constraints that require array coordinates.

Table 1-2 is provided as a reference. The array coordinates are measured from the lower left (0,0). They can be used in region constraints for specific groups of core cells, I/Os, and RAM blocks. Wild cards are also allowed.

I/O and cell coordinates are used for placement constraints. Two coordinate systems are needed because there is not a one-to-one correspondence between I/O cells and core cells. In addition, the I/O coordinate system changes depending on the die/package combination.

Core cell coordinates start at the lower left corner (represented as (1,1)) or at (1,5) if memory blocks are present at the bottom. Memory coordinates use the same system and are indicated in Table 1-2. The memory coordinates for an APA1000 are illustrated in Figure 1-8. For more information on how to use constraints, see the *Designer User's Guide* or online help for ProASIC^PLUS software tools.

Table 1-2 • **Array Coordinates**

	Logic Tile				Memory Rows		All	
	Min.		Max.		Bottom	Top		
Device	**x**	**y**	**x**	**y**	**y**	**y**	**Min.**	**Max.**
APA075	1	1	96	32	–	(33,33) or (33, 35)	0,0	97, 37
APA150	1	1	128	48	–	(49,49) or (49, 51)	0,0	129, 53
APA300	1	5	128	68	(1,1) or (1,3)	(69,69) or (69, 71)	0,0	129, 73
APA450	1	5	192	68	(1,1) or (1,3)	(69,69) or (69, 71)	0,0	193, 73
APA600	1	5	224	100	(1,1) or (1,3)	(101,101) or (101, 103)	0,0	225, 105
APA750	1	5	256	132	(1,1) or (1,3)	(133,133) or (133, 135)	0,0	257, 137
APA1000	1	5	352	164	(1,1) or (1,3)	(165,165) or (165, 167)	0,0	353, 169

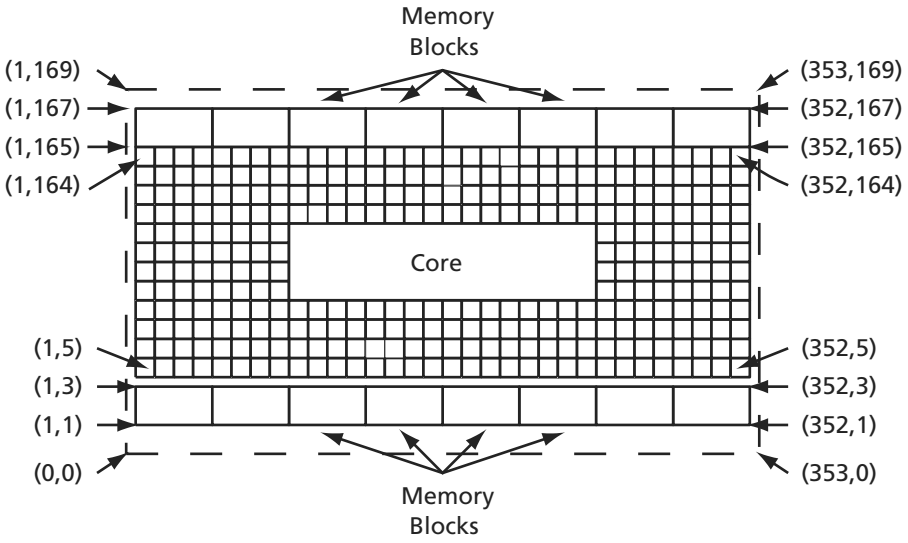


Figure 1-8 • **Core Cell Coordinates for the APA1000**

Power-Up Sequencing

While ProASIC^PLUS devices are live at power-up, the order of V_{DD} and V_{DDP} power-up is important during system start-up. V_{DD} should be powered up simultaneously with V_{DDP} on ProASIC^PLUS devices. Failure to follow these guidelines may result in undesirable pin behavior during system start-up. For more information, refer to Actel's *Power-Up Behavior of ProASIC^PLUS Devices* application note.

LVPECL Input Pads

In addition to standard I/O pads and power pads, ProASIC^PLUS devices have a single LVPECL input pad on both the east and west sides of the device, along with AVDD and AGND pins to power the PLL block. The LVPECL pad cell consists of an input buffer (containing a low voltage differential amplifier) and a signal and its complement, PPECL (I/P) (PECLN) and NPECL (PECLREF). The LVPECL input pad cell differs from the standard I/O cell in that it is operated from V_{DD} only.

Since it is exclusively an input, it requires no output signal, output enable signal, or output configuration bits. As a special high-speed differential input, it also does not require pull ups. Recommended termination for LVPECL inputs is shown in Figure 1-10. The LVPECL pad cell compares voltages on the PPECL (I/P) pad (as illustrated in Figure 1-11) and the NPECL pad and sends the results to the global MUX (Figure 1-14 on page 1-14). This high-speed, low-skew output essentially controls the clock conditioning circuit.

LVPECLs are designed to meet LVPECL JEDEC receiver standard levels (Table 1-5).

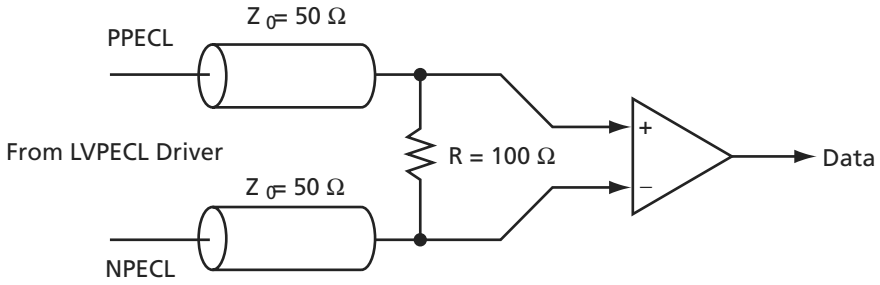


Figure 1-10 • **Recommended Termination for LVPECL Inputs**

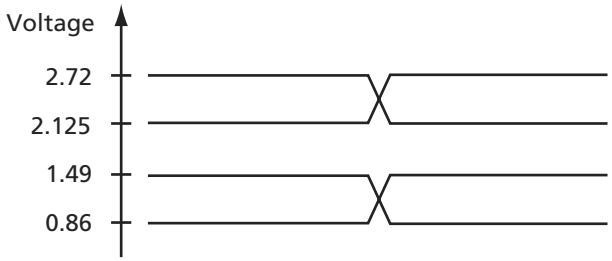


Figure 1-11 • **LVPECL High and Low Threshold Values**

Table 1-5 • **LVPECL Receiver Specifications**

Symbol	Parameter	Min.	Max	Units
V_{IH}	Input High Voltage	1.49	2.72	V
V_{IL}	Input Low Voltage	0.86	2.125	V
V_{ID}	Differential Input Voltage	0.3	V_{DD}	V

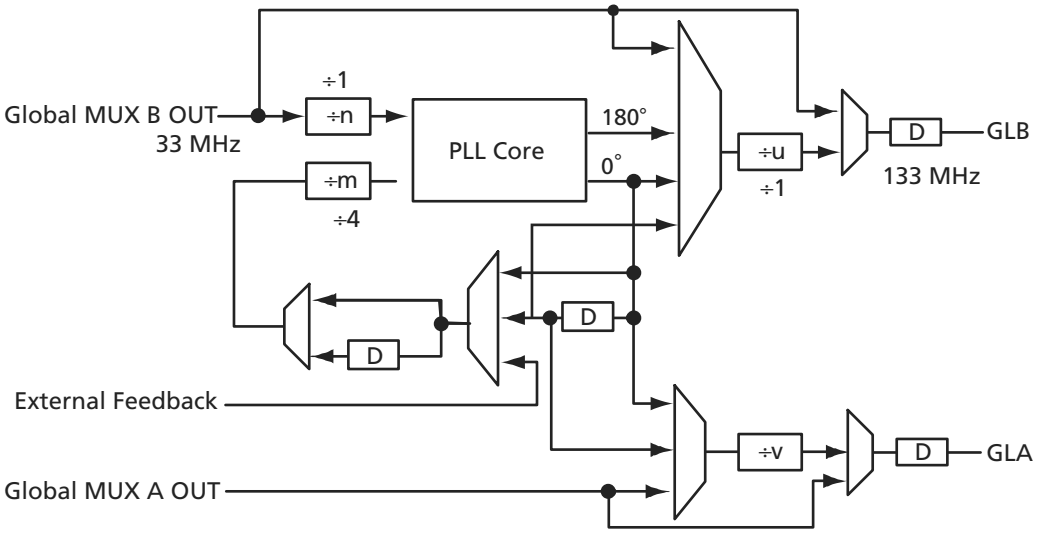


Figure 1-16 • **Using the PLL 33 MHz In, 133 MHz Out**

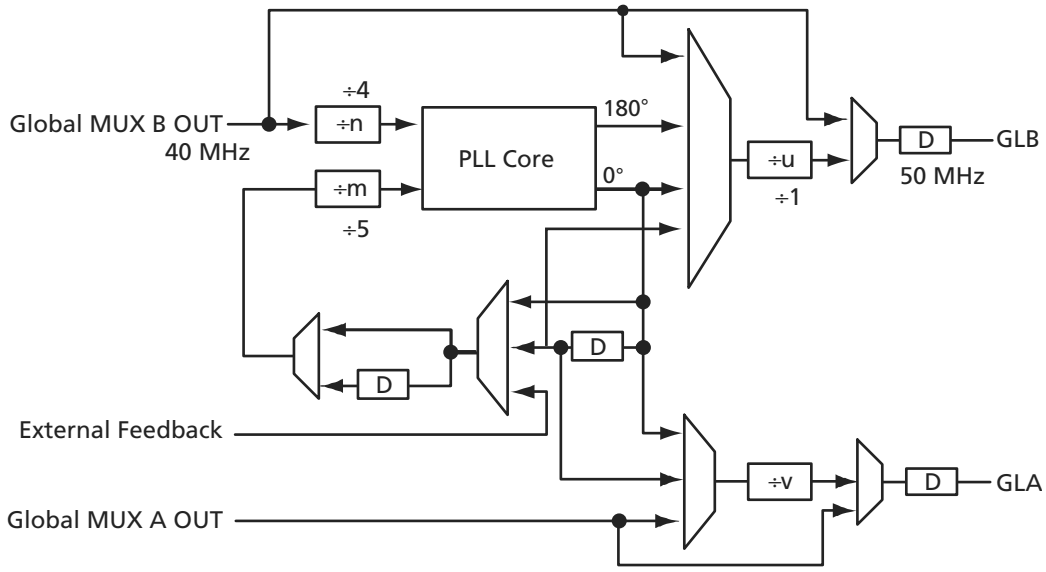


Figure 1-17 • **Using the PLL 40 MHz In, 50 MHz Out**

PLL Electrical Specifications

Parameter	Value $T_J \leq$ –40°C	Value $T_J >$ –40°C	Notes
Frequency Ranges			
Reference Frequency f_{IN} (min.)	2.0 MHz	1.5 MHz	Clock conditioning circuitry (min.) lowest input frequency
Reference Frequency f_{IN} (max.)	180 MHz	180 MHz	Clock conditioning circuitry (max.) highest input frequency
OSC Frequency f_{VCO} (min.)	60	24 MHz	Lowest output frequency voltage controlled oscillator
OSC Frequency f_{VCO} (max.)	180	180 MHz	Highest output frequency voltage controlled oscillator
Clock Conditioning Circuitry f_{OUT} (min.)	$f_{IN} \leq 40$ = 18 MHz $f_{IN} > 40$ = 16 MHz	6 MHz	Lowest output frequency clock conditioning circuitry
Clock Conditioning Circuitry f_{OUT} (max.)	180	180 MHz	Highest output frequency clock conditioning circuitry
Acquisition Time from Cold Start			
Acquisition Time (max.)	80 µs	30 µs	$f_{VCO} \leq 40$ MHz
Acquisition Time (max.)	80 µs	80 µs	$f_{VCO} > 40$ MHz
Long Term Jitter Peak-to-Peak Max.*			
Temperature		**Frequency MHz**	
		f_{VCO}< 10 / **10<f_{VCO}<60** / **f_{VCO} >60**	
25°C (or higher)		±1% / ±2% / ±1%	Jitter(ps) = Jitter(%)*period For example: Jitter in picoseconds at 100 MHz = 0.01 * (1/100E6) = 100 ps
0°C		±1.5% / ±2.5% / ±1%	
–40°C		±2.5% / ±3.5% / ±1%	
–55°C		±2.5% / ±3.5% / ±1%	
Power Consumption			
Analog Supply Power (max.*)		6.9 mW per PLL	
Digital Supply Current (max.)		7 µW/MHz	
Duty Cycle		50% ±0.5%	
Input Jitter Tolerance		5% input period (max. 5 ns)	Maximum jitter allowable on an input clock to acquire and maintain lock.

Note: **High clock frequencies (>60 MHz) under typical setup conditions*

Table 1-12 • **ProASIC^PLUS Memory Configurations by Device**

Device	Bottom	Top	Maximum Width		Maximum Depth	
			D	W	D	W
APA750	32	32	256	288	4,096	9
APA1000	44	44	256	396	5,632	9

Table 1-13 • **Basic Memory Configurations**

Type	Write Access	Read Access	Parity	Library Cell Name
RAM	Asynchronous	Asynchronous	Checked	RAM256x9AA
RAM	Asynchronous	Asynchronous	Generated	RAM256x9AAP
RAM	Asynchronous	Synchronous Transparent	Checked	RAM256x9AST
RAM	Asynchronous	Synchronous Transparent	Generated	RAM256x9ASTP
RAM	Asynchronous	Synchronous Pipelined	Checked	RAM256x9ASR
RAM	Asynchronous	Synchronous Pipelined	Generated	RAM256x9ASRP
RAM	Synchronous	Asynchronous	Checked	RAM256x9SA
RAM	Synchronous	Asynchronous	Generated	RAM256xSAP
RAM	Synchronous	Synchronous Transparent	Checked	RAM256x9SST
RAM	Synchronous	Synchronous Transparent	Generated	RAM256x9SSTP
RAM	Synchronous	Synchronous Pipelined	Checked	RAM256x9SSR
RAM	Synchronous	Synchronous Pipelined	Generated	RAM256x9SSRP
FIFO	Asynchronous	Asynchronous	Checked	FIFO256x9AA
FIFO	Asynchronous	Asynchronous	Generated	FIFO256x9AAP
FIFO	Asynchronous	Synchronous Transparent	Checked	FIFO256x9AST
FIFO	Asynchronous	Synchronous Transparent	Generated	FIFO256x9ASTP
FIFO	Asynchronous	Synchronous Pipelined	Checked	FIFO256x9ASR
FIFO	Asynchronous	Synchronous Pipelined	Generated	FIFO256x9ASRP
FIFO	Synchronous	Asynchronous	Checked	FIFO256x9SA
FIFO	Synchronous	Asynchronous	Generated	FIFO256x9SAP
FIFO	Synchronous	Synchronous Transparent	Checked	FIFO256x9SST
FIFO	Synchronous	Synchronous Transparent	Generated	FIFO256x9SSTP
FIFO	Synchronous	Synchronous Pipelined	Checked	FIFO256x9SSR
FIFO	Synchronous	Synchronous Pipelined	Generated	FIFO256x9SSRP

Package Thermal Characteristics

The ProASIC^PLUS family is available in several package types with a range of pin counts. Actel has selected packages based on high pin count, reliability factors, and superior thermal characteristics.

Thermal resistance defines the ability of a package to conduct heat away from the silicon, through the package to the surrounding air. Junction-to-ambient thermal resistance is measured in degrees Celsius/Watt and is represented as Theta ja (Θ_{ja}). The lower the thermal resistance, the more efficiently a package will dissipate heat.

A package's maximum allowed power (P) is a function of maximum junction temperature (T_J), maximum ambient operating temperature (T_A), and junction-to-ambient thermal resistance Θ_{ja}. Maximum junction temperature is the maximum allowable temperature on the active surface of the IC and is 110° C. P is defined as:

$$P = \frac{T_J - T_A}{\Theta_{ja}}$$

EQ 1-4

Θ_{ja} is a function of the rate (in linear feet per minute (lfpm)) of airflow in contact with the package. When the estimated power consumption exceeds the maximum allowed power, other means of cooling, such as increasing the airflow rate, must be used. The maximum power dissipation allowed for a Military temperature device is specified as a function of Θ_{jc}. The absolute maximum junction temperature is 150°C.

The calculation of the absolute maximum power dissipation allowed for a Military temperature application is illustrated in the following example for a 456-pin PBGA package:

$$\text{Maximum Power Allowed} = \frac{\text{Max. junction temp. (°C)} - \text{Max. case temp. (°C)}}{\theta_{jc}(\text{°C/W})} = \frac{150\text{°C} - 125\text{°C}}{3.0\text{°C/W}} = 8.333\text{W}$$

EQ 1-5

Table 1-16 • **Package Thermal Characteristics**

Plastic Packages	Pin Count	θ_{jc}	θ_{ja} Still Air	θ_{ja} 1.0 m/s 200 ft./min.	θ_{ja} 2.5 m/s 500 ft./min.	Units
Thin Quad Flat Pack (TQFP)	100	14.0	33.5	27.4	25.0	°C/W
Thin Quad Flat Pack (TQFP)	144	11.0	33.5	28.0	25.7	°C/W
Plastic Quad Flat Pack (PQFP)[1]	208	8.0	26.1	22.5	20.8	°C/W
PQFP with Heat spreader[2]	208	3.8	16.2	13.3	11.9	°C/W
Plastic Ball Grid Array (PBGA)	456	3.0	15.6	12.5	11.6	°C/W
Fine Pitch Ball Grid Array (FBGA)	144	3.8	26.9	22.9	21.5	°C/W
Fine Pitch Ball Grid Array (FBGA)	256	3.8	26.6	22.8	21.5	°C/W
Fine Pitch Ball Grid Array (FBGA)[3]	484	3.2	18.0	14.7	13.6	°C/W
Fine Pitch Ball Grid Array (FBGA)[4]	484	3.2	20.5	17.0	15.9	°C/W
Fine Pitch Ball Grid Array (FBGA)	676	3.2	16.4	13.0	12.0	°C/W
Fine Pitch Ball Grid Array (FBGA)	896	2.4	13.6	10.4	9.4	°C/W
Fine Pitch Ball Grid Array (FBGA)	1152	1.8	12.0	8.9	7.9	°C/W
Ceramic Quad Flat Pack (CQFP)	208	2.0	22.0	19.8	18.0	°C/W
Ceramic Quad Flat Pack (CQFP)	352	2.0	17.9	16.1	14.7	°C/W
Ceramic Column Grid Array (CCGA/LGA)	624	6.5	8.9	8.5	8.0	°C/W

Notes:

1. *Valid for the following devices irrespective of temperature grade: APA075, APA150, and APA300*
2. *Valid for the following devices irrespective of temperature grade: APA450, APA600, APA750, and APA1000*
3. *Depopulated Array*
4. *Full array*

Calculating Typical Power Dissipation

ProASIC^PLUS device power is calculated with both a static and an active component. The active component is a function of both the number of tiles utilized and the system speed. Power dissipation can be calculated using the following formula:

Total Power Consumption—P_{total}

$P_{total} = P_{dc} + P_{ac}$

where:

P_{dc} = 7 mW for the APA075
8 mW for the APA150
11 mW for the APA300
12 mW for the APA450
12 mW for the APA600
13 mW for the APA750
19 mW for the APA1000
P_{dc} includes the static components of $P_{VDDP} + P_{VDD} + P_{AVDD}$

P_{ac} = $P_{clock} + P_{storage} + P_{logic} + P_{outputs} + P_{inputs} + P_{pll} + P_{memory}$

Global Clock Contribution—P_{clock}

P_{clock}, the clock component of power dissipation, is given by the piece-wise model:

for R < 15000 the model is: (P1 + (P2*R) - (P7*R2)) * Fs (lightly-loaded clock trees)

for R > 15000 the model is: (P10 + P11*R) * Fs (heavily-loaded clock trees)

where:

P1 = 100 µW/MHz is the basic power consumption of the clock tree per MHz of the clock

P2 = 1.3 µW/MHz is the incremental power consumption of the clock tree per storage tile – also per MHz of the clock

P7 = 0.00003 µW/MHz is a correction factor for partially-loaded clock trees

P10 = 6850 µW/MHz is the basic power consumption of the clock tree per MHz of the clock

P11 = 0.4 µW/MHz is the incremental power consumption of the clock tree per storage tile – also per MHz of the clock

R = the number of storage tiles clocked by this clock

Fs = the clock frequency

Storage-Tile Contribution—$P_{storage}$

$P_{storage}$, the storage-tile (Register) component of AC power dissipation, is given by

$P_{storage} = P5 * ms * Fs$

where:

P5 = 1.1 µW/MHz is the average power consumption of a storage tile per MHz of its output toggling rate. The maximum output toggling rate is Fs/2.

ms = the number of storage tiles (Register) switching during each Fs cycle

Fs = the clock frequency

Table 1-20 • **Recommended Maximum Operating Conditions Programming and PLL Supplies**

Parameter	Condition	Commercial/Industrial/Military/MIL-STD-883		Units
		Minimum	Maximum	
V_{PP}	During Programming	15.8	16.5	V
	Normal Operation[1]	0	16.5	V
V_{PN}	During Programming	–13.8	–13.2	V
	Normal Operation[2]	–13.8	0.5	V
I_{PP}	During Programming		25	mA
I_{PN}	During Programming		10	mA
AVDD		V_{DD}	V_{DD}	V
AGND		GND	GND	V

Notes:
1. *Please refer to the "VPP Programming Supply Pin" section on page 1-77 for more information.*
2. *Please refer to the "VPN Programming Supply Pin" section on page 1-77 for more information.*

Table 1-21 • **Recommended Operating Conditions**

Parameter	Symbol	Limits		
		Commercial	Industrial	Military/MIL-STD-883
DC Supply Voltage (2.5 V I/Os)	V_{DD} and V_{DDP}	2.5 V ± 0.2 V	2.5 V ± 0.2 V	2.5 V ± 0.2 V
DC Supply Voltage (3.3 V I/Os)	V_{DDP} V_{DD}	3.3 V ± 0.3 V 2.5 V ± 0.2 V	3.3 V ± 0.3 V 2.5 V ± 0.2 V	3.3 V ± 0.3 V 2.5 V ± 0.2 V
Operating Ambient Temperature Range	T_A, T_C	0°C to 70°C	–40°C to 85°C	–55°C (T_A) to 125°C (T_C)
Maximum Operating Junction Temperature	T_J	110°C	110°C	150°C

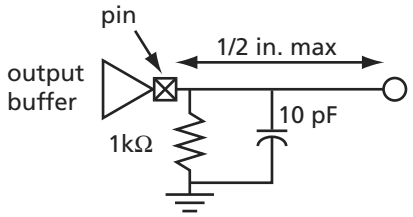
Note: *For I/O long-term reliability, external pull-up resistors cannot be used to increase output voltage above V_{DDP}.*

Table 1-26 • **AC Specifications (3.3 V PCI Revision 2.2 Operation)**

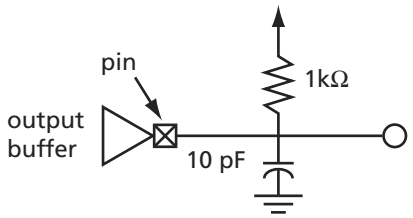
Symbol	Parameter	Condition	Commercial/Industrial/Military/MIL-STD- 883		Units
			Min.	Max.	
$I_{OH(AC)}$	Switching Current High	$0 < V_{OUT} \le 0.3V_{DDP}$*	$-12V_{DDP}$		mA
		$0.3V_{DDP} \le V_{OUT} < 0.9V_{DDP}$*	$(-17.1 + (V_{DDP} - V_{OUT}))$		mA
		$0.7V_{DDP} < V_{OUT} < V_{DDP}$*		See equation C – page 124 of the PCI Specification document rev. 2.2	
	(Test Point)	$V_{OUT} = 0.7V_{DDP}$*		$-32V_{DDP}$	mA
$I_{OL(AC)}$	Switching Current Low	$V_{DDP} > V_{OUT} \ge 0.6V_{DDP}$*	$16V_{DDP}$		mA
		$0.6V_{DDP} > V_{OUT} > 0.1V_{DDP}$ [1]	$(26.7V_{OUT})$		mA
		$0.18V_{DDP} > V_{OUT} > 0$*		See equation D – page 124 of the PCI Specification document rev. 2.2	
	(Test Point)	$V_{OUT} = 0.18V_{DDP}$		$38V_{DDP}$	mA
I_{CL}	Low Clamp Current	$-3 < V_{IN} \le -1$	$-25 + (V_{IN} + 1)/0.015$		mA
I_{CH}	High Clamp Current	$V_{DDP} + 4 > V_{IN} \ge V_{DDP} + 1$	$25 + (V_{IN} - V_{DDP} - 1)/0.015$		mA
$slew_R$	Output Rise Slew Rate	$0.2V_{DDP}$ to $0.6V_{DDP}$ load*	1	4	V/ns
$slew_F$	Output Fall Slew Rate	$0.6V_{DDP}$ to $0.2V_{DDP}$ load*	1	4	V/ns

Note: ** Refer to the PCI Specification document rev. 2.2.*

Pad Loading Applicable to the Rising Edge PCI



Pad Loading Applicable to the Falling Edge PCI



Tristate Buffer Delays

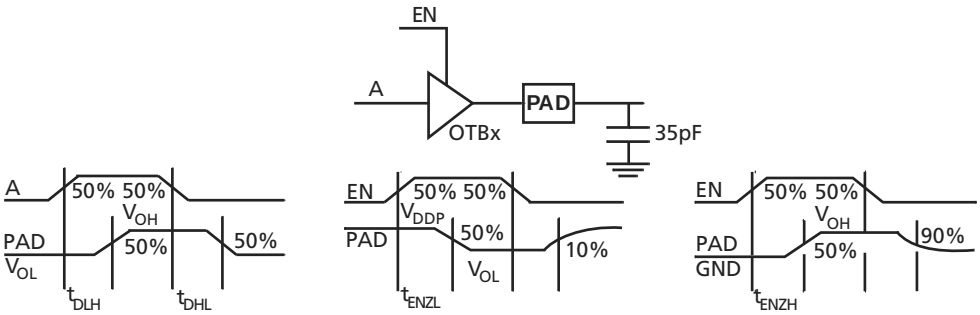


Figure 1-26 • **Tristate Buffer Delays**

Table 1-27 • **Worst-Case Commercial Conditions**
V_{DDP} = 3.0 V, V_{DD} = 2.3 V, 35 pF load, T_J = 70°C

Macro Type	Description	Max t_{DLH}[1]		Max t_{DHL}[2]		Max t_{ENZH}[3]		Max t_{ENZL}[4]		Units
		Std.	–F	Std.	–F	Std.	–F	Std.	–F	
OTB33PH	3.3 V, PCI Output Current, High Slew Rate	2.0	2.4	2.2	2.6	2.2	2.6	2.0	2.4	ns
OTB33PN	3.3 V, High Output Current, Nominal Slew Rate	2.2	2.6	2.9	3.5	2.4	2.9	2.1	2.5	ns
OTB33PL	3.3 V, High Output Current, Low Slew Rate	2.5	3.0	3.2	3.9	2.7	3.3	2.8	3.4	ns
OTB33LH	3.3 V, Low Output Current, High Slew Rate	2.6	3.1	4.0	4.8	2.8	3.4	3.0	3.6	ns
OTB33LN	3.3 V, Low Output Current, Nominal Slew Rate	2.9	3.5	4.3	5.2	3.2	3.8	4.1	4.9	ns
OTB33LL	3.3 V, Low Output Current, Low Slew Rate	3.0	3.6	5.6	6.7	3.3	3.9	5.5	6.6	ns

Notes:

1. *t_{DLH}=Data-to-Pad High*
2. *t_{DHL}=Data-to-Pad Low*
3. *t_{ENZH}=Enable-to-Pad, Z to High*
4. *t_{ENZL} = Enable-to-Pad, Z to Low*
5. *All –F parts are only available as commercial.*

Table 1-28 • **Worst-Case Commercial Conditions**
V_{DDP} = 2.3 V, V_{DD} = 2.3 V, 35 pF load, T_J = 70°C

Macro Type	Description	Max t_{DLH}[1]		Max t_{DHL}[2]		Max t_{ENZH}[3]		Max t_{ENZL}[4]		Units
		Std.	–F	Std.	–F	Std.	–F	Std.	–F	
OTB25LPHH	2.5 V, Low Power, High Output Current, High Slew Rate[5]	2.0	2.4	2.1	2.5	2.3	2.7	2.0	2.4	ns
OTB25LPHN	2.5 V, Low Power, High Output Current, Nominal Slew Rate[5]	2.4	2.9	3.0	3.6	2.7	3.2	2.1	2.5	ns
OTB25LPHL	2.5 V, Low Power, High Output Current, Low Slew Rate[5]	2.9	3.5	3.2	3.8	3.1	3.8	2.7	3.2	ns
OTB25LPLH	2.5 V, Low Power, Low Output Current, High Slew Rate[5]	2.7	3.3	4.6	5.5	3.0	3.6	2.6	3.1	ns

Notes:

1. *t_{DLH}=Data-to-Pad High*
2. *t_{DHL}=Data-to-Pad Low*
3. *t_{ENZH}=Enable-to-Pad, Z to High*
4. *t_{ENZL} = Enable-to-Pad, Z to Low*
5. *Low power I/O work with V_{DDP}=2.5 V ±10% only. V_{DDP}=2.3 V for delays.*
6. *All –F parts are only available as commercial.*

Table 1-28 • **Worst-Case Commercial Conditions**
V_{DDP} = 2.3 V, V_{DD} = 2.3 V, 35 pF load, T_J = 70°C

Macro Type	Description	Max t_{DLH}[1]		Max t_{DHL}[2]		Max t_{ENZH}[3]		Max t_{ENZL}[4]		Units
		Std.	–F	Std.	–F	Std.	–F	Std.	–F	
OTB25LPLN	2.5 V, Low Power, Low Output Current, Nominal Slew Rate[5]	3.5	4.2	4.2	5.1	3.8	4.5	3.8	4.6	ns
OTB25LPLL	2.5 V, Low Power, Low Output Current, Low Slew Rate[5]	4.0	4.8	5.3	6.4	4.2	5.1	5.1	6.1	ns

Notes:

1. *t_{DLH}=Data-to-Pad High*
2. *t_{DHL}=Data-to-Pad Low*
3. *t_{ENZH}=Enable-to-Pad, Z to High*
4. *t_{ENZL} = Enable-to-Pad, Z to Low*
5. *Low power I/O work with V_{DDP}=2.5 V ±10% only. V_{DDP}=2.3 V for delays.*
6. *All –F parts are only available as commercial.*

Table 1-29 • **Worst-Case Military Conditions**
V_{DDP} = 3.0 V, V_{DD} = 2.3 V, 35 pF load, T_J = 125°C for Military/MIL-STD-883

Macro Type	Description	Max t_{DLH}[1]	Max t_{DHL}[2]	Max t_{ENZH}[3]	Max t_{ENZL}[4]	Units
		Std.	Std.	Std.	Std.	
OTB33PH	3.3 V, PCI Output Current, High Slew Rate	2.2	2.4	2.3	2.1	ns
OTB33PN	3.3 V, High Output Current, Nominal Slew Rate	2.4	3.2	2.7	2.3	ns
OTB33PL	3.3 V, High Output Current, Low Slew Rate	2.7	3.5	2.9	3.0	ns
OTB33LH	3.3 V, Low Output Current, High Slew Rate	2.7	4.3	3.0	3.1	ns
OTB33LN	3.3 V, Low Output Current, Nominal Slew Rate	3.3	4.7	3.4	4.4	ns
OTB33LL	3.3 V, Low Output Current, Low Slew Rate	3.2	6.0	3.5	5.9	ns

Notes:

1. *t_{DLH}=Data-to-Pad High*
2. *t_{DHL}=Data-to-Pad Low*
3. *t_{ENZH}=Enable-to-Pad, Z to High*
4. *t_{ENZL} = Enable-to-Pad, Z to Low*

Table 1-30 • **Worst-Case Military Conditions**
V_{DDP} = 2.3 V, V_{DD} = 2.3 V, 35 pF load, T_J = 125°C for Military/MIL-STD-883

Macro Type	Description	Max t_{DLH}[1]	Max t_{DHL}[2]	Max t_{ENZH}[3]	Max t_{ENZL}[4]	Units
		Std.	Std.	Std.	Std.	
OTB25LPHH	2.5 V, Low Power, High Output Current, High Slew Rate[5]	2.3	2.3	2.4	2.1	ns
OTB25LPHN	2.5 V, Low Power, High Output Current, Nominal Slew Rate[5]	2.7	3.2	2.8	2.1	ns
OTB25LPHL	2.5 V, Low Power, High Output Current, Low Slew Rate[5]	3.2	3.5	3.3	2.8	ns
OTB25LPLH	2.5 V, Low Power, Low Output Current, High Slew Rate[5]	3.0	5.0	3.2	2.8	ns
OTB25LPLN	2.5 V, Low Power, Low Output Current, Nominal Slew Rate[5]	3.7	4.5	4.1	4.1	ns
OTB25LPLL	2.5 V, Low Power, Low Output Current, Low Slew Rate[5]	4.4	5.8	4.4	5.4	ns

Notes:

1. *t_{DLH}=Data-to-Pad High*
2. *t_{DHL}=Data-to-Pad Low*
3. *t_{ENZH}=Enable-to-Pad, Z to High*
4. *t_{ENZL} = Enable-to-Pad, Z to Low*
5. *Low power I/O work with V_{DDP}=2.5V ±10% only. V_{DDP}=2.3V for delays.*

Predicted Global Routing Delay

Table 1-43 • **Worst-Case Commercial Conditions[1]**
V_{DDP} = 3.0 V, V_{DD} = 2.3 V, T_J = 70°C

Parameter	Description	Max.		Units
		Std.	–F[2]	
t_{RCKH}	Input Low to High[3]	1.1	1.3	ns
t_{RCKL}	Input High to Low[3]	1.0	1.2	ns
t_{RCKH}	Input Low to High[4]	0.8	1.0	ns
t_{RCKL}	Input High to Low[4]	0.8	1.0	ns

Notes:

1. *The timing delay difference between tile locations is less than 15ps.*
2. *All –F parts are only available as commercial.*
3. *Highly loaded row 50%.*
4. *Minimally loaded row.*

Table 1-44 • **Worst-Case Military Conditions**
V_{DDP} = 3.0V, V_{DD} = 2.3V, T_J = 125°C for Military/MIL-STD-883

Parameter	Description	Max.	Units
t_{RCKH}	Input Low to High (high loaded row of 50%)	1.1	ns
t_{RCKL}	Input High to Low (high loaded row of 50%)	1.0	ns
t_{RCKH}	Input Low to High (minimally loaded row)	0.8	ns
t_{RCKL}	Input High to Low (minimally loaded row)	0.8	ns

Note: ** The timing delay difference between tile locations is less than 15 ps.*

Global Routing Skew

Table 1-45 • **Worst-Case Commercial Conditions**
V_{DDP} = 3.0 V, V_{DD} = 2.3 V, T_J = 70°C

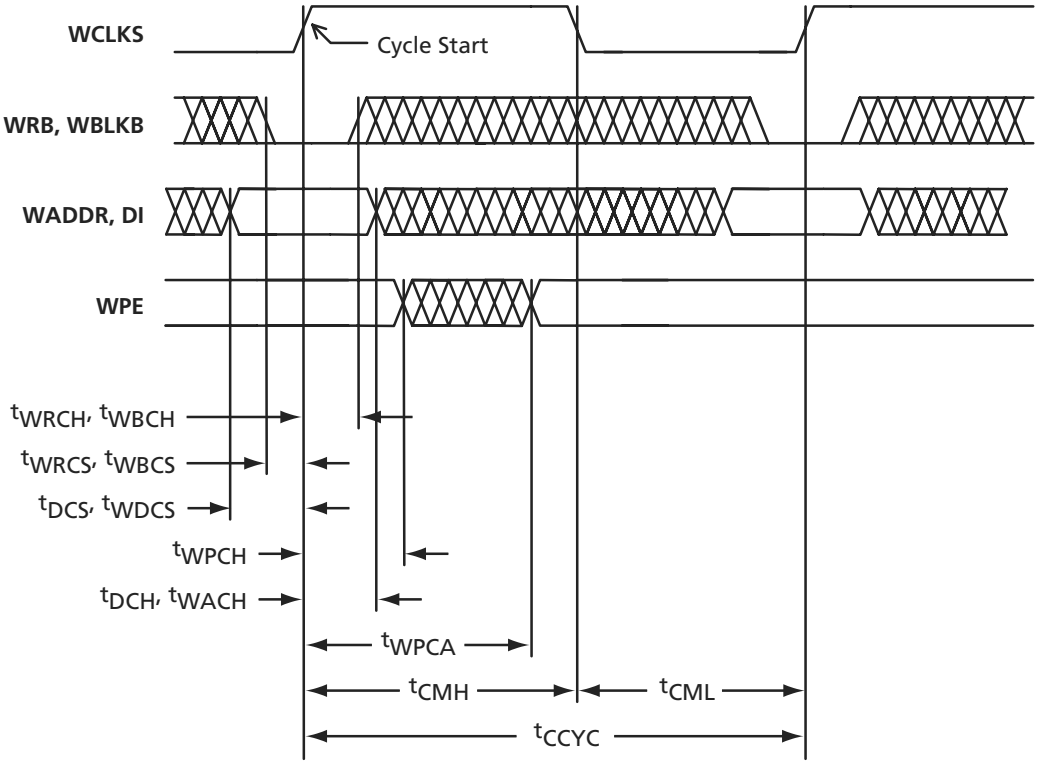
Parameter	Description	Max.		Units
		Std.	–F*	
t_{RCKSWH}	Maximum Skew Low to High	270	320	ps
t_{RCKSHH}	Maximum Skew High to Low	270	320	ps

Note: **All –F parts are only available as commercial.*

Table 1-46 • **Worst-Case Commercial Conditions**
V_{DDP} = 3.0V, V_{DD} = 2.3V, T_J = 125°C for Military/MIL-STD-883

Parameter	Description	Max.	Units
t_{RCKSWH}	Maximum Skew Low to High	270	ps
t_{RCKSHH}	Maximum Skew High to Low	270	ps

Synchronous SRAM Write



Note: *The plot shows the normal operation status.*

Figure 1-36 • **Synchronous SRAM Write**

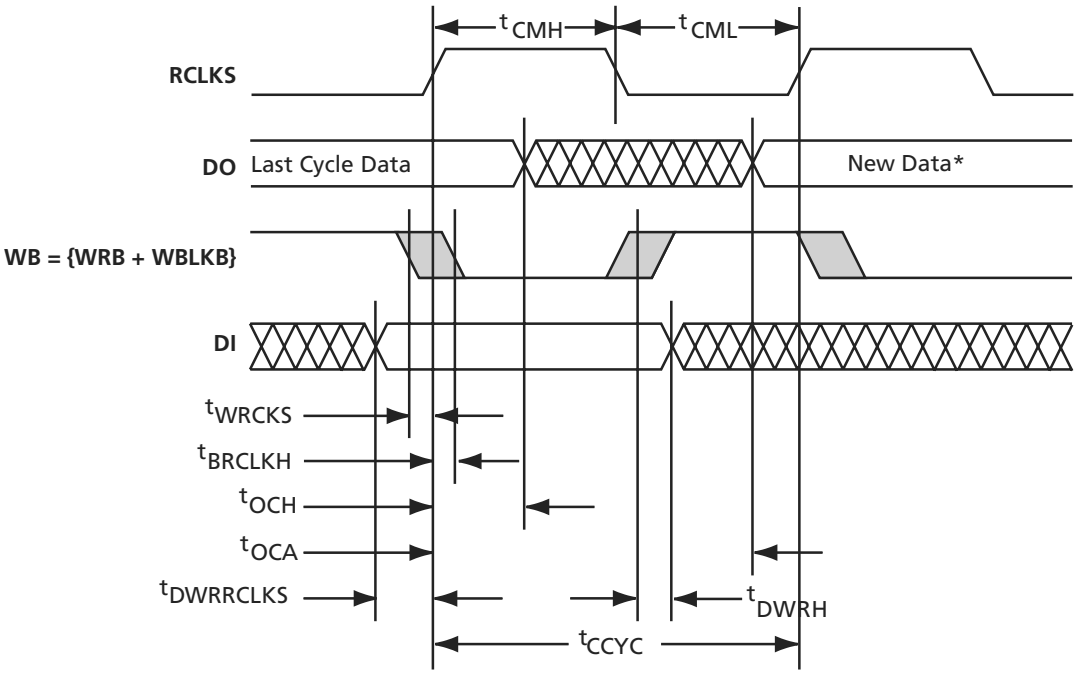
Table 1-57 • **T_J = 0°C to 110°C; V_{DD} = 2.3 V to 2.7 V for Commercial/industrial**
T_J = –55°C to 150°C, V_{DD} = 2.3 V to 2.7 V for Military/MIL-STD-883

Symbol t_{xxx}	Description	Min.	Max.	Units	Notes
CCYC	Cycle time	7.5		ns	
CMH	Clock high phase	3.0		ns	
CML	Clock low phase	3.0		ns	
DCH	DI hold from WCLKS ↑	0.5		ns	
DCS	DI setup to WCLKS ↑	1.0		ns	
WACH	WADDR hold from WCLKS ↑	0.5		ns	
WDCS	WADDR setup to WCLKS ↑	1.0		ns	
WPCA	New WPE access from WCLKS ↑	3.0		ns	WPE is invalid while PARGEN is active
WPCH	Old WPE valid from WCLKS ↑		0.5	ns	
WRCH, WBCH	WRB & WBLKB hold from WCLKS ↑	0.5		ns	
WRCS, WBCS	WRB & WBLKB setup to WCLKS ↑	1.0		ns	

Notes:

1. *On simultaneous read and write accesses to the same location, DI is output to DO.*
2. *All –F speed grade devices are 20% slower than the standard numbers.*

Asynchronous Write and Synchronous Read to the Same Location



* New data is read if WB ↓ occurs before setup time.
The stored data is read if WB ↓ occurs after hold time.

Note: *The plot shows the normal operation status.*

Figure 1-38 • **Asynchronous Write and Synchronous Read to the Same Location**

Table 1-59 • **T_J = 0°C to 110°C; V_{DD} = 2.3 V to 2.7 V for Commercial/industrial**
T_J = –55°C to 150°C, V_{DD} = 2.3 V to 2.7 V for Military/MIL-STD-883

Symbol t_{xxx}	Description	Min.	Max.	Units	Notes
CCYC	Cycle time	7.5		ns	
CMH	Clock high phase	3.0		ns	
CML	Clock low phase	3.0		ns	
WBRCLKS	WB ↓ to RCLKS ↑ setup time	–0.1		ns	
WBRCLKH	WB ↓ to RCLKS ↑ hold time		7.0	ns	
OCH	Old DO valid from RCLKS ↑		3.0	ns	OCA/OCH displayed for Access Timed Output
OCA	New DO valid from RCLKS ↑	7.5		ns	
DWRRCLKS	DI to RCLKS ↑ setup time	0		ns	
DWRH	DI to WB ↑ hold time		1.5	ns	

Notes:

1. *This behavior is valid for Access Timed Output and Pipelined Mode Output. The table shows the timings of an Access Timed Output.*
2. *In asynchronous write and synchronous read access to the same location, the new write data will be read out if the active write signal edge occurs before or at the same time as the active read clock edge. If WB changes to low after hold time, the data will be read.*
3. *A setup or hold time violation will result in unknown output data.*
4. *All –F speed grade devices are 20% slower than the standard numbers.*

Asynchronous FIFO Full and Empty Transitions

The asynchronous FIFO accepts writes and reads while not full or not empty. When the FIFO is full, all writes are inhibited. Conversely, when the FIFO is empty, all reads are inhibited. A problem is created if the FIFO is written to during the transition from full to not full, or read during the transition from empty to not empty. The exact time at which the write or read operation changes from inhibited to accepted after the read (write) signal which causes the transition from full or empty to not full or not empty is indeterminate. For slow cycles, this indeterminate period starts 1 ns after the RB (WB) transition, which deactivates full or not empty and ends 3 ns after the RB (WB) transition. For fast cycles, the indeterminate period ends 3 ns (7.5 ns – RDL (WRL)) after the RB (WB) transition, whichever is later (Table 1-1 on page 1-7).

The timing diagram for write is shown in Figure 1-38 on page 1-65. The timing diagram for read is shown in Figure 1-39 on page 1-66. For basic SRAM configurations, see Table 1-14 on page 1-25. When reset is asserted, the empty flag will be asserted, the counters will reset, the outputs go to zero, but the internal RAM is not erased.

Enclosed Timing Diagrams – FIFO Mode:

The following timing diagrams apply only to single cell; they are not applicable to cascaded cells. For more information, refer to the *ProASIC^PLUS RAM/FIFO Blocks* application note.

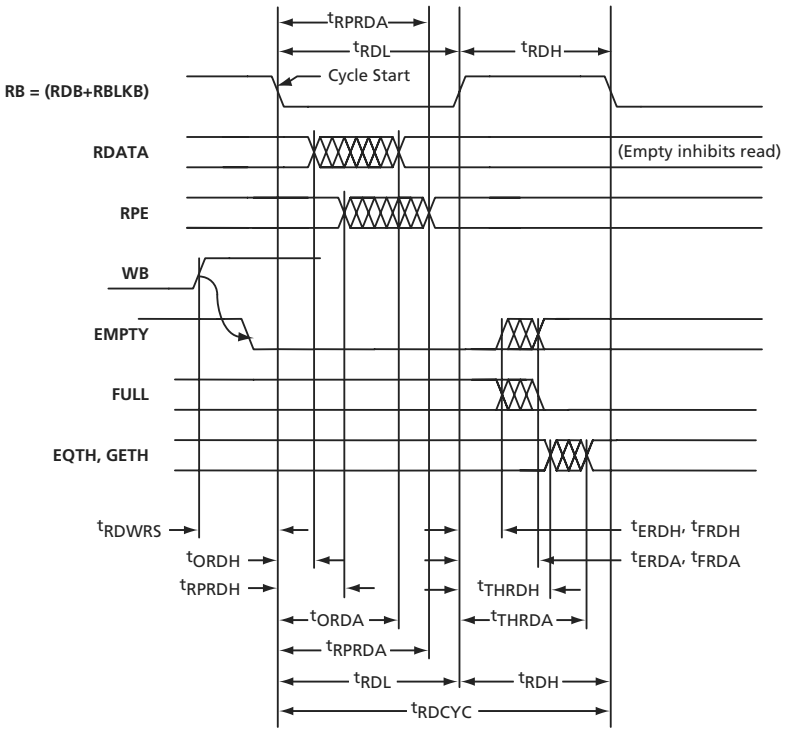
- "Asynchronous FIFO Read" section on page 1-70
- "Asynchronous FIFO Write" section on page 1-71
- "Synchronous FIFO Read, Access Timed Output Strobe (Synchronous Transparent)" section on page 1-72
- "Synchronous FIFO Read, Pipeline Mode Outputs (Synchronous Pipelined)" section on page 1-73
- "Synchronous FIFO Write" section on page 1-74
- "FIFO Reset" section on page 1-75

Table 1-62 • **Memory Block FIFO Interface Signals**

FIFO Signal	Bits	In/Out	Description
WCLKS	1	In	Write clock used for synchronization on write side
RCLKS	1	In	Read clock used for synchronization on read side
LEVEL <0:7>*	8	In	Direct configuration implements static flag logic
RBLKB	1	In	Read block select (active Low)
RDB	1	In	Read pulse (active Low)
RESET	1	In	Reset for FIFO pointers (active Low)
WBLKB	1	In	Write block select (active Low)
DI<0:8>	9	In	Input data bits <0:8>, <8> will be generated if PARGEN is true
WRB	1	In	Write pulse (active Low)
FULL, EMPTY	2	Out	FIFO flags. FULL prevents write and EMPTY prevents read
EQTH, GEQTH*	2	Out	EQTH is true when the FIFO holds the number of words specified by the LEVEL signal. GEQTH is true when the FIFO holds (LEVEL) words or more
DO<0:8>	9	Out	Output data bits <0:8>
RPE	1	Out	Read parity error (active High)
WPE	1	Out	Write parity error (active High)
LGDEP <0:2>	3	In	Configures DEPTH of the FIFO to $2^{(LGDEP+1)}$
PARODD	1	In	Selects Odd parity generation/detect when high, Even when low

Note: **LEVEL is always eight bits (0000.0000, 0000.0001). That means for values of DEPTH greater than 256, not all values will be possible, e.g. for DEPTH=512, the LEVEL can only have the values 2, 4, . . ., 512. The LEVEL signal circuit will generate signals that indicate whether the FIFO is exactly filled to the value of LEVEL (EQTH) or filled equal or higher (GEQTH) than the specified LEVEL. Since counting starts at 0, EQTH will become true when the FIFO holds (LEVEL+1) words for 512-bit FIFOs.*

Asynchronous FIFO Read



Note: *The plot shows the normal operation status.*

Figure 1-43 • **Asynchronous FIFO Read**

Table 1-63 • **T_J = 0°C to 110°C; V_{DD} = 2.3 V to 2.7 V for Commercial/industrial**
T_J = –55°C to 150°C, V_{DD} = 2.3 V to 2.7 V for Military/MIL-STD-883

Symbol t_{xxx}	Description	Min.	Max.	Units	Notes
ERDH, FRDH, THRDH	Old EMPTY, FULL, EQTH, & GETH valid hold time from RB ↑		0.5	ns	Empty/full/thresh are invalid from the end of hold until the new access is complete
ERDA	New EMPTY access from RB ↑	3.0[1]		ns	
FRDA	FULL↓ access from RB ↑	3.0[1]		ns	
ORDA	New DO access from RB ↓	7.5		ns	
ORDH	Old DO valid from RB ↓		3.0	ns	
RDCYC	Read cycle time	7.5		ns	
RDWRS	WB ↑, clearing EMPTY, setup to RB ↓	3.0[2]		ns	Enabling the read operation
			1.0	ns	Inhibiting the read operation
RDH	RB high phase	3.0		ns	Inactive
RDL	RB low phase	3.0		ns	Active
RPRDA	New RPE access from RB ↓	9.5		ns	
RPRDH	Old RPE valid from RB ↓		4.0	ns	
THRDA	EQTH or GETH access from RB↑	4.5		ns	

Notes:

1. *At fast cycles, ERDA and FRDA = MAX (7.5 ns – RDL), 3.0 ns.*
2. *At fast cycles, RDWRS (for enabling read) = MAX (7.5 ns – WRL), 3.0 ns.*
3. *All –F speed grade devices are 20% slower than the standard numbers.*