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Understanding <u>Embedded - FPGAs (Field</u> <u>Programmable Gate Array)</u>

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	129024
Number of I/O	356
Number of Gates	600000
Voltage - Supply	2.3V ~ 2.7V
Mounting Type	Surface Mount
Operating Temperature	-55°C ~ 125°C (TC)
Package / Case	456-BBGA
Supplier Device Package	456-PBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/apa600-bg456m

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Device Resources

	User I/Os ²												
	Commercial/Industrial										Milita	r y/MIL-S 1	D-883B
Device	TQFP 100-Pin	TQFP 144-Pin	PQFP 208-Pin	PBGA 456-Pin	FBGA 144-Pin	FBGA 256-Pin	FBGA 484-Pin	FBGA 676-Pin	FBGA 896-Pin	FBGA 1152-Pin	CQFP 208-Pin	CQFP 352-Pin	CCGA/ LGA 624-Pin
APA075	66	107	158		100								
APA150	66		158	242	100	186 ³							
APA300			158 ⁴	290 ⁴	100 ⁴	186 ^{3, 4}					158	248	
APA450			158	344	100	186 ³	344 ³						
APA600			158 ⁴	356 ⁴		186 ^{3, 4}	370 ³	454			158	248	440
APA750			158	356				454	562 ⁵				
APA1000			158 ⁴	356 ⁴					642 ^{4, 5}	712 ⁵	158	248	440

Notes:

1. Package Definitions: TQFP = Thin Quad Flat Pack, PQFP = Plastic Quad Flat Pack, PBGA = Plastic Ball Grid Array, FBGA = Fine Pitch Ball Grid Array, CQFP = Ceramic Quad Flat Pack, CCGA = Ceramic Column Grid Array, LGA = Land Grid Array

2. Each pair of PECL I/Os is counted as one user I/O.

3. FG256 and FG484 are footprint-compatible packages.

4. Military Temperature Plastic Package Offering

5. FG896 and FG1152 are footprint-compatible packages.

General Guideline

Maximum performance numbers in this datasheet are based on characterized data. Actel does not guarantee performance beyond the limits specified within the datasheet.

ProASIC^{PLUS} Architecture

The proprietary ProASIC^{PLUS} architecture provides granularity comparable to gate arrays.

The ProASIC^{PLUS} device core consists of a Sea-of-Tiles (Figure 1-1). Each tile can be configured as a three-input logic function (e.g., NAND gate, D-Flip-Flop, etc.) by programming the appropriate Flash switch interconnections (Figure 1-2 and Figure 1-3 on page 1-3). Tiles and larger functions are connected with any of the four levels of routing hierarchy. Flash switches are distributed throughout the device to provide nonvolatile, reconfigurable interconnect programming. Flash switches are programmed to connect signal lines to

the appropriate logic cell inputs and outputs. Dedicated high-performance lines are connected as needed for fast, low-skew global signal distribution throughout the core. Maximum core utilization is possible for virtually any design.

ProASIC^{PLUS} devices also contain embedded, two-port SRAM blocks with built-in FIFO/RAM control logic. Programming options include synchronous or asynchronous operation, two-port RAM configurations, user defined depth and width, and parity generation or checking. Please see the "Embedded Memory Configurations" section on page 1-23 for more information.



Figure 1-1 • The ProASIC^{PLUS} Device Architecture



Figure 1-2 • Flash Switch



Figure 1-3 • Core Logic Tile

Live at Power-Up

The Actel Flash-based ProASICPLUS devices support Level 0 of the live at power-up (LAPU) classification standard. This feature helps in system component initialization, executing critical tasks before the processor wakes up, setting up and configuring memory blocks, clock generation, and bus activity management. The LAPU feature of Flash-based ProASICPLUS devices greatly simplifies total system design and reduces total system cost, often eliminating the need for Complex Programmable Logic Device (CPLD) and clock generation PLLs that are used for this purpose in a system. In addition, glitches and brownouts in system power will not corrupt the ProASICPLUS device's Flash configuration, and unlike SRAM-based FPGAs, the device will not have to be reloaded when system power is restored. This enables the reduction or complete removal of the configuration PROM, expensive voltage monitor, brownout detection, and clock generator devices from the PCB design. Flash-based ProASICPLUS devices simplify total system design, and reduce cost and design risk. while increasing system reliability and improving system initialization time.

Flash Switch

Unlike SRAM FPGAs, ProASIC^{PLUS} uses a live-on-power-up ISP Flash switch as its programming element.

In the ProASIC^{PLUS} Flash switch, two transistors share the floating gate, which stores the programming information. One is the sensing transistor, which is only used for writing and verification of the floating gate voltage. The other is the switching transistor. It can be used in the architecture to connect/separate routing nets or to configure logic. It is also used to erase the floating gate (Figure 1-2 on page 1-2).

Logic Tile

The logic tile cell (Figure 1-3) has three inputs (any or all of which can be inverted) and one output (which can connect to both ultra-fast local and efficient long-line routing resources). Any three-input, one-output logic function (except a three-input XOR) can be configured as one tile. The tile can be configured as a latch with clear or set or as a flip-flop with clear or set. Thus, the tiles can flexibly map logic and sequential gates of a design.

Routing Resources

The routing structure of ProASIC^{PLUS} devices is designed to provide high performance through a flexible fourlevel hierarchy of routing resources: ultra-fast local resources, efficient long-line resources, high-speed, very long-line resources, and high performance global networks.

The ultra-fast local resources are dedicated lines that allow the output of each tile to connect directly to every input of the eight surrounding tiles (Figure 1-4).

The efficient long-line resources provide routing for longer distances and higher fanout connections. These resources vary in length (spanning 1, 2, or 4 tiles), run both vertically and horizontally, and cover the entire ProASIC^{PLUS} device (Figure 1-5 on page 1-5). Each tile can drive signals onto the efficient long-line resources, which

can in turn access every input of every tile. Active buffers are inserted automatically by routing software to limit the loading effects due to distance and fanout.

The high-speed, very long-line resources, which span the entire device with minimal delay, are used to route very long or very high fanout nets. (Figure 1-6 on page 1-6).

The high-performance global networks are low-skew, high fanout nets that are accessible from external pins or from internal logic (Figure 1-7 on page 1-7). These nets are typically used to distribute clocks, resets, and other high fanout nets requiring a minimum skew. The global networks are implemented as clock trees, and signals can be introduced at any junction. These can be employed hierarchically with signals accessing every input on all tiles.



Figure 1-4 • Ultra-Fast Local Resources

Array Coordinates

During many place-and-route operations in Actel's Designer software tool, it is possible to set constraints that require array coordinates.

Table 1-2 is provided as a reference. The array coordinates are measured from the lower left (0,0). They can be used in region constraints for specific groups of core cells, I/Os, and RAM blocks. Wild cards are also allowed.

I/O and cell coordinates are used for placement constraints. Two coordinate systems are needed because there is not a one-to-one correspondence between I/O cells and core cells. In addition, the I/O coordinate system changes depending on the die/package combination.

Core cell coordinates start at the lower left corner (represented as (1,1)) or at (1,5) if memory blocks are present at the bottom. Memory coordinates use the same system and are indicated in Table 1-2. The memory coordinates for an APA1000 are illustrated in Figure 1-8. For more information on how to use constraints, see the *Designer User's Guide* or online help for ProASIC^{PLUS} software tools.

Table 1-2 •	Array Coordinates
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		Lo	gic Tile		Me	emory Rows		
	Min. Max.		Bottom Top		All			
Device	х	У	x	У	У	У	Min.	Max.
APA075	1	1	96	32	-	(33,33) or (33, 35)	0,0	97, 37
APA150	1	1	128	48	-	(49,49) or (49, 51)	0,0	129, 53
APA300	1	5	128	68	(1,1) or (1,3)	(69,69) or (69, 71)	0,0	129, 73
APA450	1	5	192	68	(1,1) or (1,3)	(69,69) or (69, 71)	0,0	193, 73
APA600	1	5	224	100	(1,1) or (1,3)	(101,101) or (101, 103)	0,0	225, 105
APA750	1	5	256	132	(1,1) or (1,3)	(133,133) or (133, 135)	0,0	257, 137
APA1000	1	5	352	164	(1,1) or (1,3)	(165,165) or (165, 167)	0,0	353, 169



Figure 1-8 • Core Cell Coordinates for the APA1000

Boundary Scan (JTAG)

ProASIC^{PLUS} devices are compatible with IEEE Standard 1149.1, which defines a set of hardware architecture and mechanisms for cost-effective, board-level testing. The basic ProASIC^{PLUS} boundary-scan logic circuit is composed of the TAP (test access port), TAP controller, test data registers, and instruction register (Figure 1-12). This circuit supports all mandatory IEEE 1149.1 instructions (EXTEST, SAMPLE/PRELOAD and BYPASS) and the optional IDCODE instruction (Table 1-6).

Each test section is accessed through the TAP, which has five associated pins: TCK (test clock input), TDI and TDO (test data input and output), TMS (test mode selector) and TRST (test reset input). TMS, TDI and TRST are equipped with pull-up resistors to ensure proper operation when no input data is supplied to them. These pins are dedicated for boundary-scan test usage. Actel recommends that a nominal 20 k Ω pull-up resistor is added to TDO and TCK pins.

The TAP controller is a four-bit state machine (16 states) that operates as shown in Figure 1-13 on page 1-12. The '1's and '0's represent the values that must be present at TMS at a rising edge of TCK for the given state transition to occur. IR and DR indicate that the instruction register or the data register is operating in that state.

ProASIC^{PLUS} devices have to be programmed at least once for complete boundary-scan functionality to be available. Prior to being programmed, EXTEST is not available. If boundary-scan functionality is required prior to programming, refer to online technical support on the Actel website and search for ProASIC^{PLUS} BSDL.



Figure 1-12 •	ProASIC ^{PLUS} J	JTAG Boundary	Scan Test	Logic Circuit

Table 1-6Boundary-Scan Opcodes

	Hex Opcode
EXTEST	00
SAMPLE/PRELOAD	01
IDCODE	OF

Table 1-6 •	Boundary-Scan	Opcodes
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	Hex Opcode
CLAMP	05
BYPASS	FF

B [®]User Security

ProASICPLUS devices have FlashLock protection bits that, FlashLockonce programmed, block the entire programmed contents from being read externally. Please refer to Table 1-11 for details on the number of bits in the key for each device. If locked, the user can only reprogram the device employing the user-defined security key. This protects the device from being read back and duplicated. Since programmed data is stored in nonvolatile memory cells (actually very small capacitors) rather than in the wiring, physical deconstruction cannot be used to compromise data. This type of security breach is further discouraged by the placement of the memory cells beneath the four metal layers (whose removal cannot be accomplished without disturbing the charge in the capacitor). This is the highest security provided in the industry. For more information, refer to Actel's Design Security in Nonvolatile Flash and Antifuse FPGAs white paper.

Device	Key Size
APA075	79 bits
APA150	79 bits
APA300	79 bits
APA450	119 bits
APA600	167 bits
APA750	191 bits
APA1000	263 bits

Table 1-11 • Flashlock Key Size by Device

Embedded Memory Floorplan

The embedded memory is located across the top and bottom of the device in 256x9 blocks (Figure 1-1 on page 1-2). Depending on the device, up to 88 blocks are available to support a variety of memory configurations. Each block can be programmed as an independent memory array or combined (using dedicated memory routing resources) to form larger, more complex memory configurations. A single memory configuration could include blocks from both the top and bottom memory locations.

Table 1-12 • ProASIC^{PLUS} Memory Configurations by Device

Embedded Memory Configurations

The embedded memory in the ProASIC^{PLUS} family provides great configuration flexibility (Table 1-12). Each ProASIC^{PLUS} block is designed and optimized as a two-port memory (one read, one write). This provides 198 kbits of two-port and/or single port memory in the APA1000 device.

Each memory block can be configured as FIFO or SRAM, with independent selection of synchronous or asynchronous read and write ports (Table 1-13). Additional characteristics include programmable flags as well as parity checking and generation. Figure 1-21 on page 1-25 and Figure 1-22 on page 1-26 show the block diagrams of the basic SRAM and FIFO blocks. Table 1-14 on page 1-25 and Table 1-15 on page 1-26 describe memory block SRAM and FIFO interface signals, respectively. A single memory block is designed to operate at up to 150 MHz (standard speed grade typical conditions). Each block is comprised of 256 9-bit words (one read port, one write port). The memory blocks may be cascaded in width and/or depth to create the desired memory organization. (Figure 1-23 on page 1-27). This provides optimal bit widths of 9 (one block), 18, 36, and 72, and optimal depths of 256, 512, 768, and 1,024. Refer to Actel's SmartGen User's Guide for more information.

Figure 1-24 on page 1-27 gives an example of optimal memory usage. Ten blocks with 23,040 bits have been used to generate three arrays of various widths and depths. Figure 1-25 on page 1-27 shows how RAM blocks can be used in parallel to create extra read ports. In this example, using only 10 of the 88 available blocks of the APA1000 yields an effective 6,912 bits of multiple port RAM. The Actel SmartGen software facilitates building wider and deeper memory configurations for optimal memory usage.

			Maximum Width		Maximu	m Depth
Device	Bottom	Тор	D	W	D	W
APA075	0	12	256	108	1,536	9
APA150	0	16	256	144	2,048	9
APA300	16	16	256	144	2,048	9
APA450	24	24	256	216	3,072	9
APA600	28	28	256	252	3,584	9



Note: Each RAM block contains a multiplexer (called DMUX) for each output signal, increasing design efficiency. These DMUX cells do not consume any core logic tiles and connect directly to high-speed routing resources between the RAM blocks. They are used when RAM blocks are cascaded and are automatically inserted by the software tools.

Figure 1-22 • Basic FIFO Block Diagrams

FIFO Signal	Bits	In/Out	Description
WCLKS	1	In	Write clock used for synchronization on write side
RCLKS	1	In	Read clock used for synchronization on read side
LEVEL <0:7>	8	In	Direct configuration implements static flag logic
RBLKB	1	In	Read block select (active Low)
RDB	1	In	Read pulse (active Low)
RESET	1	In	Reset for FIFO pointers (active Low)
WBLKB	1	In	Write block select (active Low)
DI<0:8>	9	In	Input data bits <0:8>, <8> will be generated parity if PARGEN is true
WRB	1	In	Write pulse (active Low)
FULL, EMPTY	2	Out	FIFO flags. FULL prevents write and EMPTY prevents read
EQTH, GEQTH	2	Out	EQTH is true when the FIFO holds the number of words specified by the LEVEL signal. GEQTH is true when the FIFO holds (LEVEL) words or more
DO<0:8>	9	Out	Output data bits <0:8>. <8> will be parity output if PARGEN is true.
RPE	1	Out	Read parity error (active High)
WPE	1	Out	Write parity error (active High)
LGDEP <0:2>	3	In	Configures DEPTH of the FIFO to 2 (LGDEP+1)
PARODD	1	In	Parity generation/detect – Even when Low, Odd when High

Table 1-15 • Memory Block FIFO Interface Signals	Table 1-15	٠	Memory	Block	FIFO	Interface	Signals
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Operating Conditions

Standard and -F parts are the same unless otherwise noted. All -F parts are only available as commercial.

Table 1-17 • Absolute Maximum Ratings*

Parameter	Condition	Minimum	Maximum	Units
Supply Voltage Core (V _{DD})		-0.3	3.0	V
Supply Voltage I/O Ring (V _{DDP})		-0.3	4.0	V
DC Input Voltage		-0.3	V _{DDP} + 0.3	V
PCI DC Input Voltage		-1.0	V _{DDP} + 1.0	V
PCI DC Input Clamp Current (absolute)	$V_{IN} < -1$ or $V_{IN} = V_{DDP} + 1$ V	10		mA
LVPECL Input Voltage		-0.3	V _{DDP} + 0.5	V
GND		0	0	V

Note: *Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. Devices should not be operated outside the Recommended Operating Conditions.

Table 1-18	٠	Programming, Storage, and Operating Limits
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			Storage Te	mperature	Operating
Product Grade	Programming Cycles (min.)	Program Retention (min.)	Min.	Max.	T _J Max. Junction Temperature
Commercial	500	20 years	–55°C	110°C	110°C
Industrial	500	20 years	–55°C	110°C	110°C
Military	100	Refer to Table 1-19 on page 1-35	–65°C 150°C		150°C
MIL-STD-883	100	Refer to Table 1-19 on page 1-35	–65°C	150°C	150°C

Performance Retention

For devices operated and stored at 110°C or less, the performance retention period is 20 years after programming. For devices operated and stored at temperatures greater than 110°C, refer to Table 1-19 on page 1-35 to determine the performance retention period. Actel does not guarantee performance if the performance retention period is exceeded. Designers can determine the performance retention period from the following table.

Evaluate the percentage of time spent at the highest temperature, then determine the next highest temperature to which the device will be exposed. In Table 1-19 on page 1-35, find the temperature profile that most closely matches the application. Example – the ambient temperature of a system cycles between 100°C (25% of the time) and 50°C (75% of the time). No forced ventilation cooling system is in use. An APA600-PQ208M FPGA operates in the system, dissipating 1 W. The package thermal resistance (junction-to-ambient) in still air Θ_{ja} is 20°C/W, indicating that the junction temperature of the FPGA will be 120°C (25% of the time) and 70°C (75% of the time). The entry in Table 1-19 on page 1-35, which most closely matches the application, is 25% at 125°C with 75% at 110°C. Performance retention in this example is at least 16.0 years.

Note that exceeding the stated retention period may result in a performance degradation in the FPGA below the worst-case performance indicated in the Actel Timer. To ensure that performance does not degrade below the worst-case values in the Actel Timer, the FPGA must be reprogrammed within the performance retention period. In addition, note that performance retention is independent of whether or not the FPGA is operating. The retention period of a device in storage at a given temperature will be the same as the retention period of a device operating at that junction temperature.

			Comn Milita	nercial/Ind ry/MIL-STD	ustrial/ -883 ^{1, 2}	
Symbol	Parameter	Conditions	Min.	Тур.	Max.	Units
I _{OSH}	Output Short Circuit Current High High Drive (OB25LPH) Low Drive (OB25LPL)	$V_{IN} = V_{SS}$ $V_{IN} = V_{SS}$	-120 -100			mA
I _{OSL}	Output Short Circuit Current Low High Drive (OB25LPH) Low Drive (OB25LPL)	$V_{IN} = V_{DDP}$ $V_{IN} = V_{DDP}$			100 30	mA
CI/O	I/O Pad Capacitance				10	pF
C _{CLK}	Clock Input Pad Capacitance				10	pF

Table 1-22 • DC Electrical Specifications (V_{DDP} = 2.5 V \pm 0.2V) (Continued)

Notes:

1. All process conditions. Commercial/Industrial: Junction Temperature: -40 to +110°C.

2. All process conditions. Military: Junction Temperature: -55 to +150°C.

3. All –F parts are available only as commercial.

4. No pull-up resistor.

5. This will not exceed 2 mA total per device.

6. During transitions, the input signal may overshoot to V_{DDP} +1.0V for a limited time of no larger than 10% of the duty cycle.

7. During transitions, the input signal may undershoot to -1.0V for a limited time of no larger than 10% of the duty cycle.

Table 1-23DC Electrical Specifications (VP3.3 V±0.3 Vand VP2.5 V±0.2 V) (Continued)Applies to Commercial and Industrial Temperature Only

			Commercial/Industrial ¹				
Symbol	Parameter	Conditions	ľ	Min.	Тур.	Max.	Units
I _{OZ}	Tristate Output Leakage	$V_{OH} = GND \text{ or } V_{DD}$	Std.	-10		10	μA
	Current		-F ^{2, 4}	-10		100	μΑ
I _{OSH}	Output Short Circuit Current High 3.3 V High Drive (OB33P) 3.3 V Low Drive (OB33L)	$V_{IN} = GND$ $V_{IN} = GND$		-200 -100			
I _{OSL}	Output Short Circuit Current Low 3.3 V High Drive 3.3 V Low Drive	$V_{IN} = V_{DD}$ $V_{IN} = V_{DD}$				200 100	
CI/O	I/O Pad Capacitance					10	pF
C _{CLK}	Clock Input Pad Capacitance					10	pF

Notes:

1. All process conditions. Commercial/Industrial: Junction Temperature: -40 to +110°C.

2. All –F parts are only available as commercial.

3. No pull-up resistor required.

4. This will not exceed 2 mA total per device.

5. During transitions, the input signal may overshoot to V_{DDP} +1.0 V for a limited time of no larger than 10% of the duty cycle.

6. During transitions, the input signal may undershoot to -1.0 V for a limited time of no larger than 10% of the duty cycle.

Tristate Buffer Delays



Figure 1-26 • Tristate Buffer Delays

Table 1-27 • Worst-Case Commercial Conditions $V_{DDP} = 3.0 \text{ V}, V_{DD} = 2.3 \text{ V}, 35 \text{ pF load}, T_1 = 70^{\circ}\text{C}$

		Max t _{DLH} 1		Max t _{DHL} 2		Max t _{ENZH} ³		Max t _{ENZL} 4		
Macro Type	Description	Std.	-F	Std.	-F	Std.	-F	Std.	-F	Units
OTB33PH	3.3 V, PCI Output Current, High Slew Rate	2.0	2.4	2.2	2.6	2.2	2.6	2.0	2.4	ns
OTB33PN	3.3 V, High Output Current, Nominal Slew Rate	2.2	2.6	2.9	3.5	2.4	2.9	2.1	2.5	ns
OTB33PL	3.3 V, High Output Current, Low Slew Rate	2.5	3.0	3.2	3.9	2.7	3.3	2.8	3.4	ns
OTB33LH	3.3 V, Low Output Current, High Slew Rate	2.6	3.1	4.0	4.8	2.8	3.4	3.0	3.6	ns
OTB33LN	3.3 V, Low Output Current, Nominal Slew Rate	2.9	3.5	4.3	5.2	3.2	3.8	4.1	4.9	ns
OTB33LL	3.3 V, Low Output Current, Low Slew Rate	3.0	3.6	5.6	6.7	3.3	3.9	5.5	6.6	ns

Notes:

- 1. t_{DLH}=Data-to-Pad High
- 2. t_{DHL}=Data-to-Pad Low
- 3. t_{ENZH}=Enable-to-Pad, Z to High
- 4. t_{ENZL} = Enable-to-Pad, Z to Low
- 5. All –F parts are only available as commercial.

Table 1-28 Worst-Case Commercial Conditions

 V_{DDP} = 2.3 V, V_{DD} = 2.3 V, 35 pF load, T_J = 70°C

		Max t _{DLH} 1		Max t _{DHL} 2		Max t _{ENZH} ³		Max t _{ENZL} 4		
Macro Type	Description	Std.	-F	Std.	-F	Std.	-F	Std.	-F	Units
OTB25LPHH	2.5 V, Low Power, High Output Current, High Slew Rate ⁵	2.0	2.4	2.1	2.5	2.3	2.7	2.0	2.4	ns
OTB25LPHN	2.5 V, Low Power, High Output Current, Nominal Slew Rate ⁵	2.4	2.9	3.0	3.6	2.7	3.2	2.1	2.5	ns
OTB25LPHL	2.5 V, Low Power, High Output Current, Low Slew Rate ⁵	2.9	3.5	3.2	3.8	3.1	3.8	2.7	3.2	ns
OTB25LPLH	2.5 V, Low Power, Low Output Current, High Slew Rate ⁵	2.7	3.3	4.6	5.5	3.0	3.6	2.6	3.1	ns

Notes:

- 1. t_{DLH}=Data-to-Pad High
- 2. t_{DHL}=Data-to-Pad Low
- 3. t_{ENZH} =Enable-to-Pad, Z to High
- 4. t_{ENZL} = Enable-to-Pad, Z to Low
- 5. Low power I/O work with $V_{DDP}=2.5 V \pm 10\%$ only. $V_{DDP}=2.3 V$ for delays.
- 6. All –F parts are only available as commercial.

Table 1-37 • Worst-Case Military Conditions

 V_{DDP} = 3.0V, V_{DD} = 2.3V, T_{J} = 125°C for Military/MIL-STD-883

		Max. t _{INYH} 1	Max. t _{INYL} ²	
Macro Type	Description	Std.	Std.	Units
IB33	3.3V, CMOS Input Levels ³ , No Pull-up Resistor	0.5	0.6	ns
IB33S	3.3V, CMOS Input Levels ³ , No Pull-up Resistor, Schmitt Trigger	0.6	0.8	ns

Notes:

- 1. $t_{INYH} = Input Pad-to-Y High$
- 2. $t_{INYL} = Input Pad-to-Y Low$
- 3. LVTTL delays are the same as CMOS delays.
- 4. For LP Macros, V_{DDP}=2.3V for delays.

Table 1-38 • Worst-Case Military Conditions

V_{DDP} = 2.3V, V_{DD} = 2.3V, T_J = 125°C for Military/MIL-STD-883

		Max. t _{INYH} 1	Max. t _{INYL} ²	
Macro Type	Description	Std.	Std.	Units
IB25LP	2.5V, CMOS Input Levels ³ , Low Power	0.9	0.7	ns
IB25LPS	2.5V, CMOS Input Levels ³ , Low Power, Schmitt Trigger	0.8	1.0	ns

Notes:

- 1. $t_{INYH} = Input Pad-to-Y High$
- 2. $t_{INYL} = Input Pad-to-Y Low$
- 3. LVTTL delays are the same as CMOS delays.
- 4. For LP Macros, V_{DDP} =2.3V for delays.

Table 1-50 • JTAG Switching Characteristics

Description	Symbol	Min	Мах	Unit
Output delay from TCK falling to TDI, TMS	t _{TCKTDI}	-4	4	ns
TDO Setup time before TCK rising	t _{TDOTCK}	10		ns
TDO Hold time after TCK rising	t _{TCKTDO}	0		ns
TCK period	t _{TCK}	100 ²	1,000	ns
RCK period	t _{RCK}	100	1,000	ns

Notes:

1. For DC electrical specifications of the JTAG pins (TCK, TDI, TMS, TDO, TRST), refer to Table 1-22 on page 1-37 when $V_{DDP} = 2.5 V$ and Table 1-24 on page 1-41 when $V_{DDP} = 3.3 V$.

2. If RCK is being used, there is no minimum on the TCK period.



Figure 1-30 • JTAG Operation Timing

Asynchronous SRAM Write



Note: The plot shows the normal operation status.

Figure 1-33 • Asynchronous SRAM Write

Table 1-54T_J = 0°C to 110°C; V_{DD} = 2.3 V to 2.7 V for Commercial/industrialT_J = -55°C to 150°C, V_{DD} = 2.3 V to 2.7 V for Military/MIL-STD-883B

Symbol t _{xxx}	Description	Min.	Max.	Units	Notes
AWRH	WADDR hold from WB ↑	1.0		ns	
AWRS	WADDR setup to WB \downarrow	0.5		ns	
DWRH	DI hold from WB ↑	1.5		ns	
DWRS	DI setup to WB ↑	0.5		ns	PARGEN is inactive.
DWRS	DI setup to WB ↑	2.5		ns	PARGEN is active.
WPDA	WPE access from DI	3.0		ns	WPE is invalid, while PARGEN is
WPDH	WPE hold from DI		1.0	ns	active.
WRCYC	Cycle time	7.5		ns	
WRMH	WB high phase	3.0		ns	Inactive
WRML	WB low phase	3.0		ns	Active

Note: All –F speed grade devices are 20% slower than the standard numbers.



Synchronous Write and Asynchronous Read to the Same Location

Note: The plot shows the normal operation status.

Figure 1-40 • Synchronous Write and Asynchronous Read to the Same Location

Table 1-61 $T_J = 0^{\circ}C$ to 110°C; $V_{DD} = 2.3$ V to 2.7 V for Commercial/industrial $T_J = -55^{\circ}C$ to 150°C, $V_{DD} = 2.3$ V to 2.7 V for Military/MIL-STD-883

Symbol t _{xxx}	Description	Min.	Max.	Units	Notes
ORDA	New DO access from RB \downarrow	7.5		ns	
ORDH	Old DO valid from RB \downarrow		3.0	ns	
OWRA	New DO access from WCLKS \downarrow	3.0		ns	
OWRH	Old DO valid from WCLKS \downarrow		0.5	ns	
RAWCLKS	RB ↓ or RADDR from WCLKS ↑	5.0		ns	
RAWCLKH	RB \uparrow or RADDR from WCLKS \downarrow	5.0		ns	

Notes:

1. During an asynchronous read cycle, each write operation (synchronous or asynchronous) to the same location will automatically trigger a read operation which updates the read data.

2. Violation of RAWCLKS will disturb access to OLD data.

3. Violation of RAWCLKH will disturb access to NEWER data.

Asynchronous FIFO Read



Note: The plot shows the normal operation status.

Figure 1-43 • Asynchronous FIFO Read

Table 1-63T_J = 0°C to 110°C; V_{DD} = 2.3 V to 2.7 V for Commercial/industrialT_J = -55°C to 150°C, V_{DD} = 2.3 V to 2.7 V for Military/MIL-STD-883

Symbol t _{xxx}	Description	Min.	Max.	Units	Notes
ERDH, FRDH, THRDH	Old EMPTY, FULL, EQTH, & GETH valid hold time from RB \uparrow		0.5	ns	Empty/full/thresh are invalid from the end of hold until the new access is complete
ERDA	New EMPTY access from RB \uparrow	3.0 ¹		ns	
FRDA	FULL↓ access from RB ↑	3.0 ¹		ns	
ORDA	New DO access from RB \downarrow	7.5		ns	
ORDH	Old DO valid from RB \downarrow		3.0	ns	
RDCYC	Read cycle time	7.5		ns	
RDWRS	WB \uparrow , clearing EMPTY, setup to RB \downarrow	3.0 ²		ns	Enabling the read operation
			1.0	ns	Inhibiting the read operation
RDH	RB high phase	3.0		ns	Inactive
RDL	RB low phase	3.0		ns	Active
RPRDA	New RPE access from RB \downarrow	9.5		ns	
RPRDH	Old RPE valid from RB \downarrow		4.0	ns	
THRDA	EQTH or GETH access from RB [↑]	4.5		ns	

Notes:

1. At fast cycles, ERDA and FRDA = MAX (7.5 ns – RDL), 3.0 ns.

2. At fast cycles, RDWRS (for enabling read) = MAX (7.5 ns – WRL), 3.0 ns.

Synchronous FIFO Read, Pipeline Mode Outputs (Synchronous Pipelined)



Note: The plot shows the normal operation status.

Figure 1-46 •	Synchronous	FIFO Read,	Pipeline Mo	de Outputs	(Synchronous	Pipelined)
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Table 1-66T_J = 0°C to 110°C; V_{DD} = 2.3 V to 2.7 V for Commercial/industrialT_J = -55°C to 150°C, V_{DD} = 2.3 V to 2.7 V for Military/MIL-STD-883

Symbol t _{xxx}	Description	Min.	Max.	Units	Notes
CCYC	Cycle time	7.5		ns	
СМН	Clock high phase	3.0		ns	
CML	Clock low phase	3.0		ns	
ECBA	New EMPTY access from RCLKS \downarrow	3.0 ¹		ns	
FCBA	FULL \downarrow access from RCLKS \downarrow	3.0 ¹		ns	
ЕСВН, FCBH, ТНСВН	Old EMPTY, FULL, EQTH, & GETH valid hold time from RCLKS \downarrow		1.0	ns	Empty/full/thresh are invalid from the end of hold until the new access is complete
OCA	New DO access from RCLKS \uparrow	2.0		ns	
OCH	Old DO valid from RCLKS 1		0.75	ns	
RDCH	RDB hold from RCLKS ↑	0.5		ns	
RDCS	RDB setup to RCLKS ↑	1.0		ns	
RPCA	New RPE access from RCLKS \uparrow	4.0		ns	
RPCH	Old RPE valid from RCLKS \uparrow		1.0	ns	
НСВА	EQTH or GETH access from RCLKS \downarrow	4.5		ns	

Notes:

1. At fast cycles, ECBA and FCBA = MAX (7.5 ns - CMS), 3.0 ns.

Synchronous FIFO Write



Note: The plot shows the normal operation status.

Figure 1-47 • Synchronous FIFO Write

Table 1-67 • $T_J = 0^{\circ}$ C to 110°C; $V_{DD} = 2.3$ V to 2.7 V for Commercial/industrial $T_J = -55^{\circ}$ C to 150°C, $V_{DD} = 2.3$ V to 2.7 V for Military/MIL-STD-883

Symbol t _{xxx}	Description	Min.	Max.	Units	Notes
CCYC	Cycle time	7.5		ns	
СМН	Clock high phase	3.0		ns	
CML	Clock low phase	3.0		ns	
DCH	DI hold from WCLKS ↑	0.5		ns	
DCS	DI setup to WCLKS ↑	1.0		ns	
FCBA	New FULL access from WCLKS \downarrow	3.0 ¹		ns	
ECBA	EMPTY \downarrow access from WCLKS \downarrow	3.0 ¹		ns	
ЕСВН, FCBH, HCBH	Old EMPTY, FULL, EQTH, & GETH valid hold time from WCLKS \downarrow		1.0	ns	Empty/full/thresh are invalid from the end of hold until the new access is complete
НСВА	EQTH or GETH access from WCLKS \downarrow	4.5		ns	
WPCA	New WPE access from WCLKS \uparrow	3.0		ns	WPE is invalid, while PARGEN is active
WPCH	Old WPE valid from WCLKS ↑		0.5	ns	
WRCH, WBCH	WRB & WBLKB hold from WCLKS \uparrow	0.5		ns	
WRCS, WBCS	WRB & WBLKB setup to WCLKS ↑	1.0		ns	

Notes:

1. At fast cycles, ECBA and FCBA = MAX (7.5 ns – CMH), 3.0 ns.

V_{PP} Programming Supply Pin

This pin may be connected to any voltage between GND and 16.5 V during normal operation, or it can be left unconnected.² For information on using this pin during programming, see the *In-System Programming ProASIC*^{PLUS} *Devices* application note. Actel recommends floating the pin or connecting it to V_{DDP}

V_{PN} Programming Supply Pin

This pin may be connected to any voltage between 0.5V and -13.8 V during normal operation, or it can be left unconnected.³ For information on using this pin during programming, see the *In-System Programming ProASIC*^{PLUS} Devices application note. Actel recommends floating the pin or connecting it to GND.

Recommended Design Practice for V_{PN}/V_{PP}

ProASIC^{PLUS} Devices – APA450, APA600, APA750, APA1000

Bypass capacitors are required from V_{PP} to GND and V_{PN} to GND for all ProASIC^{PLUS} devices during programming. During the erase cycle, ProASIC^{PLUS} devices may have current surges on the V_{PP} and V_{PN} power supplies. The only way to maintain the integrity of the power distribution to the ProASIC^{PLUS} device during these current surges is to counteract the inductance of the finite length conductors that distribute the power to the device. This can be accomplished by providing sufficient bypass capacitance between the V_{PP} and V_{PN} pins and GND (using the shortest paths possible). Without sufficient bypass capacitance to counteract the inductance, the V_{PP} and V_{PN} pins may incur a voltage spike beyond the voltage that the device can withstand. This issue applies to all programming configurations.

The solution prevents spikes from damaging the ProASIC^{PLUS} devices. Bypass capacitors are required for the V_{PP} and V_{PN} pads. Use a 0.01 μ F to 0.1 μ F ceramic capacitor with a 25 V or greater rating. To filter low-frequency noise (decoupling), use a 4.7 μ F (low ESR, <1 < Ω , tantalum, 25 V or greater rating) capacitor. The capacitors should be located as close to the device pins as possible (within 2.5 cm is desirable). The smaller, high-frequency capacitor should be placed closer to the device pins than the larger low-frequency capacitor. The same dual-capacitor circuit should be used on both the V_{PP} and V_{PN} pins (Figure 1-49).

ProASIC^{PLUS} Devices – APA075, APA150, APA300

These devices do not require bypass capacitors on the V_{PP} and V_{PN} pins as long as the total combined distance of the programming cable and the trace length on the board is less than or equal to 30 inches. Note: For trace lengths greater than 30 inches, use the bypass capacitor recommendations in the previous section.



Figure 1-49 • ProASICPLUS V_{PP} and V_{PN} Capacitor Requirements

2. There is a nominal 40 k Ω pull-up resistor on V_{PP}

3. There is a nominal 40 k pull-down resistor on V_{PN}