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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	129024
Number of I/O	158
Number of Gates	600000
Voltage - Supply	2.3V ~ 2.7V
Mounting Type	Surface Mount
Operating Temperature	-55°C ~ 125°C (TC)
Package / Case	208-BFCQFP with Tie Bar
Supplier Device Package	208-CQFP (75x75)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/apa600-cq208m

Device Resources

	User I/Os[2]												
	Commercial/Industrial										Military/MIL-STD-883B		
Device	TQFP 100-Pin	TQFP 144-Pin	PQFP 208-Pin	PBGA 456-Pin	FBGA 144-Pin	FBGA 256-Pin	FBGA 484-Pin	FBGA 676-Pin	FBGA 896-Pin	FBGA 1152-Pin	CQFP 208-Pin	CQFP 352-Pin	CCGA/ LGA 624-Pin
APA075	66	107	158		100								
APA150	66		158	242	100	186 [3]							
APA300			158 [4]	290 [4]	100 [4]	186 [3, 4]					158	248	
APA450			158	344	100	186 [3]	344 [3]						
APA600			158 [4]	356 [4]		186 [3, 4]	370 [3]	454			158	248	440
APA750			158	356				454	562 [5]				
APA1000			158 [4]	356 [4]					642 [4, 5]	712 [5]	158	248	440

Notes:

1. *Package Definitions: TQFP = Thin Quad Flat Pack, PQFP = Plastic Quad Flat Pack, PBGA = Plastic Ball Grid Array, FBGA = Fine Pitch Ball Grid Array, CQFP = Ceramic Quad Flat Pack, CCGA = Ceramic Column Grid Array, LGA = Land Grid Array*
2. *Each pair of PECL I/Os is counted as one user I/O.*
3. *FG256 and FG484 are footprint-compatible packages.*
4. *Military Temperature Plastic Package Offering*
5. *FG896 and FG1152 are footprint-compatible packages.*

General Guideline

Maximum performance numbers in this datasheet are based on characterized data. Actel does not guarantee performance beyond the limits specified within the datasheet.

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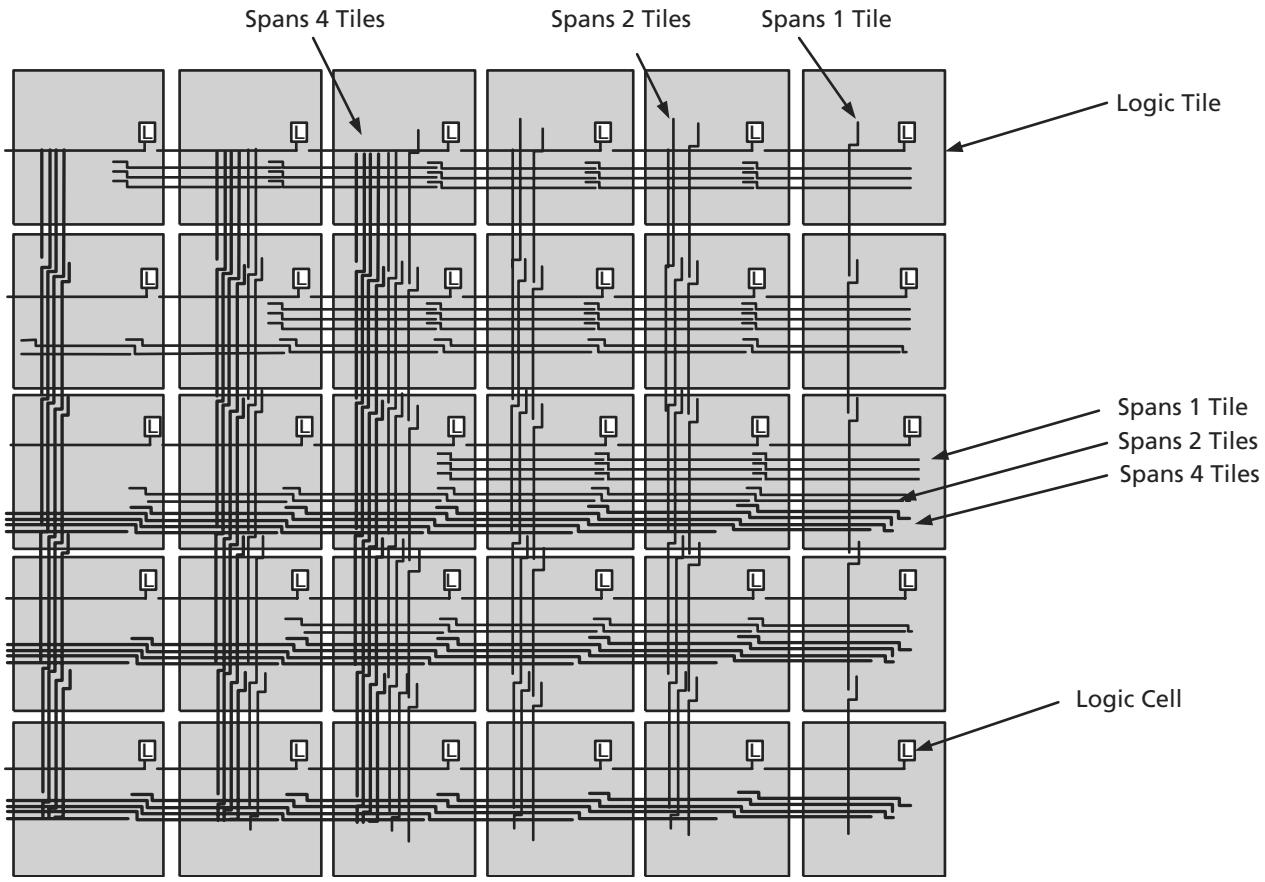
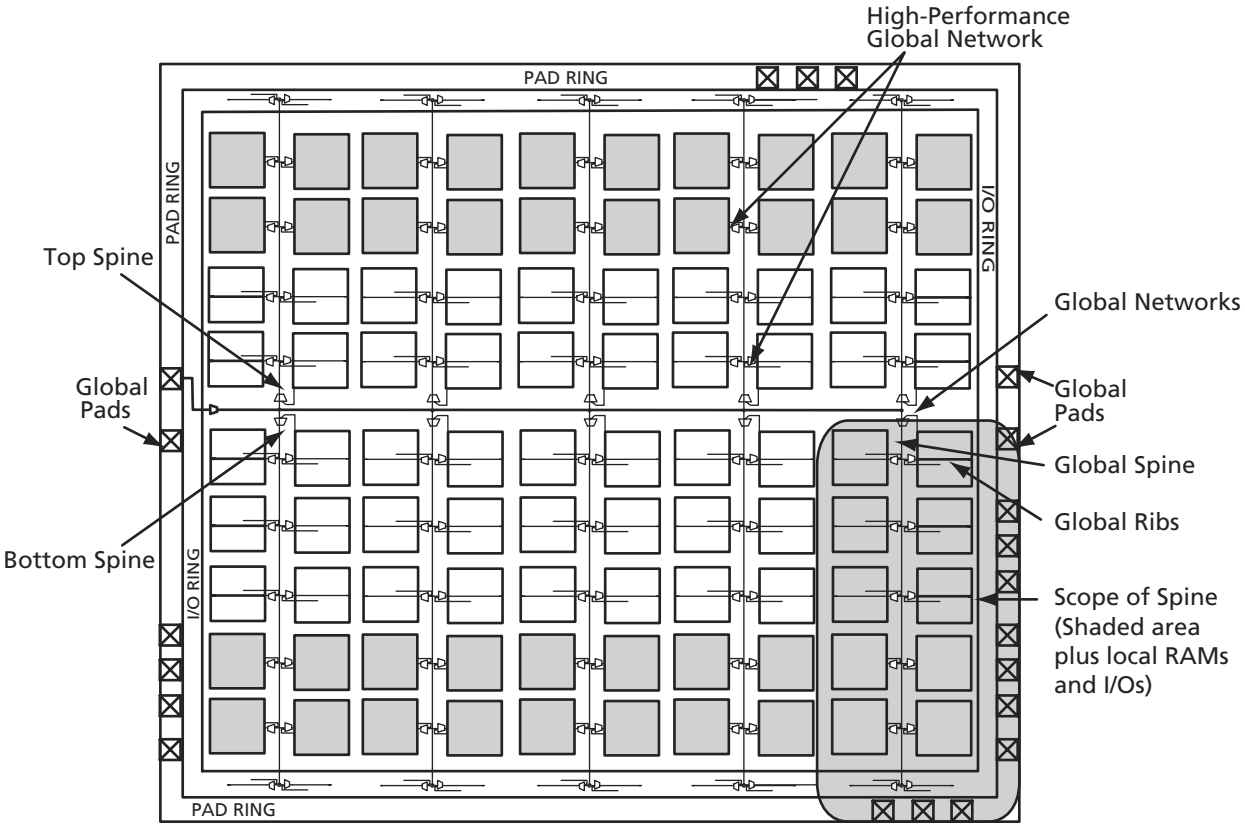


Figure 1-5 • **Efficient Long-Line Resources**

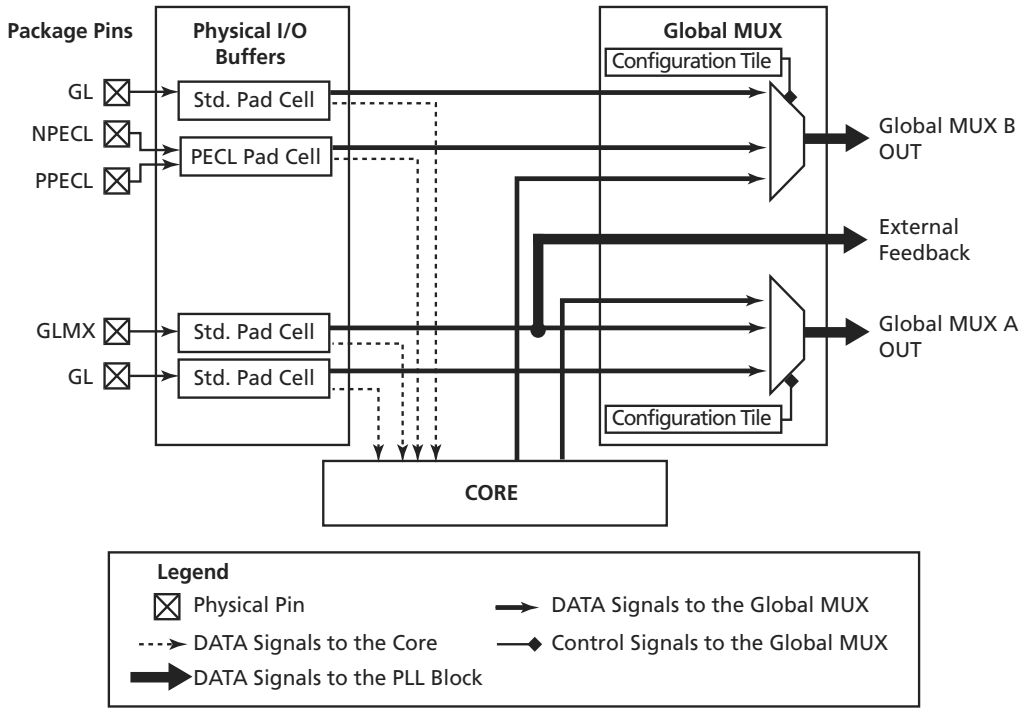


Note: *This figure shows routing for only one global path.*

Figure 1-7 • **High-Performance Global Network**

Table 1-1 • **Clock Spines**

	APA075	APA150	APA300	APA450	APA600	APA750	APA1000
Global Clock Networks (Trees)	4	4	4	4	4	4	4
Clock Spines/Tree	6	8	8	12	14	16	22
Total Spines	24	32	32	48	56	64	88
Top or Bottom Spine Height (Tiles)	16	24	32	32	48	64	80
Tiles in Each Top or Bottom Spine	512	768	1,024	1,024	1,536	2,048	2,560
Total Tiles	3,072	6,144	8,192	12,288	21,504	32,768	56,320



Note: *When a signal from an I/O tile is connected to the core, it cannot be connected to the Global MUX at the same time.*

Figure 1-15 • **Input Connectors to ProASIC^PLUS Clock Conditioning Circuitry**

Table 1-7 • **Clock-Conditioning Circuitry MUX Settings**

MUX	Datapath	Comments
FBSEL		
1	Internal Feedback	
2	Internal Feedback and Advance Clock Using FBDLY	–0.25 to –4 ns in 0.25 ns increments
3	External Feedback (EXTFB)	
XDLYSEL		
0	Feedback Unchanged	
1	Deskew feedback by advancing clock by system delay	Fixed delay of -2.95 ns
OBMUX	**GLB**	
0	Primary bypass, no divider	
1	Primary bypass, use divider	
2	Delay Clock Using FBDLY	+0.25 to +4 ns in 0.25 ns increments
4	Phase Shift Clock by 0°	
5	Reserved	
6	Phase Shift Clock by +180°	
7	Reserved	
OAMUX	**GLA**	
0	Secondary bypass, no divider	
1	Secondary bypass, use divider	
2	Delay Clock Using FBDLY	+0.25 to +4 ns in 0.25 ns increments
3	Phase Shift Clock by 0°	

Table 1-8 • **Clock-Conditioning Circuitry Delay-Line Settings**

Delay Line	Delay Value (ns)
DLYB	
0	0
1	+0.25
2	+0.50
3	+4.0
DLYA	
0	0
1	+0.25
2	+0.50
3	+4.0

Lock Signal

An active-high Lock signal (added via the SmartGen PLL development tool) indicates that the PLL has locked to the incoming clock signal. The PLL will acquire and maintain lock even when there is jitter on the incoming clock signal. The PLL will maintain lock with an input jitter up to 5% of the input period, with a maximum of 5 ns. Users can employ the Lock signal as a soft reset of the logic driven by GLB and/or GLA. Note if F_{IN} is not within specified frequencies, then both the F_{OUT} and lock signal are indeterminate.

PLL Configuration Options

The PLL can be configured during design (via Flash-configuration bits set in the programming bitstream) or dynamically during device operation, thus eliminating the need to reprogram the device. The dynamic configuration bits are loaded into a serial-in/parallel-out shift register provided in the clock conditioning circuit. The shift register can be accessed either from user logic within the device or via the JTAG port. Another option is internal dynamic configuration via user-designed hardware. Refer to Actel's *ProASIC^PLUS PLL Dynamic Reconfiguration Using JTAG* application note for more information.

For information on the clock conditioning circuit, refer to Actel's *Using ProASIC^PLUS Clock Conditioning Circuits* application note.

Sample Implementations

Frequency Synthesis

Figure 1-16 on page 1-17 illustrates an example where the PLL is used to multiply a 33 MHz external clock up to 133 MHz. Figure 1-17 on page 1-17 uses two dividers to synthesize a 50 MHz output clock from a 40 MHz input reference clock. The input frequency of 40 MHz is multiplied by five and divided by four, giving an output clock (GLB) frequency of 50 MHz. When dividers are used, a given ratio can be generated in multiple ways, allowing the user to stay within the operating frequency ranges of the PLL. For example, in this case the input divider could have been two and the output divider also two, giving us a division of the input frequency by four to go with the feedback loop division (effective multiplication) by five.

Adjustable Clock Delay

Figure 1-18 on page 1-18 illustrates the delay of the input clock by employing one of the adjustable delay lines. This is easily done in ProASIC^PLUS by bypassing the PLL core entirely and using the output delay line. Notice also that the output clock can be effectively advanced relative to the input clock by using the delay line in the feedback path. This is shown in Figure 1-19 on page 1-18.

Clock Skew Minimization

Figure 1-20 on page 1-19 indicates how feedback from the clock network can be used to create minimal skew between the distributed clock network and the input clock. The input clock is fed to the reference clock input of the PLL. The output clock (GLA) feeds a clock network. The feedback input to the PLL uses a clock input delayed by a routing network. The PLL then adjusts the phase of the input clock to match the delayed clock, thus providing nearly zero effective skew between the two clocks. Refer to Actel's *Using ProASIC^PLUS Clock Conditioning Circuits* application note for more information.

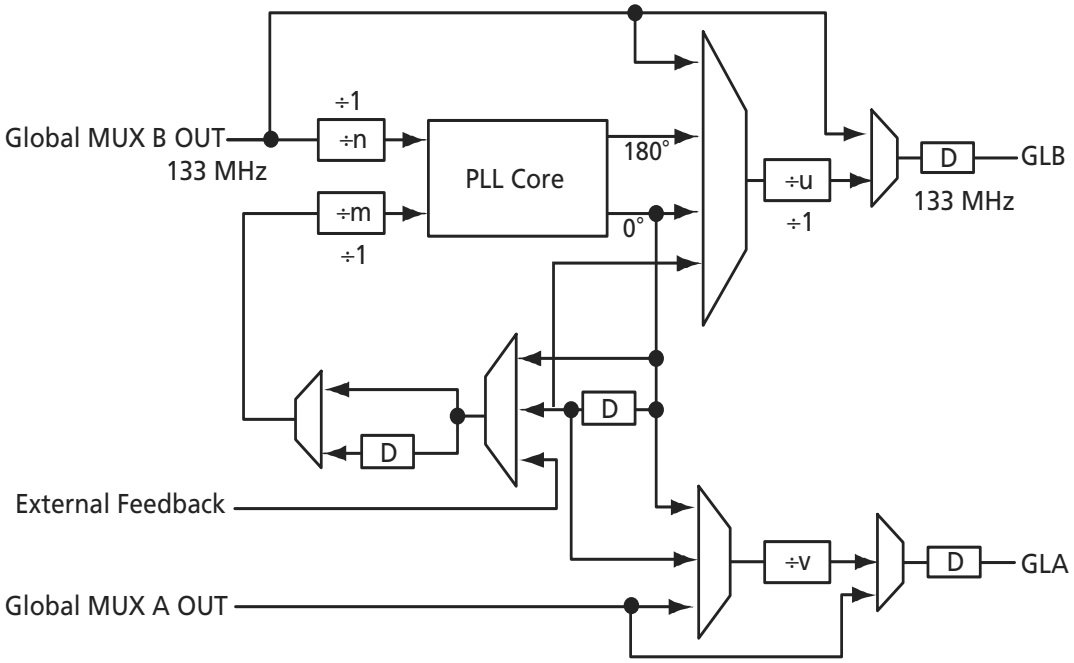


Figure 1-18 • **Using the PLL to Delay the Input Clock**

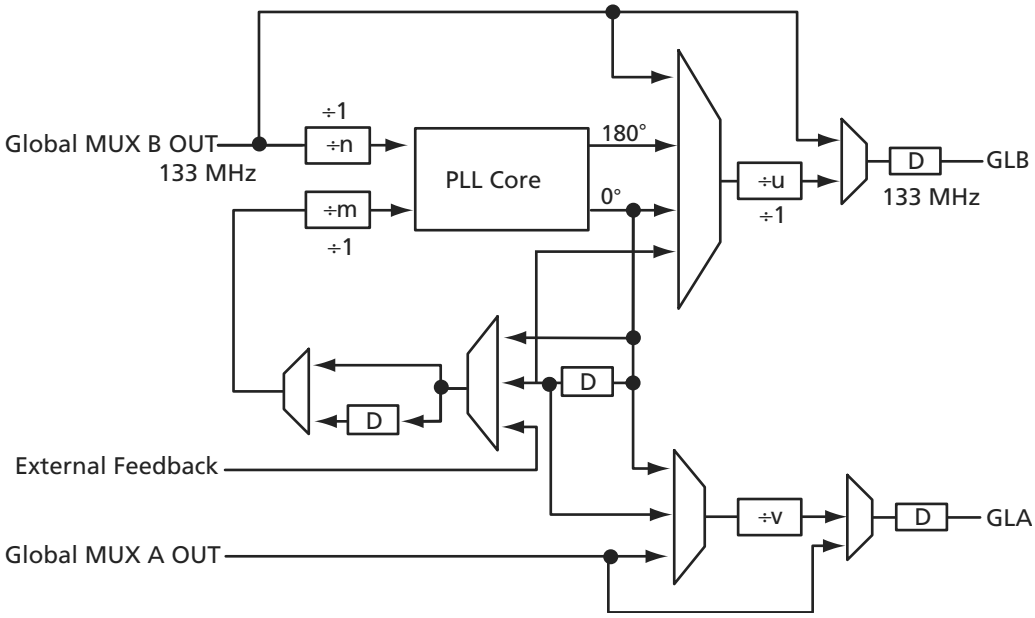
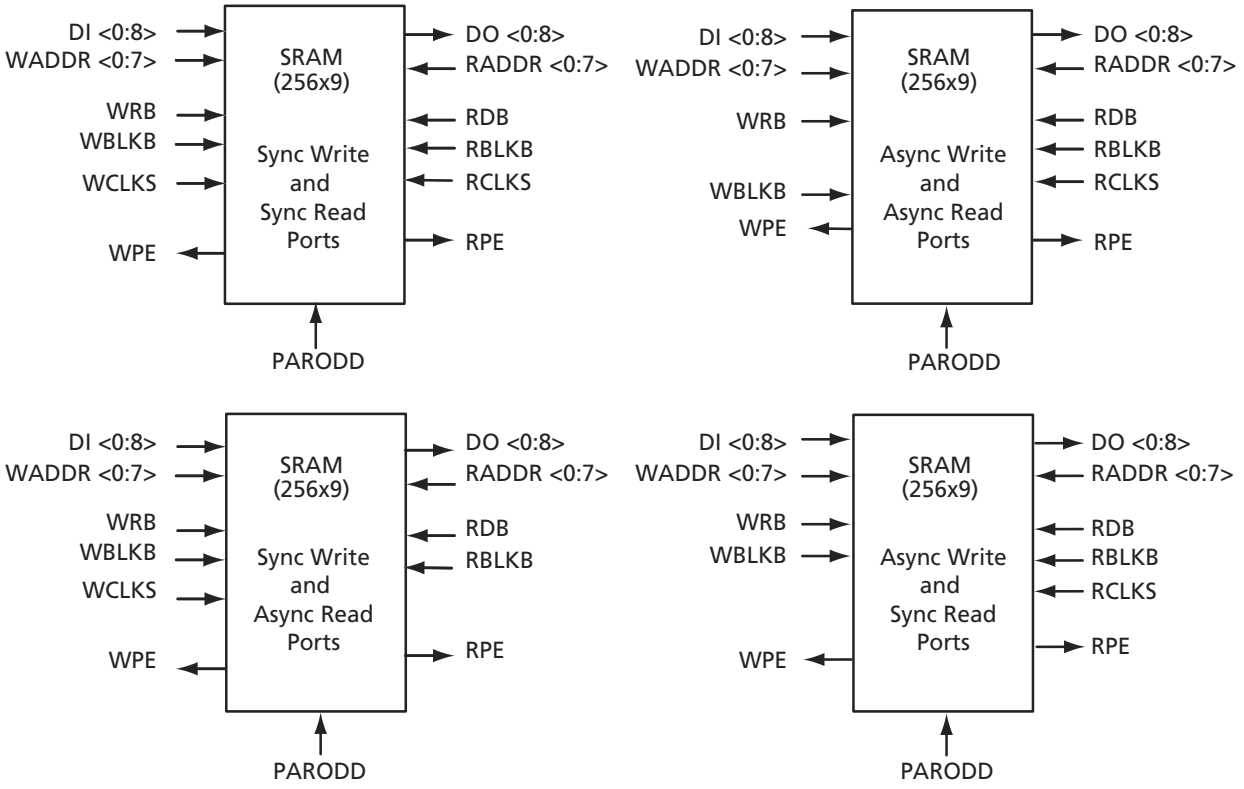


Figure 1-19 • **Using the PLL to Advance the Input Clock**



Note: *Each RAM block contains a multiplexer (called DMUX) for each output signal, increasing design efficiency. These DMUX cells do not consume any core logic tiles and connect directly to high-speed routing resources between the RAM blocks. They are used when RAM blocks are cascaded and are automatically inserted by the software tools.*

Figure 1-21 • **Example SRAM Block Diagrams**

Table 1-14 • **Memory Block SRAM Interface Signals**

SRAM Signal	Bits	In/Out	Description
WCLKS	1	In	Write clock used on synchronization on write side
RCLKS	1	In	Read clock used on synchronization on read side
RADDR<0:7>	8	In	Read address
RBLKB	1	In	Read block select (active Low)
RDB	1	In	Read pulse (active Low)
WADDR<0:7>	8	In	Write address
WBLKB	1	In	Write block select (active Low)
DI<0:8>	9	In	Input data bits <0:8>, <8> can be used for parity In
WRB	1	In	Write pulse (active Low)
DO<0:8>	9	Out	Output data bits <0:8>, <8> can be used for parity Out
RPE	1	Out	Read parity error (active High)
WPE	1	Out	Write parity error (active High)
PARODD	1	In	Selects Odd parity generation/detect when High, Even parity when Low

Note: *Not all signals shown are used in all modes.*

Design Environment

The ProASIC^PLUS family of FPGAs is fully supported by both Actel's Libero® Integrated Design Environment (IDE) and Designer FPGA Development software. Actel Libero IDE is an integrated design manager that seamlessly integrates design tools while guiding the user through the design flow, managing all design and log files, and passing necessary design data among tools. Additionally, Libero IDE allows users to integrate both schematic and HDL synthesis into a single flow and verify the entire design in a single environment (see Actel's website for more information about *Libero IDE*). Libero IDE includes Synplify® AE from Synplicity®, ViewDraw® AE from Mentor Graphics®, Model*Sim*® HDL Simulator from Mentor Graphics, WaveFormer Lite™ AE from SynaptiCAD®, PALACE™ AE Physical Synthesis from Magma, and Designer software from Actel.

PALACE is an effective tool when designing with ProASIC^PLUS. PALACE AE Physical Synthesis from Magma takes an EDIF netlist and optimizes the performance of ProASIC^PLUS devices through a physical placement-driven process, ensuring that timing closure is easily achieved.

Actel's Designer software is a place-and-route tool that provides a comprehensive suite of back-end support tools for FPGA development. The Designer software includes the following:

- Timer – a world-class integrated static timing analyzer and constraints editor that support timing-driven place-and-route
- NetlistViewer – a design netlist schematic viewer
- ChipPlanner – a graphical floorplanner viewer and editor
- SmartPower – allows the designer to quickly estimate the power consumption of a design
- PinEditor – a graphical application for editing pin assignments and I/O attributes
- I/O Attribute Editor – displays all assigned and unassigned I/O macros and their attributes in a spreadsheet format

With the Designer software, a user can lock the design pins before layout while minimally impacting the results of place-and-route. Additionally, Actel's back-annotation flow is compatible with all the major simulators. Another tool included in the Designer software is the SmartGen macro builder, which easily creates popular and commonly used logic functions for implementation into your schematic or HDL design.

Actel's Designer software is compatible with the most popular FPGA design entry and verification tools from EDA vendors, such as Mentor Graphics, Synplicity, Synopsys, and Cadence Design Systems. The Designer software is available for both the Windows and UNIX operating systems.

ISP

The user can generate *.bit or *.stp programming files from the Designer software and can use these files to program a device.

ProASIC^PLUS devices can be programmed in-system. For more information on ISP of ProASIC^PLUS devices, refer to the *In-System Programming ProASIC^PLUS Devices* and *Performing Internal In-System Programming Using Actel's ProASIC^PLUS Devices* application notes. Prior to being programmed for the first time, the ProASIC^PLUS device I/Os are in a tristate condition with the pull-up resistor option enabled.

Related Documents

Application Notes

Efficient Use of ProASIC Clock Trees
http://www.actel.com/documents/A500K_Clocktree_AN.pdf
I/O Features in ProASIC^PLUS Flash FPGAs
http://www.actel.com/documents/APA_LVPECL_AN.pdf
Power-Up Behavior of ProASIC^PLUS Devices
http://www.actel.com/documents/APA_PowerUp_AN.pdf
ProASIC^PLUS PLL Dynamic Reconfiguration Using JTAG
http://www.actel.com/documents/APA_PLLdynamic_AN.pdf
Using ProASIC^PLUS Clock Conditioning Circuits
http://www.actel.com/documents/APA_PLL_AN.pdf
In-System Programming ProASIC^PLUS Devices
http://www.actel.com/documents/APA_External_ISP_AN.pdf
Performing Internal In-System Programming Using Actel's ProASIC^PLUS Devices
http://www.actel.com/documents/APA_Microprocessor_AN.pdf
ProASIC^PLUS RAM and FIFO Blocks
http://www.actel.com/documents/APA_RAM_FIFO_AN.pdf

White Paper

Design Security in Nonvolatile Flash and Antifuse FPGAs
http://www.actel.com/documents/DesignSecurity_WP.pdf

User's Guide

Designer User's Guide
http://www.actel.com/documents/designer_UG.pdf
SmartGen Cores Reference Guide
http://www.actel.com/documents/gen_refguide_ug.pdf
ProASIC and ProASIC^PLUS Macro Library Guide
http://www.actel.com/documents/pa_libguide_UG.pdf

Additional Information

The following link contains additional information on ProASIC^PLUS devices.
http://www.actel.com/products/proasicplus/default.aspx

Calculating Typical Power Dissipation

ProASIC^PLUS device power is calculated with both a static and an active component. The active component is a function of both the number of tiles utilized and the system speed. Power dissipation can be calculated using the following formula:

Total Power Consumption—P_{total}

$P_{total} = P_{dc} + P_{ac}$

where:

P_{dc} = 7 mW for the APA075
8 mW for the APA150
11 mW for the APA300
12 mW for the APA450
12 mW for the APA600
13 mW for the APA750
19 mW for the APA1000
P_{dc} includes the static components of $P_{VDDP} + P_{VDD} + P_{AVDD}$

P_{ac} = $P_{clock} + P_{storage} + P_{logic} + P_{outputs} + P_{inputs} + P_{pll} + P_{memory}$

Global Clock Contribution—P_{clock}

P_{clock}, the clock component of power dissipation, is given by the piece-wise model:

for R < 15000 the model is: (P1 + (P2*R) - (P7*R2)) * Fs (lightly-loaded clock trees)

for R > 15000 the model is: (P10 + P11*R) * Fs (heavily-loaded clock trees)

where:

P1 = 100 µW/MHz is the basic power consumption of the clock tree per MHz of the clock

P2 = 1.3 µW/MHz is the incremental power consumption of the clock tree per storage tile – also per MHz of the clock

P7 = 0.00003 µW/MHz is a correction factor for partially-loaded clock trees

P10 = 6850 µW/MHz is the basic power consumption of the clock tree per MHz of the clock

P11 = 0.4 µW/MHz is the incremental power consumption of the clock tree per storage tile – also per MHz of the clock

R = the number of storage tiles clocked by this clock

Fs = the clock frequency

Storage-Tile Contribution—$P_{storage}$

$P_{storage}$, the storage-tile (Register) component of AC power dissipation, is given by

$P_{storage} = P5 * ms * Fs$

where:

P5 = 1.1 µW/MHz is the average power consumption of a storage tile per MHz of its output toggling rate. The maximum output toggling rate is Fs/2.

ms = the number of storage tiles (Register) switching during each Fs cycle

Fs = the clock frequency

Table 1-23 • **DC Electrical Specifications (V_{DDP} = 3.3 V ±0.3 V and V_{DD} = 2.5 V ±0.2 V) (Continued)**
Applies to Commercial and Industrial Temperature Only

Symbol	Parameter	Conditions		Commercial/Industrial[1] Min.	Typ.	Max.	Units
I_{OZ}	Tristate Output Leakage Current	V_{OH} = GND or V_{DD}	Std.	–10		10	µA
			–F[2, 4]	–10		100	µA
I_{OSH}	Output Short Circuit Current High 3.3 V High Drive (OB33P) 3.3 V Low Drive (OB33L)	 V_{IN} = GND V_{IN} = GND		 –200 –100			
I_{OSL}	Output Short Circuit Current Low 3.3 V High Drive 3.3 V Low Drive	 V_{IN} = V_{DD} V_{IN} = V_{DD}				 200 100	
$C_{I/O}$	I/O Pad Capacitance					10	pF
C_{CLK}	Clock Input Pad Capacitance					10	pF

Notes:

1. *All process conditions. Commercial/Industrial: Junction Temperature: –40 to +110°C.*
2. *All –F parts are only available as commercial.*
3. *No pull-up resistor required.*
4. *This will not exceed 2 mA total per device.*
5. *During transitions, the input signal may overshoot to V_{DDP} +1.0 V for a limited time of no larger than 10% of the duty cycle.*
6. *During transitions, the input signal may undershoot to –1.0 V for a limited time of no larger than 10% of the duty cycle.*

Input Buffer Delays

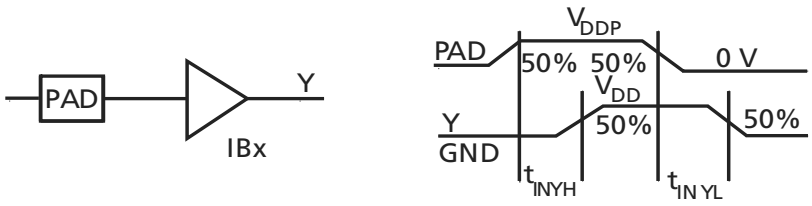


Figure 1-28 • **Input Buffer Delays**

Table 1-35 • **Worst-Case Commercial Conditions**
V_{DDP} = 3.0 V, V_{DD} = 2.3 V, T_J = 70°C

Macro Type	Description	Max. t_{INYH}[1]		Max. t_{INYL}[2]		Units
		Std.	–F	Std.	–F	
IB33	3.3 V, CMOS Input Levels[3], No Pull-up Resistor	0.4	0.5	0.6	0.7	ns
IB33S	3.3 V, CMOS Input Levels[3], No Pull-up Resistor, Schmitt Trigger	0.6	0.7	0.8	0.9	ns

Notes:

1. *t_{INYH} = Input Pad-to-Y High*
2. *t_{INYL} = Input Pad-to-Y Low*
3. *LVTTL delays are the same as CMOS delays.*
4. *For LP Macros, V_{DDP}=2.3 V for delays.*
5. *All –F parts are only available as commercial.*

Table 1-36 • **Worst-Case Commercial Conditions**
V_{DDP} = 2.3 V, V_{DD} = 2.3 V, T_J = 70°C

Macro Type	Description	Max. t_{INYH}[1]		Max. t_{INYL}[2]		Units
		Std.	–F	Std.	–F	
IB25LP	2.5 V, CMOS Input Levels[3], Low Power	0.9	1.1	0.6	0.8	ns
IB25LPS	2.5 V, CMOS Input Levels[3], Low Power, Schmitt Trigger	0.7	0.9	0.9	1.1	ns

Notes:

1. *t_{INYH} = Input Pad-to-Y High*
2. *t_{INYL} = Input Pad-to-Y Low*
3. *LVTTL delays are the same as CMOS delays.*
4. *For LP Macros, V_{DDP}=2.3 V for delays.*
5. *All –F parts are only available as commercial.*

Table 1-37 • **Worst-Case Military Conditions**
V_{DDP} = 3.0V, V_{DD} = 2.3V, T_J = 125°C for Military/MIL-STD-883

Macro Type	Description	Max. t_{INYH}[1]	Max. t_{INYL}[2]	Units
		Std.	Std.	
IB33	3.3V, CMOS Input Levels[3], No Pull-up Resistor	0.5	0.6	ns
IB33S	3.3V, CMOS Input Levels[3], No Pull-up Resistor, Schmitt Trigger	0.6	0.8	ns

Notes:

1. *t_{INYH} = Input Pad-to-Y High*
2. *t_{INYL} = Input Pad-to-Y Low*
3. *LVTTL delays are the same as CMOS delays.*
4. *For LP Macros, V_{DDP}=2.3V for delays.*

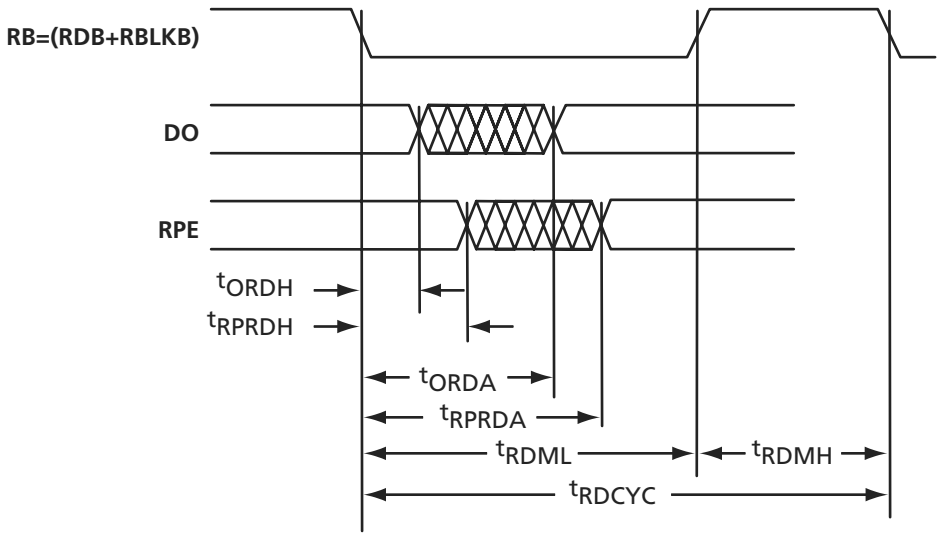
Table 1-38 • **Worst-Case Military Conditions**
V_{DDP} = 2.3V, V_{DD} = 2.3V, T_J = 125°C for Military/MIL-STD-883

Macro Type	Description	Max. t_{INYH}[1]	Max. t_{INYL}[2]	Units
		Std.	Std.	
IB25LP	2.5V, CMOS Input Levels[3], Low Power	0.9	0.7	ns
IB25LPS	2.5V, CMOS Input Levels[3], Low Power, Schmitt Trigger	0.8	1.0	ns

Notes:

1. *t_{INYH} = Input Pad-to-Y High*
2. *t_{INYL} = Input Pad-to-Y Low*
3. *LVTTL delays are the same as CMOS delays.*
4. *For LP Macros, V_{DDP}=2.3V for delays.*

Asynchronous SRAM Read, RDB Controlled



Note: *The plot shows the normal operation status.*

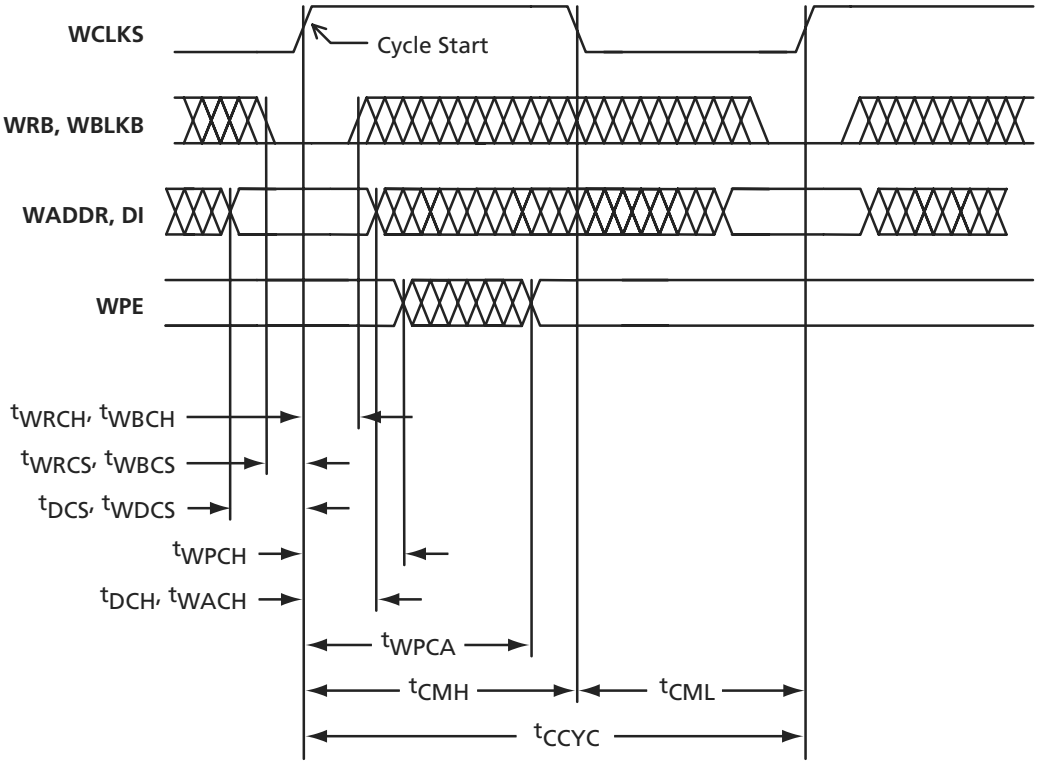
Figure 1-35 • **Asynchronous SRAM Read, RDB Controlled**

Table 1-56 • **T_J = 0°C to 110°C; V_{DD} = 2.3 V to 2.7 V for Commercial/industrial**
T_J = –55°C to 150°C, V_{DD} = 2.3 V to 2.7 V for Military/MIL-STD-883

Symbol t_{xxx}	Description	Min.	Max.	Units	Notes
ORDA	New DO access from RB ↓	7.5		ns	
ORDH	Old DO valid from RB ↓		3.0	ns	
RDCYC	Read cycle time	7.5		ns	
RDMH	RB high phase	3.0		ns	Inactive setup to new cycle
RDML	RB low phase	3.0		ns	Active
RPRDA	New RPE access from RB ↓	9.5		ns	
RPRDH	Old RPE valid from RB ↓		3.0	ns	

Note: *All –F speed grade devices are 20% slower than the standard numbers.*

Synchronous SRAM Write



Note: *The plot shows the normal operation status.*

Figure 1-36 • **Synchronous SRAM Write**

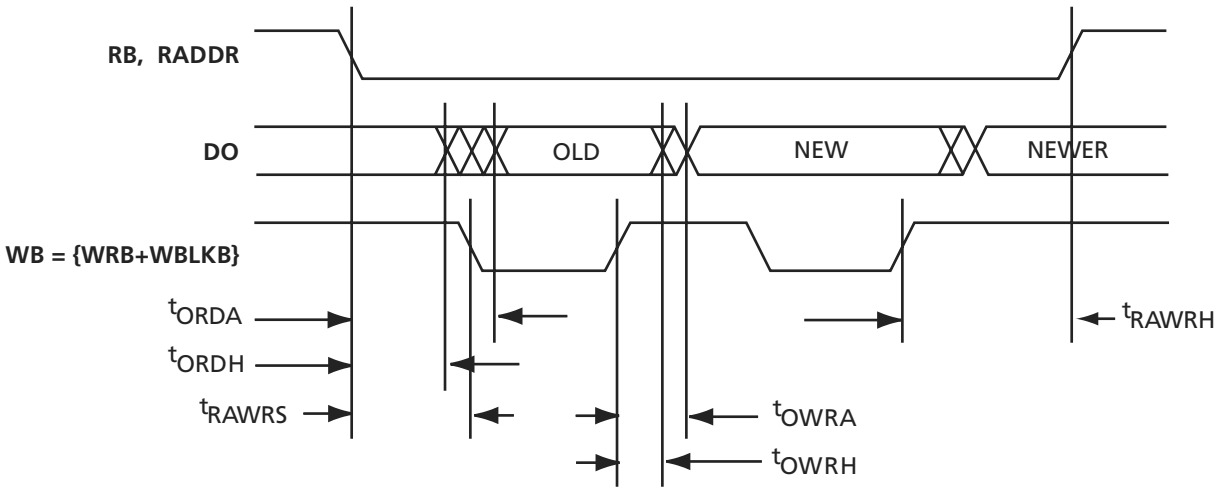
Table 1-57 • **T_J = 0°C to 110°C; V_{DD} = 2.3 V to 2.7 V for Commercial/industrial**
T_J = –55°C to 150°C, V_{DD} = 2.3 V to 2.7 V for Military/MIL-STD-883

Symbol t_{xxx}	Description	Min.	Max.	Units	Notes
CCYC	Cycle time	7.5		ns	
CMH	Clock high phase	3.0		ns	
CML	Clock low phase	3.0		ns	
DCH	DI hold from WCLKS ↑	0.5		ns	
DCS	DI setup to WCLKS ↑	1.0		ns	
WACH	WADDR hold from WCLKS ↑	0.5		ns	
WDCS	WADDR setup to WCLKS ↑	1.0		ns	
WPCA	New WPE access from WCLKS ↑	3.0		ns	WPE is invalid while PARGEN is active
WPCH	Old WPE valid from WCLKS ↑		0.5	ns	
WRCH, WBCH	WRB & WBLKB hold from WCLKS ↑	0.5		ns	
WRCS, WBCS	WRB & WBLKB setup to WCLKS ↑	1.0		ns	

Notes:

1. *On simultaneous read and write accesses to the same location, DI is output to DO.*
2. *All –F speed grade devices are 20% slower than the standard numbers.*

Asynchronous Write and Read to the Same Location



Note: *The plot shows the normal operation status.*

Figure 1-39 • **Asynchronous Write and Read to the Same Location**

Table 1-60 • **T_J = 0°C to 110°C; V_{DD} = 2.3 V to 2.7 V for Commercial/industrial**
T_J = –55°C to 150°C, V_{DD} = 2.3 V to 2.7 V for Military/MIL-STD-883

Symbol t_{xxx}	Description	Min.	Max.	Units	Notes
ORDA	New DO access from RB ↓	7.5		ns	
ORDH	Old DO valid from RB ↓		3.0	ns	
OWRA	New DO access from WB ↑	3.0		ns	
OWRH	Old DO valid from WB ↑		0.5	ns	
RAWRS	RB ↓ or RADDR from WB ↓	5.0		ns	
RAWRH	RB ↑ or RADDR from WB ↑	5.0		ns	

Notes:

1. *During an asynchronous read cycle, each write operation (synchronous or asynchronous) to the same location will automatically trigger a read operation which updates the read data. Refer to the* ProASIC^PLUS RAM and FIFO Blocks *application note for more information.*
2. *Violation or RAWRS will disturb access to the OLD data.*
3. *Violation of RAWRH will disturb access to the NEWER data.*
4. *All –F speed grade devices are 20% slower than the standard numbers.*

Asynchronous FIFO Full and Empty Transitions

The asynchronous FIFO accepts writes and reads while not full or not empty. When the FIFO is full, all writes are inhibited. Conversely, when the FIFO is empty, all reads are inhibited. A problem is created if the FIFO is written to during the transition from full to not full, or read during the transition from empty to not empty. The exact time at which the write or read operation changes from inhibited to accepted after the read (write) signal which causes the transition from full or empty to not full or not empty is indeterminate. For slow cycles, this indeterminate period starts 1 ns after the RB (WB) transition, which deactivates full or not empty and ends 3 ns after the RB (WB) transition. For fast cycles, the indeterminate period ends 3 ns (7.5 ns – RDL (WRL)) after the RB (WB) transition, whichever is later (Table 1-1 on page 1-7).

The timing diagram for write is shown in Figure 1-38 on page 1-65. The timing diagram for read is shown in Figure 1-39 on page 1-66. For basic SRAM configurations, see Table 1-14 on page 1-25. When reset is asserted, the empty flag will be asserted, the counters will reset, the outputs go to zero, but the internal RAM is not erased.

Enclosed Timing Diagrams – FIFO Mode:

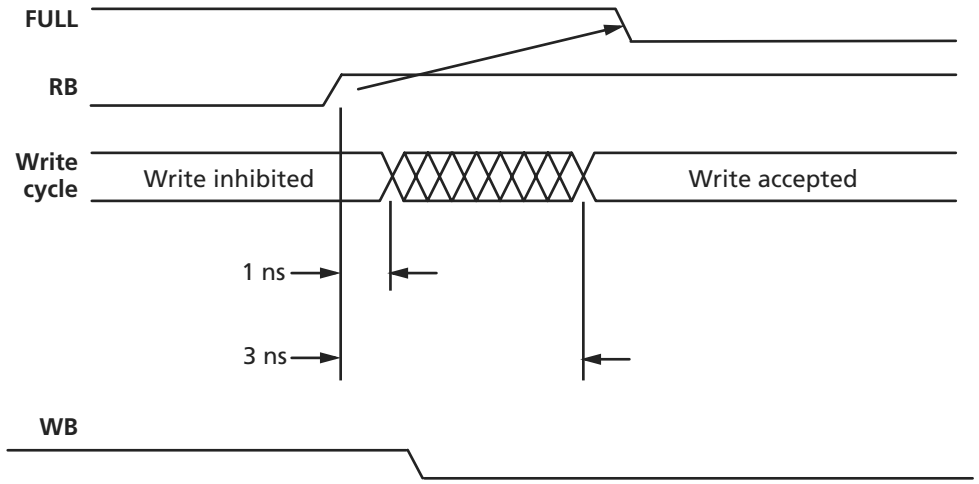
The following timing diagrams apply only to single cell; they are not applicable to cascaded cells. For more information, refer to the *ProASIC^PLUS RAM/FIFO Blocks* application note.

- "Asynchronous FIFO Read" section on page 1-70
- "Asynchronous FIFO Write" section on page 1-71
- "Synchronous FIFO Read, Access Timed Output Strobe (Synchronous Transparent)" section on page 1-72
- "Synchronous FIFO Read, Pipeline Mode Outputs (Synchronous Pipelined)" section on page 1-73
- "Synchronous FIFO Write" section on page 1-74
- "FIFO Reset" section on page 1-75

Table 1-62 • **Memory Block FIFO Interface Signals**

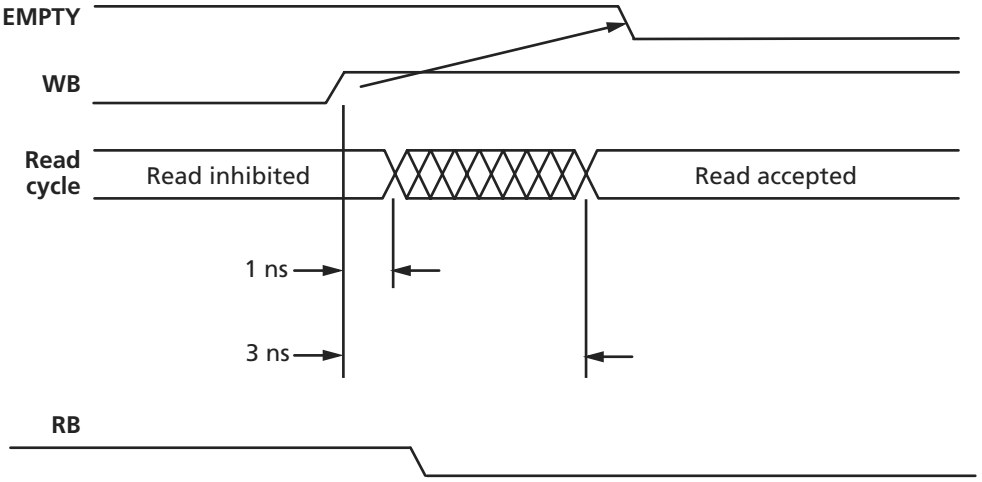
FIFO Signal	Bits	In/Out	Description
WCLKS	1	In	Write clock used for synchronization on write side
RCLKS	1	In	Read clock used for synchronization on read side
LEVEL <0:7>*	8	In	Direct configuration implements static flag logic
RBLKB	1	In	Read block select (active Low)
RDB	1	In	Read pulse (active Low)
RESET	1	In	Reset for FIFO pointers (active Low)
WBLKB	1	In	Write block select (active Low)
DI<0:8>	9	In	Input data bits <0:8>, <8> will be generated if PARGEN is true
WRB	1	In	Write pulse (active Low)
FULL, EMPTY	2	Out	FIFO flags. FULL prevents write and EMPTY prevents read
EQTH, GEQTH*	2	Out	EQTH is true when the FIFO holds the number of words specified by the LEVEL signal. GEQTH is true when the FIFO holds (LEVEL) words or more
DO<0:8>	9	Out	Output data bits <0:8>
RPE	1	Out	Read parity error (active High)
WPE	1	Out	Write parity error (active High)
LGDEP <0:2>	3	In	Configures DEPTH of the FIFO to $2^{(LGDEP+1)}$
PARODD	1	In	Selects Odd parity generation/detect when high, Even when low

Note: **LEVEL is always eight bits (0000.0000, 0000.0001). That means for values of DEPTH greater than 256, not all values will be possible, e.g. for DEPTH=512, the LEVEL can only have the values 2, 4, . . ., 512. The LEVEL signal circuit will generate signals that indicate whether the FIFO is exactly filled to the value of LEVEL (EQTH) or filled equal or higher (GEQTH) than the specified LEVEL. Since counting starts at 0, EQTH will become true when the FIFO holds (LEVEL+1) words for 512-bit FIFOs.*



Note: *All –F speed grade devices are 20% slower than the standard numbers.*

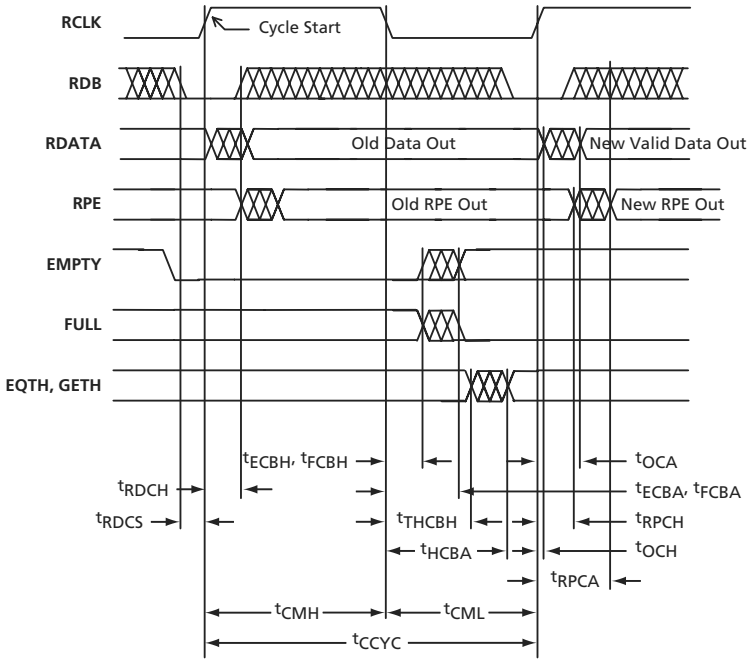
Figure 1-41 • **Write Timing Diagram**



Note: *All –F speed grade devices are 20% slower than the standard numbers.*

Figure 1-42 • **Read Timing Diagram**

Synchronous FIFO Read, Pipeline Mode Outputs (Synchronous Pipelined)



Note: *The plot shows the normal operation status.*

Figure 1-46 • **Synchronous FIFO Read, Pipeline Mode Outputs (Synchronous Pipelined)**

Table 1-66 • **T_J = 0°C to 110°C; V_{DD} = 2.3 V to 2.7 V for Commercial/industrial**
T_J = –55°C to 150°C, V_{DD} = 2.3 V to 2.7 V for Military/MIL-STD-883

Symbol t_{xxx}	Description	Min.	Max.	Units	Notes
CCYC	Cycle time	7.5		ns	
CMH	Clock high phase	3.0		ns	
CML	Clock low phase	3.0		ns	
ECBA	New EMPTY access from RCLKS ↓	3.0[1]		ns	
FCBA	FULL ↓ access from RCLKS ↓	3.0[1]		ns	
ECBH, FCBH, THCBH	Old EMPTY, FULL, EQTH, & GETH valid hold time from RCLKS ↓		1.0	ns	Empty/full/thresh are invalid from the end of hold until the new access is complete
OCA	New DO access from RCLKS ↑	2.0		ns	
OCH	Old DO valid from RCLKS ↑		0.75	ns	
RDCH	RDB hold from RCLKS ↑	0.5		ns	
RDCS	RDB setup to RCLKS ↑	1.0		ns	
RPCA	New RPE access from RCLKS ↑	4.0		ns	
RPCH	Old RPE valid from RCLKS ↑		1.0	ns	
HCBA	EQTH or GETH access from RCLKS ↓	4.5		ns	

Notes:

1. *At fast cycles, ECBA and FCBA = MAX (7.5 ns – CMS), 3.0 ns.*
2. *All –F speed grade devices are 20% slower than the standard numbers.*