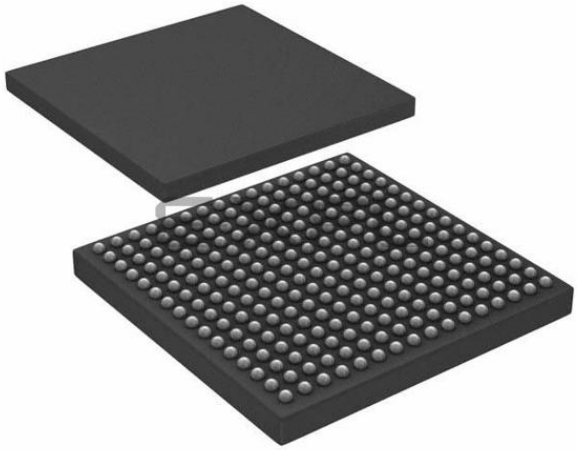


Welcome to E-XFL.COM

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	129024
Number of I/O	186
Number of Gates	600000
Voltage - Supply	2.3V ~ 2.7V
Mounting Type	Surface Mount
Operating Temperature	-55°C ~ 125°C (TC)
Package / Case	256-LBGA
Supplier Device Package	256-FPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/apa600-fg256m

Device Resources

	User I/Os[2]												
	Commercial/Industrial										Military/MIL-STD-883B		
Device	TQFP 100-Pin	TQFP 144-Pin	PQFP 208-Pin	PBGA 456-Pin	FBGA 144-Pin	FBGA 256-Pin	FBGA 484-Pin	FBGA 676-Pin	FBGA 896-Pin	FBGA 1152-Pin	CQFP 208-Pin	CQFP 352-Pin	CCGA/ LGA 624-Pin
APA075	66	107	158		100								
APA150	66		158	242	100	186 [3]							
APA300			158 [4]	290 [4]	100 [4]	186 [3, 4]					158	248	
APA450			158	344	100	186 [3]	344 [3]						
APA600			158 [4]	356 [4]		186 [3, 4]	370 [3]	454			158	248	440
APA750			158	356				454	562 [5]				
APA1000			158 [4]	356 [4]					642 [4, 5]	712 [5]	158	248	440

Notes:

1. *Package Definitions: TQFP = Thin Quad Flat Pack, PQFP = Plastic Quad Flat Pack, PBGA = Plastic Ball Grid Array, FBGA = Fine Pitch Ball Grid Array, CQFP = Ceramic Quad Flat Pack, CCGA = Ceramic Column Grid Array, LGA = Land Grid Array*
2. *Each pair of PECL I/Os is counted as one user I/O.*
3. *FG256 and FG484 are footprint-compatible packages.*
4. *Military Temperature Plastic Package Offering*
5. *FG896 and FG1152 are footprint-compatible packages.*

General Guideline

Maximum performance numbers in this datasheet are based on characterized data. Actel does not guarantee performance beyond the limits specified within the datasheet.

Table of Contents

ProASIC^PLUS Architecture

The proprietary ProASIC^PLUS architecture provides granularity comparable to gate arrays.

The ProASIC^PLUS device core consists of a Sea-of-Tiles (Figure 1-1). Each tile can be configured as a three-input logic function (e.g., NAND gate, D-Flip-Flop, etc.) by programming the appropriate Flash switch interconnections (Figure 1-2 and Figure 1-3 on page 1-3). Tiles and larger functions are connected with any of the four levels of routing hierarchy. Flash switches are distributed throughout the device to provide nonvolatile, reconfigurable interconnect programming. Flash switches are programmed to connect signal lines to the appropriate logic cell inputs and outputs. Dedicated high-performance lines are connected as needed for fast, low-skew global signal distribution throughout the core. Maximum core utilization is possible for virtually any design.

ProASIC^PLUS devices also contain embedded, two-port SRAM blocks with built-in FIFO/RAM control logic. Programming options include synchronous or asynchronous operation, two-port RAM configurations, user defined depth and width, and parity generation or checking. Please see the "Embedded Memory Configurations" section on page 1-23 for more information.

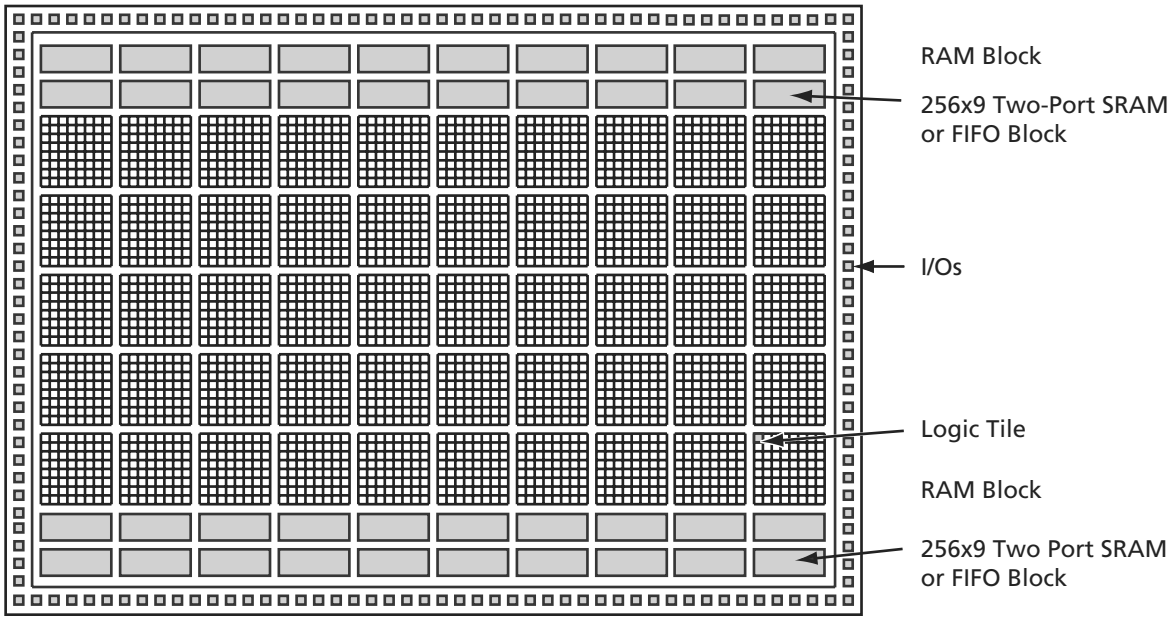


Figure 1-1 • **The ProASIC^PLUS Device Architecture**

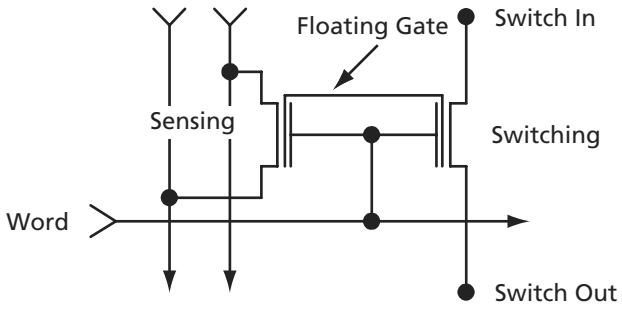
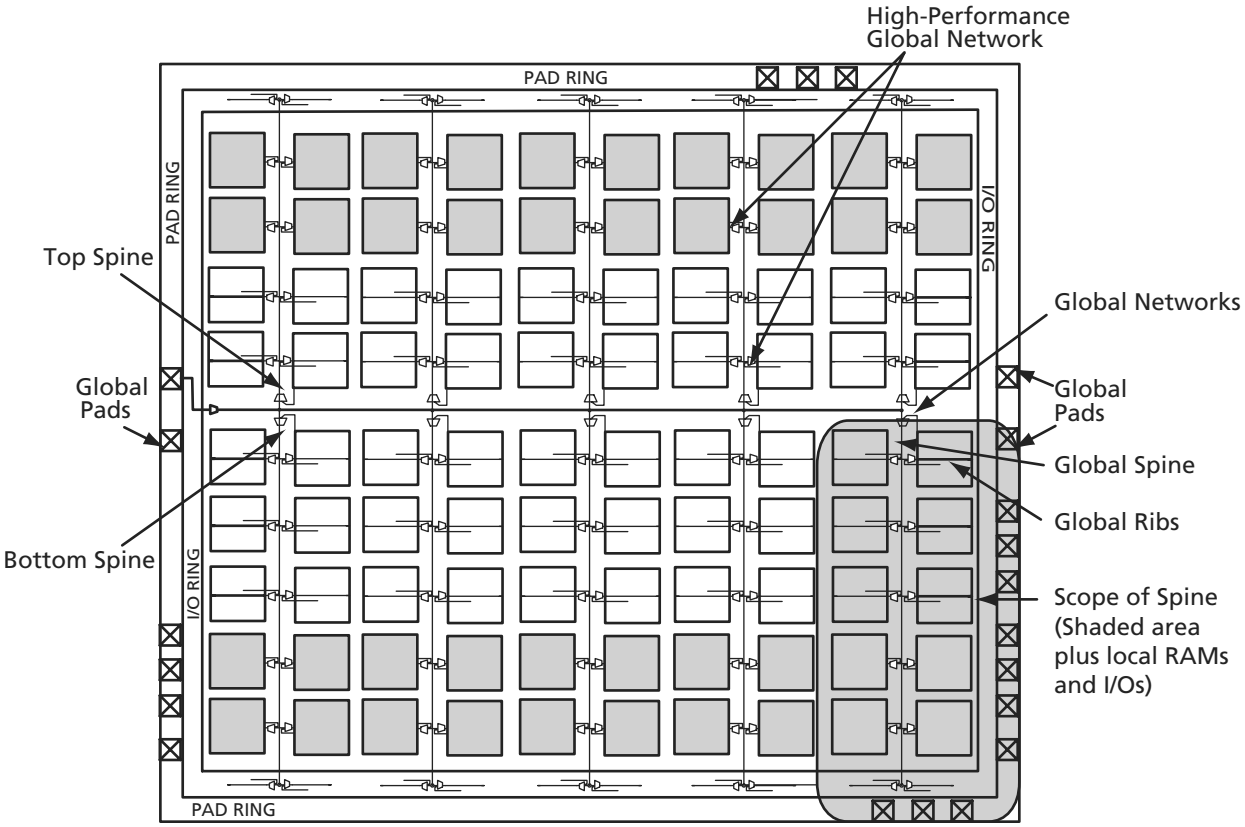


Figure 1-2 • **Flash Switch**



Note: *This figure shows routing for only one global path.*

Figure 1-7 • **High-Performance Global Network**

Table 1-1 • **Clock Spines**

	APA075	APA150	APA300	APA450	APA600	APA750	APA1000
Global Clock Networks (Trees)	4	4	4	4	4	4	4
Clock Spines/Tree	6	8	8	12	14	16	22
Total Spines	24	32	32	48	56	64	88
Top or Bottom Spine Height (Tiles)	16	24	32	32	48	64	80
Tiles in Each Top or Bottom Spine	512	768	1,024	1,024	1,536	2,048	2,560
Total Tiles	3,072	6,144	8,192	12,288	21,504	32,768	56,320

Array Coordinates

During many place-and-route operations in Actel's Designer software tool, it is possible to set constraints that require array coordinates.

Table 1-2 is provided as a reference. The array coordinates are measured from the lower left (0,0). They can be used in region constraints for specific groups of core cells, I/Os, and RAM blocks. Wild cards are also allowed.

I/O and cell coordinates are used for placement constraints. Two coordinate systems are needed because there is not a one-to-one correspondence between I/O cells and core cells. In addition, the I/O coordinate system changes depending on the die/package combination.

Core cell coordinates start at the lower left corner (represented as (1,1)) or at (1,5) if memory blocks are present at the bottom. Memory coordinates use the same system and are indicated in Table 1-2. The memory coordinates for an APA1000 are illustrated in Figure 1-8. For more information on how to use constraints, see the *Designer User's Guide* or online help for ProASIC^PLUS software tools.

Table 1-2 • **Array Coordinates**

	Logic Tile				Memory Rows		All	
	Min.		Max.		Bottom	Top		
Device	**x**	**y**	**x**	**y**	**y**	**y**	**Min.**	**Max.**
APA075	1	1	96	32	–	(33,33) or (33, 35)	0,0	97, 37
APA150	1	1	128	48	–	(49,49) or (49, 51)	0,0	129, 53
APA300	1	5	128	68	(1,1) or (1,3)	(69,69) or (69, 71)	0,0	129, 73
APA450	1	5	192	68	(1,1) or (1,3)	(69,69) or (69, 71)	0,0	193, 73
APA600	1	5	224	100	(1,1) or (1,3)	(101,101) or (101, 103)	0,0	225, 105
APA750	1	5	256	132	(1,1) or (1,3)	(133,133) or (133, 135)	0,0	257, 137
APA1000	1	5	352	164	(1,1) or (1,3)	(165,165) or (165, 167)	0,0	353, 169

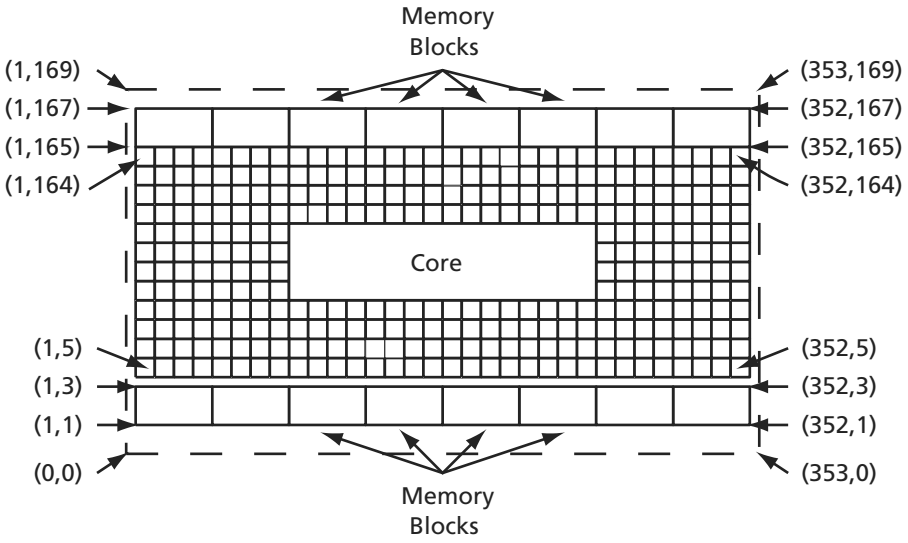


Figure 1-8 • **Core Cell Coordinates for the APA1000**

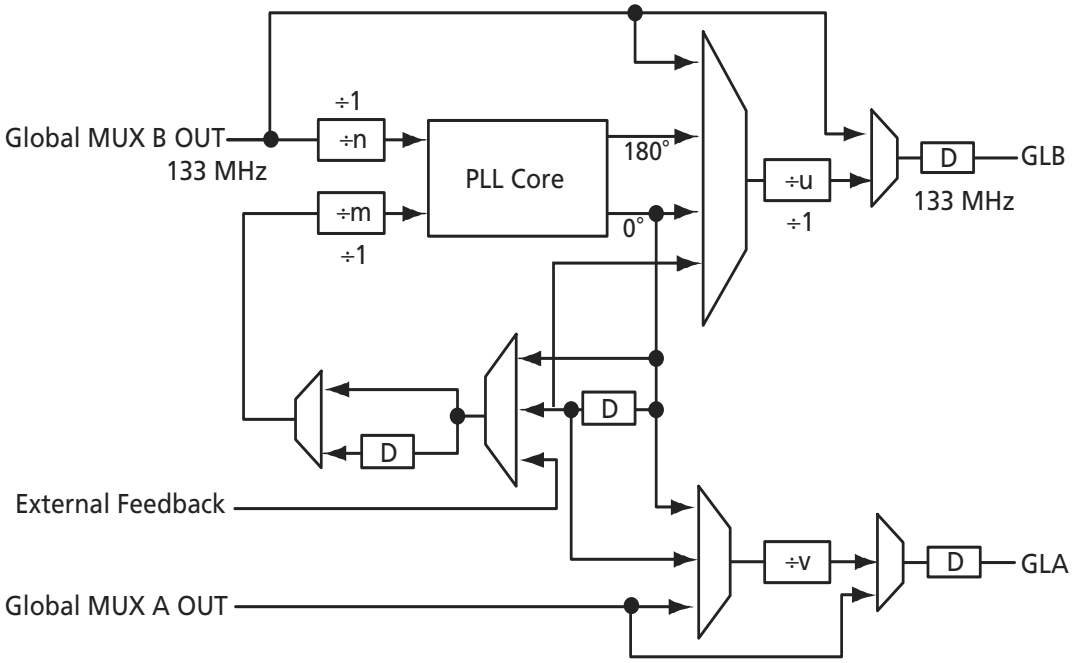


Figure 1-18 • **Using the PLL to Delay the Input Clock**

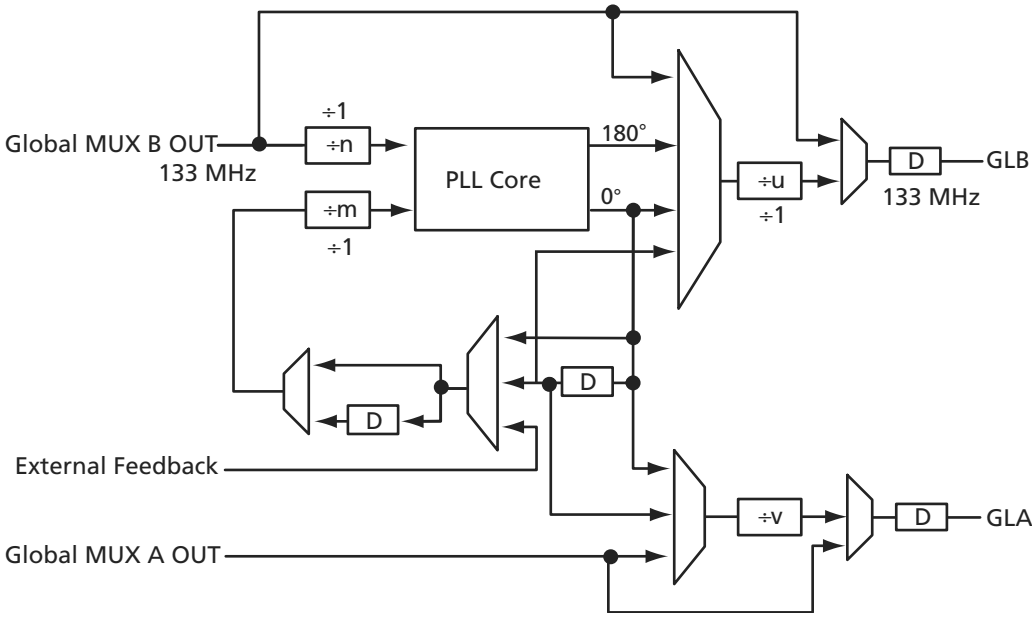


Figure 1-19 • **Using the PLL to Advance the Input Clock**

Package Thermal Characteristics

The ProASIC^PLUS family is available in several package types with a range of pin counts. Actel has selected packages based on high pin count, reliability factors, and superior thermal characteristics.

Thermal resistance defines the ability of a package to conduct heat away from the silicon, through the package to the surrounding air. Junction-to-ambient thermal resistance is measured in degrees Celsius/Watt and is represented as Theta ja (Θ_{ja}). The lower the thermal resistance, the more efficiently a package will dissipate heat.

A package's maximum allowed power (P) is a function of maximum junction temperature (T_J), maximum ambient operating temperature (T_A), and junction-to-ambient thermal resistance Θ_{ja}. Maximum junction temperature is the maximum allowable temperature on the active surface of the IC and is 110° C. P is defined as:

$$P = \frac{T_J - T_A}{\Theta_{ja}}$$

EQ 1-4

Θ_{ja} is a function of the rate (in linear feet per minute (lfpm)) of airflow in contact with the package. When the estimated power consumption exceeds the maximum allowed power, other means of cooling, such as increasing the airflow rate, must be used. The maximum power dissipation allowed for a Military temperature device is specified as a function of Θ_{jc}. The absolute maximum junction temperature is 150°C.

The calculation of the absolute maximum power dissipation allowed for a Military temperature application is illustrated in the following example for a 456-pin PBGA package:

$$\text{Maximum Power Allowed} = \frac{\text{Max. junction temp. (°C)} - \text{Max. case temp. (°C)}}{\theta_{jc}(\text{°C/W})} = \frac{150\text{°C} - 125\text{°C}}{3.0\text{°C/W}} = 8.333\text{W}$$

EQ 1-5

Table 1-16 • **Package Thermal Characteristics**

Plastic Packages	Pin Count	θ_{jc}	θ_{ja} Still Air	θ_{ja} 1.0 m/s 200 ft./min.	θ_{ja} 2.5 m/s 500 ft./min.	Units
Thin Quad Flat Pack (TQFP)	100	14.0	33.5	27.4	25.0	°C/W
Thin Quad Flat Pack (TQFP)	144	11.0	33.5	28.0	25.7	°C/W
Plastic Quad Flat Pack (PQFP)[1]	208	8.0	26.1	22.5	20.8	°C/W
PQFP with Heat spreader[2]	208	3.8	16.2	13.3	11.9	°C/W
Plastic Ball Grid Array (PBGA)	456	3.0	15.6	12.5	11.6	°C/W
Fine Pitch Ball Grid Array (FBGA)	144	3.8	26.9	22.9	21.5	°C/W
Fine Pitch Ball Grid Array (FBGA)	256	3.8	26.6	22.8	21.5	°C/W
Fine Pitch Ball Grid Array (FBGA)[3]	484	3.2	18.0	14.7	13.6	°C/W
Fine Pitch Ball Grid Array (FBGA)[4]	484	3.2	20.5	17.0	15.9	°C/W
Fine Pitch Ball Grid Array (FBGA)	676	3.2	16.4	13.0	12.0	°C/W
Fine Pitch Ball Grid Array (FBGA)	896	2.4	13.6	10.4	9.4	°C/W
Fine Pitch Ball Grid Array (FBGA)	1152	1.8	12.0	8.9	7.9	°C/W
Ceramic Quad Flat Pack (CQFP)	208	2.0	22.0	19.8	18.0	°C/W
Ceramic Quad Flat Pack (CQFP)	352	2.0	17.9	16.1	14.7	°C/W
Ceramic Column Grid Array (CCGA/LGA)	624	6.5	8.9	8.5	8.0	°C/W

Notes:

1. *Valid for the following devices irrespective of temperature grade: APA075, APA150, and APA300*
2. *Valid for the following devices irrespective of temperature grade: APA450, APA600, APA750, and APA1000*
3. *Depopulated Array*
4. *Full array*

Calculating Typical Power Dissipation

ProASIC^PLUS device power is calculated with both a static and an active component. The active component is a function of both the number of tiles utilized and the system speed. Power dissipation can be calculated using the following formula:

Total Power Consumption—P_{total}

$P_{total} = P_{dc} + P_{ac}$

where:

P_{dc} = 7 mW for the APA075
8 mW for the APA150
11 mW for the APA300
12 mW for the APA450
12 mW for the APA600
13 mW for the APA750
19 mW for the APA1000
P_{dc} includes the static components of $P_{VDDP} + P_{VDD} + P_{AVDD}$

P_{ac} = $P_{clock} + P_{storage} + P_{logic} + P_{outputs} + P_{inputs} + P_{pll} + P_{memory}$

Global Clock Contribution—P_{clock}

P_{clock}, the clock component of power dissipation, is given by the piece-wise model:

for R < 15000 the model is: (P1 + (P2*R) - (P7*R2)) * Fs (lightly-loaded clock trees)

for R > 15000 the model is: (P10 + P11*R) * Fs (heavily-loaded clock trees)

where:

P1 = 100 µW/MHz is the basic power consumption of the clock tree per MHz of the clock

P2 = 1.3 µW/MHz is the incremental power consumption of the clock tree per storage tile – also per MHz of the clock

P7 = 0.00003 µW/MHz is a correction factor for partially-loaded clock trees

P10 = 6850 µW/MHz is the basic power consumption of the clock tree per MHz of the clock

P11 = 0.4 µW/MHz is the incremental power consumption of the clock tree per storage tile – also per MHz of the clock

R = the number of storage tiles clocked by this clock

Fs = the clock frequency

Storage-Tile Contribution—$P_{storage}$

$P_{storage}$, the storage-tile (Register) component of AC power dissipation, is given by

$P_{storage} = P5 * ms * Fs$

where:

P5 = 1.1 µW/MHz is the average power consumption of a storage tile per MHz of its output toggling rate. The maximum output toggling rate is Fs/2.

ms = the number of storage tiles (Register) switching during each Fs cycle

Fs = the clock frequency

Table 1-20 • **Recommended Maximum Operating Conditions Programming and PLL Supplies**

Parameter	Condition	Commercial/Industrial/Military/MIL-STD-883		Units
		Minimum	Maximum	
V_{PP}	During Programming	15.8	16.5	V
	Normal Operation[1]	0	16.5	V
V_{PN}	During Programming	–13.8	–13.2	V
	Normal Operation[2]	–13.8	0.5	V
I_{PP}	During Programming		25	mA
I_{PN}	During Programming		10	mA
AVDD		V_{DD}	V_{DD}	V
AGND		GND	GND	V

Notes:
1. *Please refer to the "VPP Programming Supply Pin" section on page 1-77 for more information.*
2. *Please refer to the "VPN Programming Supply Pin" section on page 1-77 for more information.*

Table 1-21 • **Recommended Operating Conditions**

Parameter	Symbol	Limits		
		Commercial	Industrial	Military/MIL-STD-883
DC Supply Voltage (2.5 V I/Os)	V_{DD} and V_{DDP}	2.5 V ± 0.2 V	2.5 V ± 0.2 V	2.5 V ± 0.2 V
DC Supply Voltage (3.3 V I/Os)	V_{DDP} V_{DD}	3.3 V ± 0.3 V 2.5 V ± 0.2 V	3.3 V ± 0.3 V 2.5 V ± 0.2 V	3.3 V ± 0.3 V 2.5 V ± 0.2 V
Operating Ambient Temperature Range	T_A, T_C	0°C to 70°C	–40°C to 85°C	–55°C (T_A) to 125°C (T_C)
Maximum Operating Junction Temperature	T_J	110°C	110°C	150°C

Note: *For I/O long-term reliability, external pull-up resistors cannot be used to increase output voltage above V_{DDP}.*

Table 1-24 • **DC Electrical Specifications (V_{DDP} = 3.3 V ±0.3 V and V_{DD} = 2.5 V ±0.2 V) Applies to Military Temperature and MIL-STD-883B Temperature Only**

Symbol	Parameter	Conditions		Military/MIL-STD-883B[1] Min.	Typ.	Max.	Units
V_{OH}	Output High Voltage 3.3 V I/O, High Drive, High Slew (OB33PH) 3.3V I/O, High Drive, Normal/ Low Slew (OB33PN/OB33PL) 3.3 V I/O, Low Drive , High/ Normal/Low Slew (OB33LH/ OB33LN/OB33LL)	 I_{OH} = –8 mA I_{OH} = –16 mA I_{OH} = –3mA I_{OH} = –8mA I_{OH} = –3 mA I_{OH} = –8 mA		 0.9*V_{DDP} 2.4 0.9*V_{DDP} 2.4 0.9*V_{DDP} 2.4			V
V_{OL}	Output Low Voltage 3.3 V I/O, High Drive, High Slew (OB33PH) 3.3V I/O, High Drive, Normal/ Low Slew (OB33PN/OB33PL)) 3.3 V I/O, Low Drive, High/ Normal/Low Slew (OB33LH/ OB33LN/OB33LL)	 I_{OL} = 12 mA I_{OL} = 17 mA I_{OL} = 28 mA I_{OL} = 4 mA I_{OL} = 6 mA I_{OL} = 13 mA I_{OL} = 4 mA I_{OL} = 6 mA I_{OL} = 13 mA				 0.1V_{DDP} 0.4 0.7 0.1V_{DDP} 0.4 0.7 0.1V_{DDP} 0.4 0.7	V
V_{IH}[4]	Input High Voltage 3.3 V Schmitt Trigger Inputs 3.3 V LVTTL/LVCMOS 2.5 V Mode			1.6 2 1.7		V_{DDP} + 0.3 V_{DDP} + 0.3 V_{DDP} + 0.3	V
V_{IL}[5]	Input Low Voltage 3.3 V Schmitt Trigger Inputs 3.3 V LVTTL/LVCMOS 2.5 V Mode			–0.3 –0.3 –0.3		0.7 0.8 0.7	V
$R_{WEAKPULLUP}$	Weak Pull-up Resistance (IOB33U)	$V_{IN} \geq$ 1.5 V		7		43	kΩ
$R_{WEAKPULLUP}$	Weak Pull-up Resistance (IOB25U)	$V_{IN} \geq$ 1.5 V		7		43	kΩ
I_{IN}	Input Current	with pull up (V_{IN} = GND)		–300		–40	µA
		without pull up (V_{IN} = GND or V_{DD})		–10		10	µA
I_{DDQ}	Quiescent Supply Current (standby) Commercial	V_{IN} = GND[2] or V_{DD}	Std.		5.0	15	mA
			–F		5.0	25	mA

Notes:

1. *All process conditions. Military Temperature / MIL-STD-883 Class B: Junction Temperature: –55 to +125°C.*
2. *No pull-up resistor required.*
3. *This will not exceed 2 mA total per device.*
4. *During transitions, the input signal may overshoot to V_{DDP}+1.0 V for a limited time of no larger than 10% of the duty cycle.*
5. *During transitions, the input signal may undershoot to –1.0 V for a limited time of no larger than 10% of the duty cycle.*

Table 1-24 • **DC Electrical Specifications (V_{DDP} = 3.3 V ±0.3 V and V_{DD} = 2.5 V ±0.2 V) (Continued)**
Applies to Military Temperature and MIL-STD-883B Temperature Only

Symbol	Parameter	Conditions		Military/MIL-STD-883B[1] Min.	Typ.	Max.	Units
I_{DDQ}	Quiescent Supply Current (standby) Industrial	V_{IN} = GND[2] or V_{DD}	Std.		5.0	20	mA
I_{DDQ}	Quiescent Supply Current (standby) Military	V_{IN} = GND[2] or V_{DD}	Std.		5.0	25	mA
I_{OZ}	Tristate Output Leakage Current	V_{OH} = GND or V_{DD}	Std.	–10		10	µA
			–F[3]	–10		100	µA
I_{OSH}	Output Short Circuit Current High 3.3 V High Drive (OB33P) 3.3 V Low Drive (OB33L)	 V_{IN} = GND V_{IN} = GND		 –200 –100			
I_{OSL}	Output Short Circuit Current Low 3.3 V High Drive 3.3 V Low Drive	 V_{IN} = V_{DD} V_{IN} = V_{DD}				 200 100	
$C_{I/O}$	I/O Pad Capacitance					10	pF
C_{CLK}	Clock Input Pad Capacitance					10	pF

Notes:

1. *All process conditions. Military Temperature / MIL-STD-883 Class B: Junction Temperature: –55 to +125°C.*
2. *No pull-up resistor required.*
3. *This will not exceed 2 mA total per device.*
4. *During transitions, the input signal may overshoot to V_{DDP} +1.0 V for a limited time of no larger than 10% of the duty cycle.*
5. *During transitions, the input signal may undershoot to –1.0 V for a limited time of no larger than 10% of the duty cycle.*

Table 1-28 • **Worst-Case Commercial Conditions**
V_{DDP} = 2.3 V, V_{DD} = 2.3 V, 35 pF load, T_J = 70°C

Macro Type	Description	Max t_{DLH}[1]		Max t_{DHL}[2]		Max t_{ENZH}[3]		Max t_{ENZL}[4]		Units
		Std.	–F	Std.	–F	Std.	–F	Std.	–F	
OTB25LPLN	2.5 V, Low Power, Low Output Current, Nominal Slew Rate[5]	3.5	4.2	4.2	5.1	3.8	4.5	3.8	4.6	ns
OTB25LPLL	2.5 V, Low Power, Low Output Current, Low Slew Rate[5]	4.0	4.8	5.3	6.4	4.2	5.1	5.1	6.1	ns

Notes:

1. *t_{DLH}=Data-to-Pad High*
2. *t_{DHL}=Data-to-Pad Low*
3. *t_{ENZH}=Enable-to-Pad, Z to High*
4. *t_{ENZL} = Enable-to-Pad, Z to Low*
5. *Low power I/O work with V_{DDP}=2.5 V ±10% only. V_{DDP}=2.3 V for delays.*
6. *All –F parts are only available as commercial.*

Table 1-29 • **Worst-Case Military Conditions**
V_{DDP} = 3.0 V, V_{DD} = 2.3 V, 35 pF load, T_J = 125°C for Military/MIL-STD-883

Macro Type	Description	Max t_{DLH}[1]	Max t_{DHL}[2]	Max t_{ENZH}[3]	Max t_{ENZL}[4]	Units
		Std.	Std.	Std.	Std.	
OTB33PH	3.3 V, PCI Output Current, High Slew Rate	2.2	2.4	2.3	2.1	ns
OTB33PN	3.3 V, High Output Current, Nominal Slew Rate	2.4	3.2	2.7	2.3	ns
OTB33PL	3.3 V, High Output Current, Low Slew Rate	2.7	3.5	2.9	3.0	ns
OTB33LH	3.3 V, Low Output Current, High Slew Rate	2.7	4.3	3.0	3.1	ns
OTB33LN	3.3 V, Low Output Current, Nominal Slew Rate	3.3	4.7	3.4	4.4	ns
OTB33LL	3.3 V, Low Output Current, Low Slew Rate	3.2	6.0	3.5	5.9	ns

Notes:

1. *t_{DLH}=Data-to-Pad High*
2. *t_{DHL}=Data-to-Pad Low*
3. *t_{ENZH}=Enable-to-Pad, Z to High*
4. *t_{ENZL} = Enable-to-Pad, Z to Low*

Table 1-30 • **Worst-Case Military Conditions**
V_{DDP} = 2.3 V, V_{DD} = 2.3 V, 35 pF load, T_J = 125°C for Military/MIL-STD-883

Macro Type	Description	Max t_{DLH}[1]	Max t_{DHL}[2]	Max t_{ENZH}[3]	Max t_{ENZL}[4]	Units
		Std.	Std.	Std.	Std.	
OTB25LPHH	2.5 V, Low Power, High Output Current, High Slew Rate[5]	2.3	2.3	2.4	2.1	ns
OTB25LPHN	2.5 V, Low Power, High Output Current, Nominal Slew Rate[5]	2.7	3.2	2.8	2.1	ns
OTB25LPHL	2.5 V, Low Power, High Output Current, Low Slew Rate[5]	3.2	3.5	3.3	2.8	ns
OTB25LPLH	2.5 V, Low Power, Low Output Current, High Slew Rate[5]	3.0	5.0	3.2	2.8	ns
OTB25LPLN	2.5 V, Low Power, Low Output Current, Nominal Slew Rate[5]	3.7	4.5	4.1	4.1	ns
OTB25LPLL	2.5 V, Low Power, Low Output Current, Low Slew Rate[5]	4.4	5.8	4.4	5.4	ns

Notes:

1. *t_{DLH}=Data-to-Pad High*
2. *t_{DHL}=Data-to-Pad Low*
3. *t_{ENZH}=Enable-to-Pad, Z to High*
4. *t_{ENZL} = Enable-to-Pad, Z to Low*
5. *Low power I/O work with V_{DDP}=2.5V ±10% only. V_{DDP}=2.3V for delays.*

Input Buffer Delays

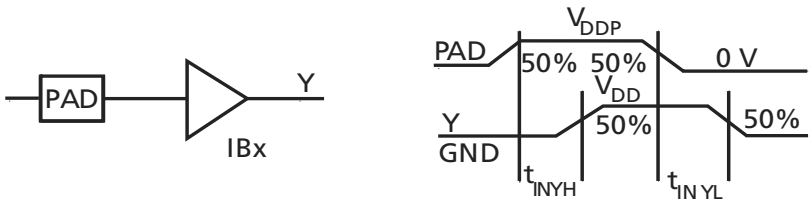


Figure 1-28 • **Input Buffer Delays**

Table 1-35 • **Worst-Case Commercial Conditions**
V_{DDP} = 3.0 V, V_{DD} = 2.3 V, T_J = 70°C

Macro Type	Description	Max. t_{INYH}[1]		Max. t_{INYL}[2]		Units
		Std.	–F	Std.	–F	
IB33	3.3 V, CMOS Input Levels[3], No Pull-up Resistor	0.4	0.5	0.6	0.7	ns
IB33S	3.3 V, CMOS Input Levels[3], No Pull-up Resistor, Schmitt Trigger	0.6	0.7	0.8	0.9	ns

Notes:

1. *t_{INYH} = Input Pad-to-Y High*
2. *t_{INYL} = Input Pad-to-Y Low*
3. *LVTTL delays are the same as CMOS delays.*
4. *For LP Macros, V_{DDP}=2.3 V for delays.*
5. *All –F parts are only available as commercial.*

Table 1-36 • **Worst-Case Commercial Conditions**
V_{DDP} = 2.3 V, V_{DD} = 2.3 V, T_J = 70°C

Macro Type	Description	Max. t_{INYH}[1]		Max. t_{INYL}[2]		Units
		Std.	–F	Std.	–F	
IB25LP	2.5 V, CMOS Input Levels[3], Low Power	0.9	1.1	0.6	0.8	ns
IB25LPS	2.5 V, CMOS Input Levels[3], Low Power, Schmitt Trigger	0.7	0.9	0.9	1.1	ns

Notes:

1. *t_{INYH} = Input Pad-to-Y High*
2. *t_{INYL} = Input Pad-to-Y Low*
3. *LVTTL delays are the same as CMOS delays.*
4. *For LP Macros, V_{DDP}=2.3 V for delays.*
5. *All –F parts are only available as commercial.*

Predicted Global Routing Delay

Table 1-43 • **Worst-Case Commercial Conditions[1]**
V_{DDP} = 3.0 V, V_{DD} = 2.3 V, T_J = 70°C

Parameter	Description	Max.		Units
		Std.	–F[2]	
t_{RCKH}	Input Low to High[3]	1.1	1.3	ns
t_{RCKL}	Input High to Low[3]	1.0	1.2	ns
t_{RCKH}	Input Low to High[4]	0.8	1.0	ns
t_{RCKL}	Input High to Low[4]	0.8	1.0	ns

Notes:

1. *The timing delay difference between tile locations is less than 15ps.*
2. *All –F parts are only available as commercial.*
3. *Highly loaded row 50%.*
4. *Minimally loaded row.*

Table 1-44 • **Worst-Case Military Conditions**
V_{DDP} = 3.0V, V_{DD} = 2.3V, T_J = 125°C for Military/MIL-STD-883

Parameter	Description	Max.	Units
t_{RCKH}	Input Low to High (high loaded row of 50%)	1.1	ns
t_{RCKL}	Input High to Low (high loaded row of 50%)	1.0	ns
t_{RCKH}	Input Low to High (minimally loaded row)	0.8	ns
t_{RCKL}	Input High to Low (minimally loaded row)	0.8	ns

Note: ** The timing delay difference between tile locations is less than 15 ps.*

Global Routing Skew

Table 1-45 • **Worst-Case Commercial Conditions**
V_{DDP} = 3.0 V, V_{DD} = 2.3 V, T_J = 70°C

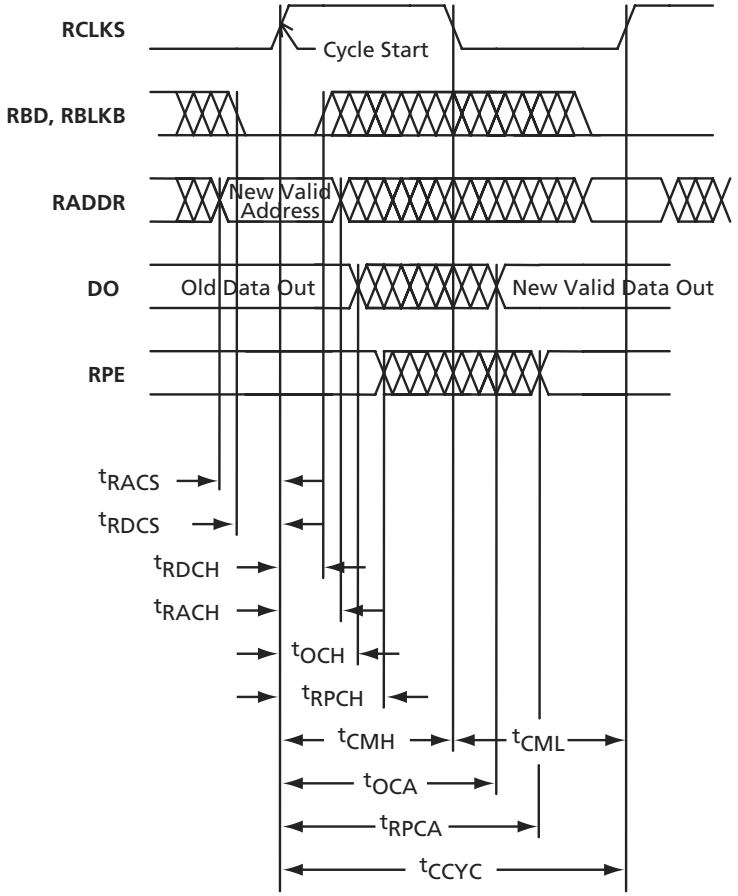
Parameter	Description	Max.		Units
		Std.	–F*	
t_{RCKSWH}	Maximum Skew Low to High	270	320	ps
t_{RCKSHH}	Maximum Skew High to Low	270	320	ps

Note: **All –F parts are only available as commercial.*

Table 1-46 • **Worst-Case Commercial Conditions**
V_{DDP} = 3.0V, V_{DD} = 2.3V, T_J = 125°C for Military/MIL-STD-883

Parameter	Description	Max.	Units
t_{RCKSWH}	Maximum Skew Low to High	270	ps
t_{RCKSHH}	Maximum Skew High to Low	270	ps

Synchronous SRAM Read, Access Timed Output Strobe (Synchronous Transparent)



Note: *The plot shows the normal operation status.*

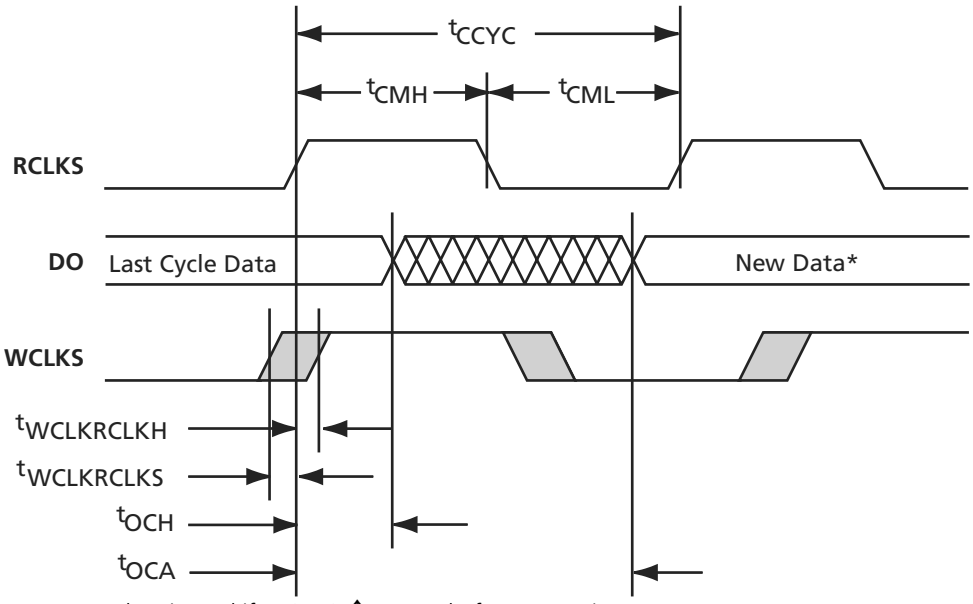
Figure 1-31 • **Synchronous SRAM Read, Access Timed Output Strobe (Synchronous Transparent)**

Table 1-52 • **T_J = 0°C to 110°C; V_{DD} = 2.3 V to 2.7 V for Commercial/industrial**
T_J = –55°C to 150°C, V_{DD} = 2.3 V to 2.7 V for Military/MIL-STD-883

Symbol t_{xxx}	Description	Min.	Max.	Units	Notes
CCYC	Cycle time	7.5		ns	
CMH	Clock high phase	3.0		ns	
CML	Clock low phase	3.0		ns	
OCA	New DO access from RCLKS ↑	7.5		ns	
OCH	Old DO valid from RCLKS ↑		3.0	ns	
RACH	RADDR hold from RCLKS ↑	0.5		ns	
RACS	RADDR setup to RCLKS ↑	1.0		ns	
RDCH	RDB hold from RCLKS ↑	0.5		ns	
RDCS	RDB setup to RCLKS ↑	1.0		ns	
RPCA	New RPE access from RCLKS ↑	9.5		ns	
RPCH	Old RPE valid from RCLKS ↑		3.0	ns	

Note: *All –F speed grade devices are 20% slower than the standard numbers.*

Synchronous Write and Read to the Same Location



Note: *The plot shows the normal operation status.*

Figure 1-37 • **Synchronous Write and Read to the Same Location**

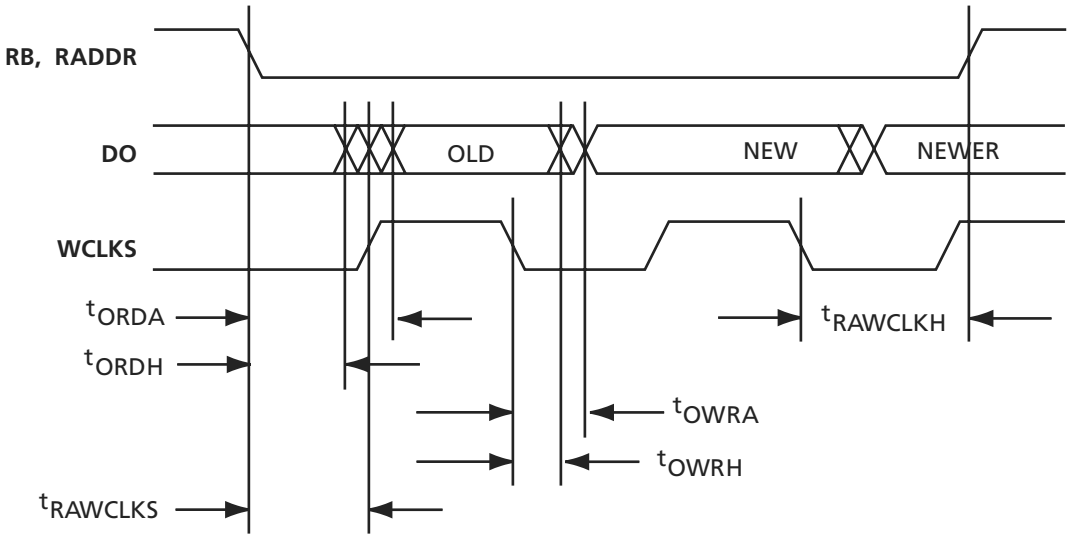
Table 1-58 • **T_J = 0°C to 110°C; V_{DD} = 2.3 V to 2.7 V for Commercial/industrial**
T_J = –55°C to 150°C, V_{DD} = 2.3 V to 2.7 V for Military/MIL-STD-883

Symbol t_{xxx}	Description	Min.	Max.	Units	Notes
CCYC	Cycle time	7.5		ns	
CMH	Clock high phase	3.0		ns	
CML	Clock low phase	3.0		ns	
WCLKRCLKS	WCLKS ↑ to RCLKS ↑ setup time	– 0.1		ns	
WCLKRCLKH	WCLKS ↑ to RCLKS ↑ hold time		7.0	ns	
OCH	Old DO valid from RCLKS ↑		3.0	ns	OCA/OCH displayed for Access Timed Output
OCA	New DO valid from RCLKS ↑	7.5		ns	

Notes:

1. *This behavior is valid for Access Timed Output and Pipelined Mode Output. The table shows the timings of an Access Timed Output.*
2. *During synchronous write and synchronous read access to the same location, the new write data will be read out if the active write clock edge occurs before or at the same time as the active read clock edge. The negative setup time insures this behavior for WCLKS and RCLKS driven by the same design signal.*
3. *If WCLKS changes after the hold time, the data will be read.*
4. *A setup or hold time violation will result in unknown output data.*
5. *All –F speed grade devices are 20% slower than the standard numbers.*

Synchronous Write and Asynchronous Read to the Same Location



Note: *The plot shows the normal operation status.*

Figure 1-40 • **Synchronous Write and Asynchronous Read to the Same Location**

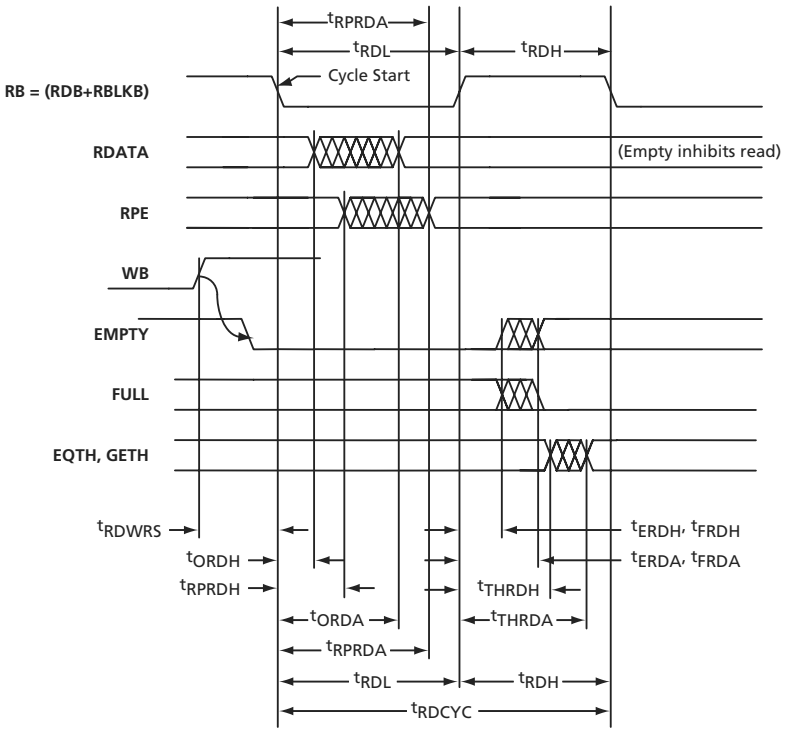
Table 1-61 • **T_J = 0°C to 110°C; V_{DD} = 2.3 V to 2.7 V for Commercial/industrial**
T_J = –55°C to 150°C, V_{DD} = 2.3 V to 2.7 V for Military/MIL-STD-883

Symbol t_{xxx}	Description	Min.	Max.	Units	Notes
ORDA	New DO access from RB ↓	7.5		ns	
ORDH	Old DO valid from RB ↓		3.0	ns	
OWRA	New DO access from WCLKS ↓	3.0		ns	
OWRH	Old DO valid from WCLKS ↓		0.5	ns	
RAWCLKS	RB ↓ or RADDR from WCLKS ↑	5.0		ns	
RAWCLKH	RB ↑ or RADDR from WCLKS ↓	5.0		ns	

Notes:

1. *During an asynchronous read cycle, each write operation (synchronous or asynchronous) to the same location will automatically trigger a read operation which updates the read data.*
2. *Violation of RAWCLKS will disturb access to OLD data.*
3. *Violation of RAWCLKH will disturb access to NEWER data.*
4. *All –F speed grade devices are 20% slower than the standard numbers.*

Asynchronous FIFO Read



Note: *The plot shows the normal operation status.*

Figure 1-43 • **Asynchronous FIFO Read**

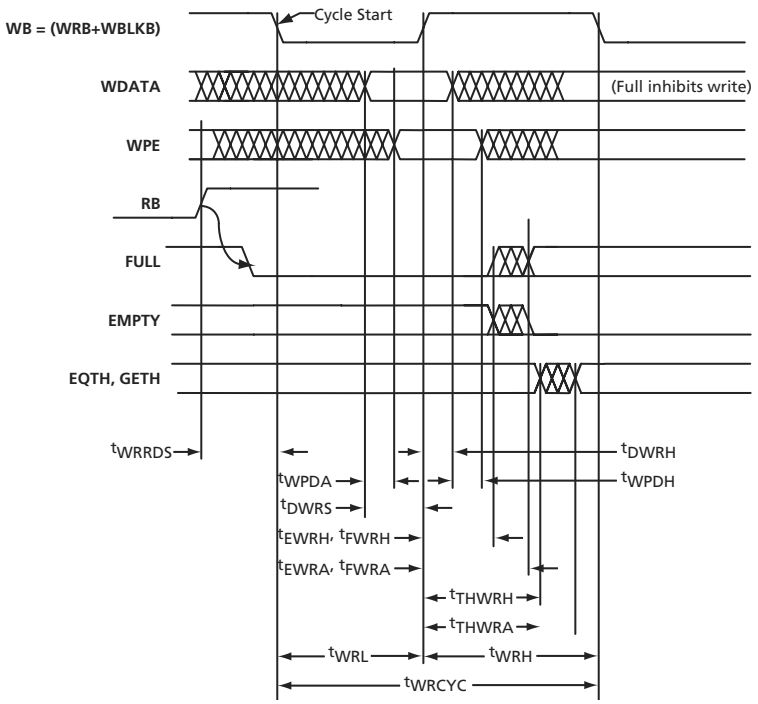
Table 1-63 • **T_J = 0°C to 110°C; V_{DD} = 2.3 V to 2.7 V for Commercial/industrial**
T_J = –55°C to 150°C, V_{DD} = 2.3 V to 2.7 V for Military/MIL-STD-883

Symbol t_{xxx}	Description	Min.	Max.	Units	Notes
ERDH, FRDH, THRDH	Old EMPTY, FULL, EQTH, & GETH valid hold time from RB ↑		0.5	ns	Empty/full/thresh are invalid from the end of hold until the new access is complete
ERDA	New EMPTY access from RB ↑	3.0[1]		ns	
FRDA	FULL↓ access from RB ↑	3.0[1]		ns	
ORDA	New DO access from RB ↓	7.5		ns	
ORDH	Old DO valid from RB ↓		3.0	ns	
RDCYC	Read cycle time	7.5		ns	
RDWRS	WB ↑, clearing EMPTY, setup to RB ↓	3.0[2]		ns	Enabling the read operation
			1.0	ns	Inhibiting the read operation
RDH	RB high phase	3.0		ns	Inactive
RDL	RB low phase	3.0		ns	Active
RPRDA	New RPE access from RB ↓	9.5		ns	
RPRDH	Old RPE valid from RB ↓		4.0	ns	
THRDA	EQTH or GETH access from RB↑	4.5		ns	

Notes:

1. *At fast cycles, ERDA and FRDA = MAX (7.5 ns – RDL), 3.0 ns.*
2. *At fast cycles, RDWRS (for enabling read) = MAX (7.5 ns – WRL), 3.0 ns.*
3. *All –F speed grade devices are 20% slower than the standard numbers.*

Asynchronous FIFO Write



Note: *The plot shows the normal operation status.*

Figure 1-44 • **Asynchronous FIFO Write**

Table 1-64 • **T_J = 0°C to 110°C; V_{DD} = 2.3 V to 2.7 V for Commercial/industrial**
T_J = –55°C to 150°C, V_{DD} = 2.3 V to 2.7 V for Military/MIL-STD-883

Symbol t_{xxx}	Description	Min.	Max.	Units	Notes
DWRH	DI hold from WB ↑	1.5		ns	
DWRS	DI setup to WB ↑	0.5		ns	PARGEN is inactive
DWRS	DI setup to WB ↑	2.5		ns	PARGEN is active
EWRH, FWRH, THWRH	Old EMPTY, FULL, EQTH, & GETH valid hold time after WB ↑		0.5	ns	Empty/full/thresh are invalid from the end of hold until the new access is complete
EWRA	EMPTY ↓ access from WB ↑	3.0[1]		ns	
FWRA	New FULL access from WB ↑	3.0[1]		ns	
THWRA	EQTH or GETH access from WB ↑	4.5		ns	
WPDA	WPE access from DI	3.0		ns	WPE is invalid while PARGEN is active
WPDH	WPE hold from DI		1.0	ns	
WRCYC	Cycle time	7.5		ns	
WRRDS	RB ↑, clearing FULL, setup to WB ↓	3.0[2]		ns	Enabling the write operation
			1.0		Inhibiting the write operation
WRH	WB high phase	3.0		ns	Inactive
WRL	WB low phase	3.0		ns	Active

Notes:

1. *At fast cycles, EWRA, FWRA = MAX (7.5 ns – WRL), 3.0 ns.*
2. *At fast cycles, WRRDS (for enabling write) = MAX (7.5 ns – RDL), 3.0 ns.*
3. *All –F speed grade devices are 20% slower than the standard numbers.*
4. *After FIFO reset, WRB needs an initial falling edge prior to any write actions.*

V_{PP} Programming Supply Pin

This pin may be connected to any voltage between GND and 16.5 V during normal operation, or it can be left unconnected.[2] For information on using this pin during programming, see the *In-System Programming ProASIC^PLUS Devices* application note. Actel recommends floating the pin or connecting it to V_{DDP}.

V_{PN} Programming Supply Pin

This pin may be connected to any voltage between 0.5V and –13.8 V during normal operation, or it can be left unconnected.[3] For information on using this pin during programming, see the *In-System Programming ProASIC^PLUS Devices* application note. Actel recommends floating the pin or connecting it to GND.

Recommended Design Practice for V_{PN}/V_{PP}

ProASIC^PLUS Devices – APA450, APA600, APA750, APA1000

Bypass capacitors are required from V_{PP} to GND and V_{PN} to GND for all ProASIC^PLUS devices during programming. During the erase cycle, ProASIC^PLUS devices may have current surges on the V_{PP} and V_{PN} power supplies. The only way to maintain the integrity of the power distribution to the ProASIC^PLUS device during these current surges is to counteract the inductance of the finite length conductors that distribute the power to the device. This can be accomplished by providing sufficient bypass capacitance between the V_{PP} and V_{PN} pins and GND (using the shortest paths possible). Without sufficient bypass capacitance to counteract the inductance, the V_{PP} and V_{PN} pins may incur a voltage spike beyond the voltage that the device can withstand. This issue applies to all programming configurations.

The solution prevents spikes from damaging the ProASIC^PLUS devices. Bypass capacitors are required for the V_{PP} and V_{PN} pads. Use a 0.01 µF to 0.1 µF ceramic capacitor with a 25 V or greater rating. To filter low-frequency noise (decoupling), use a 4.7 µF (low ESR, <1 <Ω, tantalum, 25 V or greater rating) capacitor. The capacitors should be located as close to the device pins as possible (within 2.5 cm is desirable). The smaller, high-frequency capacitor should be placed closer to the device pins than the larger low-frequency capacitor. The same dual-capacitor circuit should be used on both the V_{PP} and V_{PN} pins (Figure 1-49).

ProASIC^PLUS Devices – APA075, APA150, APA300

These devices do not require bypass capacitors on the V_{PP} and V_{PN} pins as long as the total combined distance of the programming cable and the trace length on the board is less than or equal to 30 inches. Note: For trace lengths greater than 30 inches, use the bypass capacitor recommendations in the previous section.

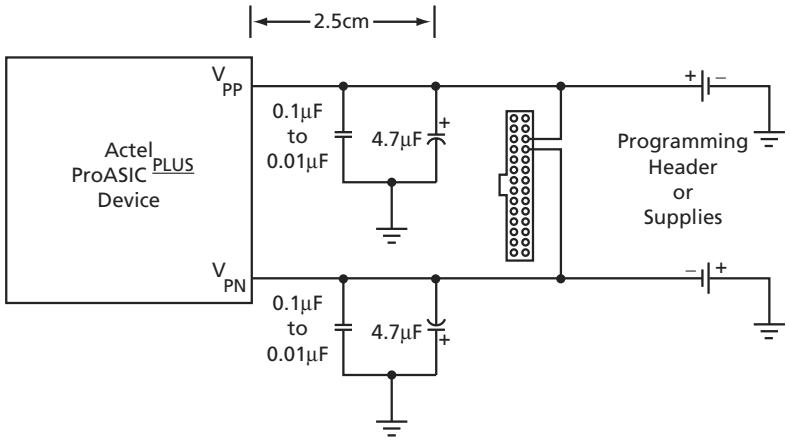


Figure 1-49 • **ProASIC^PLUS V_{PP} and V_{PN} Capacitor Requirements**

2. *There is a nominal 40 kΩ pull-up resistor on V_{PP}*
3. *There is a nominal 40 kΩ pull-down resistor on V_{PN}.*