Welcome to E-XFL.COM

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	129024
Number of I/O	186
Number of Gates	600000
Voltage - Supply	2.3V ~ 2.7V
Mounting Type	Surface Mount
Operating Temperature	-55°C ~ 125°C (TC)
Package / Case	256-LBGA
Supplier Device Package	256-FPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/apa600-fgg256m

ProASIC^PLUS Architecture

The proprietary ProASIC^PLUS architecture provides granularity comparable to gate arrays.

The ProASIC^PLUS device core consists of a Sea-of-Tiles (Figure 1-1). Each tile can be configured as a three-input logic function (e.g., NAND gate, D-Flip-Flop, etc.) by programming the appropriate Flash switch interconnections (Figure 1-2 and Figure 1-3 on page 1-3). Tiles and larger functions are connected with any of the four levels of routing hierarchy. Flash switches are distributed throughout the device to provide nonvolatile, reconfigurable interconnect programming. Flash switches are programmed to connect signal lines to the appropriate logic cell inputs and outputs. Dedicated high-performance lines are connected as needed for fast, low-skew global signal distribution throughout the core. Maximum core utilization is possible for virtually any design.

ProASIC^PLUS devices also contain embedded, two-port SRAM blocks with built-in FIFO/RAM control logic. Programming options include synchronous or asynchronous operation, two-port RAM configurations, user defined depth and width, and parity generation or checking. Please see the "Embedded Memory Configurations" section on page 1-23 for more information.

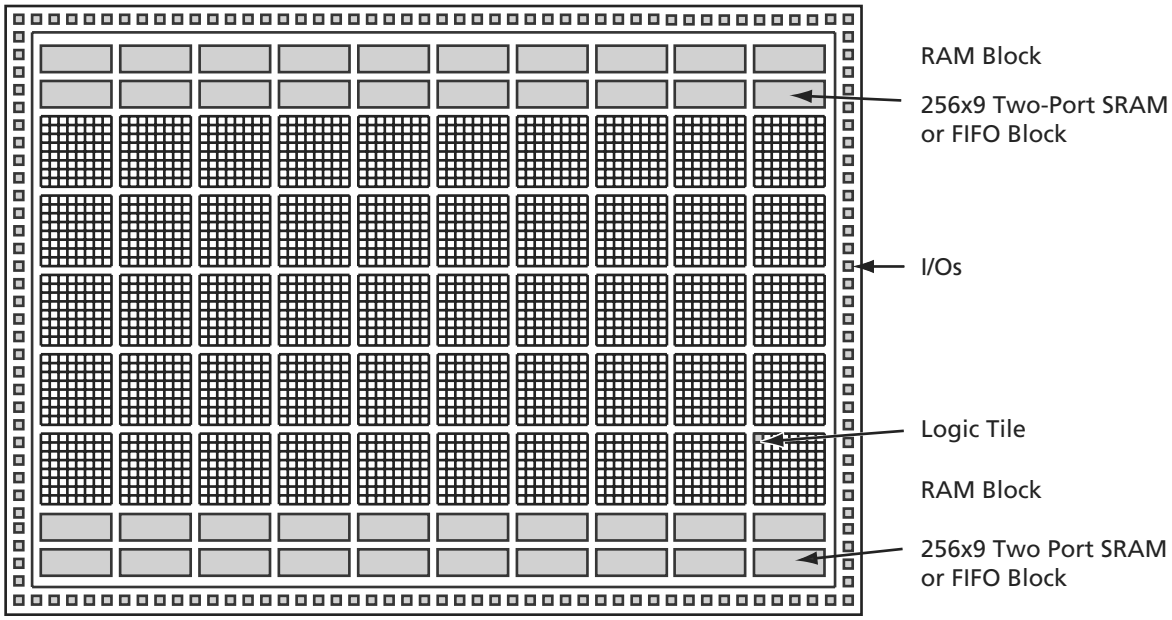


Figure 1-1 • **The ProASIC^PLUS Device Architecture**

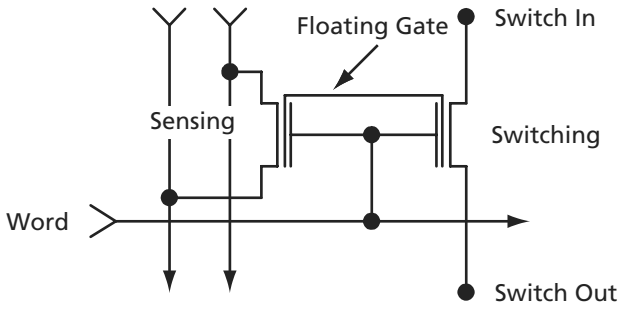


Figure 1-2 • **Flash Switch**

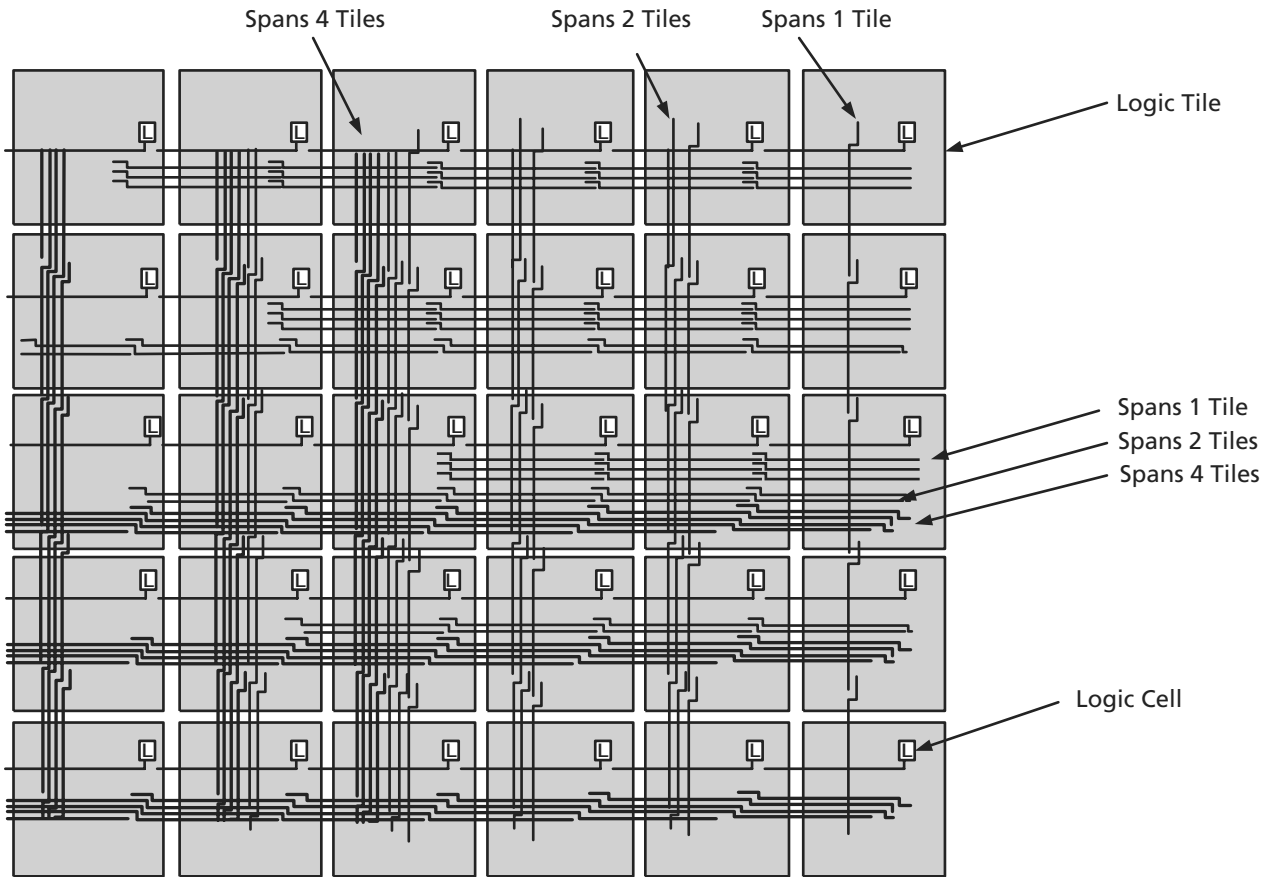


Figure 1-5 • **Efficient Long-Line Resources**

Array Coordinates

During many place-and-route operations in Actel's Designer software tool, it is possible to set constraints that require array coordinates.

Table 1-2 is provided as a reference. The array coordinates are measured from the lower left (0,0). They can be used in region constraints for specific groups of core cells, I/Os, and RAM blocks. Wild cards are also allowed.

I/O and cell coordinates are used for placement constraints. Two coordinate systems are needed because there is not a one-to-one correspondence between I/O cells and core cells. In addition, the I/O coordinate system changes depending on the die/package combination.

Core cell coordinates start at the lower left corner (represented as (1,1)) or at (1,5) if memory blocks are present at the bottom. Memory coordinates use the same system and are indicated in Table 1-2. The memory coordinates for an APA1000 are illustrated in Figure 1-8. For more information on how to use constraints, see the *Designer User's Guide* or online help for ProASIC^PLUS software tools.

Table 1-2 • **Array Coordinates**

	Logic Tile				Memory Rows		All	
	Min.		Max.		Bottom	Top		
Device	**x**	**y**	**x**	**y**	**y**	**y**	**Min.**	**Max.**
APA075	1	1	96	32	–	(33,33) or (33, 35)	0,0	97, 37
APA150	1	1	128	48	–	(49,49) or (49, 51)	0,0	129, 53
APA300	1	5	128	68	(1,1) or (1,3)	(69,69) or (69, 71)	0,0	129, 73
APA450	1	5	192	68	(1,1) or (1,3)	(69,69) or (69, 71)	0,0	193, 73
APA600	1	5	224	100	(1,1) or (1,3)	(101,101) or (101, 103)	0,0	225, 105
APA750	1	5	256	132	(1,1) or (1,3)	(133,133) or (133, 135)	0,0	257, 137
APA1000	1	5	352	164	(1,1) or (1,3)	(165,165) or (165, 167)	0,0	353, 169

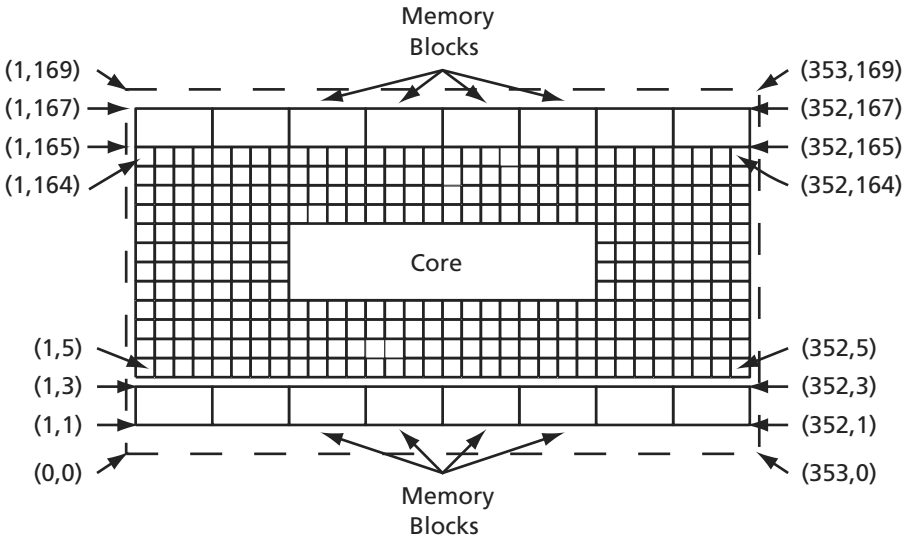


Figure 1-8 • **Core Cell Coordinates for the APA1000**

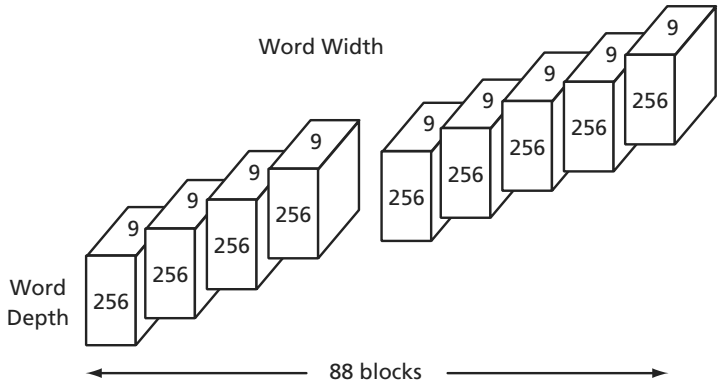


Figure 1-23 • **APA1000 Memory Block Architecture**

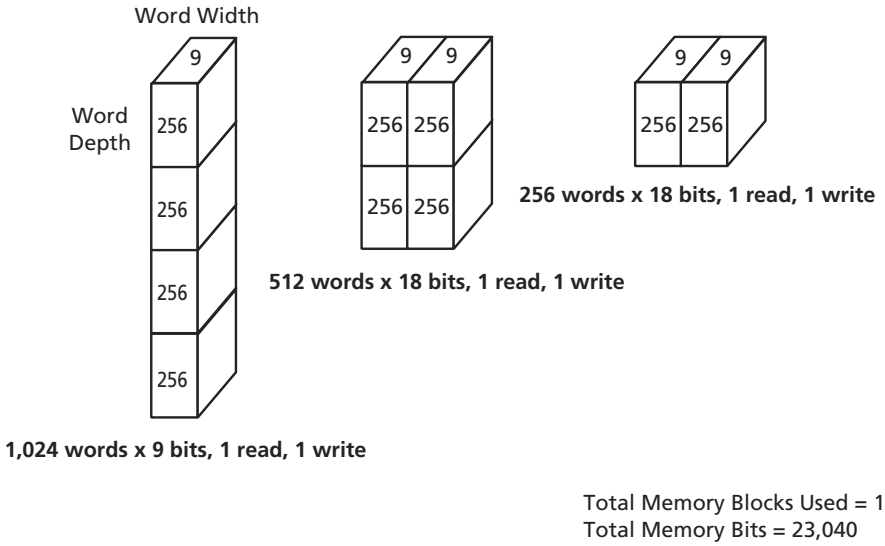


Figure 1-24 • **Example Showing Memory Arrays with Different Widths and Depths**

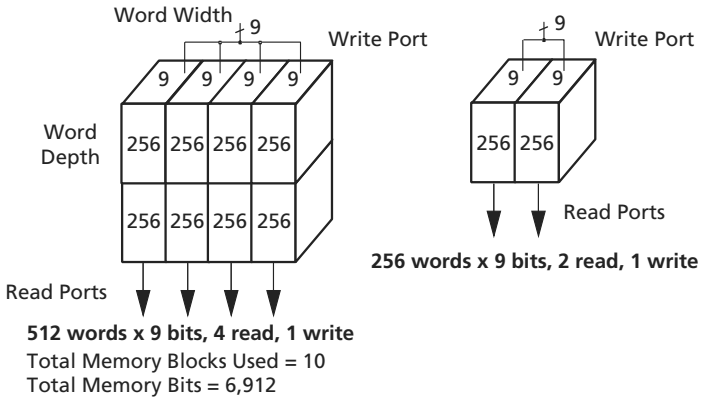


Figure 1-25 • **Multi-Port Memory Usage**

Design Environment

The ProASIC^PLUS family of FPGAs is fully supported by both Actel's Libero® Integrated Design Environment (IDE) and Designer FPGA Development software. Actel Libero IDE is an integrated design manager that seamlessly integrates design tools while guiding the user through the design flow, managing all design and log files, and passing necessary design data among tools. Additionally, Libero IDE allows users to integrate both schematic and HDL synthesis into a single flow and verify the entire design in a single environment (see Actel's website for more information about *Libero IDE*). Libero IDE includes Synplify® AE from Synplicity®, ViewDraw® AE from Mentor Graphics®, Model*Sim*® HDL Simulator from Mentor Graphics, WaveFormer Lite™ AE from SynaptiCAD®, PALACE™ AE Physical Synthesis from Magma, and Designer software from Actel.

PALACE is an effective tool when designing with ProASIC^PLUS. PALACE AE Physical Synthesis from Magma takes an EDIF netlist and optimizes the performance of ProASIC^PLUS devices through a physical placement-driven process, ensuring that timing closure is easily achieved.

Actel's Designer software is a place-and-route tool that provides a comprehensive suite of back-end support tools for FPGA development. The Designer software includes the following:

- Timer – a world-class integrated static timing analyzer and constraints editor that support timing-driven place-and-route
- NetlistViewer – a design netlist schematic viewer
- ChipPlanner – a graphical floorplanner viewer and editor
- SmartPower – allows the designer to quickly estimate the power consumption of a design
- PinEditor – a graphical application for editing pin assignments and I/O attributes
- I/O Attribute Editor – displays all assigned and unassigned I/O macros and their attributes in a spreadsheet format

With the Designer software, a user can lock the design pins before layout while minimally impacting the results of place-and-route. Additionally, Actel's back-annotation flow is compatible with all the major simulators. Another tool included in the Designer software is the SmartGen macro builder, which easily creates popular and commonly used logic functions for implementation into your schematic or HDL design.

Actel's Designer software is compatible with the most popular FPGA design entry and verification tools from EDA vendors, such as Mentor Graphics, Synplicity, Synopsys, and Cadence Design Systems. The Designer software is available for both the Windows and UNIX operating systems.

ISP

The user can generate *.bit or *.stp programming files from the Designer software and can use these files to program a device.

ProASIC^PLUS devices can be programmed in-system. For more information on ISP of ProASIC^PLUS devices, refer to the *In-System Programming ProASIC^PLUS Devices* and *Performing Internal In-System Programming Using Actel's ProASIC^PLUS Devices* application notes. Prior to being programmed for the first time, the ProASIC^PLUS device I/Os are in a tristate condition with the pull-up resistor option enabled.

Calculating Typical Power Dissipation

ProASIC^PLUS device power is calculated with both a static and an active component. The active component is a function of both the number of tiles utilized and the system speed. Power dissipation can be calculated using the following formula:

Total Power Consumption—P_{total}

$P_{total} = P_{dc} + P_{ac}$

where:

P_{dc} = 7 mW for the APA075
8 mW for the APA150
11 mW for the APA300
12 mW for the APA450
12 mW for the APA600
13 mW for the APA750
19 mW for the APA1000
P_{dc} includes the static components of $P_{VDDP} + P_{VDD} + P_{AVDD}$

P_{ac} = $P_{clock} + P_{storage} + P_{logic} + P_{outputs} + P_{inputs} + P_{pll} + P_{memory}$

Global Clock Contribution—P_{clock}

P_{clock}, the clock component of power dissipation, is given by the piece-wise model:

for R < 15000 the model is: (P1 + (P2*R) - (P7*R2)) * Fs (lightly-loaded clock trees)

for R > 15000 the model is: (P10 + P11*R) * Fs (heavily-loaded clock trees)

where:

P1 = 100 µW/MHz is the basic power consumption of the clock tree per MHz of the clock

P2 = 1.3 µW/MHz is the incremental power consumption of the clock tree per storage tile – also per MHz of the clock

P7 = 0.00003 µW/MHz is a correction factor for partially-loaded clock trees

P10 = 6850 µW/MHz is the basic power consumption of the clock tree per MHz of the clock

P11 = 0.4 µW/MHz is the incremental power consumption of the clock tree per storage tile – also per MHz of the clock

R = the number of storage tiles clocked by this clock

Fs = the clock frequency

Storage-Tile Contribution—$P_{storage}$

$P_{storage}$, the storage-tile (Register) component of AC power dissipation, is given by

$P_{storage} = P5 * ms * Fs$

where:

P5 = 1.1 µW/MHz is the average power consumption of a storage tile per MHz of its output toggling rate. The maximum output toggling rate is Fs/2.

ms = the number of storage tiles (Register) switching during each Fs cycle

Fs = the clock frequency

The following is an APA750 example using a shift register design with 13,440 storage tiles (Register) and 0 logic tiles. This design has one clock at 10 MHz, and 24 outputs toggling at 5 MHz. We then calculate the various components as follows:

P_{clock}

Fs = 10 MHz

R = 13,440

=> $P_{clock} = (P1 + (P2*R) - (P7*R^2)) * Fs = 121.5$ mW

$P_{storage}$

ms = 13,440 (in a shift register 100% of storage tiles are toggling at each clock cycle and Fs = 10 MHz)

=> $P_{storage} = P5 * ms * Fs = 147.8$ mW

P_{logic}

mc = 0 (no logic tiles in this shift register)

=> $P_{logic} = 0$ mW

$P_{outputs}$

C_{load} = 40 pF

V_{DDP} = 3.3 V

p = 24

Fp = 5 MHz

=> $P_{outputs} = (P4 + (C_{load} * V_{DDP}^2)) * p * Fp = 91.4$ mW

P_{inputs}

q = 1

Fq = 10 MHz

=> $P_{inputs} = P8 * q * Fq = 0.3$ mW

P_{memory}

N_{memory} = 0 (no RAM/FIFO blocks in this shift register)

=> $P_{memory} = 0$ mW

P_{ac}

=> 361 mW

P_{total}

$P_{dc} + P_{ac} = 374$ mW (typical)

Table 1-22 • **DC Electrical Specifications (V_{DDP} = 2.5 V ±0.2V)**

Symbol	Parameter	Conditions		Commercial/Industrial/ Military/MIL-STD-883[1, 2] Min.	Typ.	Max.	Units
V_{OH}	Output High Voltage						
	High Drive (OB25LPH)	I_{OH} = –6 mA		2.1			
		I_{OH} = –12 mA		2.0			
		I_{OH} = –24 mA		1.7			V
	Low Drive (OB25LPL)	I_{OH} = –3 mA		2.1			
		I_{OH} = –6 mA		1.9			
		I_{OH} = –8 mA		1.7			
V_{OL}	Output Low Voltage						
	High Drive (OB25LPH)	I_{OL} = 8 mA				0.2	
		I_{OL} = 15 mA				0.4	
		I_{OL} = 24 mA				0.7	V
	Low Drive (OB25LPL)	I_{OL} = 4 mA				0.2	
		I_{OL} = 8 mA				0.4	
		I_{OL} = 15 mA				0.7	
V_{IH}[6]	Input High Voltage			1.7		V_{DDP} + 0.3	V
V_{IL}[7]	Input Low Voltage			–0.3		0.7	V
$R_{WEAKPULLUP}$	Weak Pull-up Resistance (OTB25LPU)	$V_{IN} \geq$ 1.25 V		6		56	kΩ
HYST	Input Hysteresis Schmitt	See Table 1-4 on page 1-9		0.3	0.35	0.45	V
I_{IN}	Input Current	with pull up (V_{IN} = GND)		–240		– 20	µA
		without pull up (V_{IN} = GND or V_{DD})		–10		10	µA
I_{DDQ}	Quiescent Supply Current (standby) Commercial	V_{IN} = GND[4] or V_{DD}	Std.		5.0	15	mA
			–F[3]		5.0	25	mA
I_{DDQ}	Quiescent Supply Current (standby) Industrial	V_{IN} = GND[4] or V_{DD}	Std.		5.0	20	mA
I_{DDQ}	Quiescent Supply Current (standby) Military/MIL-STD-883	V_{IN} = GND[4] or V_{DD}	Std.		5.0	25	mA
I_{OZ}	Tristate Output Leakage Current	V_{OH} = GND or V_{DD}	Std.	–10		10	µA
			–F[3, 5]	–10		100	µA

Notes:

1. *All process conditions. Commercial/Industrial: Junction Temperature: –40 to +110°C.*
2. *All process conditions. Military: Junction Temperature: –55 to +150°C.*
3. *All –F parts are available only as commercial.*
4. *No pull-up resistor.*
5. *This will not exceed 2 mA total per device.*
6. *During transitions, the input signal may overshoot to V_{DDP} +1.0V for a limited time of no larger than 10% of the duty cycle.*
7. *During transitions, the input signal may undershoot to -1.0V for a limited time of no larger than 10% of the duty cycle.*

Table 1-24 • **DC Electrical Specifications (V_{DDP} = 3.3 V ±0.3 V and V_{DD} = 2.5 V ±0.2 V) (Continued)**
Applies to Military Temperature and MIL-STD-883B Temperature Only

Symbol	Parameter	Conditions		Military/MIL-STD-883B[1] Min.	Typ.	Max.	Units
I_{DDQ}	Quiescent Supply Current (standby) Industrial	V_{IN} = GND[2] or V_{DD}	Std.		5.0	20	mA
I_{DDQ}	Quiescent Supply Current (standby) Military	V_{IN} = GND[2] or V_{DD}	Std.		5.0	25	mA
I_{OZ}	Tristate Output Leakage Current	V_{OH} = GND or V_{DD}	Std.	–10		10	µA
			–F[3]	–10		100	µA
I_{OSH}	Output Short Circuit Current High 3.3 V High Drive (OB33P) 3.3 V Low Drive (OB33L)	 V_{IN} = GND V_{IN} = GND		 –200 –100			
I_{OSL}	Output Short Circuit Current Low 3.3 V High Drive 3.3 V Low Drive	 V_{IN} = V_{DD} V_{IN} = V_{DD}				 200 100	
$C_{I/O}$	I/O Pad Capacitance					10	pF
C_{CLK}	Clock Input Pad Capacitance					10	pF

Notes:

1. *All process conditions. Military Temperature / MIL-STD-883 Class B: Junction Temperature: –55 to +125°C.*
2. *No pull-up resistor required.*
3. *This will not exceed 2 mA total per device.*
4. *During transitions, the input signal may overshoot to V_{DDP} +1.0 V for a limited time of no larger than 10% of the duty cycle.*
5. *During transitions, the input signal may undershoot to –1.0 V for a limited time of no larger than 10% of the duty cycle.*

Table 1-28 • **Worst-Case Commercial Conditions**
V_{DDP} = 2.3 V, V_{DD} = 2.3 V, 35 pF load, T_J = 70°C

Macro Type	Description	Max t_{DLH}[1]		Max t_{DHL}[2]		Max t_{ENZH}[3]		Max t_{ENZL}[4]		Units
		Std.	–F	Std.	–F	Std.	–F	Std.	–F	
OTB25LPLN	2.5 V, Low Power, Low Output Current, Nominal Slew Rate[5]	3.5	4.2	4.2	5.1	3.8	4.5	3.8	4.6	ns
OTB25LPLL	2.5 V, Low Power, Low Output Current, Low Slew Rate[5]	4.0	4.8	5.3	6.4	4.2	5.1	5.1	6.1	ns

Notes:

1. *t_{DLH}=Data-to-Pad High*
2. *t_{DHL}=Data-to-Pad Low*
3. *t_{ENZH}=Enable-to-Pad, Z to High*
4. *t_{ENZL} = Enable-to-Pad, Z to Low*
5. *Low power I/O work with V_{DDP}=2.5 V ±10% only. V_{DDP}=2.3 V for delays.*
6. *All –F parts are only available as commercial.*

Table 1-29 • **Worst-Case Military Conditions**
V_{DDP} = 3.0 V, V_{DD} = 2.3 V, 35 pF load, T_J = 125°C for Military/MIL-STD-883

Macro Type	Description	Max t_{DLH}[1]	Max t_{DHL}[2]	Max t_{ENZH}[3]	Max t_{ENZL}[4]	Units
		Std.	Std.	Std.	Std.	
OTB33PH	3.3 V, PCI Output Current, High Slew Rate	2.2	2.4	2.3	2.1	ns
OTB33PN	3.3 V, High Output Current, Nominal Slew Rate	2.4	3.2	2.7	2.3	ns
OTB33PL	3.3 V, High Output Current, Low Slew Rate	2.7	3.5	2.9	3.0	ns
OTB33LH	3.3 V, Low Output Current, High Slew Rate	2.7	4.3	3.0	3.1	ns
OTB33LN	3.3 V, Low Output Current, Nominal Slew Rate	3.3	4.7	3.4	4.4	ns
OTB33LL	3.3 V, Low Output Current, Low Slew Rate	3.2	6.0	3.5	5.9	ns

Notes:

1. *t_{DLH}=Data-to-Pad High*
2. *t_{DHL}=Data-to-Pad Low*
3. *t_{ENZH}=Enable-to-Pad, Z to High*
4. *t_{ENZL} = Enable-to-Pad, Z to Low*

Table 1-30 • **Worst-Case Military Conditions**
V_{DDP} = 2.3 V, V_{DD} = 2.3 V, 35 pF load, T_J = 125°C for Military/MIL-STD-883

Macro Type	Description	Max t_{DLH}[1]	Max t_{DHL}[2]	Max t_{ENZH}[3]	Max t_{ENZL}[4]	Units
		Std.	Std.	Std.	Std.	
OTB25LPHH	2.5 V, Low Power, High Output Current, High Slew Rate[5]	2.3	2.3	2.4	2.1	ns
OTB25LPHN	2.5 V, Low Power, High Output Current, Nominal Slew Rate[5]	2.7	3.2	2.8	2.1	ns
OTB25LPHL	2.5 V, Low Power, High Output Current, Low Slew Rate[5]	3.2	3.5	3.3	2.8	ns
OTB25LPLH	2.5 V, Low Power, Low Output Current, High Slew Rate[5]	3.0	5.0	3.2	2.8	ns
OTB25LPLN	2.5 V, Low Power, Low Output Current, Nominal Slew Rate[5]	3.7	4.5	4.1	4.1	ns
OTB25LPLL	2.5 V, Low Power, Low Output Current, Low Slew Rate[5]	4.4	5.8	4.4	5.4	ns

Notes:

1. *t_{DLH}=Data-to-Pad High*
2. *t_{DHL}=Data-to-Pad Low*
3. *t_{ENZH}=Enable-to-Pad, Z to High*
4. *t_{ENZL} = Enable-to-Pad, Z to Low*
5. *Low power I/O work with V_{DDP}=2.5V ±10% only. V_{DDP}=2.3V for delays.*

Table 1-33 • **Worst-Case Military Conditions**
V_{DDP} = 3.0V, V_{DD} = 2.3V, 35 pF load, T_J = 125°C for Military/MIL-STD-883

Macro Type	Description	Max. t_{DLH}[1] Std.	Max. t_{DHL}[2] Std.	Units
OB33PH	3.3V, PCI Output Current, High Slew Rate	2.1	2.3	ns
OB33PN	3.3V, High Output Current, Nominal Slew Rate	2.5	3.2	ns
OB33PL	3.3V, High Output Current, Low Slew Rate	2.7	3.5	ns
OB33LH	3.3V, Low Output Current, High Slew Rate	2.7	4.3	ns
OB33LN	3.3V, Low Output Current, Nominal Slew Rate	3.3	4.7	ns
OB33LL	3.3V, Low Output Current, Low Slew Rate	3.3	6.1	ns

Notes:

1. *t_{DLH} = Data-to-Pad High*
2. *t_{DHL} = Data-to-Pad Low*

Table 1-34 • **Worst-Case Military Conditions**
V_{DDP} = 2.3 V, V_{DD} = 2.3V, 35 pF load, T_J = 125°C for Military/MIL-STD-883

Macro Type	Description	Max. t_{DLH}[1] Std.	Max. t_{DHL}[2] Std.	Units
OB25LPHH	2.5V, Low Power, High Output Current, High Slew Rate[3]	2.3	2.4	ns
OB25LPHN	2.5V, Low Power, High Output Current, Nominal Slew Rate[3]	2.7	3.3	ns
OB25LPHL	2.5V, Low Power, High Output Current, Low Slew Rate[3]	3.2	3.5	ns
OB25LPLH	2.5V, Low Power, Low Output Current, High Slew Rate[3]	3.0	5.0	ns
OB25LPLN	2.5V, Low Power, Low Output Current, Nominal Slew Rate[3]	3.9	4.6	ns
OB25LPLL	2.5V, Low Power, Low Output Current, Low Slew Rate[3]	4.3	5.7	ns

Notes:

1. *t_{DLH} = Data-to-Pad High*
2. *t_{DHL} = Data-to-Pad Low*
3. *Low power I/O work with V_{DDP}=2.5V ±10% only. V_{DDP}=2.3V for delays.*

Embedded Memory Specifications

This section discusses ProASIC^PLUS SRAM/FIFO embedded memory and its interface signals, including timing diagrams that show the relationships of signals as they pertain to single embedded memory blocks (Table 1-51). Table 1-13 on page 1-24 shows basic SRAM and FIFO configurations. Simultaneous read and write to the same location must be done with care. On such accesses the DI bus is output to the DO bus. Refer to the *ProASIC^PLUS RAM and FIFO Blocks* application note for more information.

Enclosed Timing Diagrams—SRAM Mode:

- "Synchronous SRAM Read, Access Timed Output Strobe (Synchronous Transparent)" section on page 1-58
- "Synchronous SRAM Read, Pipeline Mode Outputs (Synchronous Pipelined)" section on page 1-59
- "Asynchronous SRAM Write" section on page 1-60
- "Asynchronous SRAM Read, Address Controlled, RDB=0" section on page 1-61
- "Asynchronous SRAM Read, RDB Controlled" section on page 1-62
- "Synchronous SRAM Write"
- Embedded Memory Specifications

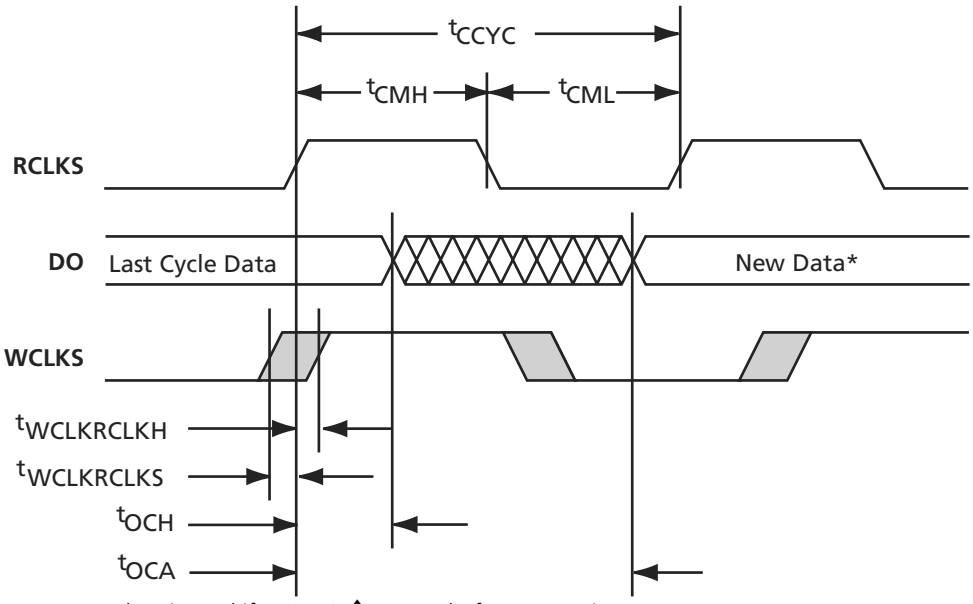
The difference between synchronous transparent and pipeline modes is the timing of all the output signals from the memory. In transparent mode, the outputs will change within the same clock cycle to reflect the data requested by the currently valid access to the memory. If clock cycles are short (high clock speed), the data requires most of the clock cycle to change to valid values (stable signals). Processing of this data in the same clock cycle is nearly impossible. Most designers add registers at all outputs of the memory to push the data processing into the next clock cycle. An entire clock cycle can then be used to process the data. To simplify use of this memory setup, suitable registers have been implemented as part of the memory primitive and are available to the user in the synchronous pipeline mode. In this mode, the output signals will change shortly after the second rising edge, following the initiation of the read access.

Table 1-51 • **Memory Block SRAM Interface Signals**

SRAM Signal	Bits	In/Out	Description
WCLKS	1	In	Write clock used on synchronization on write side
RCLKS	1	In	Read clock used on synchronization on read side
RADDR<0:7>	8	In	Read address
RBLKB	1	In	True read block select (active Low)
RDB	1	In	True read pulse (active Low)
WADDR<0:7>	8	In	Write address
WBLKB	1	In	Write block select (active Low)
DI<0:8>	9	In	Input data bits <0:8>, <8> can be used for parity In
WRB	1	In	Negative true write pulse
DO<0:8>	9	Out	Output data bits <0:8>, <8> can be used for parity Out
RPE	1	Out	Read parity error (active High)
WPE	1	Out	Write parity error (active High)
PARODD	1	In	Selects Odd parity generation/detect when high, Even when low

Note: *Not all signals shown are used in all modes.*

Synchronous Write and Read to the Same Location



Note: *The plot shows the normal operation status.*

Figure 1-37 • **Synchronous Write and Read to the Same Location**

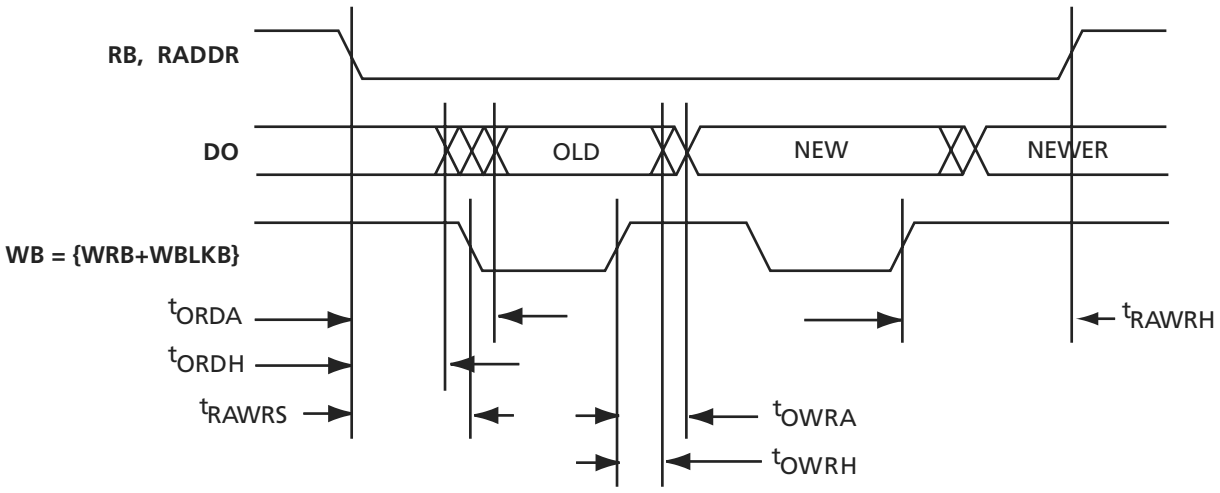
Table 1-58 • **T_J = 0°C to 110°C; V_{DD} = 2.3 V to 2.7 V for Commercial/industrial**
T_J = –55°C to 150°C, V_{DD} = 2.3 V to 2.7 V for Military/MIL-STD-883

Symbol t_{xxx}	Description	Min.	Max.	Units	Notes
CCYC	Cycle time	7.5		ns	
CMH	Clock high phase	3.0		ns	
CML	Clock low phase	3.0		ns	
WCLKRCLKS	WCLKS ↑ to RCLKS ↑ setup time	– 0.1		ns	
WCLKRCLKH	WCLKS ↑ to RCLKS ↑ hold time		7.0	ns	
OCH	Old DO valid from RCLKS ↑		3.0	ns	OCA/OCH displayed for Access Timed Output
OCA	New DO valid from RCLKS ↑	7.5		ns	

Notes:

1. *This behavior is valid for Access Timed Output and Pipelined Mode Output. The table shows the timings of an Access Timed Output.*
2. *During synchronous write and synchronous read access to the same location, the new write data will be read out if the active write clock edge occurs before or at the same time as the active read clock edge. The negative setup time insures this behavior for WCLKS and RCLKS driven by the same design signal.*
3. *If WCLKS changes after the hold time, the data will be read.*
4. *A setup or hold time violation will result in unknown output data.*
5. *All –F speed grade devices are 20% slower than the standard numbers.*

Asynchronous Write and Read to the Same Location



Note: *The plot shows the normal operation status.*

Figure 1-39 • **Asynchronous Write and Read to the Same Location**

Table 1-60 • **T_J = 0°C to 110°C; V_{DD} = 2.3 V to 2.7 V for Commercial/industrial**
T_J = –55°C to 150°C, V_{DD} = 2.3 V to 2.7 V for Military/MIL-STD-883

Symbol t_{xxx}	Description	Min.	Max.	Units	Notes
ORDA	New DO access from RB ↓	7.5		ns	
ORDH	Old DO valid from RB ↓		3.0	ns	
OWRA	New DO access from WB ↑	3.0		ns	
OWRH	Old DO valid from WB ↑		0.5	ns	
RAWRS	RB ↓ or RADDR from WB ↓	5.0		ns	
RAWRH	RB ↑ or RADDR from WB ↑	5.0		ns	

Notes:

1. *During an asynchronous read cycle, each write operation (synchronous or asynchronous) to the same location will automatically trigger a read operation which updates the read data. Refer to the* ProASIC^PLUS RAM and FIFO Blocks *application note for more information.*
2. *Violation or RAWRS will disturb access to the OLD data.*
3. *Violation of RAWRH will disturb access to the NEWER data.*
4. *All –F speed grade devices are 20% slower than the standard numbers.*

Asynchronous FIFO Full and Empty Transitions

The asynchronous FIFO accepts writes and reads while not full or not empty. When the FIFO is full, all writes are inhibited. Conversely, when the FIFO is empty, all reads are inhibited. A problem is created if the FIFO is written to during the transition from full to not full, or read during the transition from empty to not empty. The exact time at which the write or read operation changes from inhibited to accepted after the read (write) signal which causes the transition from full or empty to not full or not empty is indeterminate. For slow cycles, this indeterminate period starts 1 ns after the RB (WB) transition, which deactivates full or not empty and ends 3 ns after the RB (WB) transition. For fast cycles, the indeterminate period ends 3 ns (7.5 ns – RDL (WRL)) after the RB (WB) transition, whichever is later (Table 1-1 on page 1-7).

The timing diagram for write is shown in Figure 1-38 on page 1-65. The timing diagram for read is shown in Figure 1-39 on page 1-66. For basic SRAM configurations, see Table 1-14 on page 1-25. When reset is asserted, the empty flag will be asserted, the counters will reset, the outputs go to zero, but the internal RAM is not erased.

Enclosed Timing Diagrams – FIFO Mode:

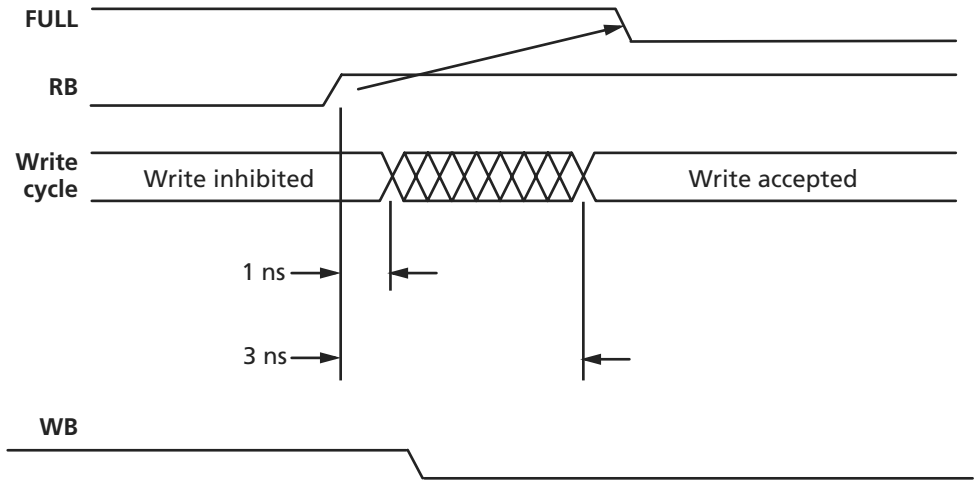
The following timing diagrams apply only to single cell; they are not applicable to cascaded cells. For more information, refer to the *ProASIC^PLUS RAM/FIFO Blocks* application note.

- "Asynchronous FIFO Read" section on page 1-70
- "Asynchronous FIFO Write" section on page 1-71
- "Synchronous FIFO Read, Access Timed Output Strobe (Synchronous Transparent)" section on page 1-72
- "Synchronous FIFO Read, Pipeline Mode Outputs (Synchronous Pipelined)" section on page 1-73
- "Synchronous FIFO Write" section on page 1-74
- "FIFO Reset" section on page 1-75

Table 1-62 • **Memory Block FIFO Interface Signals**

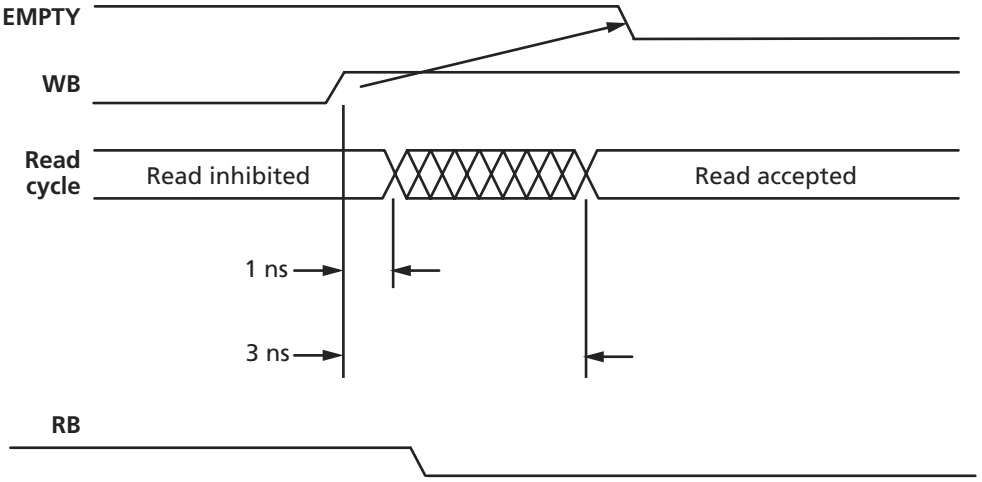
FIFO Signal	Bits	In/Out	Description
WCLKS	1	In	Write clock used for synchronization on write side
RCLKS	1	In	Read clock used for synchronization on read side
LEVEL <0:7>*	8	In	Direct configuration implements static flag logic
RBLKB	1	In	Read block select (active Low)
RDB	1	In	Read pulse (active Low)
RESET	1	In	Reset for FIFO pointers (active Low)
WBLKB	1	In	Write block select (active Low)
DI<0:8>	9	In	Input data bits <0:8>, <8> will be generated if PARGEN is true
WRB	1	In	Write pulse (active Low)
FULL, EMPTY	2	Out	FIFO flags. FULL prevents write and EMPTY prevents read
EQTH, GEQTH*	2	Out	EQTH is true when the FIFO holds the number of words specified by the LEVEL signal. GEQTH is true when the FIFO holds (LEVEL) words or more
DO<0:8>	9	Out	Output data bits <0:8>
RPE	1	Out	Read parity error (active High)
WPE	1	Out	Write parity error (active High)
LGDEP <0:2>	3	In	Configures DEPTH of the FIFO to $2^{(LGDEP+1)}$
PARODD	1	In	Selects Odd parity generation/detect when high, Even when low

Note: **LEVEL is always eight bits (0000.0000, 0000.0001). That means for values of DEPTH greater than 256, not all values will be possible, e.g. for DEPTH=512, the LEVEL can only have the values 2, 4, . . ., 512. The LEVEL signal circuit will generate signals that indicate whether the FIFO is exactly filled to the value of LEVEL (EQTH) or filled equal or higher (GEQTH) than the specified LEVEL. Since counting starts at 0, EQTH will become true when the FIFO holds (LEVEL+1) words for 512-bit FIFOs.*



Note: *All –F speed grade devices are 20% slower than the standard numbers.*

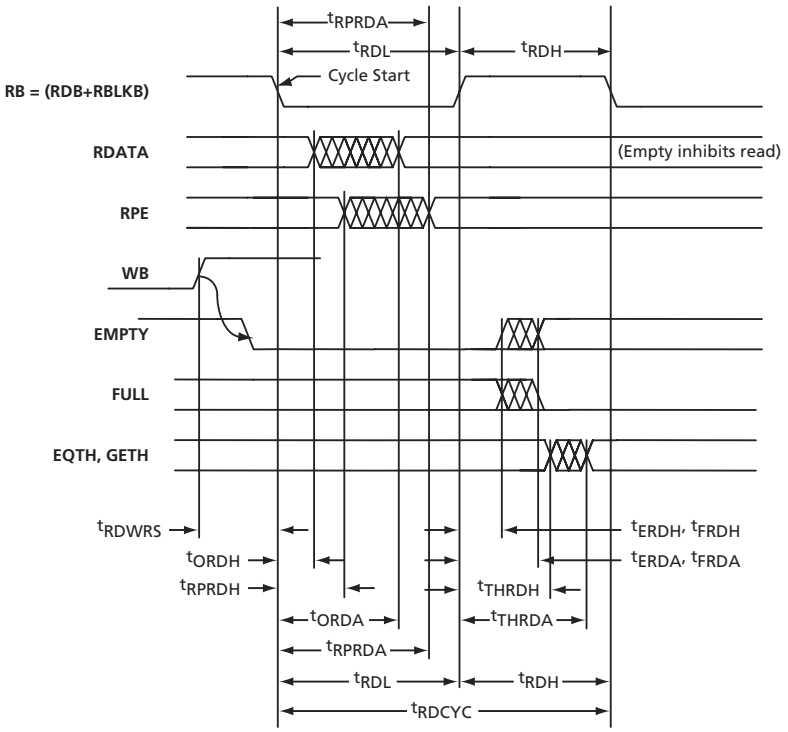
Figure 1-41 • **Write Timing Diagram**



Note: *All –F speed grade devices are 20% slower than the standard numbers.*

Figure 1-42 • **Read Timing Diagram**

Asynchronous FIFO Read



Note: *The plot shows the normal operation status.*

Figure 1-43 • **Asynchronous FIFO Read**

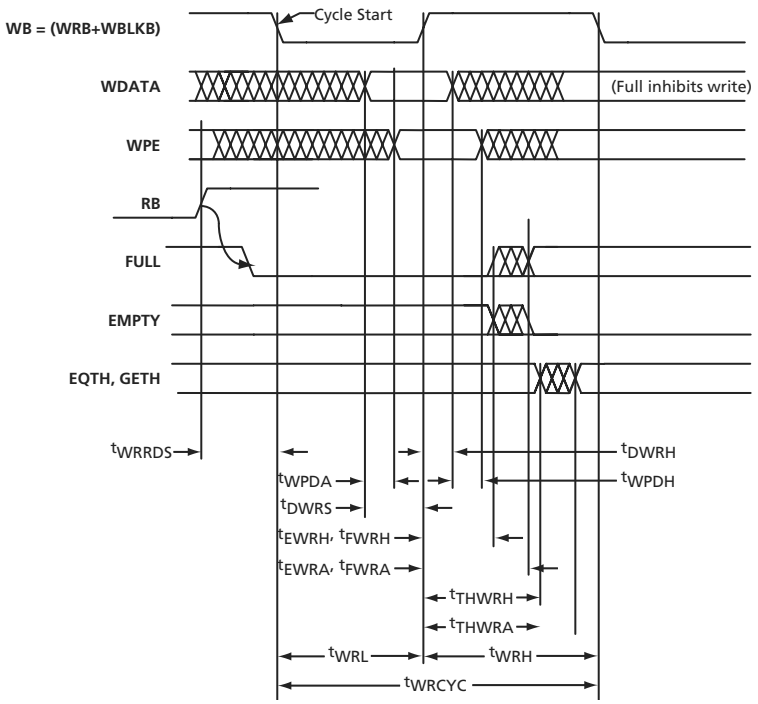
Table 1-63 • **T_J = 0°C to 110°C; V_{DD} = 2.3 V to 2.7 V for Commercial/industrial**
T_J = –55°C to 150°C, V_{DD} = 2.3 V to 2.7 V for Military/MIL-STD-883

Symbol t_{xxx}	Description	Min.	Max.	Units	Notes
ERDH, FRDH, THRDH	Old EMPTY, FULL, EQTH, & GETH valid hold time from RB ↑		0.5	ns	Empty/full/thresh are invalid from the end of hold until the new access is complete
ERDA	New EMPTY access from RB ↑	3.0[1]		ns	
FRDA	FULL↓ access from RB ↑	3.0[1]		ns	
ORDA	New DO access from RB ↓	7.5		ns	
ORDH	Old DO valid from RB ↓		3.0	ns	
RDCYC	Read cycle time	7.5		ns	
RDWRS	WB ↑, clearing EMPTY, setup to RB ↓	3.0[2]		ns	Enabling the read operation
			1.0	ns	Inhibiting the read operation
RDH	RB high phase	3.0		ns	Inactive
RDL	RB low phase	3.0		ns	Active
RPRDA	New RPE access from RB ↓	9.5		ns	
RPRDH	Old RPE valid from RB ↓		4.0	ns	
THRDA	EQTH or GETH access from RB↑	4.5		ns	

Notes:

1. *At fast cycles, ERDA and FRDA = MAX (7.5 ns – RDL), 3.0 ns.*
2. *At fast cycles, RDWRS (for enabling read) = MAX (7.5 ns – WRL), 3.0 ns.*
3. *All –F speed grade devices are 20% slower than the standard numbers.*

Asynchronous FIFO Write



Note: *The plot shows the normal operation status.*

Figure 1-44 • **Asynchronous FIFO Write**

Table 1-64 • **T_J = 0°C to 110°C; V_{DD} = 2.3 V to 2.7 V for Commercial/industrial**
T_J = –55°C to 150°C, V_{DD} = 2.3 V to 2.7 V for Military/MIL-STD-883

Symbol t_{xxx}	Description	Min.	Max.	Units	Notes
DWRH	DI hold from WB ↑	1.5		ns	
DWRS	DI setup to WB ↑	0.5		ns	PARGEN is inactive
DWRS	DI setup to WB ↑	2.5		ns	PARGEN is active
EWRH, FWRH, THWRH	Old EMPTY, FULL, EQTH, & GETH valid hold time after WB ↑		0.5	ns	Empty/full/thresh are invalid from the end of hold until the new access is complete
EWRA	EMPTY ↓ access from WB ↑	3.0[1]		ns	
FWRA	New FULL access from WB ↑	3.0[1]		ns	
THWRA	EQTH or GETH access from WB ↑	4.5		ns	
WPDA	WPE access from DI	3.0		ns	WPE is invalid while PARGEN is active
WPDH	WPE hold from DI		1.0	ns	
WRCYC	Cycle time	7.5		ns	
WRRDS	RB ↑, clearing FULL, setup to WB ↓	3.0[2]		ns	Enabling the write operation
			1.0		Inhibiting the write operation
WRH	WB high phase	3.0		ns	Inactive
WRL	WB low phase	3.0		ns	Active

Notes:

1. *At fast cycles, EWRA, FWRA = MAX (7.5 ns – WRL), 3.0 ns.*
2. *At fast cycles, WRRDS (for enabling write) = MAX (7.5 ns – RDL), 3.0 ns.*
3. *All –F speed grade devices are 20% slower than the standard numbers.*
4. *After FIFO reset, WRB needs an initial falling edge prior to any write actions.*

Pin Description

User Pins

I/O **User Input/Output**

The I/O pin functions as an input, output, tristate, or bidirectional buffer. Input and output signal levels are compatible with standard LVTTL and LVCMOS specifications. Unused I/O pins are configured as inputs with pull-up resistors.

NC **No Connect**

To maintain compatibility with other Actel ProASIC^{PLUS} products, it is recommended that this pin not be connected to the circuitry on the board.

GL **Global Pin**

Low skew input pin for clock or other global signals. This pin can be configured with an internal pull-up resistor. When it is not connected to the global network or the clock conditioning circuit, it can be configured and used as a normal I/O.

GLMX **Global Multiplexing Pin**

Low skew input pin for clock or other global signals. This pin can be used in one of two special ways (refer to Actel's *Using ProASIC^{PLUS} Clock Conditioning Circuits*).

When the external feedback option is selected for the PLL block, this pin is routed as the external feedback source to the clock conditioning circuit.

In applications where two different signals access the same global net at different times through the use of GLMXx and GLMXLx macros, this pin will be fixed as one of the source pins.

This pin can be configured with an internal pull-up resistor. When it is not connected to the global network or the clock conditioning circuit, it can be configured and used as any normal I/O. If not used, the GLMXx pin will be configured as an input with pull-up.

Dedicated Pins

GND **Ground**

Common ground supply voltage.

V_{DD} **Logic Array Power Supply Pin**

2.5 V supply voltage.

V_{DDP} **I/O Pad Power Supply Pin**

2.5 V or 3.3 V supply voltage.

TMS **Test Mode Select**

The TMS pin controls the use of boundary-scan circuitry. This pin has an internal pull-up resistor.

TCK **Test Clock**

Clock input pin for boundary scan (maximum 10 MHz). Actel recommends adding a nominal 20 kΩ pull-up resistor to this pin.

TDI **Test Data In**

Serial input for boundary scan. A dedicated pull-up resistor is included to pull this pin high when not being driven.

TDO **Test Data Out**

Serial output for boundary scan. Actel recommends adding a nominal 20kΩ pull-up resistor to this pin.

TRST **Test Reset Input**

Asynchronous, active-low input pin for resetting boundary-scan circuitry. This pin has an internal pull-up resistor. For more information, please refer to *Power-up Behavior of ProASIC^{PLUS} Devices* application note.

Special Function Pins

RCK **Running Clock**

A free running clock is needed during programming if the programmer cannot guarantee that TCK will be uninterrupted. If not used, this pin has an internal pull-up and can be left floating.

NPECL **User Negative Input**

Provides high speed clock or data signals to the PLL block. If unused, leave the pin unconnected.

PPECL **User Positive Input**

Provides high speed clock or data signals to the PLL block. If unused, leave the pin unconnected.

AVDD **PLL Power Supply**

Analog V_{DD} should be V_{DD} (core voltage) 2.5 V (nominal) and be decoupled from GND with suitable decoupling capacitors to reduce noise. For more information, refer to Actel's *Using ProASIC^{PLUS} Clock Conditioning Circuits* application note. If the clock conditioning circuitry is not used in a design, AVDD can either be left floating or tied to 2.5 V.

AGND **PLL Power Ground**

The analog ground can be connected to the system ground. For more information, refer to Actel's *Using ProASIC^{PLUS} Clock Conditioning Circuits* application note. If the PLLs or clock conditioning circuitry are not used in a design, AGND should be tied to GND.

V_{PP} Programming Supply Pin

This pin may be connected to any voltage between GND and 16.5 V during normal operation, or it can be left unconnected.[2] For information on using this pin during programming, see the *In-System Programming ProASIC^PLUS Devices* application note. Actel recommends floating the pin or connecting it to V_{DDP}.

V_{PN} Programming Supply Pin

This pin may be connected to any voltage between 0.5V and –13.8 V during normal operation, or it can be left unconnected.[3] For information on using this pin during programming, see the *In-System Programming ProASIC^PLUS Devices* application note. Actel recommends floating the pin or connecting it to GND.

Recommended Design Practice for V_{PN}/V_{PP}

ProASIC^PLUS Devices – APA450, APA600, APA750, APA1000

Bypass capacitors are required from V_{PP} to GND and V_{PN} to GND for all ProASIC^PLUS devices during programming. During the erase cycle, ProASIC^PLUS devices may have current surges on the V_{PP} and V_{PN} power supplies. The only way to maintain the integrity of the power distribution to the ProASIC^PLUS device during these current surges is to counteract the inductance of the finite length conductors that distribute the power to the device. This can be accomplished by providing sufficient bypass capacitance between the V_{PP} and V_{PN} pins and GND (using the shortest paths possible). Without sufficient bypass capacitance to counteract the inductance, the V_{PP} and V_{PN} pins may incur a voltage spike beyond the voltage that the device can withstand. This issue applies to all programming configurations.

The solution prevents spikes from damaging the ProASIC^PLUS devices. Bypass capacitors are required for the V_{PP} and V_{PN} pads. Use a 0.01 µF to 0.1 µF ceramic capacitor with a 25 V or greater rating. To filter low-frequency noise (decoupling), use a 4.7 µF (low ESR, <1 <Ω, tantalum, 25 V or greater rating) capacitor. The capacitors should be located as close to the device pins as possible (within 2.5 cm is desirable). The smaller, high-frequency capacitor should be placed closer to the device pins than the larger low-frequency capacitor. The same dual-capacitor circuit should be used on both the V_{PP} and V_{PN} pins (Figure 1-49).

ProASIC^PLUS Devices – APA075, APA150, APA300

These devices do not require bypass capacitors on the V_{PP} and V_{PN} pins as long as the total combined distance of the programming cable and the trace length on the board is less than or equal to 30 inches. Note: For trace lengths greater than 30 inches, use the bypass capacitor recommendations in the previous section.

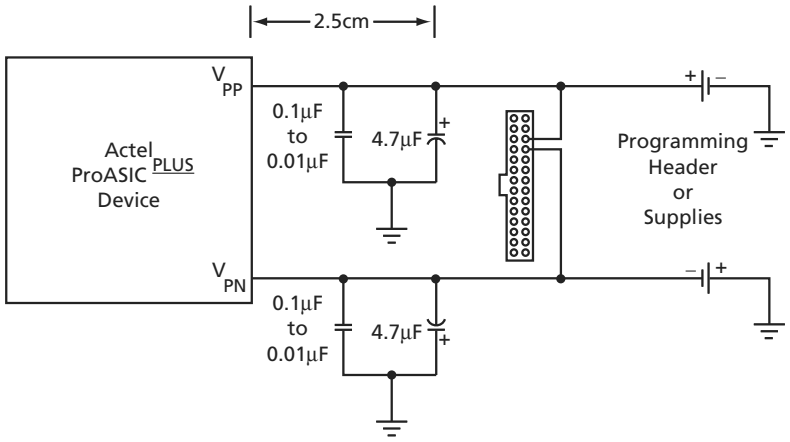


Figure 1-49 • **ProASIC^PLUS V_{PP} and V_{PN} Capacitor Requirements**

2. *There is a nominal 40 kΩ pull-up resistor on V_{PP}*
3. *There is a nominal 40 kΩ pull-down resistor on V_{PN}.*