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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	129024
Number of I/O	158
Number of Gates	600000
Voltage - Supply	2.3V ~ 2.7V
Mounting Type	Surface Mount
Operating Temperature	-55°C ~ 125°C (TC)
Package / Case	208-BFQFP
Supplier Device Package	208-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/apa600-pqg208m

Temperature Grade Offerings

Package	APA075	APA150	APA300	APA450	APA600	APA750	APA1000
TQ100	C, I	C, I					
TQ144	C, I						
PQ208	C, I	C, I	C, I, M	C, I	C, I, M	C, I	C, I, M
BG456		C, I	C, I, M	C, I	C, I, M	C, I	C, I, M
FG144	C, I	C, I	C, I, M	C, I			
FG256		C, I	C, I, M	C, I	C, I, M		
FG484				C, I	C, I, M		
FG676					C, I, M	C, I	
FG896						C, I	C, I, M
FG1152							C, I
CQ208			M, B		M, B		M, B
CQ352			M, B		M, B		M, B
CG624					M, B		M, B

Note: *C = Commercial*
I = Industrial
M = Military
B = MIL-STD-883

Speed Grade and Temperature Matrix

	–F	Std.
C	✓	✓
I		✓
M, B		✓

Note: *C = Commercial*
I = Industrial
M = Military
B = MIL-STD-883

Routing Resources

The routing structure of ProASIC^PLUS devices is designed to provide high performance through a flexible four-level hierarchy of routing resources: ultra-fast local resources, efficient long-line resources, high-speed, very long-line resources, and high performance global networks.

The ultra-fast local resources are dedicated lines that allow the output of each tile to connect directly to every input of the eight surrounding tiles (Figure 1-4).

The efficient long-line resources provide routing for longer distances and higher fanout connections. These resources vary in length (spanning 1, 2, or 4 tiles), run both vertically and horizontally, and cover the entire ProASIC^PLUS device (Figure 1-5 on page 1-5). Each tile can drive signals onto the efficient long-line resources, which can in turn access every input of every tile. Active buffers are inserted automatically by routing software to limit the loading effects due to distance and fanout.

The high-speed, very long-line resources, which span the entire device with minimal delay, are used to route very long or very high fanout nets. (Figure 1-6 on page 1-6).

The high-performance global networks are low-skew, high fanout nets that are accessible from external pins or from internal logic (Figure 1-7 on page 1-7). These nets are typically used to distribute clocks, resets, and other high fanout nets requiring a minimum skew. The global networks are implemented as clock trees, and signals can be introduced at any junction. These can be employed hierarchically with signals accessing every input on all tiles.

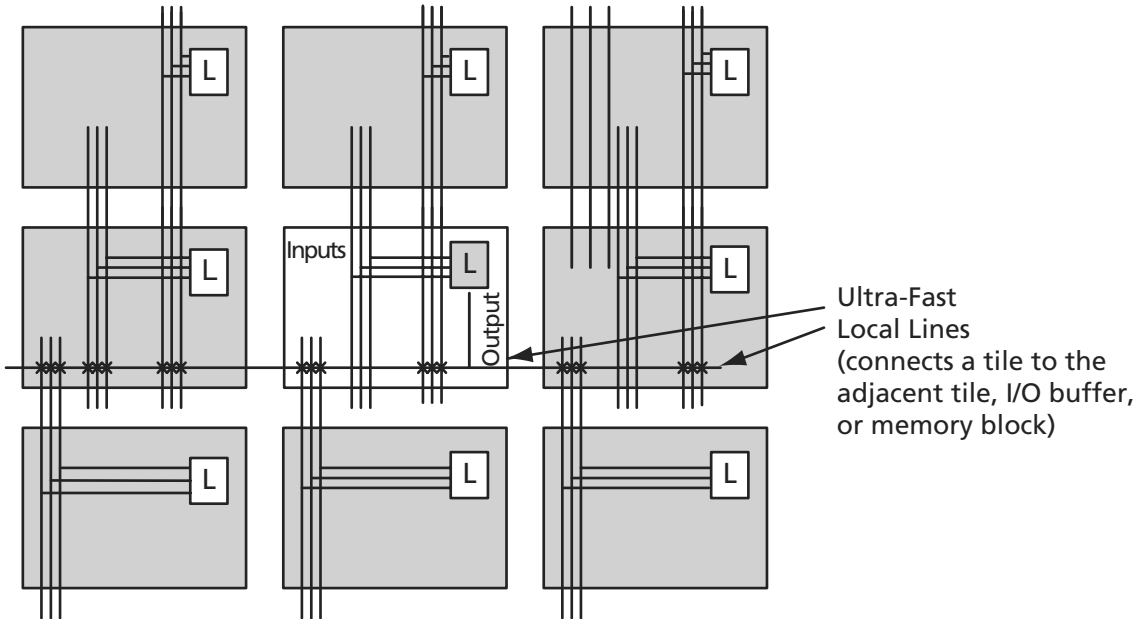


Figure 1-4 • **Ultra-Fast Local Resources**

Timing Control and Characteristics

ProASIC^PLUS Clock Management System

ProASIC^PLUS devices provide designers with very flexible clock conditioning capabilities. Each member of the ProASIC^PLUS family contains two phase-locked loop (PLL) blocks which perform the following functions:

- Clock Phase Adjustment via Programmable Delay (250 ps steps from –7 ns to +8 ns)
- Clock Skew Minimization
- Clock Frequency Synthesis

Each PLL has the following key features:

- Input Frequency Range (f_{IN}) = 1.5 to 180 MHz
- Feedback Frequency Range (f_{VCO}) = 24 to 180 MHz
- Output Frequency Range (f_{OUT}) = 8 to 180 MHz
- Output Phase Shift = 0 ° and 180 °
- Output Duty Cycle = 50%
- Low Output Jitter (max at 25°C)
  - f_{VCO} <10 MHz. Jitter ±1% or better
  - 10 MHz < f_{VCO} < 60 MHz. Jitter ±2% or better
  - f_{VCO} > 60 MHz. Jitter ±1% or better

Note: Jitter(ps) = Jitter(%)* period

For Example:

Jitter in picoseconds at 100 MHz = 0.01 * (1/100E6) = 100 ps

- Maximum Acquisition Time = 80 µs for f_{VCO} > 40 MHz
  = 30 µs for f_{VCO} < 40 MHz
- Low Power Consumption – 6.9 mW (max – analog supply) + 7.0µW/MHz (max – digital supply)

Physical Implementation

Each side of the chip contains a clock conditioning circuit based on a 180 MHz PLL block (Figure 1-14 on page 1-14). Two global multiplexed lines extend along each side of the chip to provide bidirectional access to the PLL on that side (neither MUX can be connected to the opposite side's PLL). Each global line has optional LVPECL input pads (described below). The global lines may be driven by either the LVPECL global input pad or the outputs from the PLL block, or both. Each global line can be driven by a different output from the PLL. Unused global pins can be configured as regular I/Os or left unconnected. They default to an input with pull-up. The two signals available to drive the global networks are as follows (Figure 1-15 on page 1-15, Table 1-7 on page 1-15, and Table 1-8 on page 1-16):

Global A (secondary clock)

- Output from Global MUX A
- Conditioned version of PLL output (f_{OUT}) – delayed or advanced
- Divided version of either of the above
- Further delayed version of either of the above (0.25 ns, 0.50 ns, or 4.00 ns delay)[1]

Global B

- Output from Global MUX B
- Delayed or advanced version of f_{OUT}
- Divided version of either of the above
- Further delayed version of either of the above (0.25 ns, 0.50 ns, or 4.00 ns delay)[2]

Functional Description

Each PLL block contains four programmable dividers as shown in Figure 1-14 on page 1-14. These allow frequency scaling of the input clock signal as follows:

- The n divider divides the input clock by integer factors from 1 to 32.
- The m divider in the feedback path allows multiplication of the input clock by integer factors ranging from 1 to 64.
- The two dividers together can implement any combination of multiplication and division resulting in a clock frequency between 24 and 180 MHz exiting the PLL core. This clock has a fixed 50% duty cycle.
- The output frequency of the PLL core is given by the formula EQ 1-1 (f_{REF} is the reference clock frequency):

$$f_{OUT} = f_{REF} * m/n \quad \textit{EQ 1-1}$$

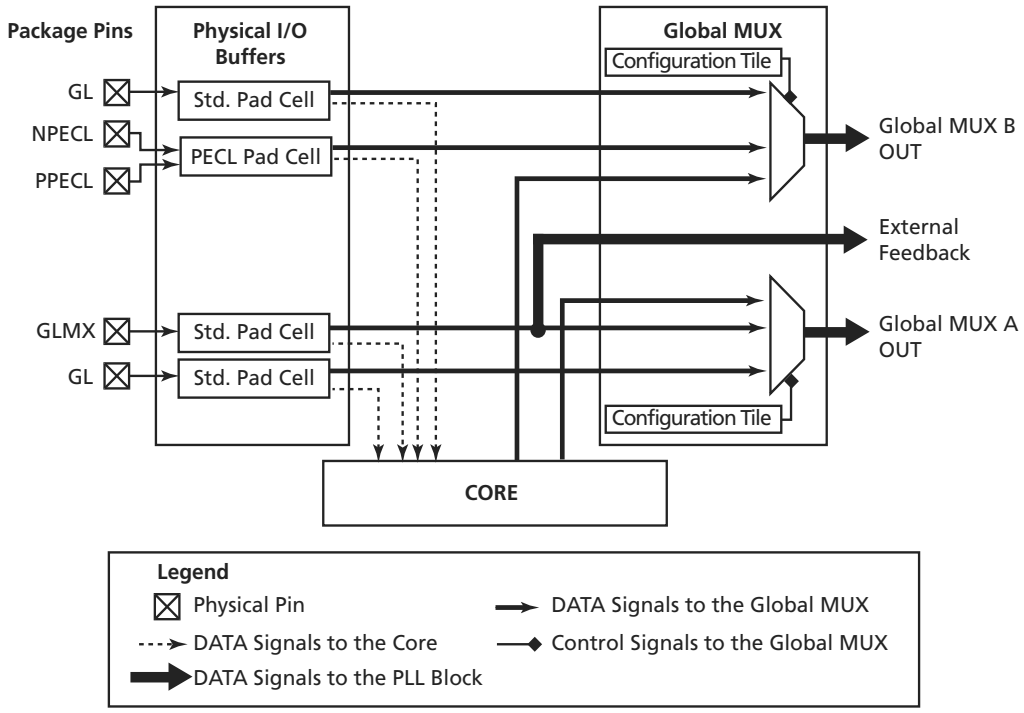
- The third and fourth dividers (u and v) permit the signals applied to the global network to each be further divided by integer factors ranging from 1 to 4.

The implementations shown in EQ2 and EQ3 enable the user to define a wide range of frequency multiplier and divisors.

$$f_{GLB} = m/(n*u) \quad \textit{EQ 1-2}$$

$$f_{GLA} = m/(n*v) \quad \textit{EQ 1-3}$$

1. This mode is available through the delay feature of the Global MUX driver.



Note: *When a signal from an I/O tile is connected to the core, it cannot be connected to the Global MUX at the same time.*

Figure 1-15 • **Input Connectors to ProASIC^PLUS Clock Conditioning Circuitry**

Table 1-7 • **Clock-Conditioning Circuitry MUX Settings**

MUX	Datapath	Comments
FBSEL		
1	Internal Feedback	
2	Internal Feedback and Advance Clock Using FBDLY	–0.25 to –4 ns in 0.25 ns increments
3	External Feedback (EXTFB)	
XDLYSEL		
0	Feedback Unchanged	
1	Deskew feedback by advancing clock by system delay	Fixed delay of -2.95 ns
OBMUX	**GLB**	
0	Primary bypass, no divider	
1	Primary bypass, use divider	
2	Delay Clock Using FBDLY	+0.25 to +4 ns in 0.25 ns increments
4	Phase Shift Clock by 0°	
5	Reserved	
6	Phase Shift Clock by +180°	
7	Reserved	
OAMUX	**GLA**	
0	Secondary bypass, no divider	
1	Secondary bypass, use divider	
2	Delay Clock Using FBDLY	+0.25 to +4 ns in 0.25 ns increments
3	Phase Shift Clock by 0°	

Table 1-8 • **Clock-Conditioning Circuitry Delay-Line Settings**

Delay Line	Delay Value (ns)
DLYB	
0	0
1	+0.25
2	+0.50
3	+4.0
DLYA	
0	0
1	+0.25
2	+0.50
3	+4.0

Lock Signal

An active-high Lock signal (added via the SmartGen PLL development tool) indicates that the PLL has locked to the incoming clock signal. The PLL will acquire and maintain lock even when there is jitter on the incoming clock signal. The PLL will maintain lock with an input jitter up to 5% of the input period, with a maximum of 5 ns. Users can employ the Lock signal as a soft reset of the logic driven by GLB and/or GLA. Note if F_{IN} is not within specified frequencies, then both the F_{OUT} and lock signal are indeterminate.

PLL Configuration Options

The PLL can be configured during design (via Flash-configuration bits set in the programming bitstream) or dynamically during device operation, thus eliminating the need to reprogram the device. The dynamic configuration bits are loaded into a serial-in/parallel-out shift register provided in the clock conditioning circuit. The shift register can be accessed either from user logic within the device or via the JTAG port. Another option is internal dynamic configuration via user-designed hardware. Refer to Actel's *ProASIC^PLUS PLL Dynamic Reconfiguration Using JTAG* application note for more information.

For information on the clock conditioning circuit, refer to Actel's *Using ProASIC^PLUS Clock Conditioning Circuits* application note.

Sample Implementations

Frequency Synthesis

Figure 1-16 on page 1-17 illustrates an example where the PLL is used to multiply a 33 MHz external clock up to 133 MHz. Figure 1-17 on page 1-17 uses two dividers to synthesize a 50 MHz output clock from a 40 MHz input reference clock. The input frequency of 40 MHz is multiplied by five and divided by four, giving an output clock (GLB) frequency of 50 MHz. When dividers are used, a given ratio can be generated in multiple ways, allowing the user to stay within the operating frequency ranges of the PLL. For example, in this case the input divider could have been two and the output divider also two, giving us a division of the input frequency by four to go with the feedback loop division (effective multiplication) by five.

Adjustable Clock Delay

Figure 1-18 on page 1-18 illustrates the delay of the input clock by employing one of the adjustable delay lines. This is easily done in ProASIC^PLUS by bypassing the PLL core entirely and using the output delay line. Notice also that the output clock can be effectively advanced relative to the input clock by using the delay line in the feedback path. This is shown in Figure 1-19 on page 1-18.

Clock Skew Minimization

Figure 1-20 on page 1-19 indicates how feedback from the clock network can be used to create minimal skew between the distributed clock network and the input clock. The input clock is fed to the reference clock input of the PLL. The output clock (GLA) feeds a clock network. The feedback input to the PLL uses a clock input delayed by a routing network. The PLL then adjusts the phase of the input clock to match the delayed clock, thus providing nearly zero effective skew between the two clocks. Refer to Actel's *Using ProASIC^PLUS Clock Conditioning Circuits* application note for more information.

PLL Electrical Specifications

Parameter	Value $T_J \leq$ –40°C	Value $T_J >$ –40°C	Notes
Frequency Ranges			
Reference Frequency f_{IN} (min.)	2.0 MHz	1.5 MHz	Clock conditioning circuitry (min.) lowest input frequency
Reference Frequency f_{IN} (max.)	180 MHz	180 MHz	Clock conditioning circuitry (max.) highest input frequency
OSC Frequency f_{VCO} (min.)	60	24 MHz	Lowest output frequency voltage controlled oscillator
OSC Frequency f_{VCO} (max.)	180	180 MHz	Highest output frequency voltage controlled oscillator
Clock Conditioning Circuitry f_{OUT} (min.)	$f_{IN} \leq 40$ = 18 MHz $f_{IN} > 40$ = 16 MHz	6 MHz	Lowest output frequency clock conditioning circuitry
Clock Conditioning Circuitry f_{OUT} (max.)	180	180 MHz	Highest output frequency clock conditioning circuitry
Acquisition Time from Cold Start			
Acquisition Time (max.)	80 µs	30 µs	$f_{VCO} \leq 40$ MHz
Acquisition Time (max.)	80 µs	80 µs	$f_{VCO} > 40$ MHz
Long Term Jitter Peak-to-Peak Max.*			
Temperature		**Frequency MHz**	
		f_{VCO}< 10 / **10<f_{VCO}<60** / **f_{VCO} >60**	
25°C (or higher)		±1% / ±2% / ±1%	Jitter(ps) = Jitter(%)*period For example: Jitter in picoseconds at 100 MHz = 0.01 * (1/100E6) = 100 ps
0°C		±1.5% / ±2.5% / ±1%	
–40°C		±2.5% / ±3.5% / ±1%	
–55°C		±2.5% / ±3.5% / ±1%	
Power Consumption			
Analog Supply Power (max.*)		6.9 mW per PLL	
Digital Supply Current (max.)		7 µW/MHz	
Duty Cycle		50% ±0.5%	
Input Jitter Tolerance		5% input period (max. 5 ns)	Maximum jitter allowable on an input clock to acquire and maintain lock.

Note: **High clock frequencies (>60 MHz) under typical setup conditions*

User Security

ProASIC^PLUS devices have FlashLock protection bits that, once programmed, block the entire programmed contents from being read externally. Please refer to Table 1-11 for details on the number of bits in the key for each device. If locked, the user can only reprogram the device employing the user-defined security key. This protects the device from being read back and duplicated. Since programmed data is stored in nonvolatile memory cells (actually very small capacitors) rather than in the wiring, physical deconstruction cannot be used to compromise data. This type of security breach is further discouraged by the placement of the memory cells beneath the four metal layers (whose removal cannot be accomplished without disturbing the charge in the capacitor). This is the highest security provided in the industry. For more information, refer to Actel's *Design Security in Nonvolatile Flash and Antifuse FPGAs* white paper.

Table 1-11 • **Flashlock Key Size by Device**

Device	Key Size
APA075	79 bits
APA150	79 bits
APA300	79 bits
APA450	119 bits
APA600	167 bits
APA750	191 bits
APA1000	263 bits

Embedded Memory Floorplan

The embedded memory is located across the top and bottom of the device in 256x9 blocks (Figure 1-1 on page 1-2). Depending on the device, up to 88 blocks are available to support a variety of memory configurations. Each block can be programmed as an independent memory array or combined (using dedicated memory routing resources) to form larger, more complex memory configurations. A single memory configuration could include blocks from both the top and bottom memory locations.

Embedded Memory Configurations

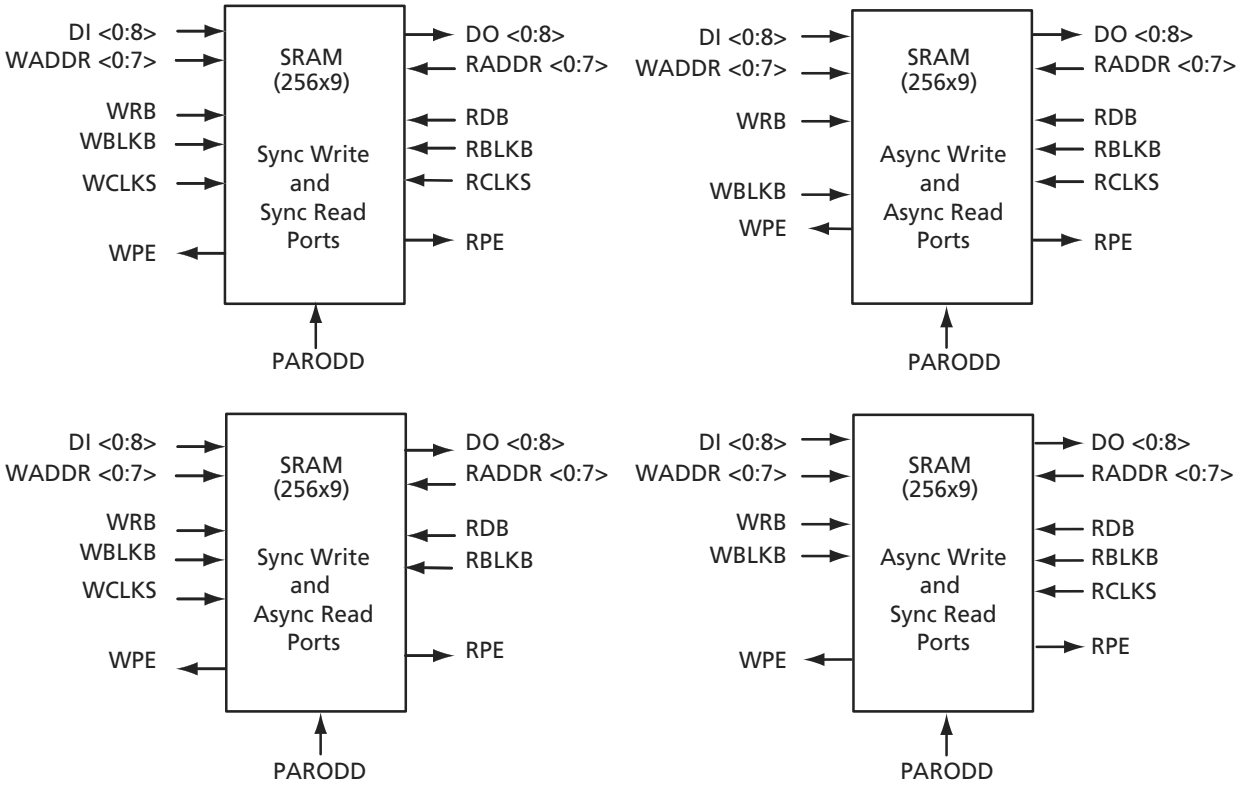
The embedded memory in the ProASIC^PLUS family provides great configuration flexibility (Table 1-12). Each ProASIC^PLUS block is designed and optimized as a two-port memory (one read, one write). This provides 198 kbits of two-port and/or single port memory in the APA1000 device.

Each memory block can be configured as FIFO or SRAM, with independent selection of synchronous or asynchronous read and write ports (Table 1-13). Additional characteristics include programmable flags as well as parity checking and generation. Figure 1-21 on page 1-25 and Figure 1-22 on page 1-26 show the block diagrams of the basic SRAM and FIFO blocks. Table 1-14 on page 1-25 and Table 1-15 on page 1-26 describe memory block SRAM and FIFO interface signals, respectively. A single memory block is designed to operate at up to 150 MHz (standard speed grade typical conditions). Each block is comprised of 256 9-bit words (one read port, one write port). The memory blocks may be cascaded in width and/or depth to create the desired memory organization. (Figure 1-23 on page 1-27). This provides optimal bit widths of 9 (one block), 18, 36, and 72, and optimal depths of 256, 512, 768, and 1,024. Refer to Actel's *SmartGen User's Guide* for more information.

Figure 1-24 on page 1-27 gives an example of optimal memory usage. Ten blocks with 23,040 bits have been used to generate three arrays of various widths and depths. Figure 1-25 on page 1-27 shows how RAM blocks can be used in parallel to create extra read ports. In this example, using only 10 of the 88 available blocks of the APA1000 yields an effective 6,912 bits of multiple port RAM. The Actel SmartGen software facilitates building wider and deeper memory configurations for optimal memory usage.

Table 1-12 • **ProASIC^PLUS Memory Configurations by Device**

Device	Bottom	Top	Maximum Width		Maximum Depth	
			D	W	D	W
APA075	0	12	256	108	1,536	9
APA150	0	16	256	144	2,048	9
APA300	16	16	256	144	2,048	9
APA450	24	24	256	216	3,072	9
APA600	28	28	256	252	3,584	9



Note: *Each RAM block contains a multiplexer (called DMUX) for each output signal, increasing design efficiency. These DMUX cells do not consume any core logic tiles and connect directly to high-speed routing resources between the RAM blocks. They are used when RAM blocks are cascaded and are automatically inserted by the software tools.*

Figure 1-21 • **Example SRAM Block Diagrams**

Table 1-14 • **Memory Block SRAM Interface Signals**

SRAM Signal	Bits	In/Out	Description
WCLKS	1	In	Write clock used on synchronization on write side
RCLKS	1	In	Read clock used on synchronization on read side
RADDR<0:7>	8	In	Read address
RBLKB	1	In	Read block select (active Low)
RDB	1	In	Read pulse (active Low)
WADDR<0:7>	8	In	Write address
WBLKB	1	In	Write block select (active Low)
DI<0:8>	9	In	Input data bits <0:8>, <8> can be used for parity In
WRB	1	In	Write pulse (active Low)
DO<0:8>	9	Out	Output data bits <0:8>, <8> can be used for parity Out
RPE	1	Out	Read parity error (active High)
WPE	1	Out	Write parity error (active High)
PARODD	1	In	Selects Odd parity generation/detect when High, Even parity when Low

Note: *Not all signals shown are used in all modes.*

Related Documents

Application Notes

Efficient Use of ProASIC Clock Trees
http://www.actel.com/documents/A500K_Clocktree_AN.pdf
I/O Features in ProASIC^PLUS Flash FPGAs
http://www.actel.com/documents/APA_LVPECL_AN.pdf
Power-Up Behavior of ProASIC^PLUS Devices
http://www.actel.com/documents/APA_PowerUp_AN.pdf
ProASIC^PLUS PLL Dynamic Reconfiguration Using JTAG
http://www.actel.com/documents/APA_PLLdynamic_AN.pdf
Using ProASIC^PLUS Clock Conditioning Circuits
http://www.actel.com/documents/APA_PLL_AN.pdf
In-System Programming ProASIC^PLUS Devices
http://www.actel.com/documents/APA_External_ISP_AN.pdf
Performing Internal In-System Programming Using Actel's ProASIC^PLUS Devices
http://www.actel.com/documents/APA_Microprocessor_AN.pdf
ProASIC^PLUS RAM and FIFO Blocks
http://www.actel.com/documents/APA_RAM_FIFO_AN.pdf

White Paper

Design Security in Nonvolatile Flash and Antifuse FPGAs
http://www.actel.com/documents/DesignSecurity_WP.pdf

User's Guide

Designer User's Guide
http://www.actel.com/documents/designer_UG.pdf
SmartGen Cores Reference Guide
http://www.actel.com/documents/gen_refguide_ug.pdf
ProASIC and ProASIC^PLUS Macro Library Guide
http://www.actel.com/documents/pa_libguide_UG.pdf

Additional Information

The following link contains additional information on ProASIC^PLUS devices.
http://www.actel.com/products/proasicplus/default.aspx

Package Thermal Characteristics

The ProASIC^PLUS family is available in several package types with a range of pin counts. Actel has selected packages based on high pin count, reliability factors, and superior thermal characteristics.

Thermal resistance defines the ability of a package to conduct heat away from the silicon, through the package to the surrounding air. Junction-to-ambient thermal resistance is measured in degrees Celsius/Watt and is represented as Theta ja (Θ_{ja}). The lower the thermal resistance, the more efficiently a package will dissipate heat.

A package's maximum allowed power (P) is a function of maximum junction temperature (T_J), maximum ambient operating temperature (T_A), and junction-to-ambient thermal resistance Θ_{ja}. Maximum junction temperature is the maximum allowable temperature on the active surface of the IC and is 110° C. P is defined as:

$$P = \frac{T_J - T_A}{\Theta_{ja}}$$

EQ 1-4

Θ_{ja} is a function of the rate (in linear feet per minute (lfpm)) of airflow in contact with the package. When the estimated power consumption exceeds the maximum allowed power, other means of cooling, such as increasing the airflow rate, must be used. The maximum power dissipation allowed for a Military temperature device is specified as a function of Θ_{jc}. The absolute maximum junction temperature is 150°C.

The calculation of the absolute maximum power dissipation allowed for a Military temperature application is illustrated in the following example for a 456-pin PBGA package:

$$\text{Maximum Power Allowed} = \frac{\text{Max. junction temp. (°C)} - \text{Max. case temp. (°C)}}{\theta_{jc}(\text{°C/W})} = \frac{150\text{°C} - 125\text{°C}}{3.0\text{°C/W}} = 8.333\text{W}$$

EQ 1-5

Table 1-16 • **Package Thermal Characteristics**

Plastic Packages	Pin Count	θ_{jc}	θ_{ja} Still Air	θ_{ja} 1.0 m/s 200 ft./min.	θ_{ja} 2.5 m/s 500 ft./min.	Units
Thin Quad Flat Pack (TQFP)	100	14.0	33.5	27.4	25.0	°C/W
Thin Quad Flat Pack (TQFP)	144	11.0	33.5	28.0	25.7	°C/W
Plastic Quad Flat Pack (PQFP)[1]	208	8.0	26.1	22.5	20.8	°C/W
PQFP with Heat spreader[2]	208	3.8	16.2	13.3	11.9	°C/W
Plastic Ball Grid Array (PBGA)	456	3.0	15.6	12.5	11.6	°C/W
Fine Pitch Ball Grid Array (FBGA)	144	3.8	26.9	22.9	21.5	°C/W
Fine Pitch Ball Grid Array (FBGA)	256	3.8	26.6	22.8	21.5	°C/W
Fine Pitch Ball Grid Array (FBGA)[3]	484	3.2	18.0	14.7	13.6	°C/W
Fine Pitch Ball Grid Array (FBGA)[4]	484	3.2	20.5	17.0	15.9	°C/W
Fine Pitch Ball Grid Array (FBGA)	676	3.2	16.4	13.0	12.0	°C/W
Fine Pitch Ball Grid Array (FBGA)	896	2.4	13.6	10.4	9.4	°C/W
Fine Pitch Ball Grid Array (FBGA)	1152	1.8	12.0	8.9	7.9	°C/W
Ceramic Quad Flat Pack (CQFP)	208	2.0	22.0	19.8	18.0	°C/W
Ceramic Quad Flat Pack (CQFP)	352	2.0	17.9	16.1	14.7	°C/W
Ceramic Column Grid Array (CCGA/LGA)	624	6.5	8.9	8.5	8.0	°C/W

Notes:

1. *Valid for the following devices irrespective of temperature grade: APA075, APA150, and APA300*
2. *Valid for the following devices irrespective of temperature grade: APA450, APA600, APA750, and APA1000*
3. *Depopulated Array*
4. *Full array*

Table 1-24 • **DC Electrical Specifications (V_{DDP} = 3.3 V ±0.3 V and V_{DD} = 2.5 V ±0.2 V) (Continued)**
Applies to Military Temperature and MIL-STD-883B Temperature Only

Symbol	Parameter	Conditions		Military/MIL-STD-883B[1] Min.	Typ.	Max.	Units
I_{DDQ}	Quiescent Supply Current (standby) Industrial	V_{IN} = GND[2] or V_{DD}	Std.		5.0	20	mA
I_{DDQ}	Quiescent Supply Current (standby) Military	V_{IN} = GND[2] or V_{DD}	Std.		5.0	25	mA
I_{OZ}	Tristate Output Leakage Current	V_{OH} = GND or V_{DD}	Std.	–10		10	µA
			–F[3]	–10		100	µA
I_{OSH}	Output Short Circuit Current High 3.3 V High Drive (OB33P) 3.3 V Low Drive (OB33L)	 V_{IN} = GND V_{IN} = GND		 –200 –100			
I_{OSL}	Output Short Circuit Current Low 3.3 V High Drive 3.3 V Low Drive	 V_{IN} = V_{DD} V_{IN} = V_{DD}				 200 100	
$C_{I/O}$	I/O Pad Capacitance					10	pF
C_{CLK}	Clock Input Pad Capacitance					10	pF

Notes:

1. *All process conditions. Military Temperature / MIL-STD-883 Class B: Junction Temperature: –55 to +125°C.*
2. *No pull-up resistor required.*
3. *This will not exceed 2 mA total per device.*
4. *During transitions, the input signal may overshoot to V_{DDP} +1.0 V for a limited time of no larger than 10% of the duty cycle.*
5. *During transitions, the input signal may undershoot to –1.0 V for a limited time of no larger than 10% of the duty cycle.*

Table 1-25 • **DC Specifications (3.3 V PCI Operation)[1]**

Symbol	Parameter	Condition		Commercial/ Industrial[2,3]		Military/MIL-STD- 883[2,3]		Units
				Min.	Max.	Min.	Max.	
V_{DD}	Supply Voltage for Core			2.3	2.7	2.3	2.7	V
V_{DDP}	Supply Voltage for I/O Ring			3.0	3.6	3.0	3.6	V
V_{IH}	Input High Voltage			$0.5V_{DDP}$	V_{DDP} + 0.5	$0.5V_{DDP}$	V_{DDP} + 0.5	V
V_{IL}	Input Low Voltage			–0.5	$0.3V_{DDP}$	–0.5	$0.3V_{DDP}$	V
I_{IPU}	Input Pull-up Voltage[4]			$0.7V_{DDP}$		$0.7V_{DDP}$		V
I_{IL}	Input Leakage Current[5]	$0 < V_{IN} < V_{DDP}$	Std.	–10	10	–50	50	µA
			–F[3, 6]	–10	100			µA
V_{OH}	Output High Voltage	I_{OUT} = –500 µA		$0.9V_{DDP}$		$0.9V_{DDP}$		V
V_{OL}	Output Low Voltage	I_{OUT} = 1500 µA			$0.1V_{DDP}$		$0.1V_{DDP}$	V
C_{IN}	Input Pin Capacitance (except CLK)				10		10	pF
C_{CLK}	CLK Pin Capacitance			5	12	5	12	pF

Notes:

1. *For PCI operation, use GL33, OTB33PH, OB33PH, IOB33PH, IB33, or IB33S macro library cell only.*
2. *All process conditions. Junction Temperature: –40 to +110°C for Commercial and Industrial devices and –55 to +125°C for Military.*
3. *All –F parts are available as commercial only.*
4. *This specification is guaranteed by design. It is the minimum voltage to which pull-up resistors are calculated to pull a floated network. Designers with applications sensitive to static power utilization should ensure that the input buffer is conducting minimum current at this input voltage.*
5. *Input leakage currents include hi-Z output leakage for all bidirectional buffers with tristate outputs.*
6. *The sum of the leakage currents for all inputs shall not exceed 2mA per device.*

Tristate Buffer Delays

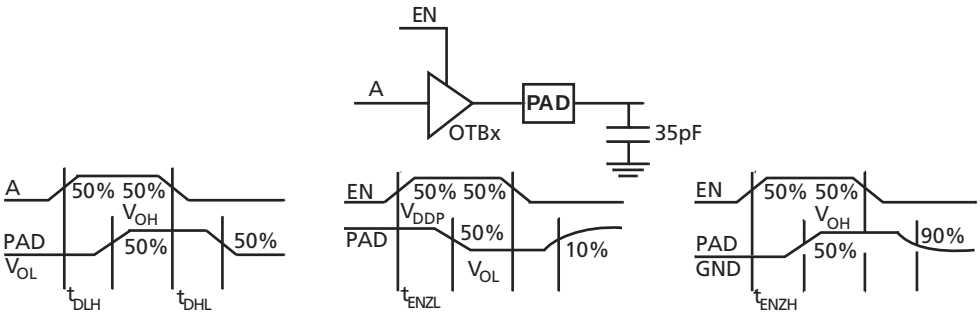


Figure 1-26 • **Tristate Buffer Delays**

Table 1-27 • **Worst-Case Commercial Conditions**
V_{DDP} = 3.0 V, V_{DD} = 2.3 V, 35 pF load, T_J = 70°C

Macro Type	Description	Max t_{DLH}[1]		Max t_{DHL}[2]		Max t_{ENZH}[3]		Max t_{ENZL}[4]		Units
		Std.	–F	Std.	–F	Std.	–F	Std.	–F	
OTB33PH	3.3 V, PCI Output Current, High Slew Rate	2.0	2.4	2.2	2.6	2.2	2.6	2.0	2.4	ns
OTB33PN	3.3 V, High Output Current, Nominal Slew Rate	2.2	2.6	2.9	3.5	2.4	2.9	2.1	2.5	ns
OTB33PL	3.3 V, High Output Current, Low Slew Rate	2.5	3.0	3.2	3.9	2.7	3.3	2.8	3.4	ns
OTB33LH	3.3 V, Low Output Current, High Slew Rate	2.6	3.1	4.0	4.8	2.8	3.4	3.0	3.6	ns
OTB33LN	3.3 V, Low Output Current, Nominal Slew Rate	2.9	3.5	4.3	5.2	3.2	3.8	4.1	4.9	ns
OTB33LL	3.3 V, Low Output Current, Low Slew Rate	3.0	3.6	5.6	6.7	3.3	3.9	5.5	6.6	ns

Notes:

1. *t_{DLH}=Data-to-Pad High*
2. *t_{DHL}=Data-to-Pad Low*
3. *t_{ENZH}=Enable-to-Pad, Z to High*
4. *t_{ENZL} = Enable-to-Pad, Z to Low*
5. *All –F parts are only available as commercial.*

Table 1-28 • **Worst-Case Commercial Conditions**
V_{DDP} = 2.3 V, V_{DD} = 2.3 V, 35 pF load, T_J = 70°C

Macro Type	Description	Max t_{DLH}[1]		Max t_{DHL}[2]		Max t_{ENZH}[3]		Max t_{ENZL}[4]		Units
		Std.	–F	Std.	–F	Std.	–F	Std.	–F	
OTB25LPHH	2.5 V, Low Power, High Output Current, High Slew Rate[5]	2.0	2.4	2.1	2.5	2.3	2.7	2.0	2.4	ns
OTB25LPHN	2.5 V, Low Power, High Output Current, Nominal Slew Rate[5]	2.4	2.9	3.0	3.6	2.7	3.2	2.1	2.5	ns
OTB25LPHL	2.5 V, Low Power, High Output Current, Low Slew Rate[5]	2.9	3.5	3.2	3.8	3.1	3.8	2.7	3.2	ns
OTB25LPLH	2.5 V, Low Power, Low Output Current, High Slew Rate[5]	2.7	3.3	4.6	5.5	3.0	3.6	2.6	3.1	ns

Notes:

1. *t_{DLH}=Data-to-Pad High*
2. *t_{DHL}=Data-to-Pad Low*
3. *t_{ENZH}=Enable-to-Pad, Z to High*
4. *t_{ENZL} = Enable-to-Pad, Z to Low*
5. *Low power I/O work with V_{DDP}=2.5 V ±10% only. V_{DDP}=2.3 V for delays.*
6. *All –F parts are only available as commercial.*

Table 1-41 • **Worst-Case Military Conditions**
V_{DDP} = 3.0V, V_{DD} = 2.3V, T_J = 125°C for Military/MIL-STD-883

Macro Type	Description	Max. t_{INYH}[1]	Max. t_{INYL}[2]
		Std.	Std.
GL33	3.3V, CMOS Input Levels[3], No Pull-up Resistor	1.1	1.1
GL33S	3.3V, CMOS Input Levels[3], No Pull-up Resistor, Schmitt Trigger	1.1	1.1
PECL	PPECL Input Levels	1.1	1.1

Notes:

1. *t_{INYH} = Input Pad-to-Y High*
2. *t_{INYL} = Input Pad-to-Y Low*
3. *LVTTL delays are the same as CMOS delays.*
4. *For LP Macros, V_{DDP}=2.3V for delays.*

Table 1-42 • **Worst-Case Military Conditions**
V_{DDP} = 2.3V, V_{DD} = 2.3V, T_J = 125°C for Military/MIL-STD-883

Macro Type	Description	Max. t_{INYH}[1]	Max. t_{INYL}[2]
		Std.	Std.
GL25LP	2.5V, CMOS Input Levels[3], Low Power	1.0	1.1
GL25LPS	2.5V, CMOS Input Levels[3], Low Power, Schmitt Trigger	1.4	1.0

Notes:

1. *t_{INYH} = Input Pad-to-Y High*
2. *t_{INYL} = Input Pad-to-Y Low*
3. *LVTTL delays are the same as CMOS delays.*
4. *For LP Macros, V_{DDP}=2.3V for delays.*

Table 1-48 • **Recommended Operating Conditions**

Parameter	Symbol	Limits	
		Commercial/Industrial	Military/MIL-STD-883
Maximum Clock Frequency*	f_{CLOCK}	180 MHz	180 MHz
Maximum RAM Frequency*	f_{RAM}	150 MHz	150 MHz
Maximum Rise/Fall Time on Inputs*			
• Schmitt Trigger Mode (10% to 90%)	t_R/t_F	N/A	100 ns
• Non-Schmitt Trigger Mode (10% to 90%)	t_R/t_F	100 ns	10 ns
Maximum LVPECL Frequency*		180 MHz	180 MHz
Maximum TCK Frequency (JTAG)	f_{TCK}	10 MHz	10 MHz

Note: **All –F parts will be 20% slower than standard commercial devices.*

Table 1-49 • **Slew Rates Measured at C = 30pF, Nominal Power Supplies and 25°C**

Type	Trig. Level	Rising Edge (ns)	Slew Rate (V/ns)	Falling Edge (ns)	Slew Rate (V/ns)	PCI Mode
OB33PH	10%-90%	1.60	1.65	1.65	1.60	Yes
OB33PN	10%-90%	1.57	1.68	3.32	0.80	No
OB33PL	10%-90%	1.57	1.68	1.99	1.32	No
OB33LH	10%-90%	3.80	0.70	4.84	0.55	No
OB33LN	10%-90%	4.19	0.63	3.37	0.78	No
OB33LL	10%-90%	5.49	0.48	2.98	0.89	No
OB25LPHH	10%-90%	1.55	1.29	1.56	1.28	No
OB25LPHN	10%-90%	1.70	1.18	2.08	0.96	No
OB25LPHL	10%-90%	1.97	1.02	2.09	0.96	No
OB25LPLH	10%-90%	3.57	0.56	3.93	0.51	No
OB25LPLN	10%-90%	4.65	0.43	3.28	0.61	No
OB25LPLL	10%-90%	5.52	0.36	3.44	0.58	No

Notes:

1. *Standard and –F parts.*
2. *All –F only available as commercial.*

Embedded Memory Specifications

This section discusses ProASIC^PLUS SRAM/FIFO embedded memory and its interface signals, including timing diagrams that show the relationships of signals as they pertain to single embedded memory blocks (Table 1-51). Table 1-13 on page 1-24 shows basic SRAM and FIFO configurations. Simultaneous read and write to the same location must be done with care. On such accesses the DI bus is output to the DO bus. Refer to the *ProASIC^PLUS RAM and FIFO Blocks* application note for more information.

Enclosed Timing Diagrams—SRAM Mode:

- "Synchronous SRAM Read, Access Timed Output Strobe (Synchronous Transparent)" section on page 1-58
- "Synchronous SRAM Read, Pipeline Mode Outputs (Synchronous Pipelined)" section on page 1-59
- "Asynchronous SRAM Write" section on page 1-60
- "Asynchronous SRAM Read, Address Controlled, RDB=0" section on page 1-61
- "Asynchronous SRAM Read, RDB Controlled" section on page 1-62
- "Synchronous SRAM Write"
- Embedded Memory Specifications

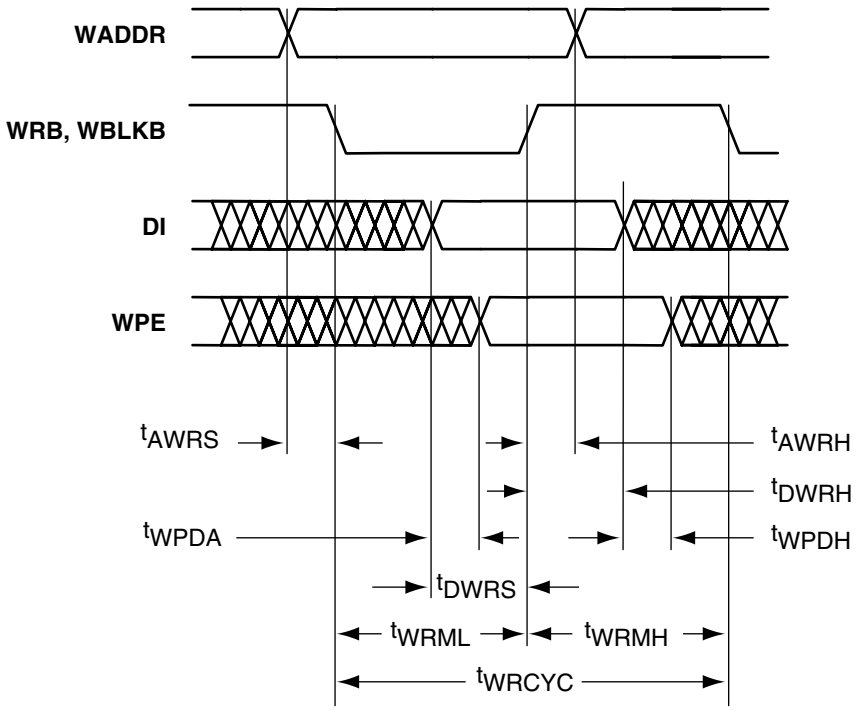
The difference between synchronous transparent and pipeline modes is the timing of all the output signals from the memory. In transparent mode, the outputs will change within the same clock cycle to reflect the data requested by the currently valid access to the memory. If clock cycles are short (high clock speed), the data requires most of the clock cycle to change to valid values (stable signals). Processing of this data in the same clock cycle is nearly impossible. Most designers add registers at all outputs of the memory to push the data processing into the next clock cycle. An entire clock cycle can then be used to process the data. To simplify use of this memory setup, suitable registers have been implemented as part of the memory primitive and are available to the user in the synchronous pipeline mode. In this mode, the output signals will change shortly after the second rising edge, following the initiation of the read access.

Table 1-51 • **Memory Block SRAM Interface Signals**

SRAM Signal	Bits	In/Out	Description
WCLKS	1	In	Write clock used on synchronization on write side
RCLKS	1	In	Read clock used on synchronization on read side
RADDR<0:7>	8	In	Read address
RBLKB	1	In	True read block select (active Low)
RDB	1	In	True read pulse (active Low)
WADDR<0:7>	8	In	Write address
WBLKB	1	In	Write block select (active Low)
DI<0:8>	9	In	Input data bits <0:8>, <8> can be used for parity In
WRB	1	In	Negative true write pulse
DO<0:8>	9	Out	Output data bits <0:8>, <8> can be used for parity Out
RPE	1	Out	Read parity error (active High)
WPE	1	Out	Write parity error (active High)
PARODD	1	In	Selects Odd parity generation/detect when high, Even when low

Note: *Not all signals shown are used in all modes.*

Asynchronous SRAM Write



Note: *The plot shows the normal operation status.*

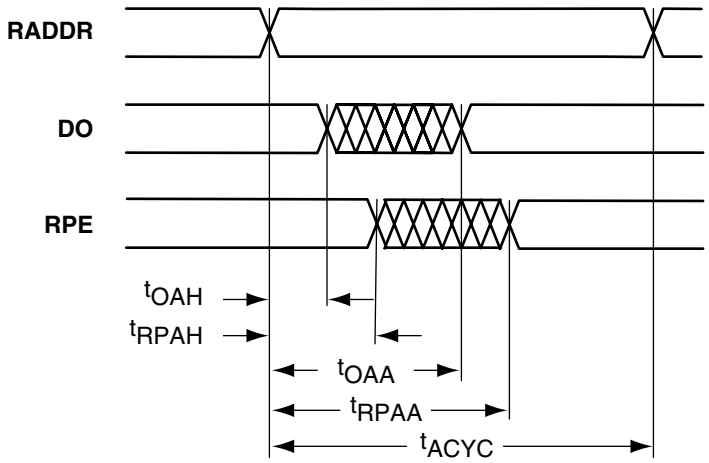
Figure 1-33 • **Asynchronous SRAM Write**

Table 1-54 • **T_J = 0°C to 110°C; V_{DD} = 2.3 V to 2.7 V for Commercial/industrial**
T_J = –55°C to 150°C, V_{DD} = 2.3 V to 2.7 V for Military/MIL-STD-883B

Symbol t_{xxx}	Description	Min.	Max.	Units	Notes
AWRH	WADDR hold from WB ↑	1.0		ns	
AWRS	WADDR setup to WB ↓	0.5		ns	
DWRH	DI hold from WB ↑	1.5		ns	
DWRS	DI setup to WB ↑	0.5		ns	PARGEN is inactive.
DWRS	DI setup to WB ↑	2.5		ns	PARGEN is active.
WPDA	WPE access from DI	3.0		ns	WPE is invalid, while PARGEN is active.
WPDH	WPE hold from DI		1.0	ns	
WRCYC	Cycle time	7.5		ns	
WRMH	WB high phase	3.0		ns	Inactive
WRML	WB low phase	3.0		ns	Active

Note: *All –F speed grade devices are 20% slower than the standard numbers.*

Asynchronous SRAM Read, Address Controlled, RDB=0



Note: *The plot shows the normal operation status.*

Figure 1-34 • **Asynchronous SRAM Read, Address Controlled, RDB=0**

Table 1-55 • **T_J = 0°C to 110°C; V_{DD} = 2.3 V to 2.7 V for Commercial/industrial**
T_J = –55°C to 150°C, V_{DD} = 2.3 V to 2.7 V for Military/MIL-STD-883B

Symbol t_{xxx}	Description	Min.	Max.	Units	Notes
ACYC	Read cycle time	7.5		ns	
OAA	New DO access from RADDR stable	7.5		ns	
OAH	Old DO hold from RADDR stable		3.0	ns	
RPAA	New RPE access from RADDR stable	10.0		ns	
RPAH	Old RPE hold from RADDR stable		3.0	ns	

Note: *All –F speed grade devices are 20% slower than the standard numbers.*

Asynchronous FIFO Full and Empty Transitions

The asynchronous FIFO accepts writes and reads while not full or not empty. When the FIFO is full, all writes are inhibited. Conversely, when the FIFO is empty, all reads are inhibited. A problem is created if the FIFO is written to during the transition from full to not full, or read during the transition from empty to not empty. The exact time at which the write or read operation changes from inhibited to accepted after the read (write) signal which causes the transition from full or empty to not full or not empty is indeterminate. For slow cycles, this indeterminate period starts 1 ns after the RB (WB) transition, which deactivates full or not empty and ends 3 ns after the RB (WB) transition. For fast cycles, the indeterminate period ends 3 ns (7.5 ns – RDL (WRL)) after the RB (WB) transition, whichever is later (Table 1-1 on page 1-7).

The timing diagram for write is shown in Figure 1-38 on page 1-65. The timing diagram for read is shown in Figure 1-39 on page 1-66. For basic SRAM configurations, see Table 1-14 on page 1-25. When reset is asserted, the empty flag will be asserted, the counters will reset, the outputs go to zero, but the internal RAM is not erased.

Enclosed Timing Diagrams – FIFO Mode:

The following timing diagrams apply only to single cell; they are not applicable to cascaded cells. For more information, refer to the *ProASIC^PLUS RAM/FIFO Blocks* application note.

- "Asynchronous FIFO Read" section on page 1-70
- "Asynchronous FIFO Write" section on page 1-71
- "Synchronous FIFO Read, Access Timed Output Strobe (Synchronous Transparent)" section on page 1-72
- "Synchronous FIFO Read, Pipeline Mode Outputs (Synchronous Pipelined)" section on page 1-73
- "Synchronous FIFO Write" section on page 1-74
- "FIFO Reset" section on page 1-75

Table 1-62 • **Memory Block FIFO Interface Signals**

FIFO Signal	Bits	In/Out	Description
WCLKS	1	In	Write clock used for synchronization on write side
RCLKS	1	In	Read clock used for synchronization on read side
LEVEL <0:7>*	8	In	Direct configuration implements static flag logic
RBLKB	1	In	Read block select (active Low)
RDB	1	In	Read pulse (active Low)
RESET	1	In	Reset for FIFO pointers (active Low)
WBLKB	1	In	Write block select (active Low)
DI<0:8>	9	In	Input data bits <0:8>, <8> will be generated if PARGEN is true
WRB	1	In	Write pulse (active Low)
FULL, EMPTY	2	Out	FIFO flags. FULL prevents write and EMPTY prevents read
EQTH, GEQTH*	2	Out	EQTH is true when the FIFO holds the number of words specified by the LEVEL signal. GEQTH is true when the FIFO holds (LEVEL) words or more
DO<0:8>	9	Out	Output data bits <0:8>
RPE	1	Out	Read parity error (active High)
WPE	1	Out	Write parity error (active High)
LGDEP <0:2>	3	In	Configures DEPTH of the FIFO to $2^{(LGDEP+1)}$
PARODD	1	In	Selects Odd parity generation/detect when high, Even when low

Note: **LEVEL is always eight bits (0000.0000, 0000.0001). That means for values of DEPTH greater than 256, not all values will be possible, e.g. for DEPTH=512, the LEVEL can only have the values 2, 4, . . ., 512. The LEVEL signal circuit will generate signals that indicate whether the FIFO is exactly filled to the value of LEVEL (EQTH) or filled equal or higher (GEQTH) than the specified LEVEL. Since counting starts at 0, EQTH will become true when the FIFO holds (LEVEL+1) words for 512-bit FIFOs.*

Pin Description

User Pins

I/O **User Input/Output**

The I/O pin functions as an input, output, tristate, or bidirectional buffer. Input and output signal levels are compatible with standard LVTTL and LVCMOS specifications. Unused I/O pins are configured as inputs with pull-up resistors.

NC **No Connect**

To maintain compatibility with other Actel ProASIC^{PLUS} products, it is recommended that this pin not be connected to the circuitry on the board.

GL **Global Pin**

Low skew input pin for clock or other global signals. This pin can be configured with an internal pull-up resistor. When it is not connected to the global network or the clock conditioning circuit, it can be configured and used as a normal I/O.

GLMX **Global Multiplexing Pin**

Low skew input pin for clock or other global signals. This pin can be used in one of two special ways (refer to Actel's *Using ProASIC^{PLUS} Clock Conditioning Circuits*).

When the external feedback option is selected for the PLL block, this pin is routed as the external feedback source to the clock conditioning circuit.

In applications where two different signals access the same global net at different times through the use of GLMXx and GLMXLx macros, this pin will be fixed as one of the source pins.

This pin can be configured with an internal pull-up resistor. When it is not connected to the global network or the clock conditioning circuit, it can be configured and used as any normal I/O. If not used, the GLMXx pin will be configured as an input with pull-up.

Dedicated Pins

GND **Ground**

Common ground supply voltage.

V_{DD} **Logic Array Power Supply Pin**

2.5 V supply voltage.

V_{DDP} **I/O Pad Power Supply Pin**

2.5 V or 3.3 V supply voltage.

TMS **Test Mode Select**

The TMS pin controls the use of boundary-scan circuitry. This pin has an internal pull-up resistor.

TCK **Test Clock**

Clock input pin for boundary scan (maximum 10 MHz). Actel recommends adding a nominal 20 kΩ pull-up resistor to this pin.

TDI **Test Data In**

Serial input for boundary scan. A dedicated pull-up resistor is included to pull this pin high when not being driven.

TDO **Test Data Out**

Serial output for boundary scan. Actel recommends adding a nominal 20kΩ pull-up resistor to this pin.

TRST **Test Reset Input**

Asynchronous, active-low input pin for resetting boundary-scan circuitry. This pin has an internal pull-up resistor. For more information, please refer to *Power-up Behavior of ProASIC^{PLUS} Devices* application note.

Special Function Pins

RCK **Running Clock**

A free running clock is needed during programming if the programmer cannot guarantee that TCK will be uninterrupted. If not used, this pin has an internal pull-up and can be left floating.

NPECL **User Negative Input**

Provides high speed clock or data signals to the PLL block. If unused, leave the pin unconnected.

PPECL **User Positive Input**

Provides high speed clock or data signals to the PLL block. If unused, leave the pin unconnected.

AVDD **PLL Power Supply**

Analog V_{DD} should be V_{DD} (core voltage) 2.5 V (nominal) and be decoupled from GND with suitable decoupling capacitors to reduce noise. For more information, refer to Actel's *Using ProASIC^{PLUS} Clock Conditioning Circuits* application note. If the clock conditioning circuitry is not used in a design, AVDD can either be left floating or tied to 2.5 V.

AGND **PLL Power Ground**

The analog ground can be connected to the system ground. For more information, refer to Actel's *Using ProASIC^{PLUS} Clock Conditioning Circuits* application note. If the PLLs or clock conditioning circuitry are not used in a design, AGND should be tied to GND.