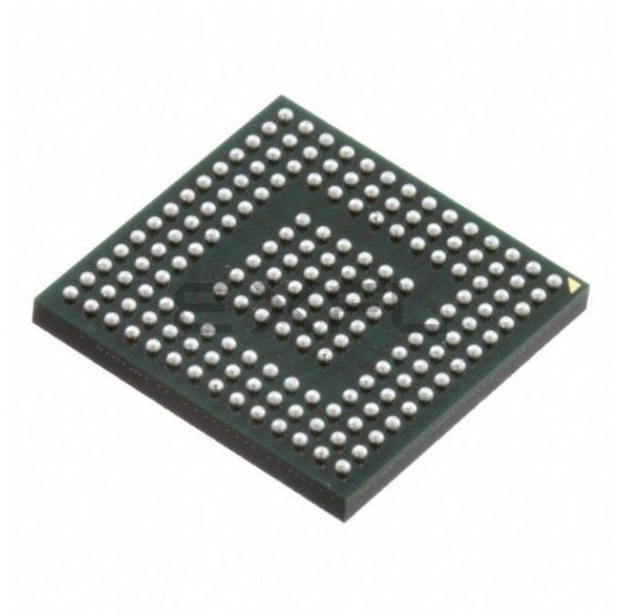

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Active
Type	Fixed Point
Interface	I²C, PPI, SPI, SPORT, UART/USART
Clock Rate	400MHz
Non-Volatile Memory	External
On-Chip RAM	116kB
Voltage - I/O	1.8V, 2.5V, 3.3V
Voltage - Core	1.30V
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	168-LFBGA, CSPBGA
Supplier Device Package	168-CSPBGA (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adbf512wbbcz402

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REVISION HISTORY

4/14—Rev. C to Rev. D

This Rev D product data sheet includes Flash memory specifications that differ from all previous data sheet versions (A, B, C).

The Flash memory specifications contained in the Rev D product data sheet are appropriate only for those products that include 16M bit SPI Flash memory.

These changes are reflected in the following sections:

(EVT), and lists their priorities are described in the *ADSP-BF51x Blackfin Processor Hardware Reference Manual* "System Interrupts" chapter.

System Interrupt Controller (SIC)

The system interrupt controller provides the mapping and routing of events from the many peripheral interrupt sources to the prioritized general-purpose interrupt inputs of the CEC. Although the processors provide a default mapping, the user can alter the mappings and priorities of interrupt events by writing the appropriate values into the interrupt assignment registers (SIC_IARx). See the *ADSP-BF51x Blackfin Processor Hardware Reference Manual* "System Interrupts" chapter for the inputs into the SIC and the default mappings into the CEC.

The SIC allows further control of event processing by providing three pairs of 32-bit interrupt control and status registers. Each register contains a bit corresponding to each of the peripheral interrupt events. For more information, see the *ADSP-BF51x Blackfin Processor Hardware Reference Manual* "System Interrupts" chapter.

DMA CONTROLLERS

The ADSP-BF51x processors have multiple independent DMA channels that support automated data transfers with minimal overhead for the processor core. DMA transfers can occur between the processor's internal memories and any of its DMA-capable peripherals. Additionally, DMA transfers can be accomplished between any of the DMA-capable peripherals and external devices connected to the external memory interfaces, including the SDRAM controller and the asynchronous memory controller. DMA-capable peripherals include the Ethernet MAC, RSI, SPORTs, SPIs, UARTs, and PPI. Each individual DMA-capable peripheral has at least one dedicated DMA channel.

The processors' DMA controller supports both one-dimensional (1-D) and two-dimensional (2-D) DMA transfers. DMA transfer initialization can be implemented from registers or from sets of parameters called descriptor blocks.

The 2-D DMA capability supports arbitrary row and column sizes up to 64K elements by 64K elements, and arbitrary row and column step sizes up to ±32K elements. Furthermore, the column step size can be less than the row step size, allowing implementation of interleaved data streams. This feature is especially useful in video applications where data can be de-interleaved on the fly.

Examples of DMA types supported by the DMA controller include:

- A single, linear buffer that stops upon completion
- A circular, auto-refreshing buffer that interrupts on each full or fractionally full buffer
- 1-D or 2-D DMA using a linked list of descriptors
- 2-D DMA using an array of descriptors, specifying only the base DMA address within a common page

In addition to the dedicated peripheral DMA channels, there are two memory DMA channels that transfer data between the various memories of the processor system. This enables transfers of blocks of data between any of the memories—including external SDRAM, ROM, SRAM, and flash memory—with minimal processor intervention. Memory DMA transfers can be controlled by a very flexible descriptor-based methodology or by a standard register-based autobuffer mechanism.

The processors also have an external DMA controller capability via dual external DMA request signals when used in conjunction with the external bus interface unit (EBIU). This functionality can be used when a high speed interface is required for external FIFOs and high bandwidth communications peripherals. It allows control of the number of data transfers for memory DMA. The number of transfers per edge is programmable. This feature can be programmed to allow memory DMA to have an increased priority on the external bus relative to the core.

PROCESSOR PERIPHERALS

The ADSP-BF51x processors contain a rich set of peripherals connected to the core via several high bandwidth buses, providing flexibility in system configuration as well as excellent overall system performance (see Figure 2). The processors contain dedicated network communication modules and high speed serial and parallel ports, an interrupt controller for flexible management of interrupts from the on-chip peripherals or external sources, and power management control functions to tailor the performance and power characteristics of the processor and system to many application scenarios.

All of the peripherals, except for the general-purpose I/O, rotary counter, TWI, three-phase PWM, real-time clock, and timers, are supported by a flexible DMA structure. There are also separate memory DMA channels dedicated to data transfers between the processor's various memory spaces, including external SDRAM and asynchronous memory. Multiple on-chip buses provide enough bandwidth to keep the processor core running along with activity on all of the on-chip and external peripherals.

Real-Time Clock

The real-time clock (RTC) provides a robust set of digital watch features, including current time, stopwatch, and alarm. The RTC is clocked by a 32.768 kHz crystal external to the processors. The RTC peripheral has a dedicated power supply so that it can remain powered up and clocked even when the rest of the processor is in a low power state. The RTC provides several programmable interrupt options, including interrupt per second, minute, hour, or day clock ticks, interrupt on programmable stopwatch countdown, or interrupt at a programmed alarm time.

The 32.768 kHz input clock frequency is divided down to a 1 Hz signal by a prescaler. The counter function of the timer consists of four counters: a 60-second counter, a 60-minute counter, a 24-hour counter, and an 32,768-day counter.

Parallel Peripheral Interface (PPI)

The ADSP-BF51x processors provide a parallel peripheral interface (PPI) that can connect directly to parallel analog-to-digital and digital-to-analog converters, ITU-R-601/656 video encoders and decoders, and other general-purpose peripherals. The PPI consists of a dedicated input clock signal, up to three frame synchronization signals, and up to 16 data signals.

In ITU-R-656 modes, the PPI receives and parses a data stream of 8-bit or 10-bit data elements. On-chip decode of embedded preamble control and synchronization information is supported.

Three distinct ITU-R-656 modes are supported:

- Active video only mode—The PPI does not read in any data between the End of Active Video (EAV) and Start of Active Video (SAV) preamble symbols, or any data present during the vertical blanking intervals. In this mode, the control byte sequences are not stored to memory; they are filtered by the PPI.
- Vertical blanking only mode—The PPI only transfers vertical blanking interval (VBI) data, as well as horizontal blanking information and control byte sequences on VBI lines.
- Entire field mode—The entire incoming bitstream is read in through the PPI. This includes active video, control preamble sequences, and ancillary data that may be embedded in horizontal and vertical blanking intervals.

Though not explicitly supported, ITU-R-656 output functionality can be achieved by setting up the entire frame structure (including active video, blanking, and control information) in memory and streaming the data out the PPI in a frame sync-less mode. The processor's 2-D DMA features facilitate this transfer by allowing the static frame buffer (blanking and control codes) to be placed in memory once, and simply updating the active video information on a per-frame basis.

The general-purpose modes of the PPI are intended to suit a wide variety of data capture and transmission applications. The modes are divided into four main categories, each allowing up to 16 bits of data transfer per PPI_CLK cycle:

- Data receive with internally generated frame syncs
- Data receive with externally generated frame syncs
- Data transmit with internally generated frame syncs
- Data transmit with externally generated frame syncs

These modes support ADC/DAC connections, as well as video communication with hardware signalling. Many of the modes support more than one level of frame synchronization. If desired, a programmable delay can be inserted between assertion of a frame sync and reception/transmission of data.

Code Security with Lockbox Secure Technology

A security system consisting of a blend of hardware and software provides customers with a flexible and rich set of code security features with Lockbox® secure technology. Key features include:

- OTP memory
- Unique chip ID
- Code authentication
- Secure mode of operation

The security scheme is based upon the concept of authentication of digital signatures using standards-based algorithms and provides a secure processing environment in which to execute code and protect assets.

DYNAMIC POWER MANAGEMENT

The ADSP-BF51x processors provide four operating modes, each with a different performance/power profile. In addition, dynamic power management provides the control functions to dynamically alter the processor core supply voltage, further reducing power dissipation. When configured for a 0 V core supply voltage, the processor enters the hibernate state. Control of clocking to each of the processor peripherals also reduces power consumption. See Table 3 for a summary of the power settings for each mode.

Table 3. Power Settings

Mode/State	PLL	PLL Bypassed	Core Clock (CCLK)	System Clock (SCLK)	Core Power
Full On	Enabled	No	Enabled	Enabled	On
Active	Enabled/ Disabled	Yes	Enabled	Enabled	On
Sleep	Enabled	—	Disabled	Enabled	On
Deep Sleep	Disabled	—	Disabled	Disabled	On
Hibernate	Disabled	—	Disabled	Disabled	Off

Full-On Operating Mode—Maximum Performance

In the full-on mode, the PLL is enabled and is not bypassed, providing capability for maximum operational frequency. This is the power-up default execution state in which maximum performance can be achieved. The processor core and all enabled peripherals run at full speed.

Active Operating Mode—Moderate Power Savings

In the active mode, the PLL is enabled but bypassed. Because the PLL is bypassed, the processor's core clock (CCLK) and system clock (SCLK) run at the input clock (CLKIN) frequency. In this mode, the CLKIN to CCLK multiplier ratio can be changed, although the changes are not realized until the full-on mode is entered. DMA access is available to appropriately configured L1 memories.

The newest IDE, CrossCore Embedded Studio, is based on the Eclipse™ framework. Supporting most Analog Devices processor families, it is the IDE of choice for future processors, including multicore devices. CrossCore Embedded Studio seamlessly integrates available software add-ins to support real time operating systems, file systems, TCP/IP stacks, USB stacks, algorithmic software modules, and evaluation hardware board support packages. For more information visit www.analog.com/cces.

The other Analog Devices IDE, VisualDSP++, supports processor families introduced prior to the release of CrossCore Embedded Studio. This IDE includes the Analog Devices VDK real time operating system and an open source TCP/IP stack. For more information visit www.analog.com/visualdsp. Note that VisualDSP++ will not support future Analog Devices processors.

EZ-KIT Lite Evaluation Board

For processor evaluation, Analog Devices provides wide range of EZ-KIT Lite® evaluation boards. Including the processor and key peripherals, the evaluation board also supports on-chip emulation capabilities and other evaluation and development features. Also available are various EZ-Extenders®, which are daughter cards delivering additional specialized functionality, including audio and video processing. For more information visit www.analog.com and search on “ezkit” or “ezextender”.

EZ-KIT Lite Evaluation Kits

For a cost-effective way to learn more about developing with Analog Devices processors, Analog Devices offer a range of EZ-KIT Lite evaluation kits. Each evaluation kit includes an EZ-KIT Lite evaluation board, directions for downloading an evaluation version of the available IDE(s), a USB cable, and a power supply. The USB controller on the EZ-KIT Lite board connects to the USB port of the user’s PC, enabling the chosen IDE evaluation suite to emulate the on-board processor in-circuit. This permits the customer to download, execute, and debug programs for the EZ-KIT Lite system. It also supports in-circuit programming of the on-board Flash device to store user-specific boot code, enabling standalone operation. With the full version of CrossCore Embedded Studio or VisualDSP++ installed (sold separately), engineers can develop software for supported EZ-KITs or any custom system utilizing supported Analog Devices processors.

Software Add-Ins for CrossCore Embedded Studio

Analog Devices offers software add-ins which seamlessly integrate with CrossCore Embedded Studio to extend its capabilities and reduce development time. Add-ins include board support packages for evaluation hardware, various middleware packages, and algorithmic modules. Documentation, help, configuration dialogs, and coding examples present in these add-ins are viewable through the CrossCore Embedded Studio IDE once the add-in is installed.

Board Support Packages for Evaluation Hardware

Software support for the EZ-KIT Lite evaluation boards and EZ-Extender daughter cards is provided by software add-ins called Board Support Packages (BSPs). The BSPs contain the required drivers, pertinent release notes, and select example code for the given evaluation hardware. A download link for a specific BSP is located on the web page for the associated EZ-KIT or EZ-Extender product. The link is found in the *Product Download* area of the product web page.

Middleware Packages

Analog Devices separately offers middleware add-ins such as real time operating systems, file systems, USB stacks, and TCP/IP stacks. For more information see the following web pages:

- www.analog.com/ucos3
- www.analog.com/ucfs
- www.analog.com/ucusbd
- www.analog.com/lwip

Algorithmic Modules

To speed development, Analog Devices offers add-ins that perform popular audio and video processing algorithms. These are available for use with both CrossCore Embedded Studio and VisualDSP++. For more information visit www.analog.com and search on “Blackfin software modules” or “SHARC software modules”.

Designing an Emulator-Compatible DSP Board (Target)

For embedded system test and debug, Analog Devices provides a family of emulators. On each JTAG DSP, Analog Devices supplies an IEEE 1149.1 JTAG Test Access Port (TAP). In-circuit emulation is facilitated by use of this JTAG interface. The emulator accesses the processor’s internal features via the processor’s TAP, allowing the developer to load code, set breakpoints, and view variables, memory, and registers. The processor must be halted to send data and commands, but once an operation is completed by the emulator, the DSP system is set to run at full speed with no impact on system timing. The emulators require the target board to include a header that supports connection of the DSP’s JTAG port to the emulator.

For details on target board design issues including mechanical layout, single processor connections, signal buffering, signal termination, and emulator pod logic, see the *EE-68: Analog Devices JTAG Emulation Technical Reference* on the Analog Devices website (www.analog.com)—use site search on “EE-68.” This document is updated regularly to keep pace with improvements to emulator support.

SIGNAL DESCRIPTIONS

The processors' signal definitions are listed in Table 8. In order to maintain maximum function and reduce package size and signal count, some signals have dual, multiplexed functions. In cases where signal function is reconfigurable, the default state is shown in plain text, while the alternate function is shown in italics.

All pins are three-stated during and immediately after reset, with the exception of the external memory interface, asynchronous and synchronous memory control, and the buffered XTAL output pin (CLKBUF). On the external memory interface, the control and address lines are driven high, with the exception of CLKOUT, which toggles at the system clock rate. During hibernate all outputs are three-stated unless otherwise noted in Table 8.

All I/O signals have their input buffers disabled with the exception of the signals noted in the data sheet that need pull-ups or pull downs if unused.

The SDA (serial data) and SCL (serial clock) pins/balls are open drain and therefore require a pullup resistor. Consult version 2.1 of the I^2C specification for the proper resistor value.

It is strongly advised to use the available IBIS models to ensure that a given board design meets overshoot/undershoot and signal integrity requirements. If no IBIS simulation is performed, it is strongly recommended to add series resistor terminations for all Driver Types A, C and D. The termination resistors should be placed near the processor to reduce transients and improve signal integrity. The resistance value, typically 33 Ω or 47 Ω, should be chosen to match the average board trace impedance. Additionally, adding a parallel termination to CLKOUT may prove useful in further enhancing signal integrity. Be sure to verify overshoot/undershoot and signal integrity specifications on actual hardware.

Table 8. Signal Descriptions

Signal Name	Type	Function	Driver Type[1]
EBIU			
ADDR19–1	O	Address Bus	A
DATA15–0	I/O	Data Bus	A
$\overline{\text{ABE1–0}}$/*SDQM1–0*	O	Byte Enable or Data Mask	A
$\overline{\text{AMS1–0}}$	O	Asynchronous Memory Bank Selects (Require pull-ups if hibernate is used)	A
$\overline{\text{ARE}}$	O	Asynchronous Memory Read Enable	A
$\overline{\text{AWE}}$	O	Asynchronous Memory Write Enable	A
$\overline{\text{SRAS}}$	O	SDRAM Row Address Strobe	A
$\overline{\text{SCAS}}$	O	SDRAM Column Address Strobe	A
$\overline{\text{SWE}}$	O	SDRAM Write Enable	A
SCKE	O	SDRAM Clock Enable (Requires a pull-down if hibernate with SDRAM self-refresh is used)	A
CLKOUT	O	SDRAM Clock Output	B
SA10	O	SDRAM A10 Signal	A
$\overline{\text{SMS}}$	O	SDRAM Bank Select	A
Port F: GPIO and Multiplexed Peripherals			
PF0/*ETxD2/PPI D0/*$\overline{\textit{SPI1SEL2}}$*/TACLK6*	I/O	GPIO/*Ethernet MII Transmit D2/PPI Data 0/SPI1 Slave Select 2/Timer6 Alternate Clock*	C
PF1/*ERxD2/PPI D1/PWM AH/TACLK7*	I/O	GPIO/*Ethernet MII Receive D2/PPI Data 1/PWM AH Output/Timer7 Alternate Clock*	C
PF2/*ETxD3/PPI D2/PWM AL*	I/O	GPIO/*Ethernet Transmit D3/PPI Data 2/PWM AL Output*	C
PF3/*ERxD3/PPI D3/PWM BH/TACLK0*	I/O	GPIO/*Ethernet MII Data Receive D3/PPI Data 3/PWM BH Output/Timer0 Alternate Clock*	C
PF4/*ERxCLK/PPI D4/PWM BL/TACLK1*	I/O	GPIO/*Ethernet MII Receive Clock/PPI Data 4/PWM BL Out/Timer1 Alternate CLK*	C
PF5/*ERxDV/PPI D5/PWM CH/TACI0*	I/O	GPIO/*Ethernet MII Receive Data Valid/PPI Data 5/PWM CH Out /Timer0 Alternate Capture Input*	C
PF6/*COL/PPI D6/PWM CL/TACI1*	I/O	GPIO/*Ethernet MII Collision/PPI Data 6/PWM CL Out/Timer1 Alternate Capture Input*	C
PF7/$\overline{\textit{SPI0SEL1}}$*/PPI D7/PWMSYNC*	I/O	GPIO/*SPI0 Slave Select 1/PPI Data 7/PWM Sync*	C

Table 8. Signal Descriptions (Continued)

Signal Name	Type	Function	Driver Type[1]
PF8/*MDC*/PPI D8/*SPI1SEL4*	I/O	GPIO/*Ethernet Management Channel Clock/PPI Data 8/SPI1 Slave Select 4*	C
PF9/*MDIO*/*PPI D9*/*TMR2*	I/O	GPIO/*Ethernet Management Channel Serial Data/PPI Data 9/Timer 2*	C
PF10/*ETxD0*/*PPI D10*/*TMR3*	I/O	GPIO/*Ethernet MII or RMII Transmit D0/PPI Data 10/Timer 3*	C
PF11/*ERxD0*/*PPI D11*/*PWM AH*/*TACI3*	I/O	GPIO/*Ethernet MII Receive D0/PPI Data 11/PWM AH output /Timer3 Alternate Capture Input*	C
PF12/*ETxD1*/*PPI D12*/*PWM AL*	I/O	GPIO/*Ethernet MII Transmit D1/PPI Data 12/PWM AL Output*	C
PF13/*ERxD1*/*PPI D13*/*PWM BH*	I/O	GPIO/*Ethernet MII or RMII Receive D1/PPI Data 13/PWM BH Output*	C
PF14/*ETxEN*/*PPI D14*/*PWM BL*	I/O	GPIO/*Ethernet MII Transmit Enable/PPI Data 14/PWM BL Out*	C
PF15[2]/*RMII PHYINT*/*PPI D15*/*PWM_SYNCA*	I/O	GPIO/*Ethernet MII PHY Interrupt/PPI Data 15/Alternate PWM Sync*	C
Port G: GPIO and Multiplexed Peripherals			
PG0/*MIICRS*/*RMIICRS*/*HWAIT*[3]/*SPI1SEL3*	I/O	GPIO/*Ethernet MII or RMII Carrier Sense or RMII Data Valid/HWAIT/SPI1 Slave Select3*	C
PG1/*ERxER*/*DMAR1*/*PWM CH*	I/O	GPIO/*Ethernet MII or RMII Receive Error/DMA Req 1/PWM CH Out*	C
PG2/*MIITxCLK*/*RMIIREF_CLK*/*DMAR0*/*PWM CL*	I/O	GPIO/*Ethernet MII or RMII Reference Clock/DMA Req 0/PWM CL Out*	C
PG3/*DR0PRI*/*RSI_DATA0*/*SPI0SEL5*/*TACLK3*	I/O	GPIO/*SPORT0 Primary Rx Data/RSI Data 0/SPI0 Slave Select 5/Timer3 Alternate CLK*	C
PG4/*RSCLK0*/*RSI_DATA1*/*TMR5*/*TACI5*	I/O	GPIO/*SPORT0 Rx Clock/RSI Data 1/Timer 5/Timer5 Alternate Capture Input*	D
PG5/*RFS0*/*RSI_DATA2*/*PPICLK*/*TMRCLK*	I/O	GPIO/*SPORT0 Rx Frame Sync/RSI Data 2/PPI Clock/External Timer Reference*	C
PG6/*TFS0*/*RSI_DATA3*/*TMR0*/*PPIFS1*	I/O	GPIO/*SPORT0 Tx Frame Sync/RSI Data 3/Timer0/PPI Frame Sync1*	C
PG7/*DT0PRI*/*RSI_CMD*/*TMR1*/*PPIFS2*	I/O	GPIO/*SPORT0 Tx Primary Data/RSI Command/Timer 1/PPI Frame Sync2*	C
PG8/*TSCLK0*/*RSI_CLK*/*TMR6*/*TACI6*	I/O	GPIO/*SPORT0 Tx Clock/RSI Clock/Timer 6/Timer6 Alternate Capture Input*	D
PG9/*DT0SEC*/*UART0TX*/*TMR4*	I/O	GPIO/*SPORT0 Secondary Tx Data/UART0 Transmit/Timer 4*	C
PG10/*DR0SEC*/*UART0RX*/*TACI4*	I/O	GPIO/*SPORT0 Secondary Rx Data/UART0 Receive/Timer4 Alternate Capture Input*	C
PG11/*SPI0SS*/*AMS2*/*SPI1SEL5*/*TACLK2*	I/O	GPIO/*SPI0 Slave Device Select/Asynchronous Memory Bank Select 2/SPI1 Slave Select 5/Timer2 Alternate CLK*	C
PG12/*SPI0SCK*/*PPICLK*/*TMRCLK*/*PTP_PPS*	I/O	GPIO/*SPI0 Clock/PPI Clock/External Timer Reference/PTP Pulse Per Second Out*	D
PG13/*SPI0MISO*[4]/*TMR0*/*PPIFS1*/ *PTP_CLKOUT*	I/O	GPIO/*SPI0 Master In Slave Out/Timer0/PPI Frame Sync1/PTP Clock Out*	C
PG14/*SPI0MOSI*/*TMR1*/*PPIFS2*/*PWM TRIP* /*PTP_AUXIN*	I/O	GPIO/*SPI0 Master Out Slave In/Timer 1/PPI Frame Sync2/PWM Trip/PTP Auxiliary Snapshot Trigger Input*	C
PG15/*SPI0SEL2*/*PPIFS3*/*AMS3*	I/O	GPIO/*SPI0 Slave Select 2/PPI Frame Sync3/Asynchronous Memory Bank Select 3*	C
Port H: GPIO and Multiplexed Peripherals			
PH0/*DR1PRI*/*SPI1SS*/*RSI_DATA4*	I/O	GPIO/*SPORT1 Primary Rx Data/SPI1 Device Select/RSI Data 4*	C
PH1/*RFS1*/*SPI1MISO*/*RSI_DATA5*	I/O	GPIO/*SPORT1 Rx Frame Sync/SPI1 Master In Slave Out/RSI Data 5*	C
PH2/*RSCLK1*/*SPI1SCK*/*RSI DATA6*	I/O	GPIO/*SPORT1 Rx Clock/SPI1 Clock/RSI Data 6*	D
PH3/*DT1PRI*/*SPI1MOSI*/*RSI DATA7*	I/O	GPIO/*SPORT1 Primary Tx Data/SPI1 Master Out Slave In/RSI Data 7*	C
PH4/*TFS1*/*AOE*/*SPI0SEL3*/*CUD*	I/O	GPIO/*SPORT1 Tx Frame Sync/Asynchronous Memory Output Enable/SPI0 Slave Select 3/Counter Up Direction*	C
PH5/*TSCLK1*/*ARDY*/*PTP_EXT_CLKIN*/*CDG*	I/O	GPIO/*SPORT1 Tx Clock/Asynchronous Memory Hardware Ready Control/ External Clock for PTP TSYNC/Counter Down Gate*	D
PH6/*DT1SEC*/*UART1TX*/*SPI1SEL1*/*CZM*	I/O	GPIO/*SPORT1 Secondary Tx Data/UART1 Transmit/SPI1 Slave Select 1 /Counter Zero Marker*	C
PH7/*DR1SEC*/*UART1RX*/*TMR7*/*TACI2*	I/O	GPIO/*SPORT1 Secondary Rx Data/UART1 Receive/Timer 7/Timer2 Alternate Clock Input*	C

Table 9 shows settings for TWI_DT in the NONGPIO_DRIVE register. Set this register prior to using the TWI port.

Table 9. TWI_DT Field Selections and V_{DDEXT}/V_{BUSTWI}

TWI_DT	V_{DDEXT} Nominal	V_{BUSTWI} Minimum	V_{BUSTWI} Nominal	V_{BUSTWI} Maximum	Unit
000 (default)	3.3	2.97	3.3	3.63	V
001	1.8	1.7	1.8	1.98	V
010	2.5	2.97	3.3	3.63	V
011	1.8	2.97	3.3	3.63	V
100	3.3	4.5	5	5.5	V
101	1.8	2.25	2.5	2.75	V
110	2.5	2.25	2.5	2.75	V
111 (reserved)	—	—	—	—	—

Clock Related Operating Conditions

Table 10 describes the timing requirements for the processor clocks. Take care in selecting MSEL, SSEL, and CSEL ratios so as not to exceed the maximum core clock and system clock. Table 11 describes phase-locked loop operating conditions.

Table 10. Core Clock (CCLK) Requirements

Parameter		Nominal Voltage Setting	Maximum	Unit
f_{CCLK}	Core Clock Frequency (V_{DDINT} = 1.33 V Minimum, All Models)	1.400 V	400	MHz
	Core Clock Frequency (V_{DDINT} = 1.23 V Minimum, Industrial/Commercial Models)	1.300 V	300	MHz
	Core Clock Frequency (V_{DDINT} = 1.14 V Minimum, Industrial Models Only)	1.200 V	200	MHz
	Core Clock Frequency (V_{DDINT} = 1.10 V Minimum, Commercial Models Only)	1.150 V	200	MHz

Table 11. Phase-Locked Loop Operating Conditions

Parameter		Min	Max	Unit
f_{VCO}	Voltage Controlled Oscillator (VCO) Frequency (Commercial/Industrial Models)	72	Instruction Rate[1]	MHz
	Voltage Controlled Oscillator (VCO) Frequency (Automotive Models)	84	Instruction Rate[1]	MHz

[1] For more information, see Ordering Guide on Page 67.

Table 12. SCLK Conditions

Parameter[1]		V_{DDEXT}/V_{DDMEM} 1.8 V Nominal Max	V_{DDEXT}/V_{DDMEM} 2.5 V or 3.3 V Nominal Max	Unit
f_{SCLK}	CLKOUT/SCLK Frequency (V_{DDINT} ≥ 1.230 V Minimum)	80	100	MHz
f_{SCLK}	CLKOUT/SCLK Frequency (V_{DDINT} < 1.230 V)	80	80	MHz

[1] f_{SCLK} must be less than or equal to f_{CCLK} and is subject to additional restrictions for SDRAM interface operation. See Table 28 on Page 33.

Parameter		Test Conditions	Min	Typical	Max	Unit
$I_{DDFLASH1}$	Flash Memory Supply Current 1—Asynchronous Read			6	9	mA
$I_{DDFLASH2}$	Flash Memory Supply Current 2—Standby			15	25	µA
$I_{DDFLASH3}$	Flash Memory Supply Current 3—Program and Erase			20	25	mA
I_{DDOTP}	V_{DDOTP} Current	V_{DDOTP} = 2.5 V, T_J = 25°C, OTP Memory Read		2		mA
I_{DDOTP}	V_{DDOTP} Current	V_{DDOTP} = 2.5 V, T_J = 25°C, OTP Memory Write		2		mA
I_{PPOTP}	V_{PPOTP} Current	V_{PPOTP} = 2.5 V, T_J = 25°C, OTP Memory Read		100		µA
I_{PPOTP}	V_{PPOTP} Current	V_{PPOTP} = Table 20 V, T_J = 25°C, OTP Memory Write		3		mA

[1] Applies to input balls.
[2] Applies to JTAG input balls (TCK, TDI, TMS, $\overline{TRST}$).
[3] Applies to three-statable balls.
[4] Applies to bidirectional balls SCL and SDA.
[5] Applies to all signal balls, except SCL and SDA.
[6] Guaranteed, but not tested.
[7] See the *ADSP-BF51x Blackfin Processor Hardware Reference Manual* for definition of sleep, deep sleep, and hibernate operating modes.
[8] Includes current on V_{DDEXT}, V_{DDMEM}, V_{DDOTP}, and V_{PPOTP} supplies. Clock inputs are tied high or low.
[9] Guaranteed maximum specifications.
[10] Unit for V_{DDINT} is V (Volts). Unit for f_{SCLK} is MHz.
[11] See Table 13 for the list of I_{DDINT} power vectors covered.

Total Power Dissipation

Total power dissipation has two components:

1. Static, including leakage current
2. Dynamic, due to transistor switching characteristics

Many operating conditions can also affect power dissipation, including temperature, voltage, operating frequency, and processor activity. Electrical Characteristics on Page 24 shows the current dissipation for internal circuitry (V_{DDINT}). $I_{DDDEEPSLEEP}$ specifies static power dissipation as a function of voltage (V_{DDINT}) and temperature (see Table 14), and I_{DDINT} specifies the total power specification for the listed test conditions, including the dynamic component as a function of voltage (V_{DDINT}) and frequency (Table 15).

There are two parts to the dynamic component. The first part is due to transistor switching in the core clock (CCLK) domain. This part is subject to an Activity Scaling Factor (ASF) which represents application code running on the processor core and L1 memories (Table 13).

The ASF is combined with the CCLK Frequency and V_{DDINT} dependent data in Table 15 to calculate this part. The second part is due to transistor switching in the system clock (SCLK) domain, which is included in the I_{DDINT} specification equation.

Table 13. Activity Scaling Factors (ASF)[1]

I_{DDINT} Power Vector	Activity Scaling Factor (ASF)
$I_{DD-PEAK}$	1.29
$I_{DD-HIGH}$	1.25
I_{DD-TYP}	1.00
I_{DD-APP}	0.85
I_{DD-NOP}	0.70
$I_{DD-IDLE}$	0.41

[1] See *Estimating Power for ASDP-BF534/BF536/BF537 Blackfin Processors (EE-297)*. The power vector information also applies to the ADSP-BF51x processors.

Table 14. Static Current—$I_{DD-DEEPSLEEP}$ (mA)

	Voltage (V_{DDINT})[1]								
T_J (°C)[1]	1.10 V	1.15 V	1.20 V	1.25 V	1.30 V	1.35 V	1.40 V	1.45 V	1.50 V
–40	0.9	1.0	1.0	1.1	1.1	1.2	1.3	1.7	1.9
–20	1.0	1.1	1.2	1.3	1.4	1.6	1.7	1.9	2.0
0	1.2	1.3	1.4	1.6	1.8	2.0	2.2	2.3	2.5

Table 14. Static Current—$I_{DD\text{-}DEEPSLEEP}$ (mA) (Continued)

T_J (°C)[1]	Voltage (V_{DDINT})[1]								
	1.10 V	1.15 V	1.20 V	1.25 V	1.30 V	1.35 V	1.40 V	1.45 V	1.50 V
25	1.8	1.9	2.1	2.3	2.5	2.8	3.1	3.3	3.7
40	2.4	2.6	2.8	3.0	3.3	3.7	4.0	4.4	4.9
55	3.3	3.5	3.8	4.3	4.6	5.0	5.5	6.1	6.7
70	4.6	5.0	5.4	6.0	6.4	7.0	7.7	8.4	9.2
85	6.5	7.1	7.7	8.3	9.1	9.9	10.8	11.8	12.8
100	9.2	10.0	10.8	11.7	12.7	13.7	15.0	16.1	17.5
105	10.3	11.1	12.1	13.1	14.2	15.3	16.6	18.0	19.4

[1] Valid frequency and voltage ranges are model-specific. See Operating Conditions on Page 22.

Table 15. Dynamic Current in CCLK Domain (mA, with ASF = 1.0)[1]

f_{CCLK} (MHz)[2]	Voltage (V_{DDINT})[2]								
	1.10 V	1.15 V	1.20 V	1.25 V	1.30 V	1.35 V	1.40 V	1.45 V	1.50 V
400	N/A	N/A	N/A	N/A	N/A	N/A	102.1	106.5	111.0
350	N/A	N/A	N/A	N/A	N/A	86.2	90.1	94.0	98.0
300	N/A	N/A	N/A	N/A	71.4	74.7	78.1	81.5	85.0
250	N/A	N/A	N/A	57.5	60.4	63.2	66.1	69.0	71.9
200	N/A	42.5	44.7	47.0	49.4	51.7	54.1	56.5	58.9
150	31.1	32.9	34.7	36.5	38.4	40.2	42.1	44.0	45.9
100	22.0	23.4	24.7	26.0	27.4	28.7	30.1	31.5	33.0

[1] The values are not guaranteed as standalone maximum specifications. They must be combined with static current per the equations of Electrical Characteristics on Page 24.
[2] Valid frequency and voltage ranges are model-specific. See Operating Conditions on Page 22.

FLASH MEMORY CHARACTERISTICS

Table 16. Reliability Characteristics

Parameter		Min	Unit	Test Method
N_{END}	Endurance	100,000	Cycles	JEDEC Standard A117
T_{DR}	Data Retention	20	Years	JEDEC Standard A103

Table 17. AC Operating Characteristics

Parameter		Min	Max	Unit
f_{CLK}	Serial Clock Frequency		$0.25 \times f_{SCLK}$	MHz
T_{SE}	Sector-Erase		450	ms
T_{BE}	Block-Erase		2000	ms
T_{SCE}	Chip-Erase		64	s
T_{BP}[1]	Byte-Program		50	µs
T_{PWU}[2]	Power-Up Time Delay Before Write Command	1	10	ms

[1] For multiple bytes after first byte within a page, $t_{BP(MAX)}$ increments by 12 × N, where N = number of bytes programmed after the first byte.
[2] Program, Erase, and Write instructions are ignored until T_{PWU} ms after flash power-on.

TIMING SPECIFICATIONS

Clock and Reset Timing

Table 24 and Figure 9 describe clock and reset operations. Per the CCLK and SCLK timing specifications in Table 10, Table 11, and Table 12 on Page 23, combinations of CLKIN and clock multipliers must not select core/peripheral clocks in excess of the processor's speed grade.

Table 24. Clock and Reset Timing

Parameter		Min	Max	Unit
Timing Requirements				
f_{CKIN}	CLKIN Frequency (Commercial/Industrial Models[1, 2, 3, 4]	12	50	MHz
f_{CKIN}	CLKIN Frequency (Automotive Models)[1, 2, 3, 4]	14	50	MHz
t_{CKINL}	CLKIN Low Pulse[1]	10		ns
t_{CKINH}	CLKIN High Pulse[1]	10		ns
t_{WRST}	$\overline{\text{RESET}}$ Asserted Pulse Width Low[5]	11 × t_{CKIN}		ns
Switching Characteristic				
$t_{BUFDLAY}$	CLKIN to CLKBUF Delay		11	ns

[1] Applies to PLL bypass mode and PLL nonbypass mode.
[2] Combinations of the CLKIN frequency and the PLL clock multiplier must not exceed the allowed f_{VCO}, f_{CCLK}, and f_{SCLK} settings discussed in Table 10 through Table 12 on Page 23.
[3] The t_{CKIN} period (see Figure 9) equals $1/f_{CKIN}$.
[4] If the DF bit in the PLL_CTL register is set, the minimum f_{CKIN} specification is 24 MHz for commercial/industrial models and 28 MHz for automotive models.
[5] Applies after power-up sequence is complete. See Table 25 and Figure 10 for power-up reset timing.

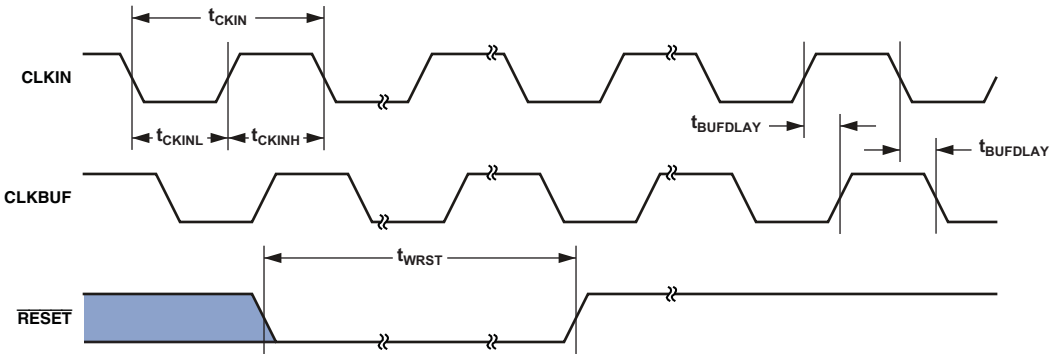

Figure 9. Clock and Reset Timing

RSI Controller Timing

Table 31 and Figure 20 describe RSI controller timing. Table 32 and Figure 21 describe RSI controller (high speed) timing.

Table 31. RSI Controller Timing

Parameter		Min	Max	Unit
Timing Requirements				
t_{ISU}	Input Setup Time	5.6		ns
t_{IH}	Input Hold Time	2		ns
Switching Characteristics				
f_{PP}[1]	Clock Frequency Data Transfer Mode	0	25	MHz
f_{OD}	Clock Frequency Identification Mode	100[2]	400	kHz
t_{WL}	Clock Low Time	10		ns
t_{WH}	Clock High Time	10		ns
t_{TLH}	Clock Rise Time		10	ns
t_{THL}	Clock Fall Time		10	ns
t_{ODLY}	Output Delay Time During Data Transfer Mode		14	ns
t_{ODLY}	Output Delay Time During Identification Mode		50	ns

[1] $t_{PP} = 1/f_{PP}$

[2] Specification can be 0 kHz, which means to stop the clock. The given minimum frequency range is for cases where a continuous clock is required.

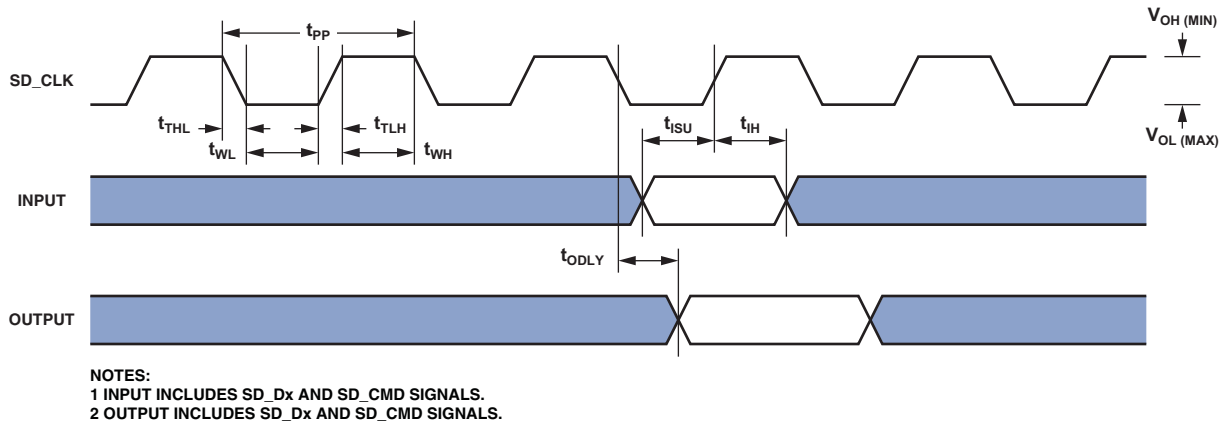

Figure 20. RSI Controller Timing

Table 32. RSI Controller Timing (High Speed Mode)

Parameter		Min	Max	Unit
Timing Requirements				
t_{ISU}	Input Setup Time	5.6		ns
t_{IH}	Input Hold Time	2		ns
Switching Characteristics				
f_{PP}[1]	Clock Frequency Data Transfer Mode	0	50	MHz
t_{WL}	Clock Low Time	7		ns
t_{WH}	Clock High Time	7		ns
t_{TLH}	Clock Rise Time		3	ns
t_{THL}	Clock Fall Time		3	ns
t_{ODLY}	Output Delay Time During Data Transfer Mode		4	ns
t_{OH}	Output Hold Time	2.75		ns

[1] $t_{PP} = 1/f_{PP}$

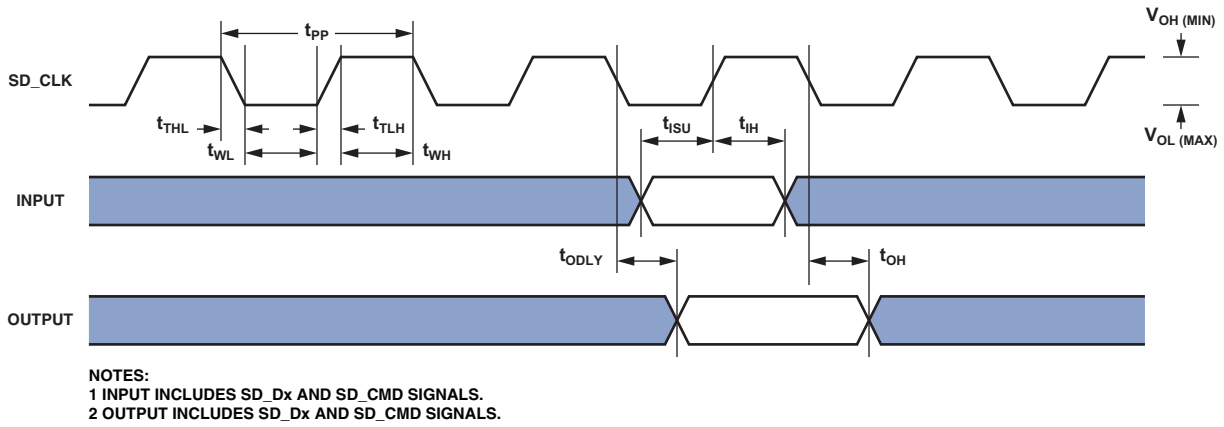

Figure 21. RSI Controller Timing (High Speed Mode)

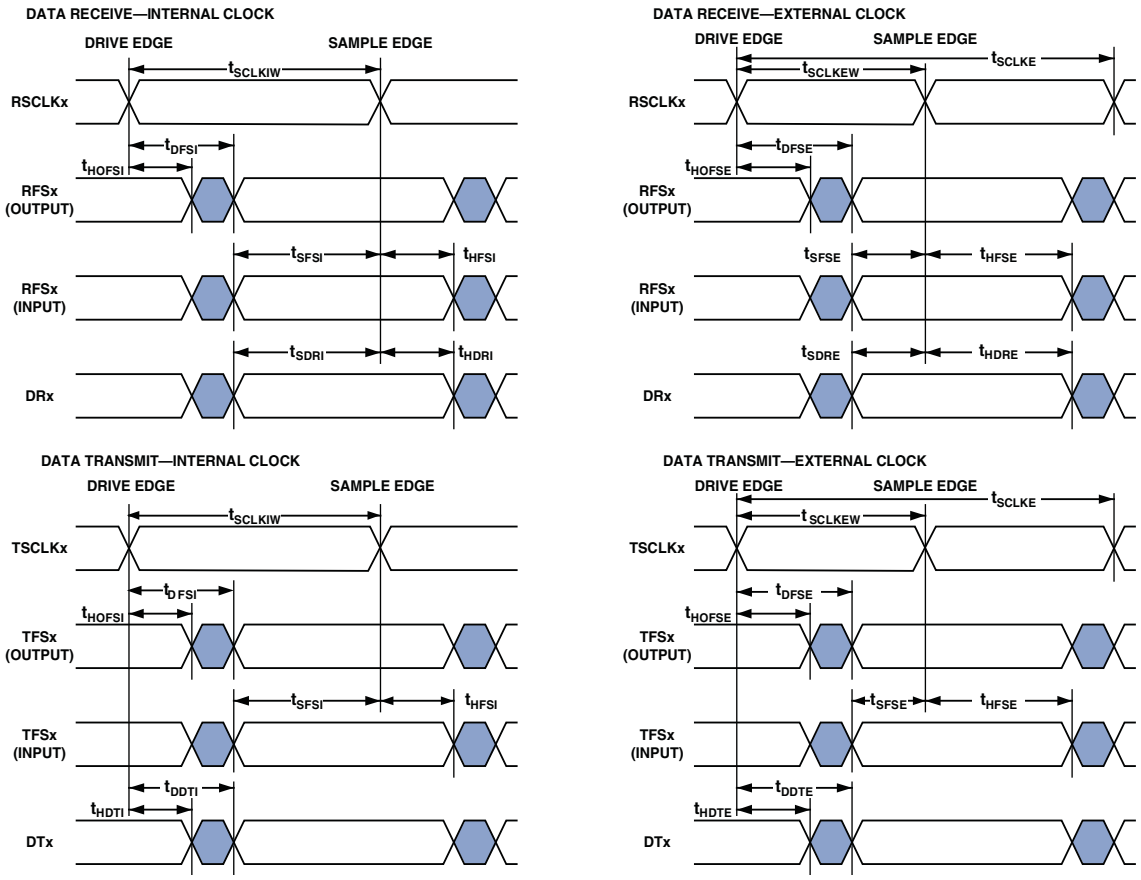

Figure 22. Serial Ports

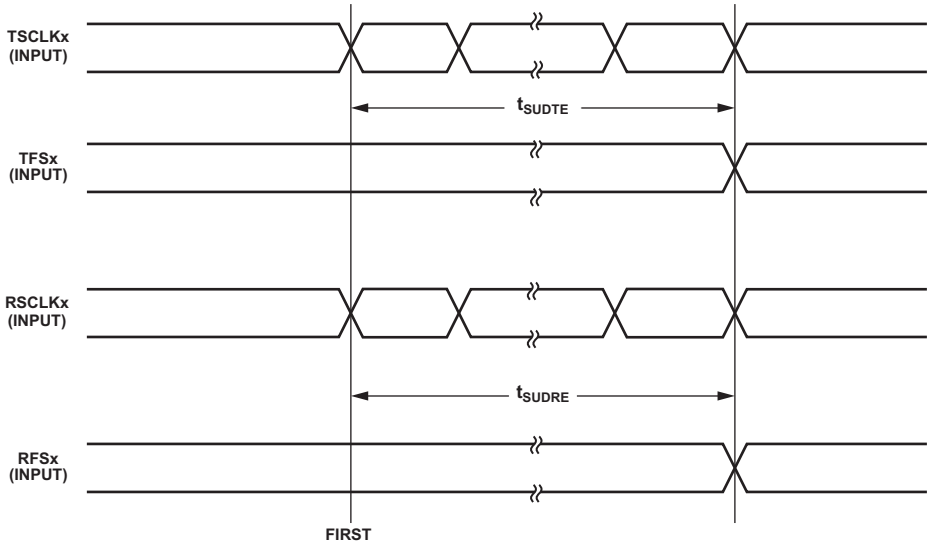

Figure 23. Serial Port Start Up with External Clock and Frame Sync

Table 35. Serial Ports—Enable and Three-State[1]

Parameter		Min	Max	Unit
Switching Characteristics				
t_{DTENE}	Data Enable Delay from External TSCLKx	0		ns
t_{DDTTE}	Data Disable Delay from External TSCLKx		t_{SCLK} + 1	ns
t_{DTENI}	Data Enable Delay from Internal TSCLKx	–2.0		ns
t_{DDTTI}	Data Disable Delay from Internal TSCLKx		t_{SCLK} + 1	ns

[1] Referenced to drive edge.

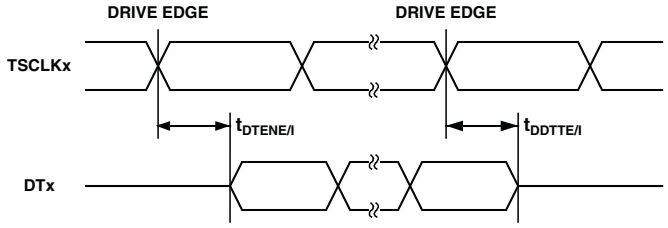

Figure 24. Enable and Three-State

JTAG Test And Emulation Port Timing

Table 49 and Figure 38 describe JTAG port operations.

Table 49. JTAG Port Timing

Parameter		Min	Max	Unit
Timing Requirements				
t_{TCK}	TCK Period	20		ns
t_{STAP}	TDI, TMS Setup Before TCK High	4		ns
t_{HTAP}	TDI, TMS Hold After TCK High	4		ns
t_{SSYS}[1]	System Inputs Setup Before TCK High	4		ns
t_{HSYS}[1]	System Inputs Hold After TCK High	5		ns
t_{TRSTW}	$\overline{TRST}$ Pulse Width[2] (measured in TCK cycles)	4		TCK
Switching Characteristics				
t_{DTDO}	TDO Delay from TCK Low		10	ns
t_{DSYS}[3]	System Outputs Delay After TCK Low	0	13	ns

[1] System Inputs = DATA15–0, SCL, SDA, TFS0, TSCLK0, RSCLK0, RFS0, DR0PRI, DR0SEC, PF15–0, PG15–0, PH7–0, MDIO, TD1, TMS, $\overline{RESET}$, $\overline{NMI}$, BMODE2–0.
[2] 50 MHz Maximum.
[3] System Outputs = DATA15–0, ADDR19–1, $\overline{ABE1–0}$, $\overline{ARE}$, $\overline{AWE}$, $\overline{AMS1–0}$, $\overline{SRAS}$, $\overline{SCAS}$, $\overline{SWE}$, SCKE, CLKOUT, SA10, $\overline{SMS}$, SCL, SDA, TSCLK0, TFS0, RFS0, RSCLK0, DT0PRI, DT0SEC, PF15–0, PG15–0, PH7–0, MDC, MDIO.

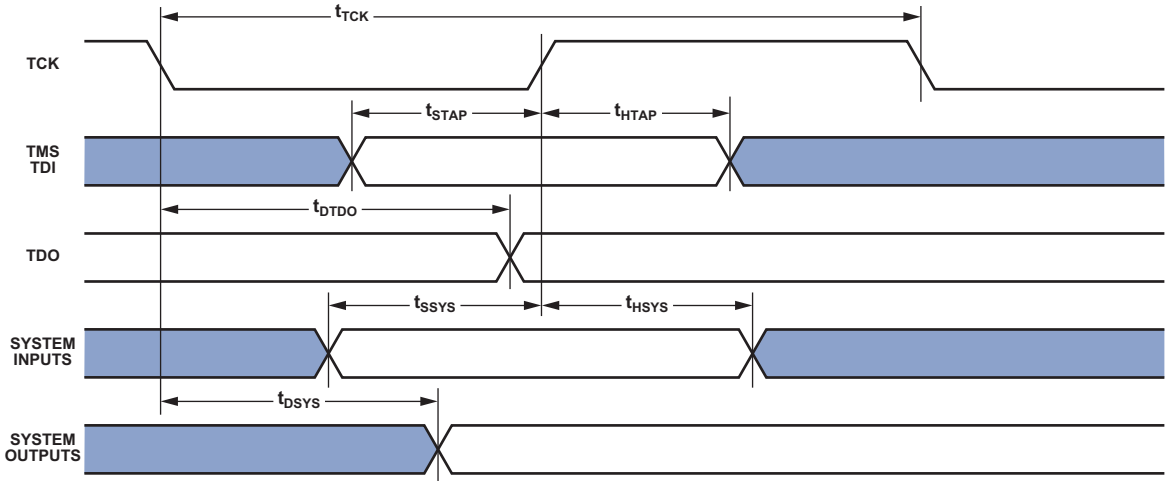

Figure 38. JTAG Port Timing

OUTPUT DRIVE CURRENTS

Figure 39 through Figure 53 show typical current-voltage characteristics for the output drivers of the ADSP-BF51xF processors.

The curves represent the current drive capability of the output drivers. See Table 8 on Page 19 for information about which driver type corresponds to a particular ball.

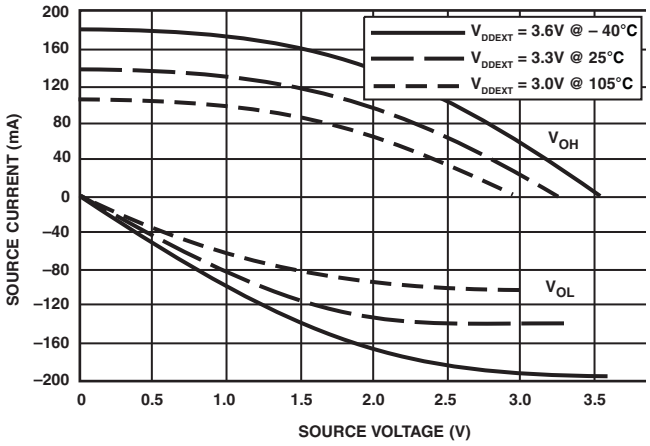

Figure 39. Driver Type A Current (3.3V V_{DDEXT}/V_{DDMEM})

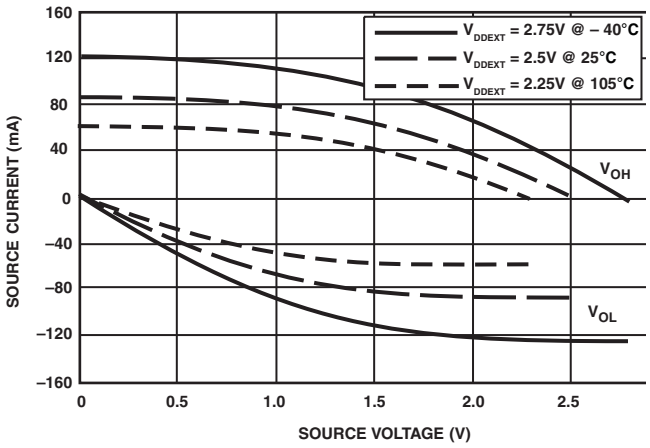

Figure 40. Driver Type A Current (2.5V V_{DDEXT}/V_{DDMEM})

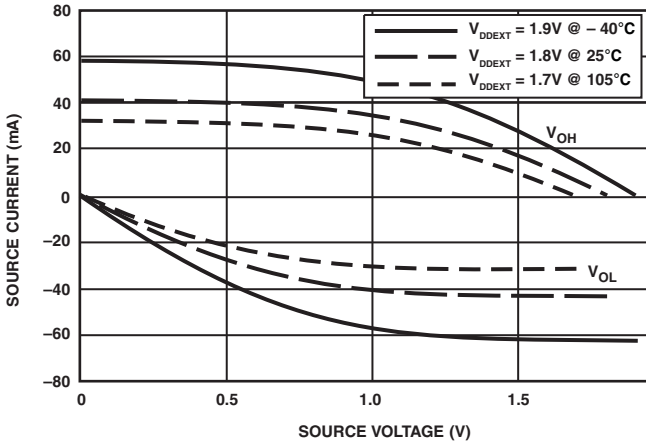

Figure 41. Driver Type A Current (1.8V V_{DDEXT}/V_{DDMEM})

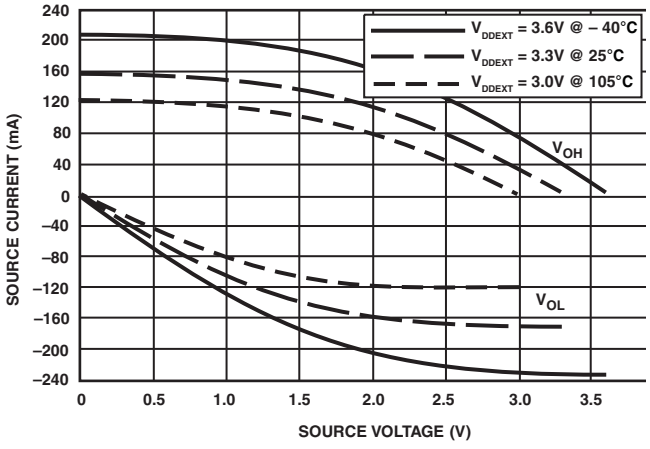

Figure 42. Driver Type B Current (3.3V V_{DDEXT}/V_{DDMEM})

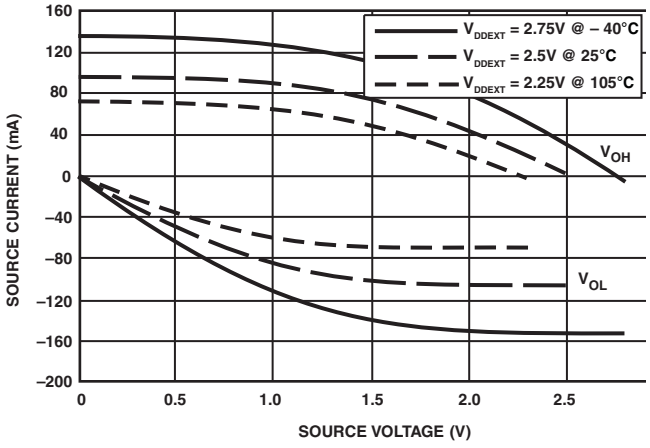

Figure 43. Driver Type B Current (2.5V V_{DDEXT}/V_{DDMEM})

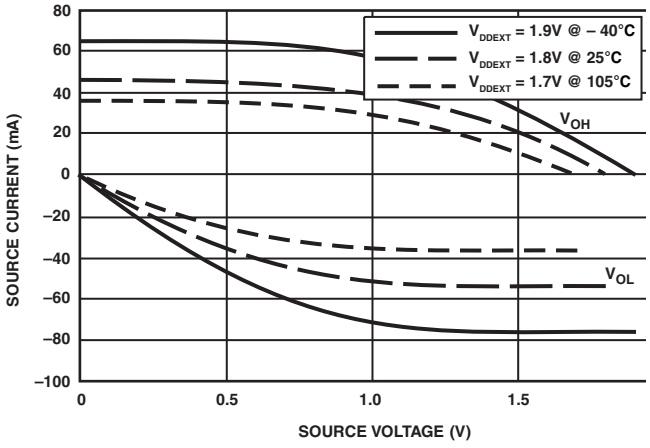

Figure 44. Driver Type B Current (1.8V V_{DDEXT}/V_{DDMEM})

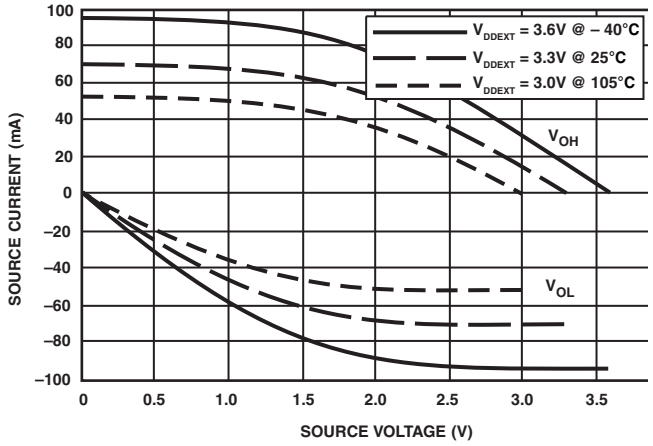

Figure 45. Driver Type C Current (3.3V V_{DDEXT}/V_{DDMEM})

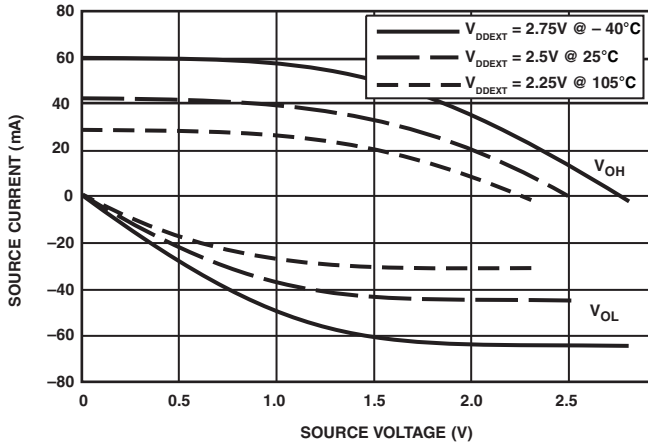

Figure 46. Drive Type C Current (2.5V V_{DDEXT}/V_{DDMEM})

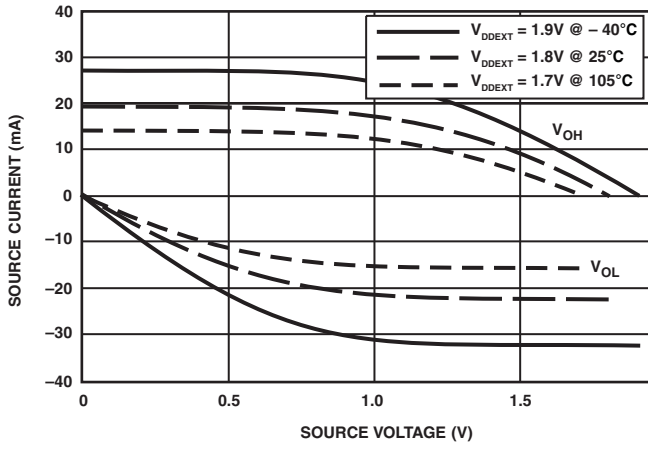

Figure 47. Driver Type C Current (1.8V V_{DDEXT}/V_{DDMEM})

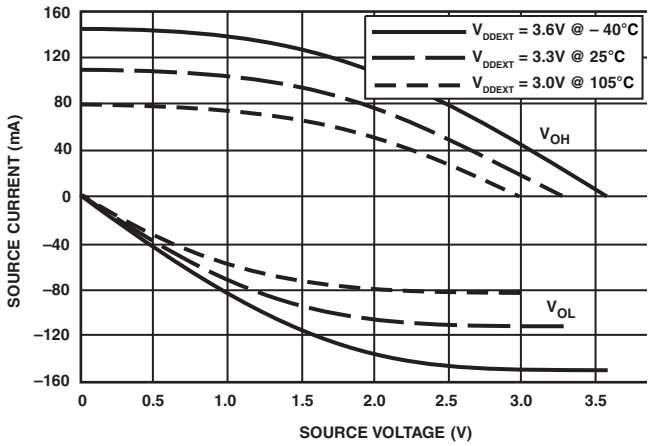

Figure 48. Driver Type D Current (3.3V V_{DDEXT}/V_{DDMEM})

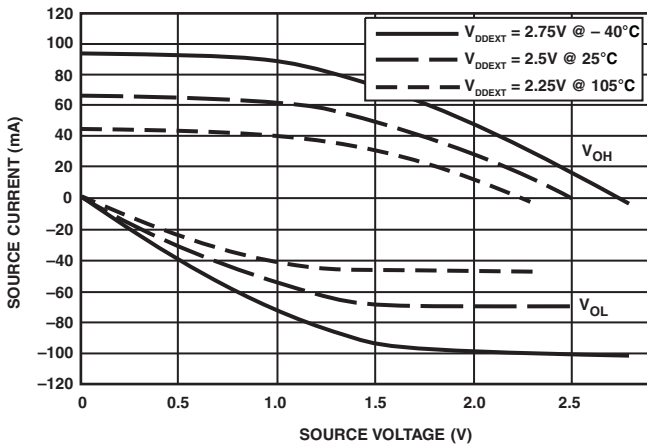

Figure 49. Driver Type D Current (2.5V V_{DDEXT}/V_{DDMEM})

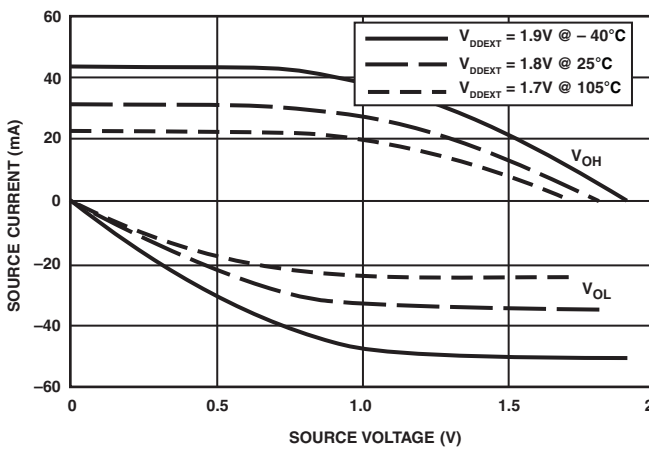

Figure 50. Driver Type D Current (1.8V V_{DDEXT}/V_{DDMEM})

THERMAL CHARACTERISTICS

To determine the junction temperature on the application printed circuit board use:

$$T_J = T_{CASE} + (\Psi_{JT} \times P_D)$$

where:

T_J = Junction temperature (°C)

T_{CASE} = Case temperature (°C) measured by customer at top center of package.

Ψ_{JT} = From Table 51

P_D = Power dissipation (see Total Power Dissipation on Page 25 for the method to calculate P_D)

Values of θ_{JA} are provided for package comparison and printed circuit board design considerations. θ_{JA} can be used for a first order approximation of T_J by the equation:

$$T_J = T_A + (\theta_{JA} \times P_D)$$

where:

T_A = Ambient temperature (°C)

Values of θ_{JC} are provided for package comparison and printed circuit board design considerations when an external heat sink is required.

Values of θ_{JB} are provided for package comparison and printed circuit board design considerations.

In Table 51, airflow measurements comply with JEDEC standards JESD51-2 and JESD51-6, and the junction-to-board measurement complies with JESD51-8. The junction-to-case measurement complies with MIL-STD-883 (Method 1012.1). All measurements use a 2S2P JEDEC test board.

The LQFP_EP package requires thermal trace squares and thermal vias to an embedded ground plane in the PCB. The paddle must be connected to ground for proper operation to data sheet specifications. Refer to JEDEC standard JESD51-5 for more information.

Table 50. Thermal Characteristics for SQ-176-2 Package

Parameter	Condition	Typical	Unit
θ_{JA}	0 Linear m/s Airflow	17.4	°C/W
θ_{JMA}	1 Linear m/s Airflow	14.8	°C/W
θ_{JMA}	2 Linear m/s Airflow	14.0	°C/W
θ_{JC}	Not Applicable	7.8	°C/W
Ψ_{JT}	0 Linear m/s Airflow	0.28	°C/W
Ψ_{JT}	1 Linear m/s Airflow	0.39	°C/W
Ψ_{JT}	2 Linear m/s Airflow	0.48	°C/W

Table 51. Thermal Characteristics for BC-168-1 Package

Parameter	Condition	Typical	Unit
θ_{JA}	0 Linear m/s Airflow	30.5	°C/W
θ_{JMA}	1 Linear m/s Airflow	27.6	°C/W
θ_{JMA}	2 Linear m/s Airflow	26.3	°C/W
θ_{JC}	Not Applicable	11.1	°C/W
Ψ_{JT}	0 Linear m/s Airflow	0.20	°C/W
Ψ_{JT}	1 Linear m/s Airflow	0.35	°C/W
Ψ_{JT}	2 Linear m/s Airflow	0.45	°C/W

Figure 69 shows the top view of the LQFP_EP lead configuration. Figure 70 shows the bottom view of the LQFP_EP lead configuration.

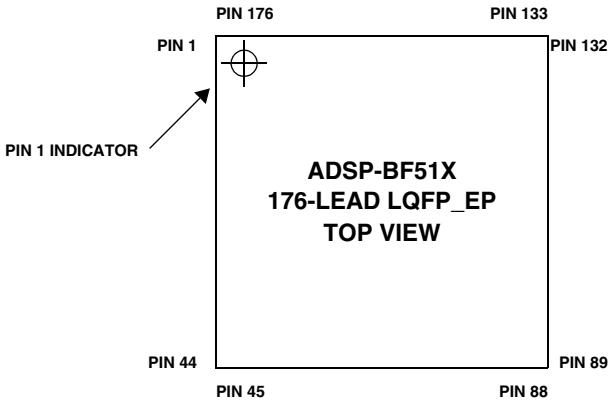

Figure 69. 176-Lead LQFP_EP Lead Configuration (Top View)

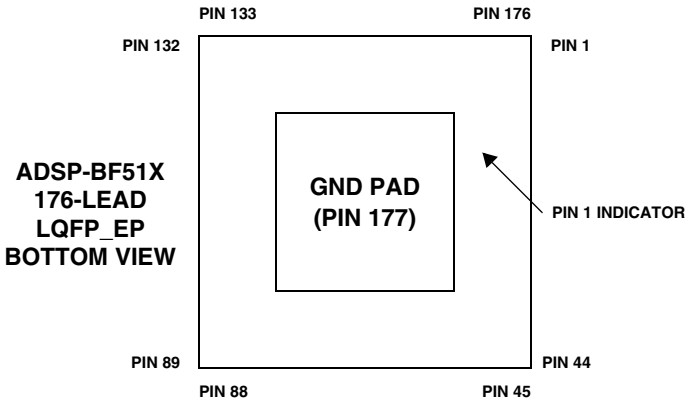

Figure 70. 176-Lead LQFP_EP Lead Configuration (Bottom View)

OUTLINE DIMENSIONS

Dimensions in Figure 73 are shown in millimeters.

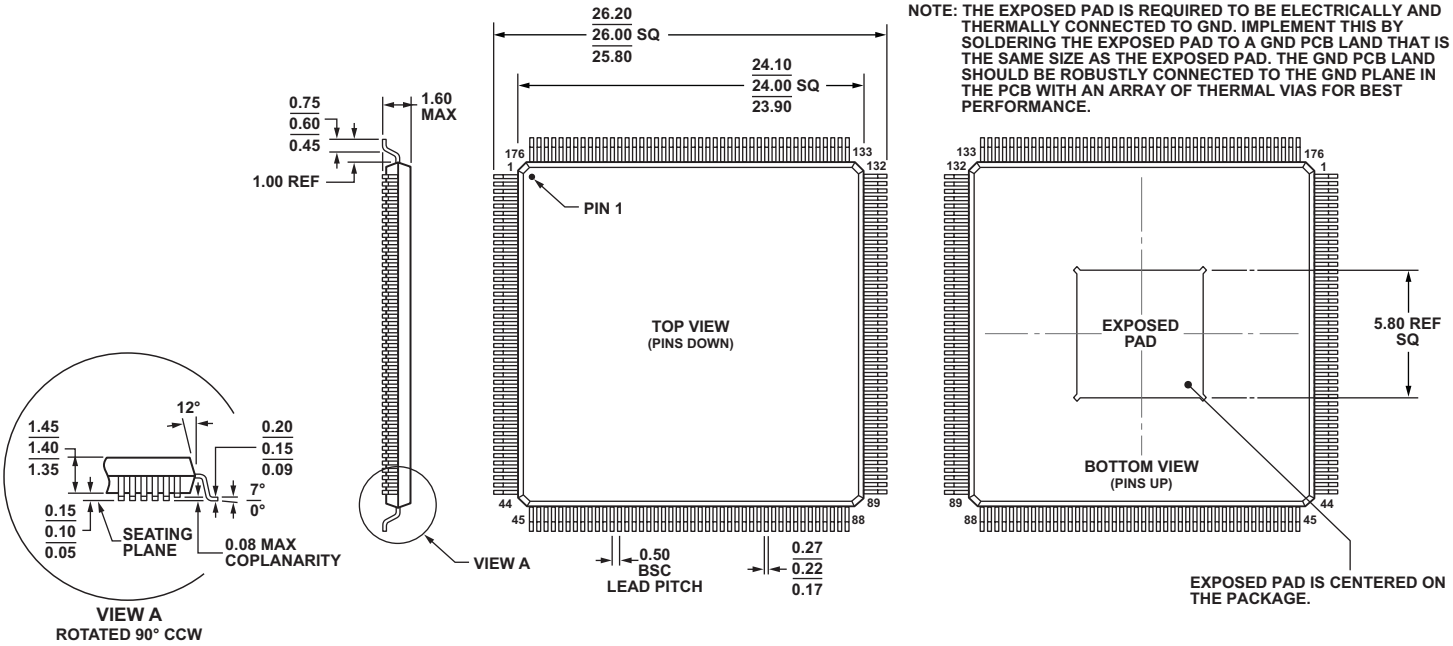

Figure 73. 176-Lead Low Profile Quad Flat Package [LQFP_EP]
(SQ-176-2)
Dimensions shown in millimeters