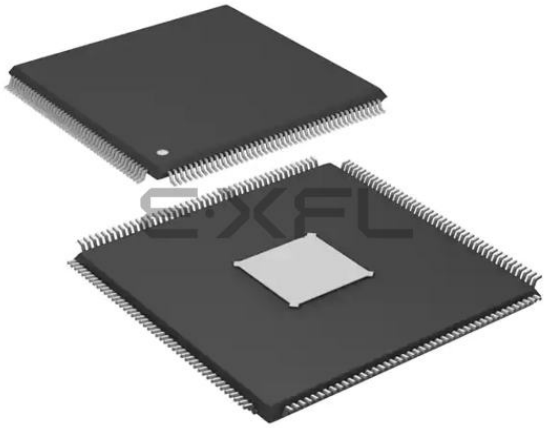

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

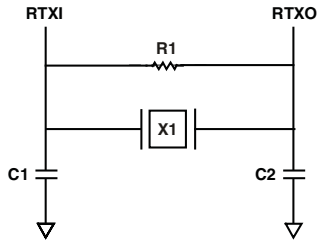
Details	
Product Status	Active
Type	Fixed Point
Interface	I²C, PPI, SPI, SPORT, UART/USART
Clock Rate	400MHz
Non-Volatile Memory	External
On-Chip RAM	116kB
Voltage - I/O	1.8V, 2.5V, 3.3V
Voltage - Core	1.30V
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP Exposed Pad
Supplier Device Package	176-LQFP-EP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adbf512wbswz402

When enabled, the alarm function generates an interrupt when the output of the timer matches the programmed value in the alarm control register. There are two alarms: The first alarm is for a time of day. The second alarm is for a day and time of that day.

The stopwatch function counts down from a programmed value, with one-second resolution. When the stopwatch is enabled and the counter underflows, an interrupt is generated.

Like the other peripherals, the RTC can wake up the processor from sleep mode upon generation of any RTC wakeup event. Additionally, an RTC wakeup event can wake up the processor from deep sleep mode or cause a transition from the hibernate state.

Connect RTC signals RTXI and RTXO with external components as shown in Figure 5.



SUGGESTED COMPONENTS:
X1 = ECLIPTEK EC38J (THROUGH-HOLE PACKAGE) OR
EPSON MC405 12 pF LOAD (SURFACE-MOUNT PACKAGE)
C1 = 22 pF
C2 = 22 pF
R1 = 10 MΩ
NOTE: C1 AND C2 ARE SPECIFIC TO CRYSTAL SPECIFIED FOR X1. CONTACT CRYSTAL MANUFACTURER FOR DETAILS. C1 AND C2 SPECIFICATIONS ASSUME BOARD TRACE CAPACITANCE OF 3 pF.

Figure 5. External Components for RTC

Watchdog Timer

The ADSP-BF51x processors include a 32-bit timer that can be used to implement a software watchdog function. A software watchdog can improve system availability by forcing the processor to a known state through generation of a hardware reset, nonmaskable interrupt (NMI), or general-purpose interrupt, if the timer expires before being reset by software. The programmer initializes the count value of the timer, enables the appropriate interrupt, then enables the timer. Thereafter, the software must reload the counter before it counts to zero from the programmed value. This protects the system from remaining in an unknown state where software, which would normally reset the timer, has stopped running due to an external noise condition or software error.

If configured to generate a hardware reset, the watchdog timer resets both the core and the processor peripherals. After a reset, software can determine if the watchdog was the source of the hardware reset by interrogating a status bit in the watchdog timer control register.

The timer is clocked by the system clock (SCLK) at a maximum frequency of f_{SCLK}.

Timers

There are nine general-purpose programmable timer units in the ADSP-BF51x processors. Eight timers have an external signal that can be configured either as a pulse width modulator (PWM) or timer output, as an input to clock the timer, or as a mechanism for measuring pulse widths and periods of external events. These timers can be synchronized to an external clock input to the several other associated PF signals, an external clock input to the PPI_CLK input signal, or to the internal SCLK.

The timer units can be used in conjunction with the two UARTs to measure the width of the pulses in the data stream to provide a software auto-baud detect function for the respective serial channels.

The timers can generate interrupts to the processor core providing periodic events for synchronization, either to the system clock or to a count of external signals.

In addition to the eight general-purpose programmable timers, a ninth timer is also provided. This extra timer is clocked by the internal processor clock and is typically used as a system tick clock for generation of operating system periodic interrupts.

3-Phase PWM

The processors integrate a flexible and programmable 3-phase PWM waveform generator that can be programmed to generate the required switching patterns to drive a 3-phase voltage source inverter for ac induction (ACIM) or permanent magnet synchronous (PMSM) motor control. In addition, the PWM block contains special functions that considerably simplify the generation of the required PWM switching patterns for control of the electronically commutated motor (ECM) or brushless dc motor (BDCM). Software can enable a special mode for switched reluctance motors (SRM).

Features of the 3-phase PWM generation unit are:

- 16-bit center-based PWM generation unit
- Programmable PWM pulse width
- Single/double update modes
- Programmable dead time and switching frequency
- Twos-complement implementation which permits smooth transition to full ON and full OFF states
- Possibility to synchronize the PWM generation to an external synchronization
- Special provisions for BDCM operation (crossover and output enable functions)
- Wide variety of special switched reluctance (SR) operating modes
- Output polarity and clock gating control
- Dedicated asynchronous PWM shutdown signal

General-Purpose (GP) Counter

A 32-bit GP counter is provided that can sense 2-bit quadrature or binary codes as typically emitted by industrial drives or manual thumb wheels. The counter can also operate in

general-purpose up/down count modes. Then, count direction is either controlled by a level-sensitive input signal or by two edge detectors.

A third input can provide flexible zero marker support and can alternatively be used to input the push-button signal of thumb wheels. All three signals have a programmable debouncing circuit.

An internal signal forwarded to the GP timer unit enables one timer to measure the intervals between count events. Boundary registers enable auto-zero operation or simple system warning by interrupts when programmable count values are exceeded.

Serial Ports

The ADSP-BF51x processors incorporate two dual-channel synchronous serial ports (SPORT0 and SPORT1) for serial and multiprocessor communications. The SPORTs support the following features:

Serial port data can be automatically transferred to and from on-chip memory/external memory via dedicated DMA channels. Each of the serial ports can work in conjunction with another serial port to provide TDM support. In this configuration, one SPORT provides two transmit signals while the other SPORT provides the two receive signals. The frame sync and clock are shared.

Serial ports operate in five modes:

- Standard DSP serial mode
- Multichannel (TDM) mode
- I^2S mode
- Packed I^2S mode
- Left-justified mode

Serial Peripheral Interface (SPI) Ports

The processors have two SPI-compatible ports (SPI0 and SPI1) that enable the processor to communicate with multiple SPI-compatible devices.

The SPI interface uses three signals for transferring data: two data signals (master output-slave input–MOSI, and master input-slave output–MISO) and a clock signal (serial clock–SCK). An SPI chip select input signal ($\overline{\text{SPIxSS}}$) lets other SPI devices select the processor, and multiple SPI chip select output signals let the processor select other SPI devices. The SPI select signals are reconfigured general-purpose I/O signals. Using these signals, the SPI port provides a full-duplex, synchronous serial interface, which supports both master/slave modes and multimaster environments.

The SPI port baud rate and clock phase/polarities are programmable, and it has an integrated DMA channel, configurable to support transmit or receive data streams. The SPI's DMA channel can only service unidirectional accesses at any given time.

UART Ports

The processors provide two full-duplex universal asynchronous receiver/transmitter (UART) ports, which are fully compatible with PC-standard UARTs. Each UART port provides a simplified UART interface to other peripherals or hosts, supporting full-duplex, DMA-supported, asynchronous transfers of serial data. A UART port includes support for five to eight data bits, and none, even, or odd parity. Optionally, an additional address bit can be transferred to interrupt only addressed nodes in multi-drop bus (MDB) systems. A frame is terminates by one, one and a half, two or two and a half stop bits.

The UART ports support automatic hardware flow control through the Clear To Send (CTS) input and Request To Send (RTS) output with programmable assertion FIFO levels.

To help support the Local Interconnect Network (LIN) protocols, a special command causes the transmitter to queue a break command of programmable bit length into the transmit buffer. Similarly, the number of stop bits can be extended by a programmable inter-frame space.

The capabilities of the UARTs are further extended with support for the Infrared Data Association (IrDA®) serial infrared physical layer link specification (SIR) protocol.

2-Wire Interface (TWI)

The processors include a TWI module for providing a simple exchange method of control data between multiple devices. The TWI is compatible with the widely used I^2C® bus standard. The TWI module offers the capabilities of simultaneous master and slave operation, support for both 7-bit addressing and multimedia data arbitration. The TWI interface utilizes two signals for transferring clock (SCL) and data (SDA) and supports the protocol at speeds up to 400k bits/sec. The TWI interface signals are compatible with 5 V logic levels.

Additionally, the processor's TWI module is fully compatible with serial camera control bus (SCCB) functionality for easier control of various CMOS camera sensor devices.

Removable Storage Interface (RSI)

The RSI controller, available on the ADSP-BF514/ADSP-BF514F16/ADSP-BF516/ADSP-BF518/ADSP-BF518F16 processors, acts as the host interface for multi-media cards (MMC), secure digital memory cards (SD Card), secure digital input/output cards (SDIO), and CE-ATA hard disk drives. The following list describes the main features of the RSI controller.

- Support for a single MMC, SD memory, SDIO card or CE-ATA hard disk drive
- Support for 1-bit and 4-bit SD modes
- Support for 1-bit, 4-bit and 8-bit MMC modes
- Support for 4-bit and 8-bit CE-ATA hard disk drives
- A ten-signal external interface with clock, command, and up to eight data lines
- Card detection using one of the data signals
- Card interface clock generation from SCLK
- SDIO interrupt and read wait features
- CE-ATA command completion signal recognition and disable

In the active mode, it is possible to disable the PLL through the PLL control register (PLL_CTL). If disabled, the PLL must be re-enabled before transitioning to the full-on or sleep modes.

Sleep Operating Mode—High Dynamic Power Savings

The sleep mode reduces dynamic power dissipation by disabling the clock to the processor core (CCLK). The PLL and system clock (SCLK), however, continue to operate in this mode. Typically an external event or RTC activity wakes up the processor. When in the sleep mode, asserting wakeup causes the processor to sense the value of the BYPASS bit in the PLL control register (PLL_CTL). If BYPASS is disabled, the processor transitions to the full on mode. If BYPASS is enabled, the processor transitions to the active mode.

System DMA access to L1 memory is not supported in sleep mode.

Deep Sleep Operating Mode—Maximum Dynamic Power Savings

The deep sleep mode maximizes dynamic power savings by disabling the clocks to the processor core (CCLK) and to all synchronous peripherals (SCLK). Asynchronous peripherals, such as the RTC, may still be running but cannot access internal resources or external memory. This powered-down mode can only be exited by assertion of the reset interrupt ($\overline{\text{RESET}}$) or by an asynchronous interrupt generated by the RTC. When in deep sleep mode, an RTC asynchronous interrupt causes the processor to transition to the Active mode. Assertion of $\overline{\text{RESET}}$ while in deep sleep mode causes the processor to transition to the full on mode.

Hibernate State—Maximum Static Power Savings

The hibernate state maximizes static power savings by disabling the voltage and clocks to the processor core (CCLK) and system blocks (SCLK). Any critical information stored internally (for example memory contents, register contents) must be written to a non-volatile storage device prior to removing power if the processor state is to be preserved. Writing b#00 to the FREQ bits in the VR_CTL register also causes the EXT_WAKE signal to transition low, which can be used to signal an external voltage regulator to shut down.

Since V_{DDEXT} is still supplied in this mode, all of the external signals three-state, unless otherwise specified. This allows other devices that may be connected to the processor to still have power applied without drawing unwanted current.

The Ethernet module can signal an external regulator to wake up using the EXT_WAKE signal. If PF15 does not connect as a $\overline{\text{PHYINT}}$ signal to an external PHY device, it can be pulled low by any other device to wake the processor up. The processor can also be woken up by a real-time clock wakeup event or by asserting the $\overline{\text{RESET}}$ pin. All hibernate wakeup events initiate the hardware reset sequence. Individual sources are enabled by the VR_CTL register. The EXT_WAKE signal is provided to indicate the occurrence of wakeup events.

With the exception of the VR_CTL and the RTC registers, all internal registers and memories lose their content in the hibernate state. State variables may be held in external SRAM or SDRAM. The SCKELOW bit in the VR_CTL register controls whether or not SDRAM operates in self-refresh mode, which allows it to retain its content while the processor is in hibernation and through the subsequent reset sequence.

Power Savings

As shown in Table 4, the processors support up to six different power domains, which maximizes flexibility while maintaining compliance with industry standards and conventions. By isolating the internal logic of the processor into its own power domain, separate from the RTC and other I/O, the processor can take advantage of dynamic power management without affecting the RTC or other I/O devices. There are no sequencing requirements for the various power domains, but all domains must be powered according to the appropriate Specifications table for processor Operating Conditions; even if the feature/peripheral is not used.

Table 4. Power Domains

Power Domain	V_{DD} Range
All internal logic, except RTC, Memory, OTP	V_{DDINT}
RTC internal logic and crystal I/O	V_{DDRTC}
Memory logic	V_{DDMEM}
OTP logic	V_{DDOTP}
Optional internal flash	$V_{DDFLASH}$
All other I/O	V_{DDEXT}

The dynamic power management feature of the processor allows both the processor's input voltage (V_{DDINT}) and clock frequency (f_{CCLK}) to be dynamically controlled.

The power dissipated by a processor is largely a function of its clock frequency and the square of the operating voltage. For example, reducing the clock frequency by 25% results in a 25% reduction in dynamic power dissipation, while reducing the voltage by 25% reduces dynamic power dissipation by more than 40%. Further, these power savings are additive, in that if the clock frequency and supply voltage are both reduced, the power savings can be dramatic, as shown in the following equations.

$$\text{Power Savings Factor} = \frac{f_{CCLKRED}}{f_{CCLKNOM}} \times \left(\frac{V_{DDINTRED}}{V_{DDINTNOM}}\right)^2 \times \left(\frac{T_{RED}}{T_{NOM}}\right)$$

$$\%\ \text{Power Savings} = (1 - \text{Power Savings Factor}) \times 100\%$$

where the variables in the equations are:

$f_{CCLKNOM}$ is the nominal core clock frequency

$f_{CCLKRED}$ is the reduced core clock frequency

$V_{DDINTNOM}$ is the nominal internal supply voltage

$V_{DDINTRED}$ is the reduced internal supply voltage

All on-chip peripherals are clocked by the system clock (SCLK). The system clock frequency is programmable by means of the SSEL3–0 bits of the PLL_DIV register. The values programmed into the SSEL fields define a divide ratio between the PLL output (VCO) and the system clock. SCLK divider values are 1 through 15. Table 5 illustrates typical system clock ratios.

Table 5. Example System Clock Ratios

Signal Name SSEL3–0	Divider Ratio VCO/SCLK	Example Frequency Ratios (MHz)	
		VCO	SCLK
0010	2:1	100	50
0110	6:1	300	50
1010	10:1	400	40

Note that the divisor ratio must be chosen to limit the system clock frequency to its maximum of f_{SCLK}. The SSEL value can be changed dynamically without any PLL lock latencies by writing the appropriate values to the PLL divisor register (PLL_DIV).

The core clock (CCLK) frequency can also be dynamically changed by means of the CSEL1–0 bits of the PLL_DIV register. Supported CCLK divider ratios are 1, 2, 4, and 8, as shown in Table 6. This programmable core clock capability is useful for fast core frequency modifications.

Table 6. Core Clock Ratios

Signal Name CSEL1–0	Divider Ratio VCO/CCLK	Example Frequency Ratios (MHz)	
		VCO	CCLK
00	1:1	300	300
01	2:1	300	150
10	4:1	400	100
11	8:1	200	25

The maximum CCLK frequency not only depends on the part's speed grade (see Page 67), it also depends on the applied V_{DDINT} voltage. See Table 10 on Page 23 for details. The maximal system clock rate (SCLK) depends on the chip package and the applied V_{DDINT}, V_{DDEXT}, and V_{DDMEM} voltages (see Table 12 on Page 23).

BOOTING MODES

The processor has several mechanisms (listed in Table 7) for automatically loading internal and external memory after a reset. The boot mode is defined by three BMODE input bits dedicated to this purpose. There are two categories of boot modes. In master boot modes the processor actively loads data from parallel or serial memories. In slave boot modes the processor receives data from external host devices.

The boot modes listed in Table 7 provide a number of mechanisms for automatically loading the processor's internal and external memories after a reset. By default, all boot modes use the slowest meaningful configuration settings. Default settings can be altered via the initialization code feature at boot time or by proper OTP programming at pre-boot time. The BMODE bits of the reset configuration register, sampled during power-on resets and software-initiated resets, implement the modes shown in Table 7.

Table 7. Booting Modes

BMODE2–0	Description
000	Idle - No boot
001	Boot from 8- or 16-bit external flash memory
010	Boot from internal SPI memory
011	Boot from external SPI memory (EEPROM or flash)
100	Boot from SPI0 host
101	Boot from OTP memory
110	Boot from SDRAM
111	Boot from UART0 Host

- Idle/no boot mode (BMODE = 0x0)—In this mode, the processor goes into idle. The idle boot mode helps recover from illegal operating modes, such as when the user has mis configured the OTP memory.
- Boot from 8-bit or 16-bit external flash memory (BMODE = 0x1)—In this mode, the boot kernel loads the first block header from address 0x2000 0000 and—depending on instructions containing in the header—the boot kernel performs 8-bit or 16-bit boot or starts program execution at the address provided by the header. By default, all configuration settings are set for the slowest device possible (3-cycle hold time, 15-cycle R/W access times, 4-cycle setup).

  The ARDY is not enabled by default, but it can be enabled by OTP programming. Similarly, all interface behavior and timings can be customized by OTP programming. This includes activation of burst-mode or page-mode operation. In this mode, all signals belonging to the asynchronous interface are enabled at the port muxing level.
- Boot from internal SPI memory (BMODE = 0x2)—The processor uses the internal PH8 GPIO signal to load code previously loaded to the 16M bit internal SPI flash connected to SPI0. Only available on the ADSP-BF51xF processors.
- Boot from external SPI EEPROM or flash (BMODE = 0x3)—8-bit, 16-bit, 24-bit or 32-bit addressable devices are supported. The processor uses the PG15 GPIO signal (at $\overline{\text{SPI0SEL2}}$) to select a single SPI EEPROM/flash device connected to the SPI0 interface; then submits a read command and successive address bytes (0x00) until a valid 8-, 16-, 24-, or 32-bit addressable device is detected. Pull-up resistors are required on the SSEL and MISO signals. By default, a value of 0x85 is written to the SPI0_BAUD register.

SIGNAL DESCRIPTIONS

The processors' signal definitions are listed in Table 8. In order to maintain maximum function and reduce package size and signal count, some signals have dual, multiplexed functions. In cases where signal function is reconfigurable, the default state is shown in plain text, while the alternate function is shown in italics.

All pins are three-stated during and immediately after reset, with the exception of the external memory interface, asynchronous and synchronous memory control, and the buffered XTAL output pin (CLKBUF). On the external memory interface, the control and address lines are driven high, with the exception of CLKOUT, which toggles at the system clock rate. During hibernate all outputs are three-stated unless otherwise noted in Table 8.

All I/O signals have their input buffers disabled with the exception of the signals noted in the data sheet that need pull-ups or pull downs if unused.

The SDA (serial data) and SCL (serial clock) pins/balls are open drain and therefore require a pullup resistor. Consult version 2.1 of the I^2C specification for the proper resistor value.

It is strongly advised to use the available IBIS models to ensure that a given board design meets overshoot/undershoot and signal integrity requirements. If no IBIS simulation is performed, it is strongly recommended to add series resistor terminations for all Driver Types A, C and D. The termination resistors should be placed near the processor to reduce transients and improve signal integrity. The resistance value, typically 33 Ω or 47 Ω, should be chosen to match the average board trace impedance. Additionally, adding a parallel termination to CLKOUT may prove useful in further enhancing signal integrity. Be sure to verify overshoot/undershoot and signal integrity specifications on actual hardware.

Table 8. Signal Descriptions

Signal Name	Type	Function	Driver Type[1]
EBIU			
ADDR19–1	O	Address Bus	A
DATA15–0	I/O	Data Bus	A
$\overline{\text{ABE1–0}}$/*SDQM1–0*	O	Byte Enable or Data Mask	A
$\overline{\text{AMS1–0}}$	O	Asynchronous Memory Bank Selects (Require pull-ups if hibernate is used)	A
$\overline{\text{ARE}}$	O	Asynchronous Memory Read Enable	A
$\overline{\text{AWE}}$	O	Asynchronous Memory Write Enable	A
$\overline{\text{SRAS}}$	O	SDRAM Row Address Strobe	A
$\overline{\text{SCAS}}$	O	SDRAM Column Address Strobe	A
$\overline{\text{SWE}}$	O	SDRAM Write Enable	A
SCKE	O	SDRAM Clock Enable (Requires a pull-down if hibernate with SDRAM self-refresh is used)	A
CLKOUT	O	SDRAM Clock Output	B
SA10	O	SDRAM A10 Signal	A
$\overline{\text{SMS}}$	O	SDRAM Bank Select	A
Port F: GPIO and Multiplexed Peripherals			
PF0/*ETxD2/PPI D0/*$\overline{\textit{SPI1SEL2}}$*/TACLK6*	I/O	GPIO/*Ethernet MII Transmit D2/PPI Data 0/SPI1 Slave Select 2/Timer6 Alternate Clock*	C
PF1/*ERxD2/PPI D1/PWM AH/TACLK7*	I/O	GPIO/*Ethernet MII Receive D2/PPI Data 1/PWM AH Output/Timer7 Alternate Clock*	C
PF2/*ETxD3/PPI D2/PWM AL*	I/O	GPIO/*Ethernet Transmit D3/PPI Data 2/PWM AL Output*	C
PF3/*ERxD3/PPI D3/PWM BH/TACLK0*	I/O	GPIO/*Ethernet MII Data Receive D3/PPI Data 3/PWM BH Output/Timer0 Alternate Clock*	C
PF4/*ERxCLK/PPI D4/PWM BL/TACLK1*	I/O	GPIO/*Ethernet MII Receive Clock/PPI Data 4/PWM BL Out/Timer1 Alternate CLK*	C
PF5/*ERxDV/PPI D5/PWM CH/TACI0*	I/O	GPIO/*Ethernet MII Receive Data Valid/PPI Data 5/PWM CH Out /Timer0 Alternate Capture Input*	C
PF6/*COL/PPI D6/PWM CL/TACI1*	I/O	GPIO/*Ethernet MII Collision/PPI Data 6/PWM CL Out/Timer1 Alternate Capture Input*	C
PF7/$\overline{\textit{SPI0SEL1}}$*/PPI D7/PWMSYNC*	I/O	GPIO/*SPI0 Slave Select 1/PPI Data 7/PWM Sync*	C

Table 8. Signal Descriptions (Continued)

Signal Name	Type	Function	Driver Type[1]
PF8/*MDC*/PPI D8/*SPI1SEL4*	I/O	GPIO/*Ethernet Management Channel Clock/PPI Data 8/SPI1 Slave Select 4*	C
PF9/*MDIO*/*PPI D9*/*TMR2*	I/O	GPIO/*Ethernet Management Channel Serial Data/PPI Data 9/Timer 2*	C
PF10/*ETxD0*/*PPI D10*/*TMR3*	I/O	GPIO/*Ethernet MII or RMII Transmit D0/PPI Data 10/Timer 3*	C
PF11/*ERxD0*/*PPI D11*/*PWM AH*/*TACI3*	I/O	GPIO/*Ethernet MII Receive D0/PPI Data 11/PWM AH output /Timer3 Alternate Capture Input*	C
PF12/*ETxD1*/*PPI D12*/*PWM AL*	I/O	GPIO/*Ethernet MII Transmit D1/PPI Data 12/PWM AL Output*	C
PF13/*ERxD1*/*PPI D13*/*PWM BH*	I/O	GPIO/*Ethernet MII or RMII Receive D1/PPI Data 13/PWM BH Output*	C
PF14/*ETxEN*/*PPI D14*/*PWM BL*	I/O	GPIO/*Ethernet MII Transmit Enable/PPI Data 14/PWM BL Out*	C
PF15[2]/*RMII PHYINT*/*PPI D15*/*PWM_SYNCA*	I/O	GPIO/*Ethernet MII PHY Interrupt/PPI Data 15/Alternate PWM Sync*	C
Port G: GPIO and Multiplexed Peripherals			
PG0/*MIICRS*/*RMIICRS*/*HWAIT*[3]/*SPI1SEL3*	I/O	GPIO/*Ethernet MII or RMII Carrier Sense or RMII Data Valid/HWAIT/SPI1 Slave Select3*	C
PG1/*ERxER*/*DMAR1*/*PWM CH*	I/O	GPIO/*Ethernet MII or RMII Receive Error/DMA Req 1/PWM CH Out*	C
PG2/*MIITxCLK*/*RMIIREF_CLK*/*DMAR0*/*PWM CL*	I/O	GPIO/*Ethernet MII or RMII Reference Clock/DMA Req 0/PWM CL Out*	C
PG3/*DR0PRI*/*RSI_DATA0*/*SPI0SEL5*/*TACLK3*	I/O	GPIO/*SPORT0 Primary Rx Data/RSI Data 0/SPI0 Slave Select 5/Timer3 Alternate CLK*	C
PG4/*RSCLK0*/*RSI_DATA1*/*TMR5*/*TACI5*	I/O	GPIO/*SPORT0 Rx Clock/RSI Data 1/Timer 5/Timer5 Alternate Capture Input*	D
PG5/*RFS0*/*RSI_DATA2*/*PPICLK*/*TMRCLK*	I/O	GPIO/*SPORT0 Rx Frame Sync/RSI Data 2/PPI Clock/External Timer Reference*	C
PG6/*TFS0*/*RSI_DATA3*/*TMR0*/*PPIFS1*	I/O	GPIO/*SPORT0 Tx Frame Sync/RSI Data 3/Timer0/PPI Frame Sync1*	C
PG7/*DT0PRI*/*RSI_CMD*/*TMR1*/*PPIFS2*	I/O	GPIO/*SPORT0 Tx Primary Data/RSI Command/Timer 1/PPI Frame Sync2*	C
PG8/*TSCLK0*/*RSI_CLK*/*TMR6*/*TACI6*	I/O	GPIO/*SPORT0 Tx Clock/RSI Clock/Timer 6/Timer6 Alternate Capture Input*	D
PG9/*DT0SEC*/*UART0TX*/*TMR4*	I/O	GPIO/*SPORT0 Secondary Tx Data/UART0 Transmit/Timer 4*	C
PG10/*DR0SEC*/*UART0RX*/*TACI4*	I/O	GPIO/*SPORT0 Secondary Rx Data/UART0 Receive/Timer4 Alternate Capture Input*	C
PG11/*SPI0SS*/*AMS2*/*SPI1SEL5*/*TACLK2*	I/O	GPIO/*SPI0 Slave Device Select/Asynchronous Memory Bank Select 2/SPI1 Slave Select 5/Timer2 Alternate CLK*	C
PG12/*SPI0SCK*/*PPICLK*/*TMRCLK*/*PTP_PPS*	I/O	GPIO/*SPI0 Clock/PPI Clock/External Timer Reference/PTP Pulse Per Second Out*	D
PG13/*SPI0MISO*[4]/*TMR0*/*PPIFS1*/ *PTP_CLKOUT*	I/O	GPIO/*SPI0 Master In Slave Out/Timer0/PPI Frame Sync1/PTP Clock Out*	C
PG14/*SPI0MOSI*/*TMR1*/*PPIFS2*/*PWM TRIP* /*PTP_AUXIN*	I/O	GPIO/*SPI0 Master Out Slave In/Timer 1/PPI Frame Sync2/PWM Trip/PTP Auxiliary Snapshot Trigger Input*	C
PG15/*SPI0SEL2*/*PPIFS3*/*AMS3*	I/O	GPIO/*SPI0 Slave Select 2/PPI Frame Sync3/Asynchronous Memory Bank Select 3*	C
Port H: GPIO and Multiplexed Peripherals			
PH0/*DR1PRI*/*SPI1SS*/*RSI_DATA4*	I/O	GPIO/*SPORT1 Primary Rx Data/SPI1 Device Select/RSI Data 4*	C
PH1/*RFS1*/*SPI1MISO*/*RSI_DATA5*	I/O	GPIO/*SPORT1 Rx Frame Sync/SPI1 Master In Slave Out/RSI Data 5*	C
PH2/*RSCLK1*/*SPI1SCK*/*RSI DATA6*	I/O	GPIO/*SPORT1 Rx Clock/SPI1 Clock/RSI Data 6*	D
PH3/*DT1PRI*/*SPI1MOSI*/*RSI DATA7*	I/O	GPIO/*SPORT1 Primary Tx Data/SPI1 Master Out Slave In/RSI Data 7*	C
PH4/*TFS1*/*AOE*/*SPI0SEL3*/*CUD*	I/O	GPIO/*SPORT1 Tx Frame Sync/Asynchronous Memory Output Enable/SPI0 Slave Select 3/Counter Up Direction*	C
PH5/*TSCLK1*/*ARDY*/*PTP_EXT_CLKIN*/*CDG*	I/O	GPIO/*SPORT1 Tx Clock/Asynchronous Memory Hardware Ready Control/ External Clock for PTP TSYNC/Counter Down Gate*	D
PH6/*DT1SEC*/*UART1TX*/*SPI1SEL1*/*CZM*	I/O	GPIO/*SPORT1 Secondary Tx Data/UART1 Transmit/SPI1 Slave Select 1 /Counter Zero Marker*	C
PH7/*DR1SEC*/*UART1RX*/*TMR7*/*TACI2*	I/O	GPIO/*SPORT1 Secondary Rx Data/UART1 Receive/Timer 7/Timer2 Alternate Clock Input*	C

SPECIFICATIONS

Note that component specifications are subject to change without notice.

OPERATING CONDITIONS

Parameter		Conditions	Min	Nominal	Max	Unit
V_{DDINT}	Internal Supply Voltage	Industrial Models	1.14		1.47	V
	Internal Supply Voltage	Commercial Models	1.10		1.47	V
	Internal Supply Voltage	Automotive Models	1.33		1.47	V
V_{DDEXT}[1, 2]	External Supply Voltage	1.8 V I/O, Nonautomotive Models	1.7	1.8	1.9	V
	External Supply Voltage	2.5 V I/O, Nonautomotive Models	2.25	2.5	2.75	V
	External Supply Voltage	3.3 V I/O, All Models	3.0	3.3	3.6	V
V_{DDMEM}[3]	MEM Supply Voltage	1.8 V I/O, Nonautomotive Models	1.7	1.8	1.9	V
	MEM Supply Voltage	2.5 V I/O, Nonautomotive Models	2.25	2.5	2.75	V
	MEM Supply Voltage	3.3 V I/O, All Models	3.0	3.3	3.6	V
V_{DDRTC}[4]	RTC Power Supply Voltage		2.25		3.6	V
$V_{DDFLASH}$[4]	Internal SPI Flash Supply Voltage		2.7	3.3	3.6	V
V_{DDOTP}[1]	OTP Supply Voltage		2.25	2.5	2.75	V
V_{PPOTP}	OTP Programming Voltage					
	For Reads[1]		2.25	2.5	2.75	V
	For Writes[5]		6.9	7.0	7.1	V
V_{IH}	High Level Input Voltage[6, 7]	V_{DDEXT}/V_{DDMEM} = 1.90 V	1.2			V
	High Level Input Voltage[6, 8]	V_{DDEXT}/V_{DDMEM} = 2.75 V	1.7			V
	High Level Input Voltage[6, 8]	V_{DDEXT}/V_{DDMEM} = 3.6 V	2			V
V_{IHTWI}	High Level Input Voltage	V_{DDEXT} = 1.90 V/2.75 V/3.6 V	0.7 × V_{BUSTWI}		V_{BUSTWI}[9]	V
V_{IL}	Low Level Input Voltage[6, 7]	V_{DDEXT}/V_{DDMEM} = 1.7 V			0.6	V
	Low Level Input Voltage[6, 8]	V_{DDEXT}/V_{DDMEM} = 2.25 V			0.7	V
	Low Level Input Voltage[6, 8]	V_{DDEXT}/V_{DDMEM} = 3.0 V			0.8	V
V_{ILTWI}	Low Level Input Voltage	V_{DDEXT} = Minimum			0.3 × V_{BUSTWI}[10]	V
	Junction Temperature	168-Ball CSP_BGA @ $T_{AMBIENT}$ = 0°C to +70°C	0		+95	°C
	Junction Temperature	168-Ball CSP_BGA @ $T_{AMBIENT}$ = –40°C to +85°C	–40		+105	°C
	Junction Temperature	176-Lead LQFP_EP @ $T_{AMBIENT}$ = 0°C to +70°C	0		+95	°C
	Junction Temperature	176-Lead LQFP_EP @ $T_{AMBIENT}$ = –40°C to +85°C	–40		+105	°C

[1] Must remain powered (even if the associated function is not used).

[2] V_{DDEXT} is the supply to the GPIO.

[3] Pins/balls that use V_{DDMEM} are DATA15–0, ADDR19–1, $\overline{ABE1–0}$, $\overline{ARE}$, $\overline{AWE}$, $\overline{AMS1–0}$, SA10, $\overline{SWE}$, $\overline{SCAS}$, CLKOUT, $\overline{SRAS}$, $\overline{SMS}$, SCKE. These pins/balls are not tolerant to voltages higher than V_{DDMEM}. When using any of the asynchronous memory signals $\overline{AMS3–2}$, ARDY, or $\overline{AOE}$ V_{DDMEM} and V_{DDEXT} must be shorted externally.

[4] If not used, power with V_{DDEXT}.

[5] The V_{PPOTP} voltage for writes must only be applied when programming OTP memory. There is a finite amount of cumulative time that this voltage may be applied (dependent on voltage and junction temperature) over the lifetime of the part.

[6] Parameter value applies to all input and bidirectional pins/balls except SDA and SCL.

[7] Bidirectional balls (PF15–0, PG15–0, PH15–0) and input balls (RTXI, TCK, TDI, TMS, $\overline{TRST}$, CLKIN, $\overline{RESET}$, $\overline{NMI}$, and BMODE3–0) of the ADSP-BF51x processors are 2.5 V tolerant (always accept up to 2.7 V maximum V_{IH}). Voltage compliance (on outputs, V_{OH}) is limited by the V_{DDEXT} supply voltage.

[8] Bidirectional pins/balls (PF15–0, PG15–0, PH7–0) and input pins/balls (RTXI, TCK, TDI, TMS, $\overline{TRST}$, CLKIN, $\overline{RESET}$, $\overline{NMI}$, and BMODE2–0) of the ADSP-BF51x are 3.3 V tolerant (always accept up to 3.6 V maximum V_{IH}). Voltage compliance (on outputs, V_{OH}) is limited by the V_{DDEXT} supply voltage.

[9] The V_{IHTWI} min and max value vary with the selection in the TWI_DT field of the NONGPIO_DRIVE register. See V_{BUSTWI} min and max values in Table 9.

[10] SDA and SCL are pulled up to V_{BUSTWI}. See Table 9.

ELECTRICAL CHARACTERISTICS

Parameter		Test Conditions	Min	Typical	Max	Unit
V_{OH}	High Level Output Voltage	V_{DDEXT}/V_{DDMEM} = 1.7 V, I_{OH} = –0.5 mA	1.35			V
	High Level Output Voltage	V_{DDEXT}/V_{DDMEM} = 2.25 V, I_{OH} = –0.5 mA	2			V
	High Level Output Voltage	V_{DDEXT}/V_{DDMEM} = 3.0 V, I_{OH} = –0.5 mA	2.4			V
V_{OL}	Low Level Output Voltage	V_{DDEXT}/V_{DDMEM} = 1.7/2.25/3.0 V, I_{OL} = 2.0 mA			0.4	V
I_{IH}[1]	High Level Input Current	V_{DDEXT}/V_{DDMEM} = 3.6 V, V_{IN} = 3.6 V			10	µA
I_{IL}[1]	Low Level Input Current	V_{DDEXT}/V_{DDMEM} = 3.6 V, V_{IN} = 0 V			10	µA
I_{IHP}[2]	High Level Input Current JTAG	V_{DDEXT} = 3.6 V, V_{IN} = 3.6 V			75	µA
I_{OZH}[3]	Three-State Leakage Current	V_{DDEXT}/V_{DDMEM} = 3.6 V, V_{IN} = 3.6 V			10	µA
I_{OZHTWI}[4]	Three-State Leakage Current	V_{DDEXT} = 3.0 V, V_{IN} = 5.5 V			10	µA
I_{OZL}[3]	Three-State Leakage Current	V_{DDEXT}/V_{DDMEM} = 3.6 V, V_{IN} = 0 V			10	µA
C_{IN}[5, 6]	Input Capacitance	f_{IN} = 1 MHz, $T_{AMBIENT}$ = 25°C, V_{IN} = 2.5 V		5	8	pF
C_{INTWI}[4, 6]	Input Capacitance	f_{IN} = 1 MHz, $T_{AMBIENT}$ = 25°C, V_{IN} = 2.5 V			15	pF
$I_{DDDEEPSLEEP}$[7]	V_{DDINT} Current in Deep Sleep Mode	V_{DDINT} = 1.3 V, f_{CCLK} = 0 MHz, f_{SCLK} = 0 MHz, T_J = 25°C, ASF = 0.00		2.1		mA
$I_{DDSLEEP}$	V_{DDINT} Current in Sleep Mode	V_{DDINT} = 1.3 V, f_{SCLK} = 25 MHz, T_J = 25°C		5.5		mA
$I_{DD-IDLE}$	V_{DDINT} Current in Idle	V_{DDINT} = 1.3 V, f_{CCLK} = 50 MHz, f_{SCLK} = 25 MHz, T_J = 25°C, ASF = 0.41		12		mA
I_{DD-TYP}	V_{DDINT} Current	V_{DDINT} = 1.3 V, f_{CCLK} = 300 MHz, f_{SCLK} = 25 MHz, T_J = 25°C, ASF = 1.00		77		mA
I_{DD-TYP}	V_{DDINT} Current	V_{DDINT} = 1.4 V, f_{CCLK} = 400 MHz, f_{SCLK} = 25 MHz, T_J = 25°C, ASF = 1.00		108		mA
$I_{DDHIBERNATE}$[8]	Hibernate State Current	V_{DDEXT}=V_{DDMEM}=V_{DDRTC} = 3.3 V V_{DDOTP}=V_{PPOTP}=2.5 V, T_J = 25°C, CLKIN = 0 MHz		40		µA
I_{DDRTC}	V_{DDRTC} Current	V_{DDRTC} = 3.3 V, T_J = 25°C		20		µA
$I_{DDSLEEP}$[8, 9]	V_{DDINT} Current in Sleep Mode	f_{CCLK} = 0 MHz, f_{SCLK} > 0 MHz			Table 14 + (0.20 × V_{DDINT} × f_{SCLK})	mA[10]
$I_{DDDEEPSLEEP}$[8, 10]	V_{DDINT} Current in Deep Sleep Mode	f_{CCLK} = 0 MHz, f_{SCLK} = 0 MHz			Table 14	mA
I_{DDINT}[10, 11]	V_{DDINT} Current	f_{CCLK} > 0 MHz, f_{SCLK} ≥ 0 MHz			Table 14 + (Table 15 × ASF) + (0.20 × V_{DDINT} × f_{SCLK})	mA

Table 14. Static Current—$I_{DD\text{-}DEEPSLEEP}$ (mA) (Continued)

T_J (°C)[1]	Voltage (V_{DDINT})[1]								
	1.10 V	1.15 V	1.20 V	1.25 V	1.30 V	1.35 V	1.40 V	1.45 V	1.50 V
25	1.8	1.9	2.1	2.3	2.5	2.8	3.1	3.3	3.7
40	2.4	2.6	2.8	3.0	3.3	3.7	4.0	4.4	4.9
55	3.3	3.5	3.8	4.3	4.6	5.0	5.5	6.1	6.7
70	4.6	5.0	5.4	6.0	6.4	7.0	7.7	8.4	9.2
85	6.5	7.1	7.7	8.3	9.1	9.9	10.8	11.8	12.8
100	9.2	10.0	10.8	11.7	12.7	13.7	15.0	16.1	17.5
105	10.3	11.1	12.1	13.1	14.2	15.3	16.6	18.0	19.4

[1] Valid frequency and voltage ranges are model-specific. See Operating Conditions on Page 22.

Table 15. Dynamic Current in CCLK Domain (mA, with ASF = 1.0)[1]

f_{CCLK} (MHz)[2]	Voltage (V_{DDINT})[2]								
	1.10 V	1.15 V	1.20 V	1.25 V	1.30 V	1.35 V	1.40 V	1.45 V	1.50 V
400	N/A	N/A	N/A	N/A	N/A	N/A	102.1	106.5	111.0
350	N/A	N/A	N/A	N/A	N/A	86.2	90.1	94.0	98.0
300	N/A	N/A	N/A	N/A	71.4	74.7	78.1	81.5	85.0
250	N/A	N/A	N/A	57.5	60.4	63.2	66.1	69.0	71.9
200	N/A	42.5	44.7	47.0	49.4	51.7	54.1	56.5	58.9
150	31.1	32.9	34.7	36.5	38.4	40.2	42.1	44.0	45.9
100	22.0	23.4	24.7	26.0	27.4	28.7	30.1	31.5	33.0

[1] The values are not guaranteed as standalone maximum specifications. They must be combined with static current per the equations of Electrical Characteristics on Page 24.
[2] Valid frequency and voltage ranges are model-specific. See Operating Conditions on Page 22.

FLASH MEMORY CHARACTERISTICS

Table 16. Reliability Characteristics

Parameter		Min	Unit	Test Method
N_{END}	Endurance	100,000	Cycles	JEDEC Standard A117
T_{DR}	Data Retention	20	Years	JEDEC Standard A103

Table 17. AC Operating Characteristics

Parameter		Min	Max	Unit
f_{CLK}	Serial Clock Frequency		$0.25 \times f_{SCLK}$	MHz
T_{SE}	Sector-Erase		450	ms
T_{BE}	Block-Erase		2000	ms
T_{SCE}	Chip-Erase		64	s
T_{BP}[1]	Byte-Program		50	µs
T_{PWU}[2]	Power-Up Time Delay Before Write Command	1	10	ms

[1] For multiple bytes after first byte within a page, $t_{BP(MAX)}$ increments by 12 × N, where N = number of bytes programmed after the first byte.
[2] Program, Erase, and Write instructions are ignored until T_{PWU} ms after flash power-on.

Asynchronous Memory Write Cycle Timing

Table 27. Asynchronous Memory Write Cycle Timing

Parameter		Min	Max	Unit
Timing Requirements				
t_{SARDY}	ARDY Setup Before CLKOUT	4		ns
t_{HARDY}	ARDY Hold After CLKOUT	0.2		ns
Switching Characteristics				
t_{DDAT}	DATA15–0 Disable After CLKOUT		6	ns
t_{ENDAT}	DATA15–0 Enable After CLKOUT	0		ns
t_{DO}	Output Delay After CLKOUT[1]		6	ns
t_{HO}	Output Hold After CLKOUT [1]	0.8		ns

[1] Output pins/balls include $\overline{AMS3-0}$, $\overline{ABE1-0}$, ADDR19–1, DATA15–0, $\overline{AOE}$, $\overline{AWE}$.

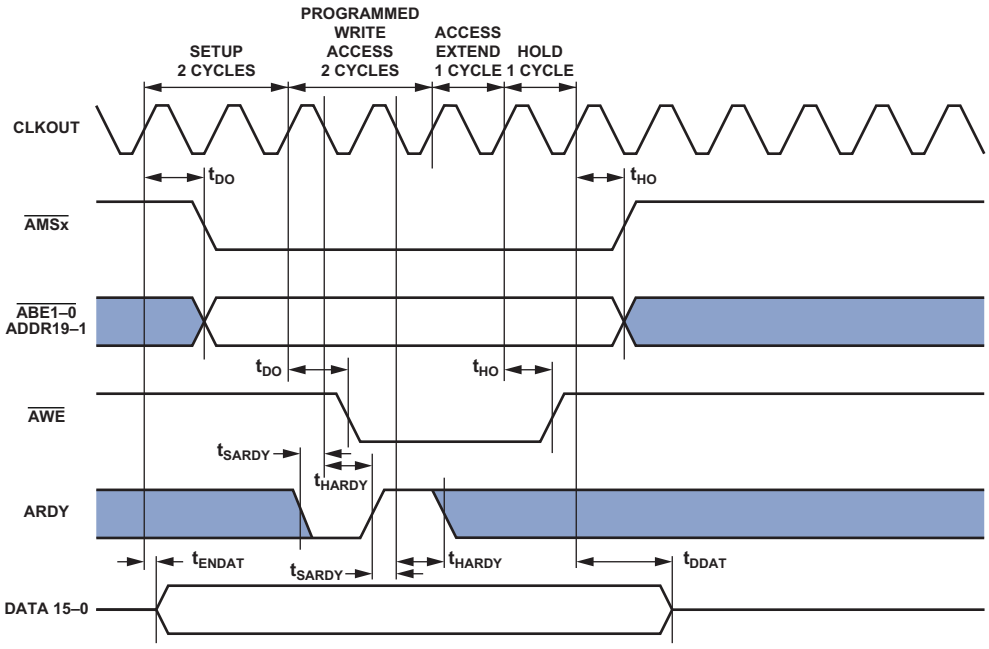


Figure 12. Asynchronous Memory Write Cycle Timing

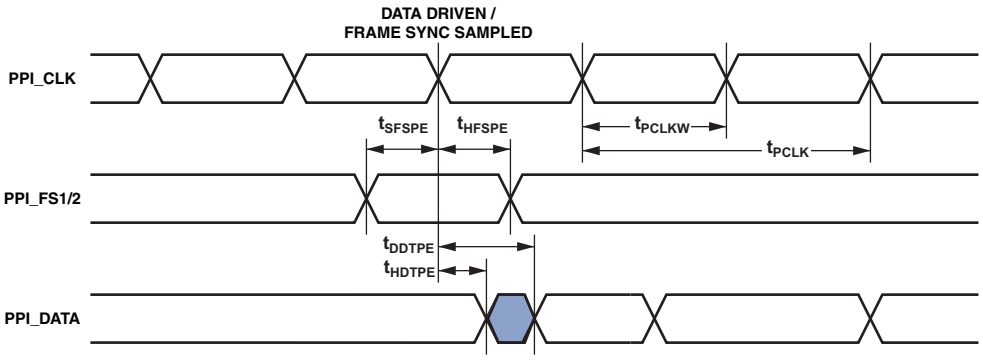


Figure 17. PPI GP Tx Mode with External Frame Sync Timing

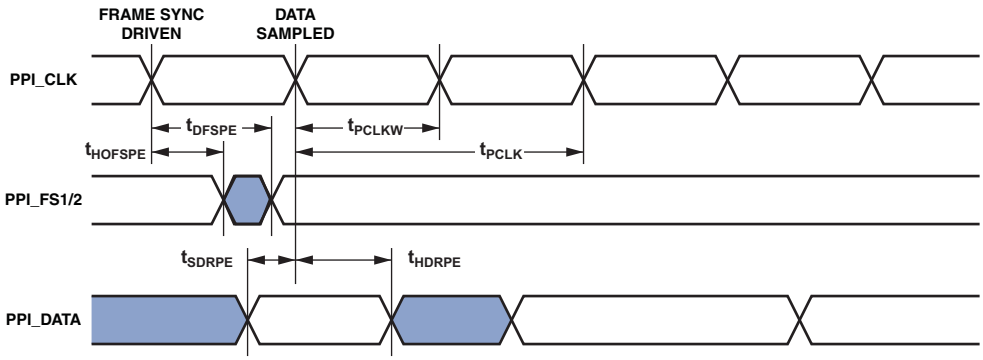


Figure 18. PPI GP Rx Mode with Internal Frame Sync Timing

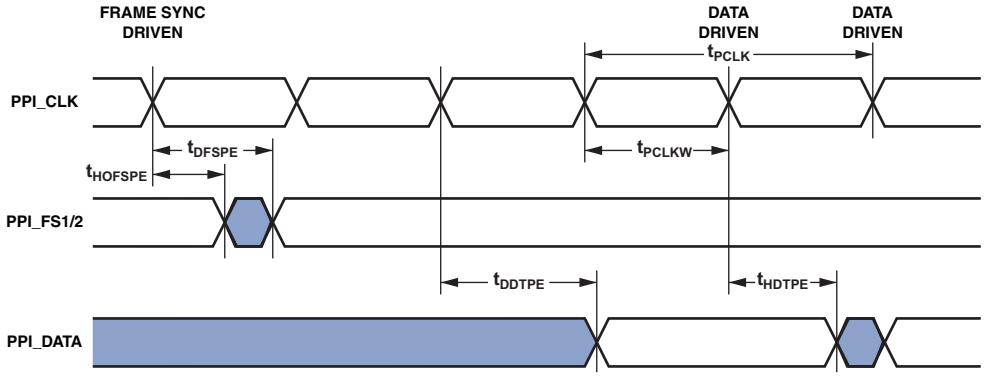


Figure 19. PPI GP Tx Mode with Internal Frame Sync Timing

RSI Controller Timing

Table 31 and Figure 20 describe RSI controller timing. Table 32 and Figure 21 describe RSI controller (high speed) timing.

Table 31. RSI Controller Timing

Parameter		Min	Max	Unit
Timing Requirements				
t_{ISU}	Input Setup Time	5.6		ns
t_{IH}	Input Hold Time	2		ns
Switching Characteristics				
f_{PP}[1]	Clock Frequency Data Transfer Mode	0	25	MHz
f_{OD}	Clock Frequency Identification Mode	100[2]	400	kHz
t_{WL}	Clock Low Time	10		ns
t_{WH}	Clock High Time	10		ns
t_{TLH}	Clock Rise Time		10	ns
t_{THL}	Clock Fall Time		10	ns
t_{ODLY}	Output Delay Time During Data Transfer Mode		14	ns
t_{ODLY}	Output Delay Time During Identification Mode		50	ns

[1] $t_{PP} = 1/f_{PP}$

[2] Specification can be 0 kHz, which means to stop the clock. The given minimum frequency range is for cases where a continuous clock is required.

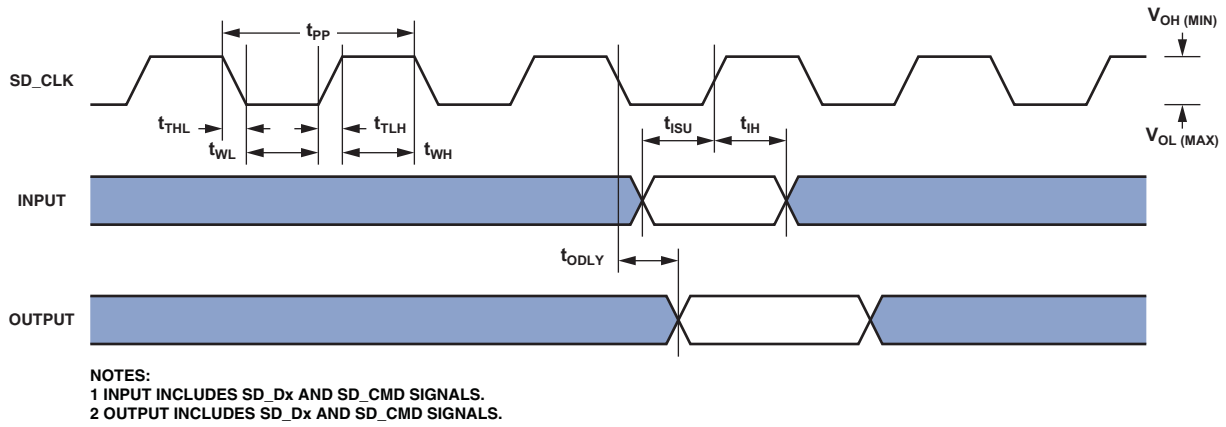


Figure 20. RSI Controller Timing

Serial Ports

Table 33 through Table 36 on Page 42 and Figure 22 on Page 40 through Figure 25 on Page 42 describe serial port operations.

Table 33. Serial Ports—External Clock

Parameter		V_{DDEXT} 1.8 V Nominal		V_{DDEXT} 2.5 V/3.3 V Nominal		Unit
		Min	Max	Min	Max	
Timing Requirements						
t_{SFSE}[1]	TFSx/RFSx Setup Before TSCLKx/RSCLKx	3		3		ns
t_{HFSE}[1]	TFSx/RFSx Hold After TSCLKx/RSCLKx	3		3		ns
t_{SDRE}[1]	Receive Data Setup Before RSCLKx	3		3		ns
t_{HDRE}[1]	Receive Data Hold After RSCLKx	3.5		3		ns
t_{SCLKEW}	TSCLKx/RSCLKx Width	7		4.5		ns
t_{SCLKE}	TSCLKx/RSCLKx Period	$2 \times t_{SCLK}$		$2 \times t_{SCLK}$		ns
t_{SUDTE}[2]	Start-Up Delay From SPORT Enable To First External TFSx	$4 \times t_{SCLKE}$		$4 \times t_{SCLKE}$		ns
t_{SUDRE}[2]	Start-Up Delay From SPORT Enable To First External RFSx	$4 \times t_{SCLKE}$		$4 \times t_{SCLKE}$		ns
Switching Characteristics						
t_{DFSE}[3]	TFSx/RFSx Delay After TSCLKx/RSCLKx (Internally Generated TFSx/RFSx)		10		10	ns
t_{HOFSE}[3]	TFSx/RFSx Hold After TSCLKx/RSCLKx (Internally Generated TFSx/RFSx)	0		0		ns
t_{DDTE}[3]	Transmit Data Delay After TSCLKx		10		10	ns
t_{HDTE}[3]	Transmit Data Hold After TSCLKx	0		0		ns

[1] Referenced to sample edge.
[2] Verified in design but untested.
[3] Referenced to drive edge.

Table 34. Serial Ports—Internal Clock

Parameter		V_{DDEXT} 1.8 V Nominal		V_{DDEXT} 2.5 V/3.3 V Nominal		Unit
		Min	Max	Min	Max	
Timing Requirements						
t_{SFSI}[1]	TFSx/RFSx Setup Before TSCLKx/RSCLKx	11		9.6		ns
t_{HFSI}[1]	TFSx/RFSx Hold After TSCLKx/RSCLKx	–1.5		–1.5		ns
t_{SDRI}[1]	Receive Data Setup Before RSCLKx	11		9.6		ns
t_{HDRI}[1]	Receive Data Hold After RSCLKx	–1.5		–1.5		ns
Switching Characteristics						
t_{DFSI}[2]	TFSx/RFSx Delay After TSCLKx/RSCLKx (Internally Generated TFSx/RFSx)		3		3	ns
t_{HOFSI}[2]	TFSx/RFSx Hold After TSCLKx/RSCLKx (Internally Generated TFSx/RFSx)	–2		–1		ns
t_{DDTI}[2]	Transmit Data Delay After TSCLKx		3		3	ns
t_{HDTI}[2]	Transmit Data Hold After TSCLKx	–1.8		–1.5		ns
t_{SCLKIW}	TSCLKx/RSCLKx Width	10		8		ns

[1] Referenced to sample edge.
[2] Referenced to drive edge.

Up/Down Counter/Rotary Encoder Timing

Table 42. Up/Down Counter/Rotary Encoder Timing

Parameter		V_{DDEXT} 1.8 V Nominal Min	V_{DDEXT} 1.8 V Nominal Max	V_{DDEXT} 2.5 V/3.3 V Nominal Min	V_{DDEXT} 2.5 V/3.3 V Nominal Max	Unit
Timing Requirements						
t_{WCOUNT}	Up/Down Counter/Rotary Encoder Input Pulse Width	t_{SCLK} + 1		t_{SCLK} + 1		ns
t_{CIS}	Counter Input Setup Time Before CLKOUT Low[1]	9		7		ns
t_{CIH}	Counter Input Hold Time After CLKOUT Low[1]	0		0		ns

[1] Either a valid setup and hold time or a valid pulse width is sufficient. There is no need to resynchronize counter inputs.

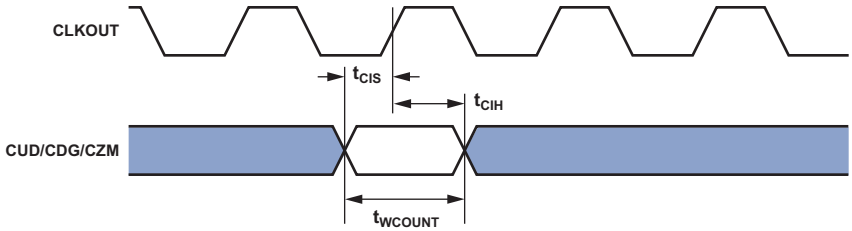


Figure 31. Up/Down Counter/Rotary Encoder Timing

10/100 Ethernet MAC Controller Timing

Table 43 through Table 48 and Figure 32 through Figure 37 describe the 10/100 Ethernet MAC Controller operations.

Table 43. 10/100 Ethernet MAC Controller Timing: MII Receive Signal

Parameter[1]		V_{DDEXT} 1.8 V Nominal Min	V_{DDEXT} 1.8 V Nominal Max	V_{DDEXT} 2.5 V/3.3 V Nominal Min	V_{DDEXT} 2.5 V/3.3 V Nominal Max	Unit
Timing Requirements						
$t_{ERXCLKF}$	ERxCLK Frequency (f_{SCLK} = SCLK Frequency)	None	25 + 1%	None	25 + 1%	MHz
$t_{ERXCLKW}$	ERxCLK Width (t_{ERxCLK} = ERxCLK Period)	t_{ERxCLK} × 40%	t_{ERxCLK} × 60%	t_{ERxCLK} × 35%	t_{ERxCLK} × 65%	ns
$t_{ERXCLKIS}$	Rx Input Valid to ERxCLK Rising Edge (Data In Setup)	7.5		7.5		ns
$t_{ERXCLKIH}$	ERxCLK Rising Edge to Rx Input Invalid (Data In Hold)	7.5		7.5		ns

[1] MII inputs synchronous to ERxCLK are ERxD3–0, ERxDV, and ERxER.

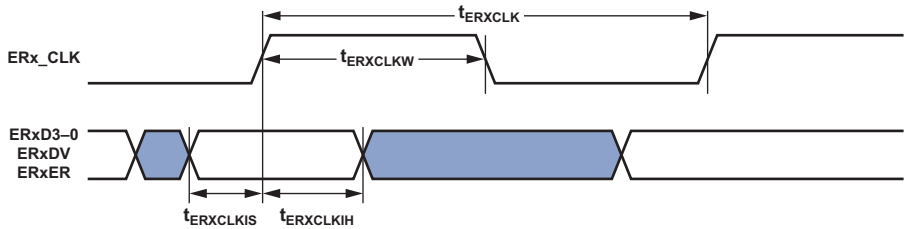


Figure 32. 10/100 Ethernet MAC Controller Timing: MII Receive Signal

Table 44. 10/100 Ethernet MAC Controller Timing: MII Transmit Signal

Parameter[1]		V_{DDEXT} 1.8 V Nominal Min	V_{DDEXT} 1.8 V Nominal Max	V_{DDEXT} 2.5 V/3.3 V Nominal Min	V_{DDEXT} 2.5 V/3.3 V Nominal Max	Unit
Switching Characteristics						
t_{ETF}	ETxCLK Frequency (f_{SCLK} = SCLK Frequency)	None	25 + 1%	None	25 + 1%	MHz
$t_{ETXCLKW}$	ETxCLK Width (t_{ETxCLK} = ETxCLK Period)	$t_{ETxCLK} \times 40\%$	$t_{ETxCLK} \times 60\%$	$t_{ETxCLK} \times 35\%$	$t_{ETxCLK} \times 65\%$	ns
$t_{ETXCLKOV}$	ETxCLK Rising Edge to Tx Output Valid (Data Out Valid)		20		20	ns
$t_{ETXCLKOH}$	ETxCLK Rising Edge to Tx Output Invalid (Data Out Hold)	0		0		ns

[1] MII outputs synchronous to ETxCLK are ETxD3–0.

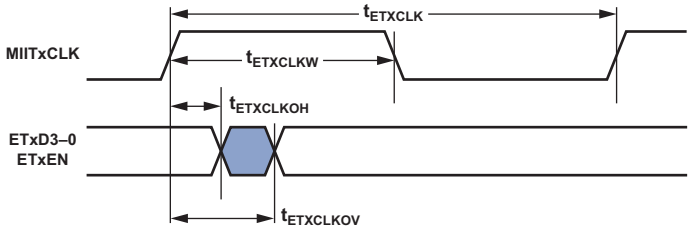


Figure 33. 10/100 Ethernet MAC Controller Timing: MII Transmit Signal

Table 45. 10/100 Ethernet MAC Controller Timing: RMII Receive Signal

Parameter[1]		V_{DDEXT} 1.8 V Nominal Min	V_{DDEXT} 1.8 V Nominal Max	V_{DDEXT} 2.5 V/3.3 V Nominal Min	V_{DDEXT} 2.5 V/3.3 V Nominal Max	Unit
Timing Requirements						
$t_{EREFCLKF}$	REF_CLK Frequency (f_{SCLK} = SCLK Frequency)	None	50 + 1%	None	50 + 1%	MHz
$t_{EREFCLKW}$	EREF_CLK Width ($t_{EREFCLK}$ = EREFCLK Period)	$t_{EREFCLK} \times 40\%$	$t_{EREFCLK} \times 60\%$	$t_{EREFCLK} \times 35\%$	$t_{EREFCLK} \times 65\%$	ns
$t_{EREFCLKIS}$	Rx Input Valid to RMII REF_CLK Rising Edge (Data In Setup)	4		4		ns
$t_{EREFCLKIH}$	RMII REF_CLK Rising Edge to Rx Input Invalid (Data In Hold)	2		2		ns

[1] RMII inputs synchronous to RMII REF_CLK are ERxD1–0, RMII CRS_DV, and ERxER.

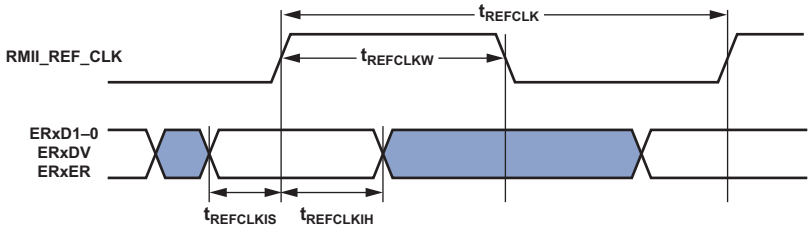


Figure 34. 10/100 Ethernet MAC Controller Timing: RMII Receive Signal

Table 46. 10/100 Ethernet MAC Controller Timing: RMII Transmit Signal

Parameter[1]		Min	Max	Unit
Switching Characteristics				
$t_{EREFCLKOV}$	RMII REF_CLK Rising Edge to Tx Output Valid (Data Out Valid)		8.1	ns
$t_{EREFCLKOH}$	RMII REF_CLK Rising Edge to Tx Output Invalid (Data Out Hold)	2		ns

[1] RMII outputs synchronous to RMII REF_CLK are ETxD1–0.

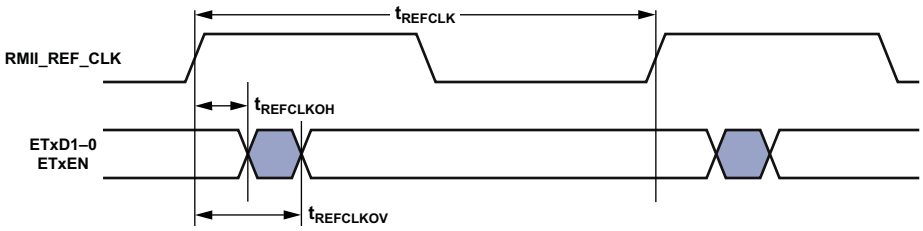


Figure 35. 10/100 Ethernet MAC Controller Timing: RMII Transmit Signal

JTAG Test And Emulation Port Timing

Table 49 and Figure 38 describe JTAG port operations.

Table 49. JTAG Port Timing

Parameter		Min	Max	Unit
Timing Requirements				
t_{TCK}	TCK Period	20		ns
t_{STAP}	TDI, TMS Setup Before TCK High	4		ns
t_{HTAP}	TDI, TMS Hold After TCK High	4		ns
t_{SSYS}[1]	System Inputs Setup Before TCK High	4		ns
t_{HSYS}[1]	System Inputs Hold After TCK High	5		ns
t_{TRSTW}	$\overline{TRST}$ Pulse Width[2] (measured in TCK cycles)	4		TCK
Switching Characteristics				
t_{DTDO}	TDO Delay from TCK Low		10	ns
t_{DSYS}[3]	System Outputs Delay After TCK Low	0	13	ns

[1] System Inputs = DATA15–0, SCL, SDA, TFS0, TSCLK0, RSCLK0, RFS0, DR0PRI, DR0SEC, PF15–0, PG15–0, PH7–0, MDIO, TD1, TMS, $\overline{RESET}$, $\overline{NMI}$, BMODE2–0.
[2] 50 MHz Maximum.
[3] System Outputs = DATA15–0, ADDR19–1, $\overline{ABE1–0}$, $\overline{ARE}$, $\overline{AWE}$, $\overline{AMS1–0}$, $\overline{SRAS}$, $\overline{SCAS}$, $\overline{SWE}$, SCKE, CLKOUT, SA10, $\overline{SMS}$, SCL, SDA, TSCLK0, TFS0, RFS0, RSCLK0, DT0PRI, DT0SEC, PF15–0, PG15–0, PH7–0, MDC, MDIO.

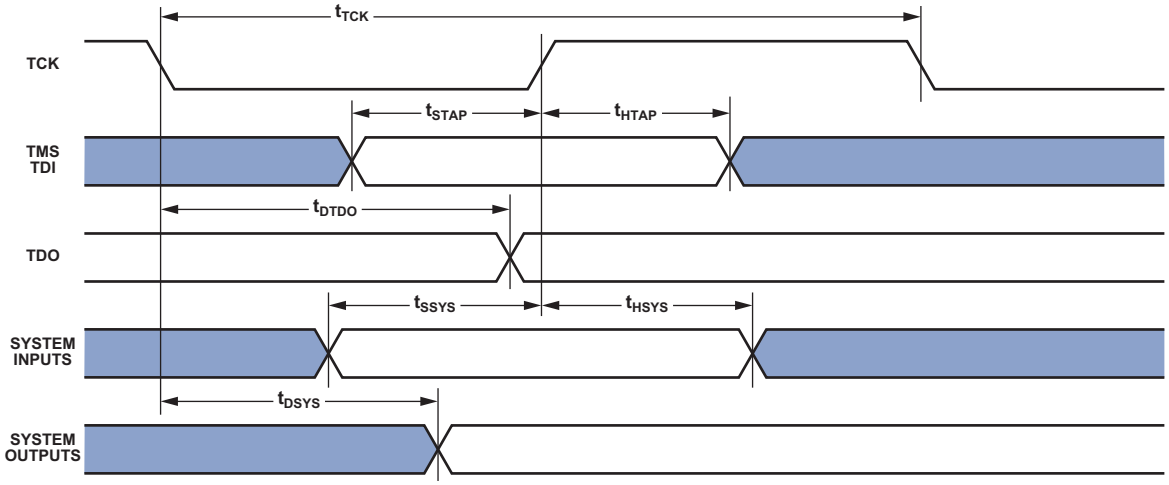


Figure 38. JTAG Port Timing

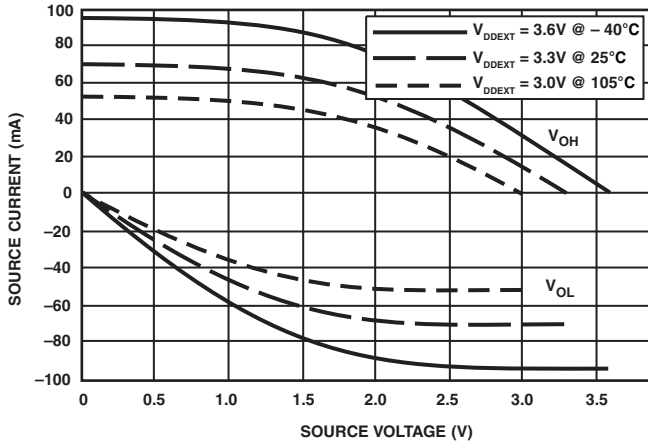


Figure 45. Driver Type C Current (3.3V V_{DDEXT}/V_{DDMEM})

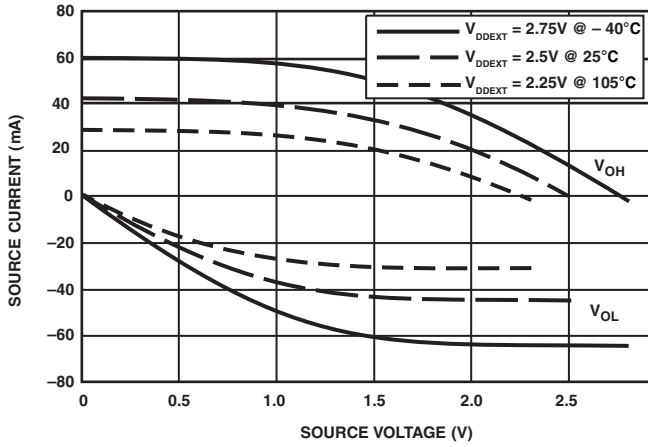


Figure 46. Drive Type C Current (2.5V V_{DDEXT}/V_{DDMEM})

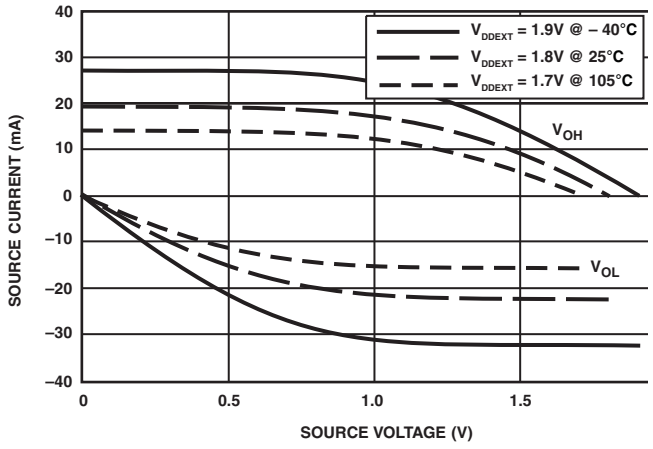


Figure 47. Driver Type C Current (1.8V V_{DDEXT}/V_{DDMEM})

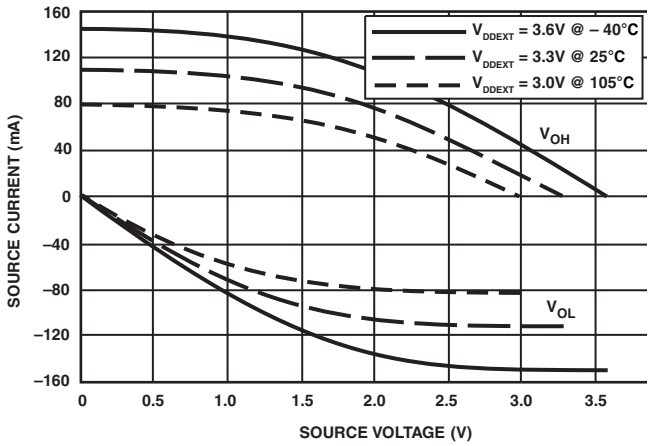


Figure 48. Driver Type D Current (3.3V V_{DDEXT}/V_{DDMEM})

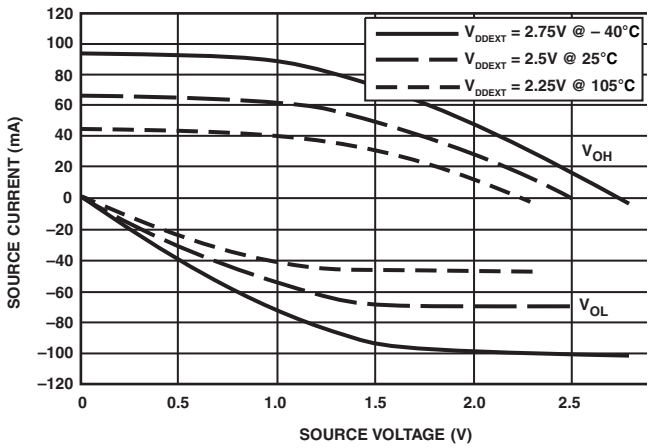


Figure 49. Driver Type D Current (2.5V V_{DDEXT}/V_{DDMEM})

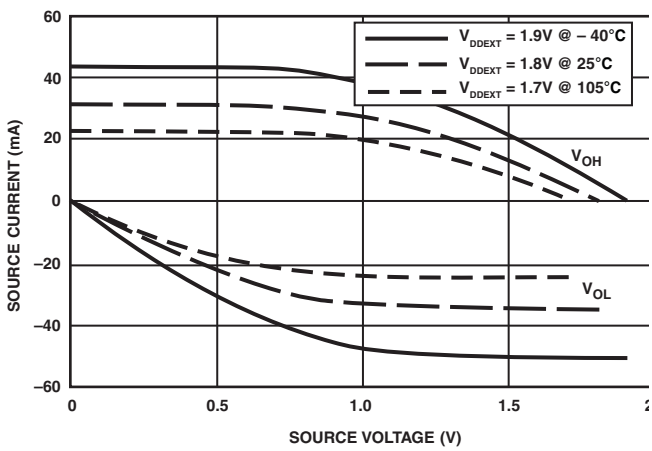


Figure 50. Driver Type D Current (1.8V V_{DDEXT}/V_{DDMEM})

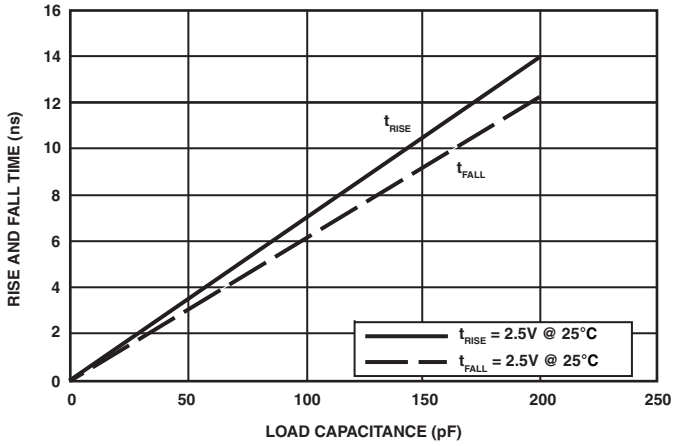


Figure 64. Driver Type C Typical Rise and Fall Times (10%–90%) vs. Load Capacitance (2.5V V_{DDEXT}/V_{DDMEM})

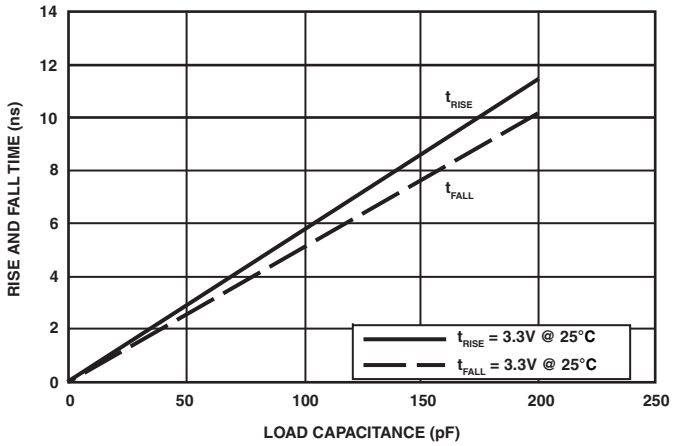


Figure 65. Driver Type C Typical Rise and Fall Times (10%–90%) vs. Load Capacitance (3.3V V_{DDEXT}/V_{DDMEM})

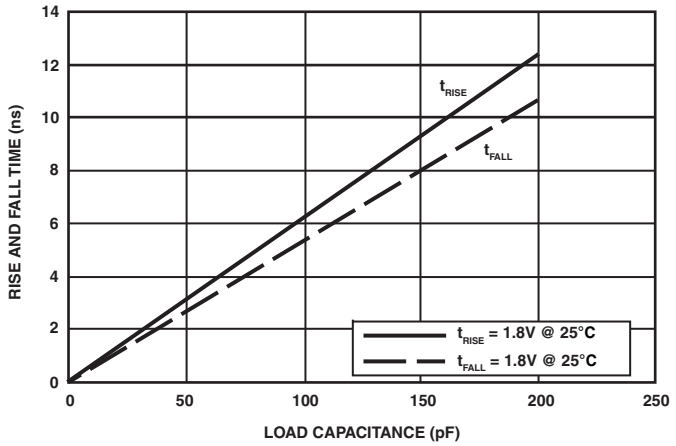


Figure 66. Driver Type D Typical Rise and Fall Times (10%–90%) vs. Load Capacitance (1.8V V_{DDEXT}/V_{DDMEM})

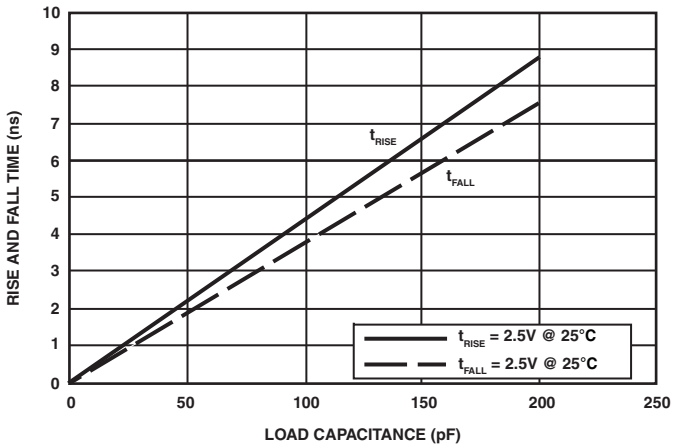


Figure 67. Driver Type D Typical Rise and Fall Times (10%–90%) vs. Load Capacitance (2.5V V_{DDEXT}/V_{DDMEM})

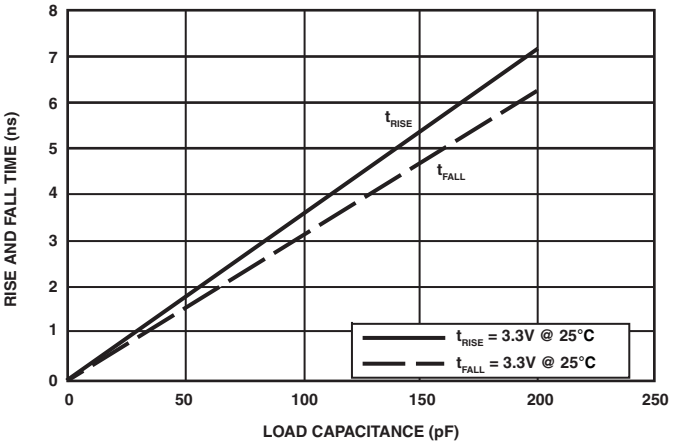


Figure 68. Driver Type D Typical Rise and Fall Times (10%–90%) vs. Load Capacitance (3.3V V_{DDEXT}/V_{DDMEM})

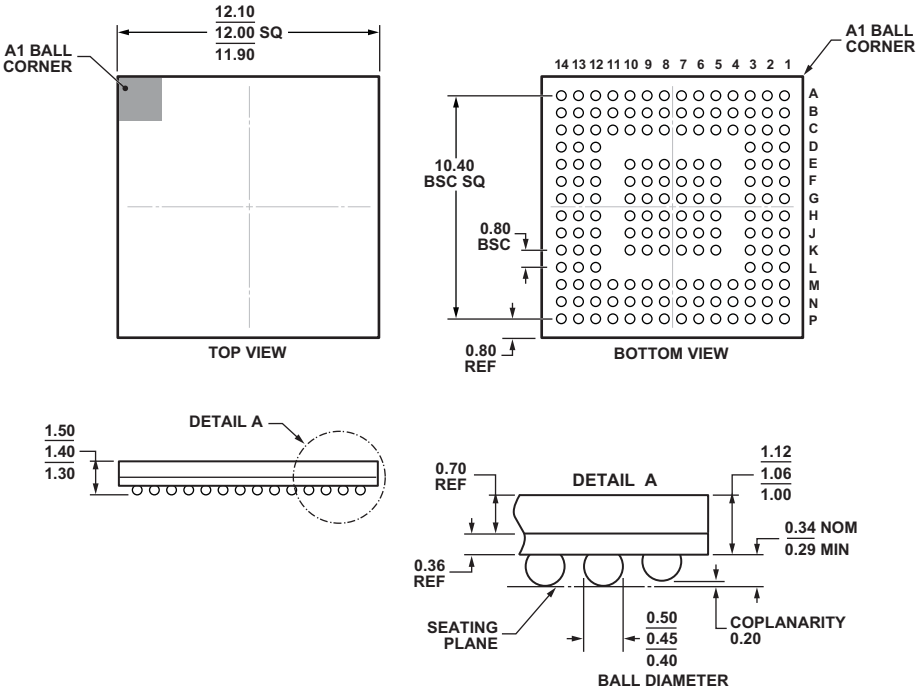


Figure 74. 168-Ball Chip Scale Package Ball Grid Array [CSP_BGA]
(BC-168-1)
Dimensions shown in millimeters

SURFACE-MOUNT DESIGN

Table 56 is provided as an aid to PCB design. For industry standard design recommendations, refer to IPC-7351, *Generic Requirements for Surface Mount Design and Land Pattern Standard.*

Table 56. BGA Data for Use with Surface-Mount Design

Package	Package Ball Attach Type	Package Solder Mask Opening	Package Ball Pad Size
168-Ball CSP_BGA	Solder Mask Defined	0.35 mm diameter	0.48 mm diameter