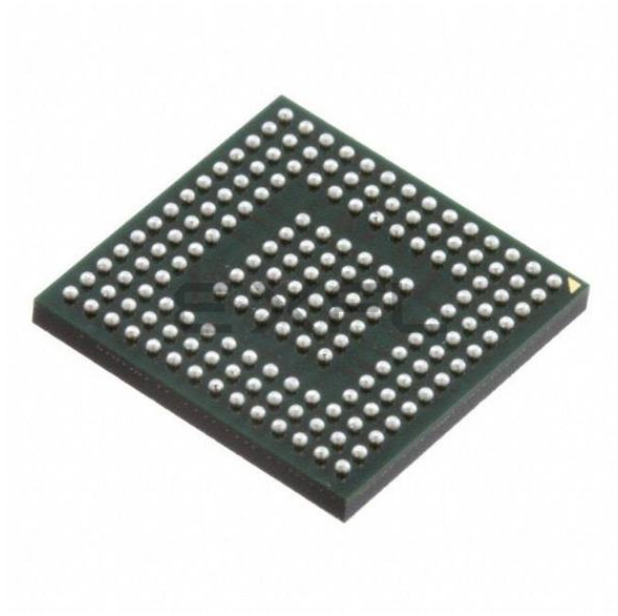

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Active
Type	Fixed Point
Interface	Ethernet, I²C, PPI, RSI, SPI, SPORT, UART/USART
Clock Rate	400MHz
Non-Volatile Memory	External
On-Chip RAM	116kB
Voltage - I/O	1.8V, 2.5V, 3.3V
Voltage - Core	1.30V
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	168-LFBGA, CSPBGA
Supplier Device Package	168-CSPBGA (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adbf518wbbcz402

GENERAL DESCRIPTION

The ADSP-BF512/ADSP-BF514/ADSP-BF514F16/ADSP-BF516/ADSP-BF518/ADSP-BF518F16 processors are members of the Blackfin® family of products, incorporating the Analog Devices/Intel Micro Signal Architecture (MSA). Blackfin processors combine a dual-MAC state-of-the-art signal processing engine, the advantages of a clean, orthogonal RISC-like microprocessor instruction set, and single-instruction, multiple-data (SIMD) multimedia capabilities into a single instruction-set architecture.

The processors are completely code compatible with other Blackfin processors.

Table 1. Processor Comparison

Feature		ADSP-BF512	ADSP-BF514	ADSP-BF514F16	ADSP-BF516	ADSP-BF518	ADSP-BF518F16
IEEE-1588		–	–	–	–	1	1
Ethernet MAC		–	–	–	1	1	1
RSI		–	1	1	1	1	1
TWI		1	1	1	1	1	1
SPORTs		2	2	2	2	2	2
UARTs		2	2	2	2	2	2
SPIs		2	2	2	2	2	2
GP Timers		8	8	8	8	8	8
Watchdog Timers		1	1	1	1	1	1
RTC		1	1	1	1	1	1
PPI		1	1	1	1	1	1
Flash (M bit)		–	–	16	–	–	16
Rotary Counter		1	1	1	1	1	1
3-Phase PWM Pairs		3	3	3	3	3	3
GPIOs		40	40	40	40	40	40
Memory (bytes)	L1 Instruction SRAM	32K					
	L1 Instruction SRAM/Cache	16K					
	L1 Data SRAM	32K					
	L1 Data SRAM/Cache	32K					
	L1 Scratchpad	4K					
	L3 Boot ROM	32K					
Maximum Speed Grade		400 MHz					
Package Options		176-Lead LQFP_EP (with Exposed Pad) 168-Ball CSP_BGA					

By integrating a rich set of industry-leading system peripherals and memory, Blackfin processors are the platform of choice for next-generation applications that require RISC-like programmability, multimedia support, and leading-edge signal processing in one integrated package.

PORTABLE LOW POWER ARCHITECTURE

Blackfin processors provide world-class power management and performance. They are produced with a low power and low voltage design methodology and feature on-chip dynamic power management, which is the ability to vary both the voltage and frequency of operation to significantly lower overall power consumption. This capability can result in a substantial reduction in power consumption, compared with just varying the frequency of operation. This allows longer battery life for portable appliances.

SYSTEM INTEGRATION

The ADSP-BF51x processors are highly integrated system-on-a-chip solutions for the next generation of embedded network connected applications. By combining industry-standard interfaces with a high performance signal processing core, cost-effective applications can be developed quickly, without the need for costly external components. The system peripherals include an IEEE-compliant 802.3 10/100 Ethernet MAC with IEEE-1588 support (ADSP-BF518/ADSP-BF518F16 only), an RSI controller, a TWI controller, two UART ports, two SPI ports, two serial ports (SPORTs), nine general-purpose 32-bit timers (eight with PWM capability), 3-phase PWM for motor control, a real-time clock, a watchdog timer, and a parallel peripheral interface (PPI).

BLACKFIN PROCESSOR CORE

As shown in Figure 2, the Blackfin processor core contains two 16-bit multipliers, two 40-bit accumulators, two 40-bit ALUs, four video ALUs, and a 40-bit shifter. The computation units process 8-, 16-, or 32-bit data from the register file.

The compute register file contains eight 32-bit registers. When performing compute operations on 16-bit operand data, the register file operates as 16 independent 16-bit registers. All operands for compute operations come from the multiported register file and instruction constant fields.

Each MAC can perform a 16-bit by 16-bit multiply in each cycle, accumulating the results into the 40-bit accumulators. Signed and unsigned formats, rounding, and saturation are supported.

The ALUs perform a traditional set of arithmetic and logical operations on 16-bit or 32-bit data. In addition, many special instructions are included to accelerate various signal processing tasks. These include bit operations such as field extract and population count, modulo 2^{32} multiply, divide primitives, saturation and rounding, and sign/exponent detection. The set of video instructions include byte alignment and packing operations, 16-bit and 8-bit adds with clipping, 8-bit average operations, and 8-bit subtract/absolute value/accumulate (SAA) operations. The compare/select and vector search instructions are also provided.

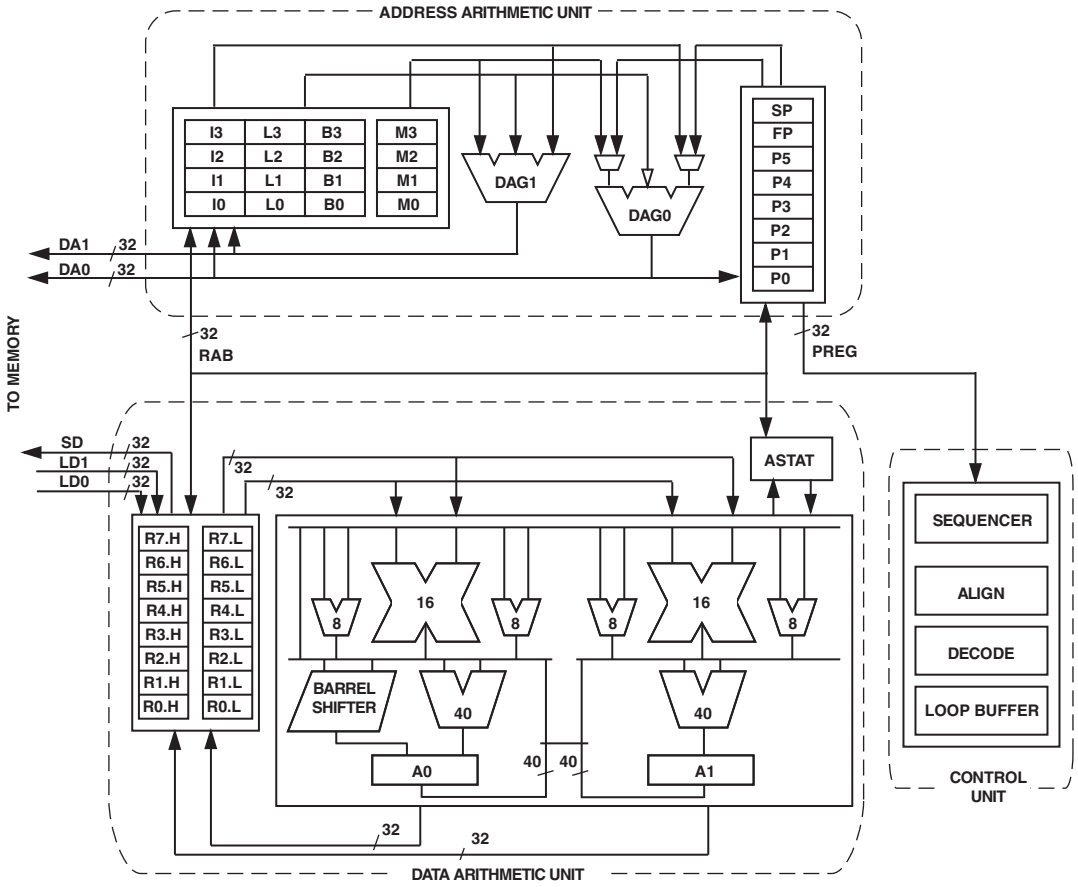

Figure 2. Blackfin Processor Core

For certain instructions, two 16-bit ALU operations can be performed simultaneously on register pairs (a 16-bit high half and 16-bit low half of a compute register). If the second ALU is used, quad 16-bit operations are possible.

The 40-bit shifter can perform shifts and rotates and is used to support normalization, field extract, and field deposit instructions.

The program sequencer controls the flow of instruction execution, including instruction alignment and decoding. For program flow control, the sequencer supports PC relative and indirect conditional jumps (with static branch prediction), and subroutine calls. Hardware is provided to support zero-overhead looping. The architecture is fully interlocked, meaning that the programmer need not manage the pipeline when executing instructions with data dependencies.

The address arithmetic unit provides two addresses for simultaneous dual fetches from memory. It contains a multiported register file consisting of four sets of 32-bit index, modify, length, and base registers (for circular buffering), and eight additional 32-bit pointer registers (for C-style indexed stack manipulation).

Blackfin processors support a modified Harvard architecture in combination with a hierarchical memory structure. Level 1 (L1) memories are those that typically operate at the full processor speed with little or no latency. At the L1 level, the instruction memory holds instructions only. The two data memories hold data, and a dedicated scratchpad data memory stores stack and local variable information.

In addition, multiple L1 memory blocks are provided, offering a configurable mix of SRAM and cache. The memory management unit (MMU) provides memory protection for individual tasks that may be operating on the core and can protect system registers from unintended access.

The architecture provides three modes of operation: user mode, supervisor mode, and emulation mode. User mode has restricted access to certain system resources, thus providing a protected software environment, while supervisor mode has unrestricted access to the system and core resources.

The Blackfin processor instruction set has been optimized so that 16-bit opcodes represent the most frequently used instructions, resulting in excellent compiled code density. Complex DSP instructions are encoded into 32-bit opcodes, representing fully featured multifunction instructions. Blackfin processors support a limited multi-issue capability, where a 32-bit

general-purpose up/down count modes. Then, count direction is either controlled by a level-sensitive input signal or by two edge detectors.

A third input can provide flexible zero marker support and can alternatively be used to input the push-button signal of thumb wheels. All three signals have a programmable debouncing circuit.

An internal signal forwarded to the GP timer unit enables one timer to measure the intervals between count events. Boundary registers enable auto-zero operation or simple system warning by interrupts when programmable count values are exceeded.

Serial Ports

The ADSP-BF51x processors incorporate two dual-channel synchronous serial ports (SPORT0 and SPORT1) for serial and multiprocessor communications. The SPORTs support the following features:

Serial port data can be automatically transferred to and from on-chip memory/external memory via dedicated DMA channels. Each of the serial ports can work in conjunction with another serial port to provide TDM support. In this configuration, one SPORT provides two transmit signals while the other SPORT provides the two receive signals. The frame sync and clock are shared.

Serial ports operate in five modes:

- Standard DSP serial mode
- Multichannel (TDM) mode
- I^2S mode
- Packed I^2S mode
- Left-justified mode

Serial Peripheral Interface (SPI) Ports

The processors have two SPI-compatible ports (SPI0 and SPI1) that enable the processor to communicate with multiple SPI-compatible devices.

The SPI interface uses three signals for transferring data: two data signals (master output-slave input–MOSI, and master input-slave output–MISO) and a clock signal (serial clock–SCK). An SPI chip select input signal ($\overline{\text{SPIxSS}}$) lets other SPI devices select the processor, and multiple SPI chip select output signals let the processor select other SPI devices. The SPI select signals are reconfigured general-purpose I/O signals. Using these signals, the SPI port provides a full-duplex, synchronous serial interface, which supports both master/slave modes and multimaster environments.

The SPI port baud rate and clock phase/polarities are programmable, and it has an integrated DMA channel, configurable to support transmit or receive data streams. The SPI's DMA channel can only service unidirectional accesses at any given time.

UART Ports

The processors provide two full-duplex universal asynchronous receiver/transmitter (UART) ports, which are fully compatible with PC-standard UARTs. Each UART port provides a simplified UART interface to other peripherals or hosts, supporting full-duplex, DMA-supported, asynchronous transfers of serial data. A UART port includes support for five to eight data bits, and none, even, or odd parity. Optionally, an additional address bit can be transferred to interrupt only addressed nodes in multi-drop bus (MDB) systems. A frame is terminates by one, one and a half, two or two and a half stop bits.

The UART ports support automatic hardware flow control through the Clear To Send (CTS) input and Request To Send (RTS) output with programmable assertion FIFO levels.

To help support the Local Interconnect Network (LIN) protocols, a special command causes the transmitter to queue a break command of programmable bit length into the transmit buffer. Similarly, the number of stop bits can be extended by a programmable inter-frame space.

The capabilities of the UARTs are further extended with support for the Infrared Data Association (IrDA®) serial infrared physical layer link specification (SIR) protocol.

2-Wire Interface (TWI)

The processors include a TWI module for providing a simple exchange method of control data between multiple devices. The TWI is compatible with the widely used I^2C® bus standard. The TWI module offers the capabilities of simultaneous master and slave operation, support for both 7-bit addressing and multimedia data arbitration. The TWI interface utilizes two signals for transferring clock (SCL) and data (SDA) and supports the protocol at speeds up to 400k bits/sec. The TWI interface signals are compatible with 5 V logic levels.

Additionally, the processor's TWI module is fully compatible with serial camera control bus (SCCB) functionality for easier control of various CMOS camera sensor devices.

Removable Storage Interface (RSI)

The RSI controller, available on the ADSP-BF514/ADSP-BF514F16/ADSP-BF516/ADSP-BF518/ADSP-BF518F16 processors, acts as the host interface for multi-media cards (MMC), secure digital memory cards (SD Card), secure digital input/output cards (SDIO), and CE-ATA hard disk drives. The following list describes the main features of the RSI controller.

- Support for a single MMC, SD memory, SDIO card or CE-ATA hard disk drive
- Support for 1-bit and 4-bit SD modes
- Support for 1-bit, 4-bit and 8-bit MMC modes
- Support for 4-bit and 8-bit CE-ATA hard disk drives
- A ten-signal external interface with clock, command, and up to eight data lines
- Card detection using one of the data signals
- Card interface clock generation from SCLK
- SDIO interrupt and read wait features
- CE-ATA command completion signal recognition and disable

10/100 Ethernet MAC

The ADSP-BF516 and ADSP-BF518/ADSP-BF518F16 processors offer the capability to directly connect to a network by way of an embedded fast Ethernet media access controller (MAC) that supports both 10-BaseT (10M bits/sec) and 100-BaseT (100M bits/sec) operation. The 10/100 Ethernet MAC peripheral on the processor is fully compliant to the IEEE 802.3-2002 standard and it provides programmable features designed to minimize supervision, bus use, or message processing by the rest of the processor system.

Some standard features are:

- Support of MII and RMII protocols for external PHYs
- Full duplex and half duplex modes
- Data framing and encapsulation: generation and detection of preamble, length padding, and FCS
- Media access management (in half-duplex operation): collision and contention handling, including control of retransmission of collision frames and of back-off timing
- Flow control (in full-duplex operation): generation and detection of pause frames
- Station management: generation of MDC/MDIO frames for read-write access to PHY registers
- Operating range for active and sleep operating modes, see Table 43 on Page 47 and Table 44 on Page 48
- Internal loopback from transmit to receive

Some advanced features are:

- Buffered crystal output to external PHY for support of a single crystal system
- Automatic checksum computation of IP header and IP payload fields of Rx frames
- Independent 32-bit descriptor-driven receive and transmit DMA channels
- Frame status delivery to memory through DMA, including frame completion semaphores for efficient buffer queue management in software
- Tx DMA support for separate descriptors for MAC header and payload to eliminate buffer copy operations
- Convenient frame alignment modes support even 32-bit alignment of encapsulated receive or transmit IP packet data in memory after the 14-byte MAC header
- Programmable Ethernet event interrupt supports any combination of:
  - Selected receive or transmit frame status conditions
  - PHY interrupt condition
  - Wakeup frame detected
  - Selected MAC management counter(s) at half-full
  - DMA descriptor error
- 47 MAC management statistics counters with selectable clear-on-read behavior and programmable interrupts on half maximum value
- Programmable receive address filters, including a 64-bin address hash table for multicast and/or unicast frames, and programmable filter modes for broadcast, multicast, unicast, control, and damaged frames
- Advanced power management supporting unattended transfer of receive and transmit frames and status to/from external memory via DMA during low power sleep mode
- System wakeup from sleep operating mode upon magic packet or any of four user-definable wakeup frame filters
- Support for 802.3Q tagged VLAN frames
- Programmable MDC clock rate and preamble suppression
- In RMII operation, seven unused signals may be configured as GPIO signals for other purposes

IEEE 1588 Support

The IEEE 1588 standard is a precision clock synchronization protocol for networked measurement and control systems. The ADSP-BF518/ADSP-BF518F16 processors include hardware support for IEEE 1588 with an integrated precision time protocol synchronization engine (PTP_TSYNC). This engine provides hardware assisted time stamping to improve the accuracy of clock synchronization between PTP nodes. The main features of the PTP_SYNC engine are:

- Support for both IEEE 1588-2002 and IEEE 1588-2008 protocol standards
- Hardware assisted time stamping capable of up to 12.5 ns resolution
- Lock adjustment
- Programmable PTM message support
- Dedicated interrupts
- Programmable alarm
- Multiple input clock sources (SCLK, MII clock, external clock)
- Programmable pulse per second (PPS) output
- Auxiliary snapshot to time stamp external events

Ports

Because of the rich set of peripherals, the processors group the many peripheral signals to four ports—port F, port G, port H, and port J. Most of the associated pins/balls are shared by multiple signals. The ports function as multiplexer controls.

General-Purpose I/O (GPIO)

The ADSP-BF51x processors have 40 bidirectional, general-purpose I/O (GPIO) signals allocated across three separate GPIO modules—PORTFIO, PORTGIO, and PORTHIO, associated with Port F, Port G, and Port H, respectively. Each GPIO-capable signal shares functionality with other peripherals via a multiplexing scheme; however, the GPIO functionality is the default state of the device upon power-up. Neither GPIO output nor input drivers are active by default. Each general-purpose port signal can be individually controlled by manipulation of the port control, status, and interrupt registers.

ADDITIONAL INFORMATION

The following publications that describe ADSP-BF512/ ADSP-BF514/ADSP-BF516/ADSP-BF518 processors (and related processors) can be accessed electronically on our website:

- *Getting Started With Blackfin Processors*
- *ADSP-BF51x Blackfin Processor Hardware Reference*
- *Blackfin Processor Programming Reference*
- *ADSP-BF512/BF514/BF514F16/BF516/BF518/BF518F16 Blackfin Processor Anomaly List*

RELATED SIGNAL CHAINS

A *signal chain* is a series of signal-conditioning electronic components that receive input (data acquired from sampling either real-time phenomena or from stored data) in tandem, with the output of one portion of the chain supplying input to the next. Signal chains are often used in signal processing applications to gather and process data or to apply system controls based on analysis of real-time phenomena. For more information about this term and related topics, see the "signal chain" entry in Wikipedia or the Glossary of EE Terms on the Analog Devices website.

Analog Devices eases signal processing system development by providing signal processing components that are designed to work together well. A tool for viewing relationships between specific applications and related components is available on the www.analog.com website.

The Application Signal Chains page in the Circuits from the Lab™ site (http://www.analog.com/circuits) provides:

- Graphical circuit block diagram presentation of signal chains for a variety of circuit types and applications
- Drill down links for components in each chain to selection guides and application information
- Reference designs applying best practice design techniques

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Table 8. Signal Descriptions (Continued)

Signal Name	Type	Function	Driver Type[1]
PF8/*MDC*/PPI D8/*SPI1SEL4*	I/O	GPIO/*Ethernet Management Channel Clock/PPI Data 8/SPI1 Slave Select 4*	C
PF9/*MDIO*/*PPI D9*/*TMR2*	I/O	GPIO/*Ethernet Management Channel Serial Data/PPI Data 9/Timer 2*	C
PF10/*ETxD0*/*PPI D10*/*TMR3*	I/O	GPIO/*Ethernet MII or RMII Transmit D0/PPI Data 10/Timer 3*	C
PF11/*ERxD0*/*PPI D11*/*PWM AH*/*TACI3*	I/O	GPIO/*Ethernet MII Receive D0/PPI Data 11/PWM AH output /Timer3 Alternate Capture Input*	C
PF12/*ETxD1*/*PPI D12*/*PWM AL*	I/O	GPIO/*Ethernet MII Transmit D1/PPI Data 12/PWM AL Output*	C
PF13/*ERxD1*/*PPI D13*/*PWM BH*	I/O	GPIO/*Ethernet MII or RMII Receive D1/PPI Data 13/PWM BH Output*	C
PF14/*ETxEN*/*PPI D14*/*PWM BL*	I/O	GPIO/*Ethernet MII Transmit Enable/PPI Data 14/PWM BL Out*	C
PF15[2]/*RMII PHYINT*/*PPI D15*/*PWM_SYNCA*	I/O	GPIO/*Ethernet MII PHY Interrupt/PPI Data 15/Alternate PWM Sync*	C
Port G: GPIO and Multiplexed Peripherals			
PG0/*MIICRS*/*RMIICRS*/*HWAIT*[3]/*SPI1SEL3*	I/O	GPIO/*Ethernet MII or RMII Carrier Sense or RMII Data Valid/HWAIT/SPI1 Slave Select3*	C
PG1/*ERxER*/*DMAR1*/*PWM CH*	I/O	GPIO/*Ethernet MII or RMII Receive Error/DMA Req 1/PWM CH Out*	C
PG2/*MIITxCLK*/*RMIIREF_CLK*/*DMAR0*/*PWM CL*	I/O	GPIO/*Ethernet MII or RMII Reference Clock/DMA Req 0/PWM CL Out*	C
PG3/*DR0PRI*/*RSI_DATA0*/*SPI0SEL5*/*TACLK3*	I/O	GPIO/*SPORT0 Primary Rx Data/RSI Data 0/SPI0 Slave Select 5/Timer3 Alternate CLK*	C
PG4/*RSCLK0*/*RSI_DATA1*/*TMR5*/*TACI5*	I/O	GPIO/*SPORT0 Rx Clock/RSI Data 1/Timer 5/Timer5 Alternate Capture Input*	D
PG5/*RFS0*/*RSI_DATA2*/*PPICLK*/*TMRCLK*	I/O	GPIO/*SPORT0 Rx Frame Sync/RSI Data 2/PPI Clock/External Timer Reference*	C
PG6/*TFS0*/*RSI_DATA3*/*TMR0*/*PPIFS1*	I/O	GPIO/*SPORT0 Tx Frame Sync/RSI Data 3/Timer0/PPI Frame Sync1*	C
PG7/*DT0PRI*/*RSI_CMD*/*TMR1*/*PPIFS2*	I/O	GPIO/*SPORT0 Tx Primary Data/RSI Command/Timer 1/PPI Frame Sync2*	C
PG8/*TSCLK0*/*RSI_CLK*/*TMR6*/*TACI6*	I/O	GPIO/*SPORT0 Tx Clock/RSI Clock/Timer 6/Timer6 Alternate Capture Input*	D
PG9/*DT0SEC*/*UART0TX*/*TMR4*	I/O	GPIO/*SPORT0 Secondary Tx Data/UART0 Transmit/Timer 4*	C
PG10/*DR0SEC*/*UART0RX*/*TACI4*	I/O	GPIO/*SPORT0 Secondary Rx Data/UART0 Receive/Timer4 Alternate Capture Input*	C
PG11/*SPI0SS*/*AMS2*/*SPI1SEL5*/*TACLK2*	I/O	GPIO/*SPI0 Slave Device Select/Asynchronous Memory Bank Select 2/SPI1 Slave Select 5/Timer2 Alternate CLK*	C
PG12/*SPI0SCK*/*PPICLK*/*TMRCLK*/*PTP_PPS*	I/O	GPIO/*SPI0 Clock/PPI Clock/External Timer Reference/PTP Pulse Per Second Out*	D
PG13/*SPI0MISO*[4]/*TMR0*/*PPIFS1*/ *PTP_CLKOUT*	I/O	GPIO/*SPI0 Master In Slave Out/Timer0/PPI Frame Sync1/PTP Clock Out*	C
PG14/*SPI0MOSI*/*TMR1*/*PPIFS2*/*PWM TRIP* /*PTP_AUXIN*	I/O	GPIO/*SPI0 Master Out Slave In/Timer 1/PPI Frame Sync2/PWM Trip/PTP Auxiliary Snapshot Trigger Input*	C
PG15/*SPI0SEL2*/*PPIFS3*/*AMS3*	I/O	GPIO/*SPI0 Slave Select 2/PPI Frame Sync3/Asynchronous Memory Bank Select 3*	C
Port H: GPIO and Multiplexed Peripherals			
PH0/*DR1PRI*/*SPI1SS*/*RSI_DATA4*	I/O	GPIO/*SPORT1 Primary Rx Data/SPI1 Device Select/RSI Data 4*	C
PH1/*RFS1*/*SPI1MISO*/*RSI_DATA5*	I/O	GPIO/*SPORT1 Rx Frame Sync/SPI1 Master In Slave Out/RSI Data 5*	C
PH2/*RSCLK1*/*SPI1SCK*/*RSI DATA6*	I/O	GPIO/*SPORT1 Rx Clock/SPI1 Clock/RSI Data 6*	D
PH3/*DT1PRI*/*SPI1MOSI*/*RSI DATA7*	I/O	GPIO/*SPORT1 Primary Tx Data/SPI1 Master Out Slave In/RSI Data 7*	C
PH4/*TFS1*/*AOE*/*SPI0SEL3*/*CUD*	I/O	GPIO/*SPORT1 Tx Frame Sync/Asynchronous Memory Output Enable/SPI0 Slave Select 3/Counter Up Direction*	C
PH5/*TSCLK1*/*ARDY*/*PTP_EXT_CLKIN*/*CDG*	I/O	GPIO/*SPORT1 Tx Clock/Asynchronous Memory Hardware Ready Control/ External Clock for PTP TSYNC/Counter Down Gate*	D
PH6/*DT1SEC*/*UART1TX*/*SPI1SEL1*/*CZM*	I/O	GPIO/*SPORT1 Secondary Tx Data/UART1 Transmit/SPI1 Slave Select 1 /Counter Zero Marker*	C
PH7/*DR1SEC*/*UART1RX*/*TMR7*/*TACI2*	I/O	GPIO/*SPORT1 Secondary Rx Data/UART1 Receive/Timer 7/Timer2 Alternate Clock Input*	C

Table 8. Signal Descriptions (Continued)

Signal Name	Type	Function	Driver Type[1]
Port J			
PJ0:SCL	I/O 5V	TWI Serial Clock (This signal is an open-drain output and requires a pull-up resistor. Consult version 2.1 of the I^2C specification for the proper resistor value.)	E
PJ1:SDA	I/O 5V	TWI Serial Data (This signal is an open-drain output and requires a pull-up resistor. Consult version 2.1 of the I^2C specification for the proper resistor value.)	E
Real Time Clock			
RTXI	I	RTC Crystal Input (This ball should be pulled low when not used.)	
RTXO	O	RTC Crystal Output (Does not three-state during hibernate)	
JTAG Port			
TCK	I	JTAG Clock	
TDO	O	JTAG Serial Data Out	C
TDI	I	JTAG Serial Data In	
TMS	I	JTAG Mode Select	
$\overline{\text{TRST}}$	I	JTAG Reset (This signal should be pulled low if the JTAG port is not used.)	
$\overline{\text{EMU}}$	O	Emulation Output	C
Clock			
CLKIN	I	Clock/Crystal Input	
XTAL	O	Crystal Output (If CLKBUF is enabled, does not three-state during hibernate)	
CLKBUF	O	Buffered XTAL Output (If enabled, does not three-state during hibernate)	C
Mode Controls			
$\overline{\text{RESET}}$	I	Reset	
$\overline{\text{NMI}}$	I	Non-maskable Interrupt (This signal should be pulled high when not used.)	
BMODE2-0	I	Boot Mode Strap 2-0	
Voltage Regulation Interface			
$\overline{\text{PG}}$	I	Power Good (This signal should be pulled low when not used.)	
EXT_WAKE	O	Wake up Indication (Does not three-state during hibernate)	C
Power Supplies		**ALL SUPPLIES MUST BE POWERED** See Operating Conditions on Page 22.	
V_{DDEXT}	P	I/O Power Supply	
V_{DDINT}	P	Internal Power Supply	
V_{DDRTC}	P	Real Time Clock Power Supply	
$V_{DDFLASH}$	P	Internal SPI Flash Power Supply	
V_{DDMEM}	P	MEM Power Supply	
V_{PPOTP}	P	OTP Programming Voltage	
V_{DDOTP}	P	OTP Power Supply	
GND	G	Ground for All Supplies	

[1] See Output Drive Currents on Page 52 for more information about each driver type.
[2] When driven low, the PF15 signal can be used to wake up the processor from the hibernate state, either in normal GPIO mode or in Ethernet mode as $\overline{\text{PHYINT}}$. If the pin/ball is used for wake up, enable the feature with the PHYWE bit in the VR_CTL register, and pull-up the signal with a resistor.
[3] Boot host wait is a GPIO signal toggled by the boot kernel. The mandatory external pull-up/pull-down resistor defines the signal polarity.
[4] A pull-up resistor is required for the boot from external SPI EEPROM or flash (BMODE = 0x3).

ABSOLUTE MAXIMUM RATINGS

Stresses greater than those listed in Table 18 may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 18. Absolute Maximum Ratings

Parameter	Rating
Internal Supply Voltage (V_{DDINT})	–0.3 V to +1.50 V
External (I/O) Supply Voltage (V_{DDEXT}/V_{DDMEM})	–0.3 V to +3.8 V
Input Voltage[1, 2]	–0.5 V to +3.6 V
Input Voltage[1, 3]	–0.5 V to +5.5 V
Output Voltage Swing	–0.5 V to V_{DDEXT}/V_{DDMEM} + 0.5 V
I_{OH}/I_{OL} Current per Pin Group[4]	80 mA (max)
Storage Temperature Range	–65°C to +150°C
Junction Temperature While biased	+110°C

[1] Applies to 100% transient duty cycle. For other duty cycles see Table 19.
[2] Applies only when V_{DDEXT} is within specifications. When V_{DDEXT} is outside specifications, the range is V_{DDEXT} ± 0.2.
[3] Applies to signals SCL, SDA.
[4] For more information, see the information preceding Table 21 and Table 22.

Table 19. Maximum Duty Cycle for Input Transient Voltage[1]

V_{IN} Min (V)[2]	V_{IN} Max (V)[2]	Maximum Duty Cycle[3]
–0.50	+3.80	100%
–0.70	+4.00	40%
–0.80	+4.10	25%
–0.90	+4.20	15%
–1.00	+4.30	10%

[1] Applies to all signal pins/balls with the exception of CLKIN, XTAL.
[2] The individual values cannot be combined for analysis of a single instance of overshoot or undershoot. The worst case observed value must fall within one of the voltages specified and the total duration of the overshoot or undershoot (exceeding the 100% case) must be less than or equal to the corresponding duty cycle.
[3] Duty cycle refers to the percentage of time the signal exceeds the value for the 100% case. It is equivalent to the measured duration of a single instance of overshoot or undershoot as a percentage of the period of occurrence.

When programming OTP memory on the ADSP-BF51x processor, the V_{PPOTP} pin/ball must be set to the write value specified in the Operating Conditions on Page 22. There is a finite amount of cumulative time that the write voltage may be applied (dependent on voltage and junction temperature) to V_{PPOTP} over the lifetime of the part. Therefore, maximum OTP memory programming time for the processor is shown in Table 20.

Table 20. Maximum OTP Memory Programming Time

VPPOTP Voltage (V)	Temperature		
	25°C	85°C	110°C
6.9	6000 sec	100 sec	25 sec
7.0	2400 sec	44 sec	12 sec
7.1	1000 sec	18 sec	4.5 sec

Table 21 and Table 22 specify the maximum total source/sink (I_{OH}/I_{OL}) current for a group of pins. Permanent damage can occur if this value is exceeded. To understand this specification, if pins PF9, PF8, PF7, PF6, and PF5 from Group 1 in Table 22 table were sourcing or sinking 2 mA each, the total current for those pins would be 10 mA. This would allow up to 70 mA total that could be sourced or sunk by the remaining pins in the group without damaging the device. Note that the V_{OH} and V_{OL} specifications have separate per-pin maximum current requirements as shown in the Electrical Characteristics table.

Table 21. Total Current Pin Groups–V_{DDMEM} Groups

Group	Pins in Group
1	DATA15, DATA14, DATA13, DATA12, DATA11, DATA10
2	DATA9, DATA8, DATA7, DATA6, DATA5, DATA4
3	DATA3, DATA2, DATA1, DATA0, ADDR19, ADDR18
4	ADDR17, ADDR16, ADDR15, ADDR14, ADDR13
5	ADDR12, ADDR11, ADDR10, ADDR9, ADDR8, ADDR7
6	ADDR6, ADDR5, ADDR4, ADDR3, ADDR2, ADDR1
7	$\overline{ABE1}$, $\overline{ABE0}$, SA10, $\overline{SWE}$, $\overline{SCAS}$, $\overline{SRAS}$
8	$\overline{SMS}$, SCKE, $\overline{AMS1}$, $\overline{ARE}$, $\overline{AWE}$, $\overline{AMS0}$, CLKOUT

Table 22. Total Current Pin Groups–V_{DDEXT} Groups

Group	Pins in Group
1	PF9, PF8, PF7, PF6, PF5, PF4, PF3, PF2
2	PF1, PF0, PG15, PG14, PG13, PG12, PG11, PG10
3	PG9, PG8, PG7, PG6, PG5, PG4, PG3, PG2, BMODE0, BMODE1, BMODE2
4	PG1, PG0, TDO, $\overline{EMU}$, TDI, TCK, $\overline{TRST}$, TMS
5	$\overline{RESET}$, $\overline{NMI}$, CLKBUF
6	PH7, PH6, PH5, PH4, PH3, PH2, PH1, PH0
7	PF15, PF14, PF13, PF12, PF11, SDA, SCL, PF10

PACKAGE INFORMATION

The information presented in Figure 8 and Table 23 provides details about the package branding for the processor. For a complete listing of product availability, see Ordering Guide on Page 67.

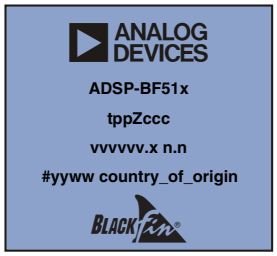


Figure 8. Product Information on Package

Table 23. Package Brand Information

Brand Key	Field Description
ADSP-BF51x	Product Name
t	Temperature Range
pp	Package Type
Z	Lead Free Option
ccc	See Ordering Guide
vvvvvv.x	Assembly Lot Code
n.n	Silicon Revision
#	RoHS Compliance Designator
yyww	Date Code

ESD SENSITIVITY

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

Table 25. Power-Up Reset Timing

Parameter		Min	Max	Unit
Timing Requirements				
$t_{RST\_IN\_PWR}$	$\overline{\text{RESET}}$ Deasserted after the V_{DDINT}, V_{DDEXT}, V_{DDRTC}, V_{DDMEM}, V_{DDOTP}, and CLKIN Pins are Stable and Within Specification	3500 × t_{CKIN}		ns

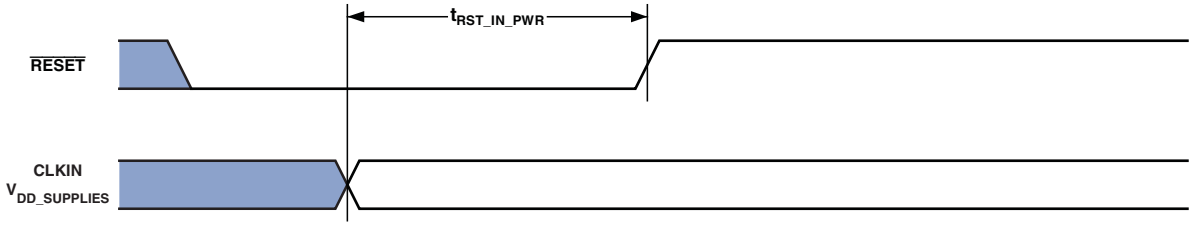


Figure 10. Power-Up Reset Timing

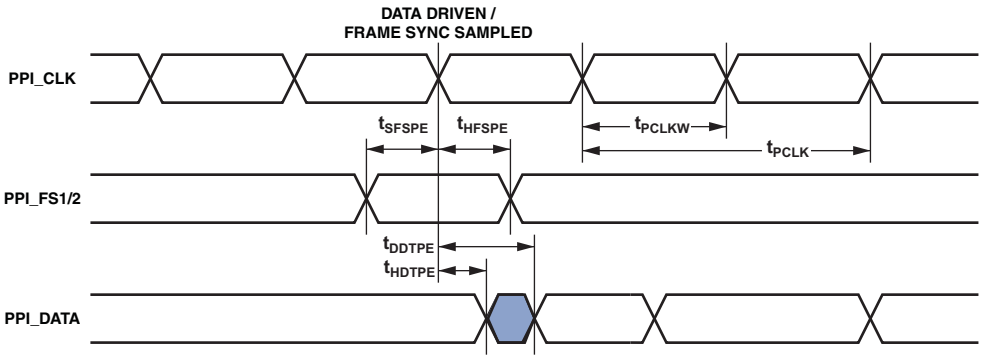


Figure 17. PPI GP Tx Mode with External Frame Sync Timing

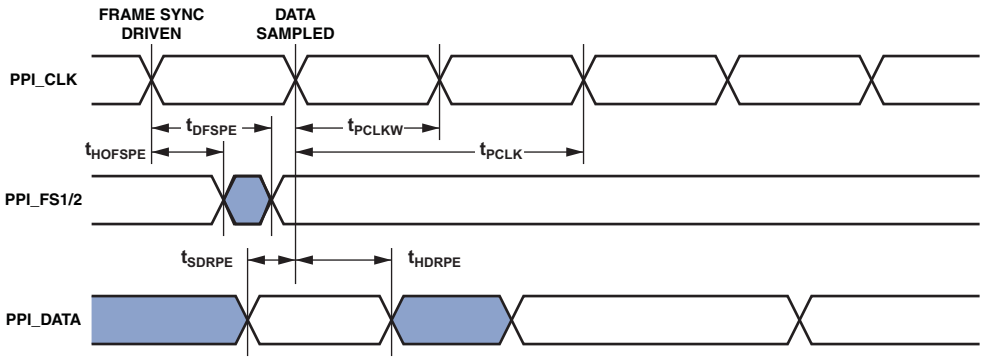


Figure 18. PPI GP Rx Mode with Internal Frame Sync Timing

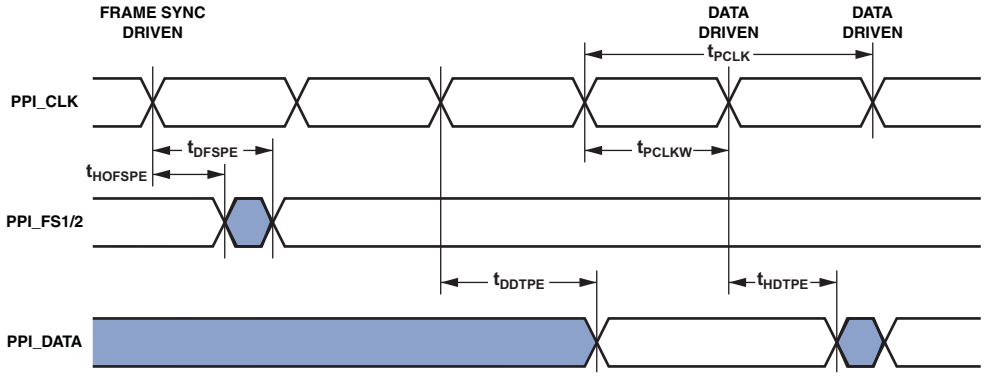


Figure 19. PPI GP Tx Mode with Internal Frame Sync Timing

Serial Ports

Table 33 through Table 36 on Page 42 and Figure 22 on Page 40 through Figure 25 on Page 42 describe serial port operations.

Table 33. Serial Ports—External Clock

Parameter		V_{DDEXT} 1.8 V Nominal		V_{DDEXT} 2.5 V/3.3 V Nominal		Unit
		Min	Max	Min	Max	
Timing Requirements						
t_{SFSE}[1]	TFSx/RFSx Setup Before TSCLKx/RSCLKx	3		3		ns
t_{HFSE}[1]	TFSx/RFSx Hold After TSCLKx/RSCLKx	3		3		ns
t_{SDRE}[1]	Receive Data Setup Before RSCLKx	3		3		ns
t_{HDRE}[1]	Receive Data Hold After RSCLKx	3.5		3		ns
t_{SCLKEW}	TSCLKx/RSCLKx Width	7		4.5		ns
t_{SCLKE}	TSCLKx/RSCLKx Period	$2 \times t_{SCLK}$		$2 \times t_{SCLK}$		ns
t_{SUDTE}[2]	Start-Up Delay From SPORT Enable To First External TFSx	$4 \times t_{SCLKE}$		$4 \times t_{SCLKE}$		ns
t_{SUDRE}[2]	Start-Up Delay From SPORT Enable To First External RFSx	$4 \times t_{SCLKE}$		$4 \times t_{SCLKE}$		ns
Switching Characteristics						
t_{DFSE}[3]	TFSx/RFSx Delay After TSCLKx/RSCLKx (Internally Generated TFSx/RFSx)		10		10	ns
t_{HOFSE}[3]	TFSx/RFSx Hold After TSCLKx/RSCLKx (Internally Generated TFSx/RFSx)	0		0		ns
t_{DDTE}[3]	Transmit Data Delay After TSCLKx		10		10	ns
t_{HDTE}[3]	Transmit Data Hold After TSCLKx	0		0		ns

[1] Referenced to sample edge.
[2] Verified in design but untested.
[3] Referenced to drive edge.

Table 34. Serial Ports—Internal Clock

Parameter		V_{DDEXT} 1.8 V Nominal		V_{DDEXT} 2.5 V/3.3 V Nominal		Unit
		Min	Max	Min	Max	
Timing Requirements						
t_{SFSI}[1]	TFSx/RFSx Setup Before TSCLKx/RSCLKx	11		9.6		ns
t_{HFSI}[1]	TFSx/RFSx Hold After TSCLKx/RSCLKx	–1.5		–1.5		ns
t_{SDRI}[1]	Receive Data Setup Before RSCLKx	11		9.6		ns
t_{HDRI}[1]	Receive Data Hold After RSCLKx	–1.5		–1.5		ns
Switching Characteristics						
t_{DFSI}[2]	TFSx/RFSx Delay After TSCLKx/RSCLKx (Internally Generated TFSx/RFSx)		3		3	ns
t_{HOFSI}[2]	TFSx/RFSx Hold After TSCLKx/RSCLKx (Internally Generated TFSx/RFSx)	–2		–1		ns
t_{DDTI}[2]	Transmit Data Delay After TSCLKx		3		3	ns
t_{HDTI}[2]	Transmit Data Hold After TSCLKx	–1.8		–1.5		ns
t_{SCLKIW}	TSCLKx/RSCLKx Width	10		8		ns

[1] Referenced to sample edge.
[2] Referenced to drive edge.

Table 35. Serial Ports—Enable and Three-State[1]

Parameter		Min	Max	Unit
Switching Characteristics				
t_{DTENE}	Data Enable Delay from External TSCLKx	0		ns
t_{DDTTE}	Data Disable Delay from External TSCLKx		t_{SCLK} + 1	ns
t_{DTENI}	Data Enable Delay from Internal TSCLKx	–2.0		ns
t_{DDTTI}	Data Disable Delay from Internal TSCLKx		t_{SCLK} + 1	ns

[1] Referenced to drive edge.

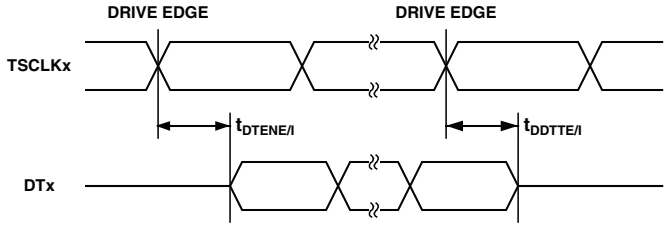


Figure 24. Enable and Three-State

Table 47. 10/100 Ethernet MAC Controller Timing: MII/RMII Asynchronous Signal

Parameter		Min	Max	Unit
Timing Requirements				
t_{ECOLH}	COL Pulse Width High[1]	$t_{ETxCLK} \times 1.5$		ns
		$t_{ERxCLK} \times 1.5$		ns
t_{ECOLL}	COL Pulse Width Low[1]	$t_{ETxCLK} \times 1.5$		ns
		$t_{ERxCLK} \times 1.5$		ns
t_{ECRSH}	CRS Pulse Width High[2]	$t_{ETxCLK} \times 1.5$		ns
t_{ECRSL}	CRS Pulse Width Low[2]	$t_{ETxCLK} \times 1.5$		ns

[1] MII/RMII asynchronous signals are COL, CRS. These signals are applicable in both MII and RMII modes. The asynchronous COL input is synchronized separately to both the ETxCLK and the ERxCLK, and must have a minimum pulse width high or low at least 1.5 times the period of the slower of the two clocks.
[2] The asynchronous CRS input is synchronized to the ETxCLK, and must have a minimum pulse width high or low at least 1.5 times the period of ETxCLK.

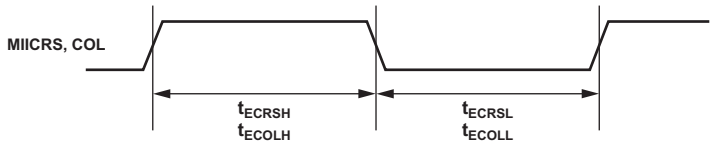


Figure 36. 10/100 Ethernet MAC Controller Timing: Asynchronous Signal

Table 48. 10/100 Ethernet MAC Controller Timing: MII Station Management

Parameter[1]		Min	Max	Unit
Timing Requirements				
t_{MDIOS}	MDIO Input Valid to MDC Rising Edge (Setup)	11.5		ns
t_{MDCIH}	MDC Rising Edge to MDIO Input Invalid (Hold)	0		ns
Switching Characteristics				
t_{MDCOV}	MDC Falling Edge to MDIO Output Valid		25	ns
t_{MDCOH}	MDC Falling Edge to MDIO Output Invalid (Hold)	–1.25		ns

[1] MDC/MDIO is a 2-wire serial bidirectional port for controlling one or more external PHYs. MDC is an output clock whose minimum period is programmable as a multiple of the system clock SCLK. MDIO is a bidirectional data line.

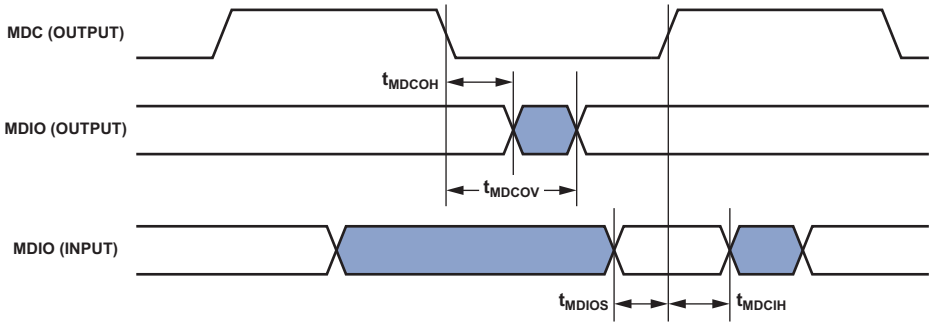


Figure 37. 10/100 Ethernet MAC Controller Timing: MII Station Management

JTAG Test And Emulation Port Timing

Table 49 and Figure 38 describe JTAG port operations.

Table 49. JTAG Port Timing

Parameter		Min	Max	Unit
Timing Requirements				
t_{TCK}	TCK Period	20		ns
t_{STAP}	TDI, TMS Setup Before TCK High	4		ns
t_{HTAP}	TDI, TMS Hold After TCK High	4		ns
t_{SSYS}[1]	System Inputs Setup Before TCK High	4		ns
t_{HSYS}[1]	System Inputs Hold After TCK High	5		ns
t_{TRSTW}	$\overline{TRST}$ Pulse Width[2] (measured in TCK cycles)	4		TCK
Switching Characteristics				
t_{DTDO}	TDO Delay from TCK Low		10	ns
t_{DSYS}[3]	System Outputs Delay After TCK Low	0	13	ns

[1] System Inputs = DATA15–0, SCL, SDA, TFS0, TSCLK0, RSCLK0, RFS0, DR0PRI, DR0SEC, PF15–0, PG15–0, PH7–0, MDIO, TD1, TMS, $\overline{RESET}$, $\overline{NMI}$, BMODE2–0.
[2] 50 MHz Maximum.
[3] System Outputs = DATA15–0, ADDR19–1, $\overline{ABE1–0}$, $\overline{ARE}$, $\overline{AWE}$, $\overline{AMS1–0}$, $\overline{SRAS}$, $\overline{SCAS}$, $\overline{SWE}$, SCKE, CLKOUT, SA10, $\overline{SMS}$, SCL, SDA, TSCLK0, TFS0, RFS0, RSCLK0, DT0PRI, DT0SEC, PF15–0, PG15–0, PH7–0, MDC, MDIO.

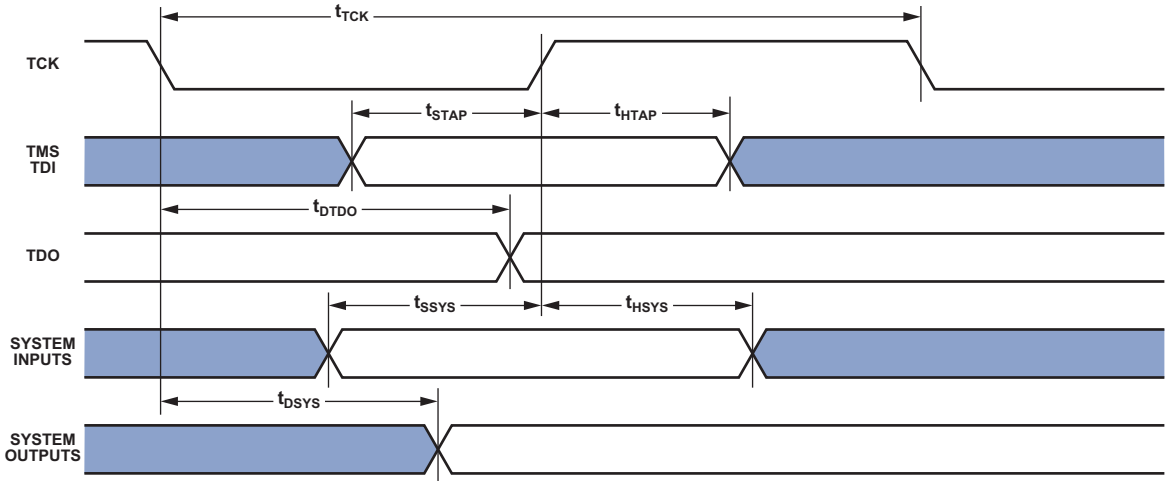


Figure 38. JTAG Port Timing

Output Disable Time Measurement

Output signals are considered to be disabled when they stop driving, go into a high impedance state, and start to decay from their output high or low voltage. The output disable time t_{DIS} is the difference between $t_{DIS\_MEASURED}$ and t_{DECAY} as shown on the left side of Figure 55.

$$t_{DIS} = t_{DIS\_MEASURED} - t_{DECAY}$$

The time for the voltage on the bus to decay by ΔV is dependent on the capacitive load C_L and the load current I_L. This decay time can be approximated by the equation:

$$t_{DECAY} = (C_L \Delta V)/I_L$$

The time t_{DECAY} is calculated with test loads C_L and I_L and with ΔV equal to 0.25 V for V_{DDEXT}/V_{DDMEM} (nominal) = 2.5 V/3.3 V and 0.15 V for V_{DDEXT}/V_{VDDMEM} (nominal) = 1.8 V.

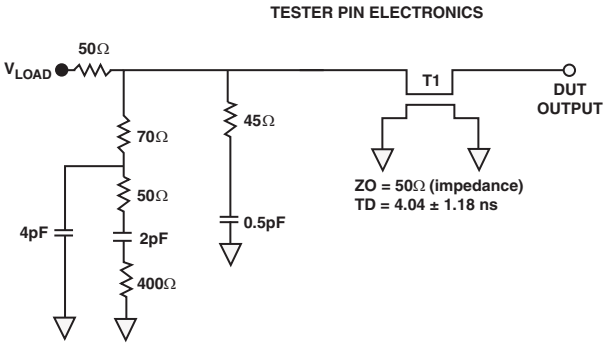
The time $t_{DIS\_MEASURED}$ is the interval from when the reference signal switches to when the output voltage decays ΔV from the measured output high or output low voltage.

Example System Hold Time Calculation

To determine the data output hold time in a particular system, first calculate t_{DECAY} using the equation given above. Choose ΔV to be the difference between the ADSP-BF51x processor's output voltage and the input threshold for the device requiring the hold time. C_L is the total bus capacitance (per data line), and I_L is the total leakage or three-state current (per data line). The hold time is t_{DECAY} plus the various output disable times as specified in the Timing Specifications on Page 29 (for example t_{DSDAT} for an SDRAM write cycle as shown in SDRAM Interface Timing on Page 33).

Capacitive Loading

Output delays and holds are based on standard capacitive loads of an average of 6 pF on all balls (see Figure 56). V_{LOAD} is equal to $(V_{DDEXT}/V_{DDMEM})/2$. The graphs of Figure 57 through Figure 68 show how output rise time varies with capacitance. The delay and hold specifications given should be derated by a factor derived from these figures. The graphs in these figures may not be linear outside the ranges shown.



NOTES:
THE WORST CASE TRANSMISSION LINE DELAY IS SHOWN AND CAN BE USED FOR THE OUTPUT TIMING ANALYSIS TO REFLECT THE TRANSMISSION LINE EFFECT AND MUST BE CONSIDERED. THE TRANSMISSION LINE (TD) IS FOR LOAD ONLY AND DOES NOT AFFECT THE DATA SHEET TIMING SPECIFICATIONS.

ANALOG DEVICES RECOMMENDS USING THE IBIS MODEL TIMING FOR A GIVEN SYSTEM REQUIREMENT. IF NECESSARY, A SYSTEM MAY INCORPORATE EXTERNAL DRIVERS TO COMPENSATE FOR ANY TIMING DIFFERENCES.

Figure 56. Equivalent Device Loading for AC Measurements (Includes All Fixtures)

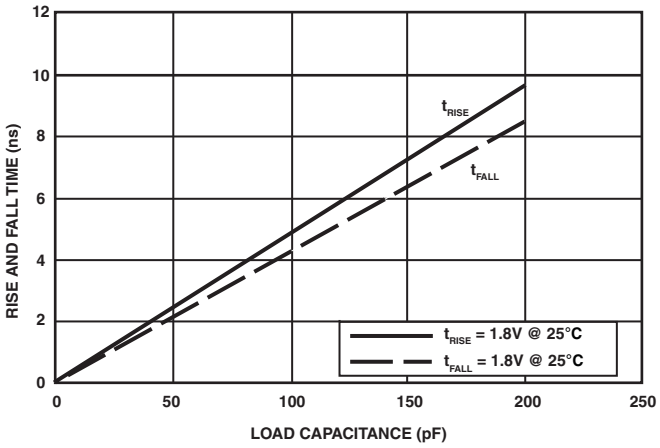


Figure 57. Driver Type A Typical Rise and Fall Times (10%–90%) vs. Load Capacitance (1.8V V_{DDEXT}/V_{DDMEM})

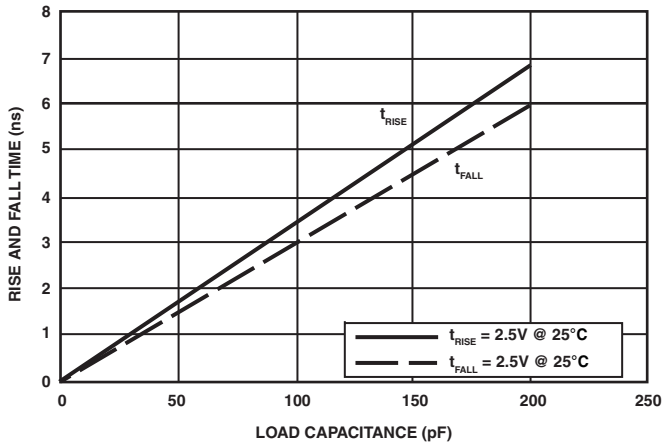


Figure 58. Driver Type A Typical Rise and Fall Times (10%–90%) vs. Load Capacitance (2.5V V_{DDEXT}/V_{DDMEM})

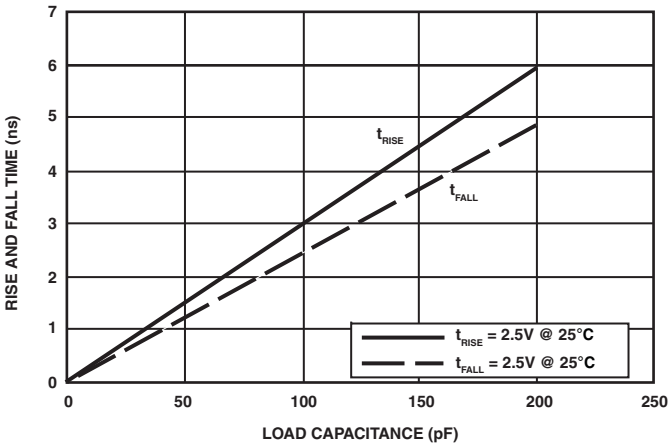


Figure 61. Driver Type B Typical Rise and Fall Times (10%–90%) vs. Load Capacitance (2.5V V_{DDEXT}/V_{DDMEM})

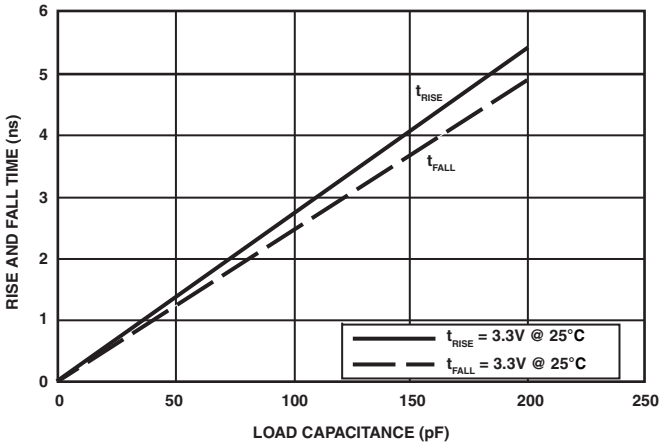


Figure 59. Driver Type A Typical Rise and Fall Times (10%–90%) vs. Load Capacitance (3.3V V_{DDEXT}/V_{DDMEM})

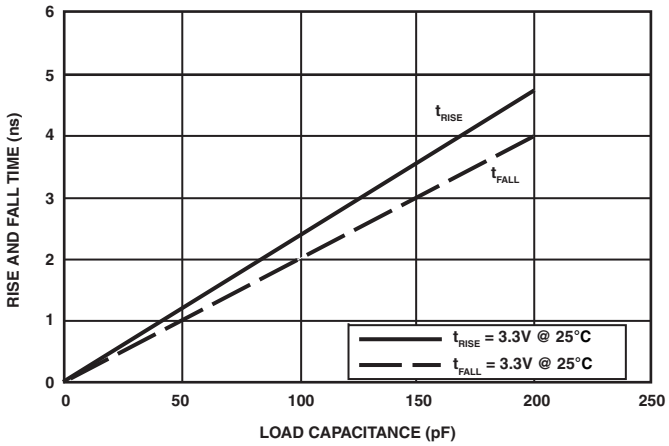


Figure 62. Driver Type B Typical Rise and Fall Times (10%–90%) vs. Load Capacitance (3.3V V_{DDEXT}/V_{DDMEM})

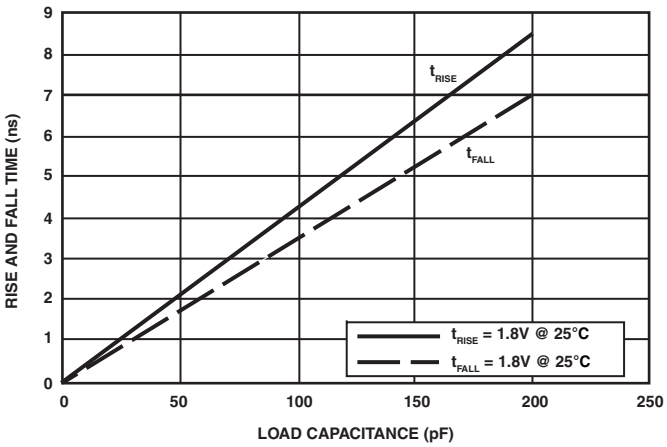


Figure 60. Driver Type B Typical Rise and Fall Times (10%–90%) vs. Load Capacitance (1.8V V_{DDEXT}/V_{DDMEM})

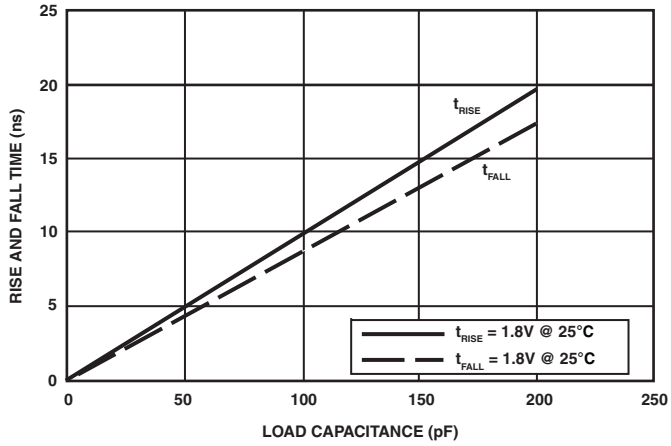


Figure 63. Driver Type C Typical Rise and Fall Times (10%–90%) vs. Load Capacitance (1.8V V_{DDEXT}/V_{DDMEM})

Table 53. 176-Lead LQFP_EP Pin Assignment (Alphabetical by Signal Mnemonic)

Lead No.	Signal	Lead No.	Signal	Lead No.	Signal	Lead No.	Signal
107	A1	58	D13	5	PF7	113	$\overline{SWE}$
106	A2	57	D14	4	PF8	53	TCK
105	A3	56	D15	3	PF9	52	TDI
103	A4	51	$\overline{EMU}$	174	PF10	50	TDO
102	A5	130	EXT_WAKE	171	PF11	55	TMS
101	A6	1	GND	168	PF12	54	$\overline{TRST}$
97	A7	2	GND	167	PF13	7	V_{DDEXT}
96	A8	15	GND	166	PF14	24	V_{DDEXT}
94	A9	22	GND	165	PF15	35	V_{DDEXT}
93	A10	43	GND	135	$\overline{PG}$	49	V_{DDEXT}
92	A11	44	GND	48	PG0	128	V_{DDEXT}
91	A12	45	GND	47	PG1	129	V_{DDEXT}
86	A13	46	GND	39	PG2	136	V_{DDEXT}
85	A14	67	GND	38	PG3	145	V_{DDEXT}
84	A15	83	GND	37	PG4	148	V_{DDEXT}
81	A16	87	GND	36	PG5	158	V_{DDEXT}
80	A17	88	GND	34	PG6	170	V_{DDEXT}
78	A18	89	GND	33	PG7	16	$V_{DDFLASH}$
77	A19	90	GND	32	PG8	17	$V_{DDFLASH}$
109	$\overline{ABE}$0	99	GND	31	PG9	29	$V_{DDFLASH}$
108	$\overline{ABE}$1	111	GND	28	PG10	126	$V_{DDFLASH}$
123	$\overline{AMS}$0	131	GND	27	PG11	14	V_{DDINT}
120	$\overline{AMS}$1	132	GND	26	PG12	23	V_{DDINT}
121	$\overline{ARE}$	133	GND	25	PG13	30	V_{DDINT}
122	$\overline{AWE}$	134	GND	21	PG14	63	V_{DDINT}
42	BMODE0	137	GND	20	PG15	79	V_{DDINT}
41	BMODE1	139	GND	162	PH0	98	V_{DDINT}
40	BMODE2	149	GND	161	PH1	100	V_{DDINT}
150	CLKBUF	151	GND	160	PH2	116	V_{DDINT}
143	CLKIN	157	GND	159	PH3	138	V_{DDINT}
125	CLKOUT	163	GND	156	PH4	152	V_{DDINT}
76	D0	169	GND	155	PH5	164	V_{DDINT}
74	D1	175	GND	154	PH6	59	V_{DDMEM}
73	D2	176	GND	153	PH7	68	V_{DDMEM}
72	D3	117	GND	146	$\overline{RESET}$	75	V_{DDMEM}
71	D4	127	NC[1]	141	RTXI	82	V_{DDMEM}
70	D5	147	$\overline{NMI}$	140	RTXO	95	V_{DDMEM}
69	D6	19	PF0	110	SA10	104	V_{DDMEM}
66	D7	18	PF1	114	$\overline{SCAS}$	112	V_{DDMEM}
65	D8	13	PF2	119	SCKE	124	V_{DDMEM}
64	D9	12	PF3	173	SCL	9	V_{DDOTP}
62	D10	11	PF4	172	SDA	142	V_{DDRTC}
61	D11	10	PF5	118	$\overline{SMS}$	8	V_{PPOTP}
60	D12	6	PF6	115	$\overline{SRAS}$	144	XTAL
						GND	177*

* Pin no. 177 is the GND supply (see Figure 70) for the processor; this pad must be **robustly** connected to GND.

[1] This pin must not be connected.

Table 55. 168-Ball CSP_BGA Ball Assignment (Alphabetical by Signal Mnemonic)

Ball No.	Signal Name	Ball No.	Signal Name	Ball No.	Signal Name	Ball No.	Signal Name	Ball No.	Signal Name	Ball No.	Signal Name
K14	A1	A11	CLKBUF	G6	GND	C4	PF10	A8	PH5	G5	V_{DDEXT}
K13	A2	A13	CLKIN	G7	GND	C7	PF11	A9	PH6	H5	V_{DDEXT}
H12	A3	D13	CLKOUT	G8	GND	B4	PF12	A10	PH7	D12	$V_{DDFLASH}$
L14	A4	M9	D0	G9	GND	A4	PF13	B10	$\overline{RESET}$	E1	$V_{DDFLASH}$
M14	A5	N9	D1	H6	GND	B5	PF14	C11	RTXI	J2	$V_{DDFLASH}$
L13	A6	M8	D2	H7	GND	A5	PF15	C12	RTXO	C9	V_{DDINT}
N14	A7	P11	D3	H8	GND	C13	$\overline{PG}$	J14	SA10	E7	V_{DDINT}
K12	A8	P10	D4	H9	GND	M4	PG0	H14	$\overline{SCAS}$	E8	V_{DDINT}
L12	A9	N8	D5	J6	GND	N2	PG1	F13	SCKE	E9	V_{DDINT}
M13	A10	P9	D6	J7	GND	L3	PG2	A2	SCL	E10	V_{DDINT}
N13	A11	P8	D7	J8	GND	L2	PG3	A3	SDA	F3	V_{DDINT}
M12	A12	P7	D8	J9	GND	M1	PG4	F12	$\overline{SMS}$	F10	V_{DDINT}
M11	A13	N7	D9	P1	GND	L1	PG5	G13	$\overline{SRAS}$	G3	V_{DDINT}
N12	A14	M7	D10	P13	GND	K1	PG6	G12	$\overline{SWE}$	G10	V_{DDINT}
J12	A15	P6	D11	P14	GND	K3	PG7	P3	TCK	H10	V_{DDINT}
N11	A16	M6	D12	G14	GND	K2	PG8	P2	TDI	J10	V_{DDINT}
M10	A17	N6	D13	C14	NC[1]	J3	PG9	N3	TDO	E12	V_{DDMEM}
N10	A18	P5	D14	B11	$\overline{NMI}$	J1	PG10	N5	TMS	J5	V_{DDMEM}
P12	A19	P4	D15	F1	PF0	H3	PG11	N4	$\overline{TRST}$	K5	V_{DDMEM}
H13	$\overline{ABE}$0	M5	$\overline{EMU}$	F2	PF1	H1	PG12	B9	V_{DDEXT}	K6	V_{DDMEM}
J13	$\overline{ABE}$1	B14	EXT_WAKE	E2	PF2	H2	PG13	B13	V_{DDEXT}	K7	V_{DDMEM}
D14	$\overline{AMS}$0	A1	GND	D1	PF3	G2	PG14	C5	V_{DDEXT}	K8	V_{DDMEM}
F14	$\overline{AMS}$1	A14	GND	C1	PF4	G1	PG15	C6	V_{DDEXT}	K9	V_{DDMEM}
E13	$\overline{ARE}$	B2	GND	D2	PF5	B6	PH0	C8	V_{DDEXT}	K10	V_{DDMEM}
E14	$\overline{AWE}$	F6	GND	E3	PF6	A7	PH1	C10	V_{DDEXT}	B1	V_{DDOTP}
M3	BMODE0	F7	GND	C2	PF7	A6	PH2	E5	V_{DDEXT}	B12	V_{DDRTC}
N1	BMODE1	F8	GND	C3	PF8	B7	PH3	E6	V_{DDEXT}	D3	V_{PPOTP}
M2	BMODE2	F9	GND	B3	PF9	B8	PH4	F5	V_{DDEXT}	A12	XTAL

[1] This pin must not be connected.

Figure 71 shows the top view of the CSP_BGA ball configuration. Figure 72 shows the bottom view of the CSP_BGA ball configuration.

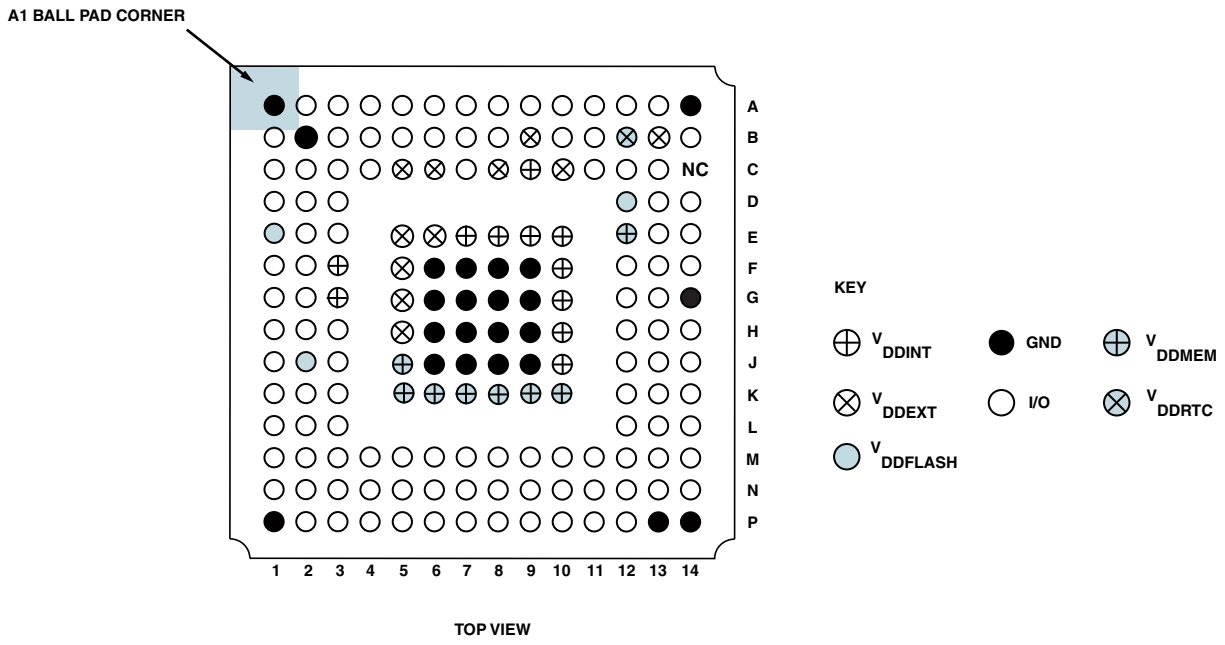


Figure 71. 168-Ball CSP_BGA Ball Configuration (Top View)

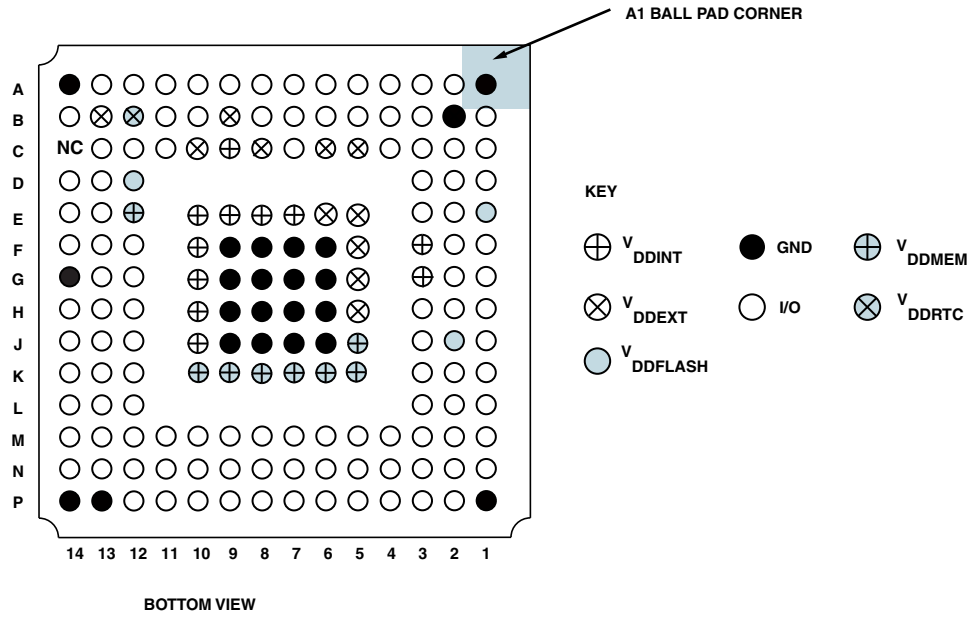


Figure 72. 168-Ball CSP_BGA Ball Configuration (Bottom View)