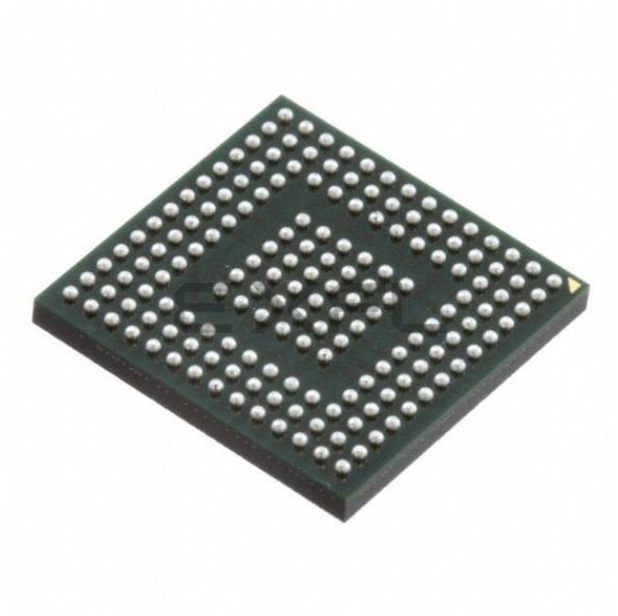


Welcome to E-XFL.COM

Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Obsolete
Type	Fixed Point
Interface	I²C, PPI, RSI, SPI, SPORT, UART/USART
Clock Rate	400MHz
Non-Volatile Memory	FLASH (16Mbit)
On-Chip RAM	116kB
Voltage - I/O	1.8V, 2.5V, 3.3V
Voltage - Core	1.30V
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	168-LFBGA, CSPBGA
Supplier Device Package	168-CSPBGA (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-bf514bbcz4f16

(EVT), and lists their priorities are described in the *ADSP-BF51x Blackfin Processor Hardware Reference Manual* "System Interrupts" chapter.

System Interrupt Controller (SIC)

The system interrupt controller provides the mapping and routing of events from the many peripheral interrupt sources to the prioritized general-purpose interrupt inputs of the CEC. Although the processors provide a default mapping, the user can alter the mappings and priorities of interrupt events by writing the appropriate values into the interrupt assignment registers (SIC_IARx). See the *ADSP-BF51x Blackfin Processor Hardware Reference Manual* "System Interrupts" chapter for the inputs into the SIC and the default mappings into the CEC.

The SIC allows further control of event processing by providing three pairs of 32-bit interrupt control and status registers. Each register contains a bit corresponding to each of the peripheral interrupt events. For more information, see the *ADSP-BF51x Blackfin Processor Hardware Reference Manual* "System Interrupts" chapter.

DMA CONTROLLERS

The ADSP-BF51x processors have multiple independent DMA channels that support automated data transfers with minimal overhead for the processor core. DMA transfers can occur between the processor's internal memories and any of its DMA-capable peripherals. Additionally, DMA transfers can be accomplished between any of the DMA-capable peripherals and external devices connected to the external memory interfaces, including the SDRAM controller and the asynchronous memory controller. DMA-capable peripherals include the Ethernet MAC, RSI, SPORTs, SPIs, UARTs, and PPI. Each individual DMA-capable peripheral has at least one dedicated DMA channel.

The processors' DMA controller supports both one-dimensional (1-D) and two-dimensional (2-D) DMA transfers. DMA transfer initialization can be implemented from registers or from sets of parameters called descriptor blocks.

The 2-D DMA capability supports arbitrary row and column sizes up to 64K elements by 64K elements, and arbitrary row and column step sizes up to ±32K elements. Furthermore, the column step size can be less than the row step size, allowing implementation of interleaved data streams. This feature is especially useful in video applications where data can be de-interleaved on the fly.

Examples of DMA types supported by the DMA controller include:

- A single, linear buffer that stops upon completion
- A circular, auto-refreshing buffer that interrupts on each full or fractionally full buffer
- 1-D or 2-D DMA using a linked list of descriptors
- 2-D DMA using an array of descriptors, specifying only the base DMA address within a common page

In addition to the dedicated peripheral DMA channels, there are two memory DMA channels that transfer data between the various memories of the processor system. This enables transfers of blocks of data between any of the memories—including external SDRAM, ROM, SRAM, and flash memory—with minimal processor intervention. Memory DMA transfers can be controlled by a very flexible descriptor-based methodology or by a standard register-based autobuffer mechanism.

The processors also have an external DMA controller capability via dual external DMA request signals when used in conjunction with the external bus interface unit (EBIU). This functionality can be used when a high speed interface is required for external FIFOs and high bandwidth communications peripherals. It allows control of the number of data transfers for memory DMA. The number of transfers per edge is programmable. This feature can be programmed to allow memory DMA to have an increased priority on the external bus relative to the core.

PROCESSOR PERIPHERALS

The ADSP-BF51x processors contain a rich set of peripherals connected to the core via several high bandwidth buses, providing flexibility in system configuration as well as excellent overall system performance (see Figure 2). The processors contain dedicated network communication modules and high speed serial and parallel ports, an interrupt controller for flexible management of interrupts from the on-chip peripherals or external sources, and power management control functions to tailor the performance and power characteristics of the processor and system to many application scenarios.

All of the peripherals, except for the general-purpose I/O, rotary counter, TWI, three-phase PWM, real-time clock, and timers, are supported by a flexible DMA structure. There are also separate memory DMA channels dedicated to data transfers between the processor's various memory spaces, including external SDRAM and asynchronous memory. Multiple on-chip buses provide enough bandwidth to keep the processor core running along with activity on all of the on-chip and external peripherals.

Real-Time Clock

The real-time clock (RTC) provides a robust set of digital watch features, including current time, stopwatch, and alarm. The RTC is clocked by a 32.768 kHz crystal external to the processors. The RTC peripheral has a dedicated power supply so that it can remain powered up and clocked even when the rest of the processor is in a low power state. The RTC provides several programmable interrupt options, including interrupt per second, minute, hour, or day clock ticks, interrupt on programmable stopwatch countdown, or interrupt at a programmed alarm time.

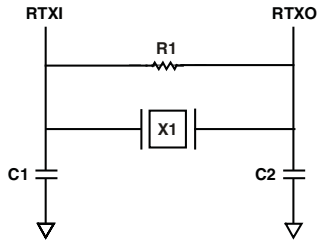
The 32.768 kHz input clock frequency is divided down to a 1 Hz signal by a prescaler. The counter function of the timer consists of four counters: a 60-second counter, a 60-minute counter, a 24-hour counter, and an 32,768-day counter.

When enabled, the alarm function generates an interrupt when the output of the timer matches the programmed value in the alarm control register. There are two alarms: The first alarm is for a time of day. The second alarm is for a day and time of that day.

The stopwatch function counts down from a programmed value, with one-second resolution. When the stopwatch is enabled and the counter underflows, an interrupt is generated.

Like the other peripherals, the RTC can wake up the processor from sleep mode upon generation of any RTC wakeup event. Additionally, an RTC wakeup event can wake up the processor from deep sleep mode or cause a transition from the hibernate state.

Connect RTC signals RTXI and RTXO with external components as shown in Figure 5.



SUGGESTED COMPONENTS:
X1 = ECLIPTEK EC38J (THROUGH-HOLE PACKAGE) OR
EPSON MC405 12 pF LOAD (SURFACE-MOUNT PACKAGE)
C1 = 22 pF
C2 = 22 pF
R1 = 10 MΩ
NOTE: C1 AND C2 ARE SPECIFIC TO CRYSTAL SPECIFIED FOR X1. CONTACT CRYSTAL MANUFACTURER FOR DETAILS. C1 AND C2 SPECIFICATIONS ASSUME BOARD TRACE CAPACITANCE OF 3 pF.

Figure 5. External Components for RTC

Watchdog Timer

The ADSP-BF51x processors include a 32-bit timer that can be used to implement a software watchdog function. A software watchdog can improve system availability by forcing the processor to a known state through generation of a hardware reset, nonmaskable interrupt (NMI), or general-purpose interrupt, if the timer expires before being reset by software. The programmer initializes the count value of the timer, enables the appropriate interrupt, then enables the timer. Thereafter, the software must reload the counter before it counts to zero from the programmed value. This protects the system from remaining in an unknown state where software, which would normally reset the timer, has stopped running due to an external noise condition or software error.

If configured to generate a hardware reset, the watchdog timer resets both the core and the processor peripherals. After a reset, software can determine if the watchdog was the source of the hardware reset by interrogating a status bit in the watchdog timer control register.

The timer is clocked by the system clock (SCLK) at a maximum frequency of f_{SCLK}.

Timers

There are nine general-purpose programmable timer units in the ADSP-BF51x processors. Eight timers have an external signal that can be configured either as a pulse width modulator (PWM) or timer output, as an input to clock the timer, or as a mechanism for measuring pulse widths and periods of external events. These timers can be synchronized to an external clock input to the several other associated PF signals, an external clock input to the PPI_CLK input signal, or to the internal SCLK.

The timer units can be used in conjunction with the two UARTs to measure the width of the pulses in the data stream to provide a software auto-baud detect function for the respective serial channels.

The timers can generate interrupts to the processor core providing periodic events for synchronization, either to the system clock or to a count of external signals.

In addition to the eight general-purpose programmable timers, a ninth timer is also provided. This extra timer is clocked by the internal processor clock and is typically used as a system tick clock for generation of operating system periodic interrupts.

3-Phase PWM

The processors integrate a flexible and programmable 3-phase PWM waveform generator that can be programmed to generate the required switching patterns to drive a 3-phase voltage source inverter for ac induction (ACIM) or permanent magnet synchronous (PMSM) motor control. In addition, the PWM block contains special functions that considerably simplify the generation of the required PWM switching patterns for control of the electronically commutated motor (ECM) or brushless dc motor (BDCM). Software can enable a special mode for switched reluctance motors (SRM).

Features of the 3-phase PWM generation unit are:

- 16-bit center-based PWM generation unit
- Programmable PWM pulse width
- Single/double update modes
- Programmable dead time and switching frequency
- Twos-complement implementation which permits smooth transition to full ON and full OFF states
- Possibility to synchronize the PWM generation to an external synchronization
- Special provisions for BDCM operation (crossover and output enable functions)
- Wide variety of special switched reluctance (SR) operating modes
- Output polarity and clock gating control
- Dedicated asynchronous PWM shutdown signal

General-Purpose (GP) Counter

A 32-bit GP counter is provided that can sense 2-bit quadrature or binary codes as typically emitted by industrial drives or manual thumb wheels. The counter can also operate in

general-purpose up/down count modes. Then, count direction is either controlled by a level-sensitive input signal or by two edge detectors.

A third input can provide flexible zero marker support and can alternatively be used to input the push-button signal of thumb wheels. All three signals have a programmable debouncing circuit.

An internal signal forwarded to the GP timer unit enables one timer to measure the intervals between count events. Boundary registers enable auto-zero operation or simple system warning by interrupts when programmable count values are exceeded.

Serial Ports

The ADSP-BF51x processors incorporate two dual-channel synchronous serial ports (SPORT0 and SPORT1) for serial and multiprocessor communications. The SPORTs support the following features:

Serial port data can be automatically transferred to and from on-chip memory/external memory via dedicated DMA channels. Each of the serial ports can work in conjunction with another serial port to provide TDM support. In this configuration, one SPORT provides two transmit signals while the other SPORT provides the two receive signals. The frame sync and clock are shared.

Serial ports operate in five modes:

- Standard DSP serial mode
- Multichannel (TDM) mode
- I^2S mode
- Packed I^2S mode
- Left-justified mode

Serial Peripheral Interface (SPI) Ports

The processors have two SPI-compatible ports (SPI0 and SPI1) that enable the processor to communicate with multiple SPI-compatible devices.

The SPI interface uses three signals for transferring data: two data signals (master output-slave input–MOSI, and master input-slave output–MISO) and a clock signal (serial clock–SCK). An SPI chip select input signal ($\overline{\text{SPIxSS}}$) lets other SPI devices select the processor, and multiple SPI chip select output signals let the processor select other SPI devices. The SPI select signals are reconfigured general-purpose I/O signals. Using these signals, the SPI port provides a full-duplex, synchronous serial interface, which supports both master/slave modes and multimaster environments.

The SPI port baud rate and clock phase/polarities are programmable, and it has an integrated DMA channel, configurable to support transmit or receive data streams. The SPI's DMA channel can only service unidirectional accesses at any given time.

UART Ports

The processors provide two full-duplex universal asynchronous receiver/transmitter (UART) ports, which are fully compatible with PC-standard UARTs. Each UART port provides a simplified UART interface to other peripherals or hosts, supporting full-duplex, DMA-supported, asynchronous transfers of serial data. A UART port includes support for five to eight data bits, and none, even, or odd parity. Optionally, an additional address bit can be transferred to interrupt only addressed nodes in multi-drop bus (MDB) systems. A frame is terminates by one, one and a half, two or two and a half stop bits.

The UART ports support automatic hardware flow control through the Clear To Send (CTS) input and Request To Send (RTS) output with programmable assertion FIFO levels.

To help support the Local Interconnect Network (LIN) protocols, a special command causes the transmitter to queue a break command of programmable bit length into the transmit buffer. Similarly, the number of stop bits can be extended by a programmable inter-frame space.

The capabilities of the UARTs are further extended with support for the Infrared Data Association (IrDA®) serial infrared physical layer link specification (SIR) protocol.

2-Wire Interface (TWI)

The processors include a TWI module for providing a simple exchange method of control data between multiple devices. The TWI is compatible with the widely used I^2C® bus standard. The TWI module offers the capabilities of simultaneous master and slave operation, support for both 7-bit addressing and multimedia data arbitration. The TWI interface utilizes two signals for transferring clock (SCL) and data (SDA) and supports the protocol at speeds up to 400k bits/sec. The TWI interface signals are compatible with 5 V logic levels.

Additionally, the processor's TWI module is fully compatible with serial camera control bus (SCCB) functionality for easier control of various CMOS camera sensor devices.

Removable Storage Interface (RSI)

The RSI controller, available on the ADSP-BF514/ADSP-BF514F16/ADSP-BF516/ADSP-BF518/ADSP-BF518F16 processors, acts as the host interface for multi-media cards (MMC), secure digital memory cards (SD Card), secure digital input/output cards (SDIO), and CE-ATA hard disk drives. The following list describes the main features of the RSI controller.

- Support for a single MMC, SD memory, SDIO card or CE-ATA hard disk drive
- Support for 1-bit and 4-bit SD modes
- Support for 1-bit, 4-bit and 8-bit MMC modes
- Support for 4-bit and 8-bit CE-ATA hard disk drives
- A ten-signal external interface with clock, command, and up to eight data lines
- Card detection using one of the data signals
- Card interface clock generation from SCLK
- SDIO interrupt and read wait features
- CE-ATA command completion signal recognition and disable

Parallel Peripheral Interface (PPI)

The ADSP-BF51x processors provide a parallel peripheral interface (PPI) that can connect directly to parallel analog-to-digital and digital-to-analog converters, ITU-R-601/656 video encoders and decoders, and other general-purpose peripherals. The PPI consists of a dedicated input clock signal, up to three frame synchronization signals, and up to 16 data signals.

In ITU-R-656 modes, the PPI receives and parses a data stream of 8-bit or 10-bit data elements. On-chip decode of embedded preamble control and synchronization information is supported.

Three distinct ITU-R-656 modes are supported:

- Active video only mode—The PPI does not read in any data between the End of Active Video (EAV) and Start of Active Video (SAV) preamble symbols, or any data present during the vertical blanking intervals. In this mode, the control byte sequences are not stored to memory; they are filtered by the PPI.
- Vertical blanking only mode—The PPI only transfers vertical blanking interval (VBI) data, as well as horizontal blanking information and control byte sequences on VBI lines.
- Entire field mode—The entire incoming bitstream is read in through the PPI. This includes active video, control preamble sequences, and ancillary data that may be embedded in horizontal and vertical blanking intervals.

Though not explicitly supported, ITU-R-656 output functionality can be achieved by setting up the entire frame structure (including active video, blanking, and control information) in memory and streaming the data out the PPI in a frame sync-less mode. The processor's 2-D DMA features facilitate this transfer by allowing the static frame buffer (blanking and control codes) to be placed in memory once, and simply updating the active video information on a per-frame basis.

The general-purpose modes of the PPI are intended to suit a wide variety of data capture and transmission applications. The modes are divided into four main categories, each allowing up to 16 bits of data transfer per PPI_CLK cycle:

- Data receive with internally generated frame syncs
- Data receive with externally generated frame syncs
- Data transmit with internally generated frame syncs
- Data transmit with externally generated frame syncs

These modes support ADC/DAC connections, as well as video communication with hardware signalling. Many of the modes support more than one level of frame synchronization. If desired, a programmable delay can be inserted between assertion of a frame sync and reception/transmission of data.

Code Security with Lockbox Secure Technology

A security system consisting of a blend of hardware and software provides customers with a flexible and rich set of code security features with Lockbox® secure technology. Key features include:

- OTP memory
- Unique chip ID
- Code authentication
- Secure mode of operation

The security scheme is based upon the concept of authentication of digital signatures using standards-based algorithms and provides a secure processing environment in which to execute code and protect assets.

DYNAMIC POWER MANAGEMENT

The ADSP-BF51x processors provide four operating modes, each with a different performance/power profile. In addition, dynamic power management provides the control functions to dynamically alter the processor core supply voltage, further reducing power dissipation. When configured for a 0 V core supply voltage, the processor enters the hibernate state. Control of clocking to each of the processor peripherals also reduces power consumption. See Table 3 for a summary of the power settings for each mode.

Table 3. Power Settings

Mode/State	PLL	PLL Bypassed	Core Clock (CCLK)	System Clock (SCLK)	Core Power
Full On	Enabled	No	Enabled	Enabled	On
Active	Enabled/ Disabled	Yes	Enabled	Enabled	On
Sleep	Enabled	—	Disabled	Enabled	On
Deep Sleep	Disabled	—	Disabled	Disabled	On
Hibernate	Disabled	—	Disabled	Disabled	Off

Full-On Operating Mode—Maximum Performance

In the full-on mode, the PLL is enabled and is not bypassed, providing capability for maximum operational frequency. This is the power-up default execution state in which maximum performance can be achieved. The processor core and all enabled peripherals run at full speed.

Active Operating Mode—Moderate Power Savings

In the active mode, the PLL is enabled but bypassed. Because the PLL is bypassed, the processor's core clock (CCLK) and system clock (SCLK) run at the input clock (CLKIN) frequency. In this mode, the CLKIN to CCLK multiplier ratio can be changed, although the changes are not realized until the full-on mode is entered. DMA access is available to appropriately configured L1 memories.

ADDITIONAL INFORMATION

The following publications that describe ADSP-BF512/ ADSP-BF514/ADSP-BF516/ADSP-BF518 processors (and related processors) can be accessed electronically on our website:

- *Getting Started With Blackfin Processors*
- *ADSP-BF51x Blackfin Processor Hardware Reference*
- *Blackfin Processor Programming Reference*
- *ADSP-BF512/BF514/BF514F16/BF516/BF518/BF518F16 Blackfin Processor Anomaly List*

RELATED SIGNAL CHAINS

A *signal chain* is a series of signal-conditioning electronic components that receive input (data acquired from sampling either real-time phenomena or from stored data) in tandem, with the output of one portion of the chain supplying input to the next. Signal chains are often used in signal processing applications to gather and process data or to apply system controls based on analysis of real-time phenomena. For more information about this term and related topics, see the "signal chain" entry in Wikipedia or the Glossary of EE Terms on the Analog Devices website.

Analog Devices eases signal processing system development by providing signal processing components that are designed to work together well. A tool for viewing relationships between specific applications and related components is available on the www.analog.com website.

The Application Signal Chains page in the Circuits from the Lab™ site (http://www.analog.com/circuits) provides:

- Graphical circuit block diagram presentation of signal chains for a variety of circuit types and applications
- Drill down links for components in each chain to selection guides and application information
- Reference designs applying best practice design techniques

LOCKBOX SECURE TECHNOLOGY DISCLAIMER

Analog Devices products containing Lockbox Secure Technology are warranted by Analog Devices as detailed in the Analog Devices Standard Terms and Conditions of Sale. To our knowledge, the Lockbox Secure Technology, when used in accordance with the data sheet and hardware reference manual specifications, provides a secure method of implementing code and data safeguards. However, Analog Devices does not guarantee that this technology provides absolute security. ACCORDINGLY, ANALOG DEVICES HEREBY DISCLAIMS ANY AND ALL EXPRESS AND IMPLIED WARRANTIES THAT THE LOCKBOX SECURE TECHNOLOGY CANNOT BE BREACHED, COMPROMISED, OR OTHERWISE CIRCUMVENTED AND IN NO EVENT SHALL ANALOG DEVICES BE LIABLE FOR ANY LOSS, DAMAGE, DESTRUCTION, OR RELEASE OF DATA, INFORMATION, PHYSICAL PROPERTY, OR INTELLECTUAL PROPERTY.

ELECTRICAL CHARACTERISTICS

Parameter		Test Conditions	Min	Typical	Max	Unit
V_{OH}	High Level Output Voltage	V_{DDEXT}/V_{DDMEM} = 1.7 V, I_{OH} = –0.5 mA	1.35			V
	High Level Output Voltage	V_{DDEXT}/V_{DDMEM} = 2.25 V, I_{OH} = –0.5 mA	2			V
	High Level Output Voltage	V_{DDEXT}/V_{DDMEM} = 3.0 V, I_{OH} = –0.5 mA	2.4			V
V_{OL}	Low Level Output Voltage	V_{DDEXT}/V_{DDMEM} = 1.7/2.25/3.0 V, I_{OL} = 2.0 mA			0.4	V
I_{IH}[1]	High Level Input Current	V_{DDEXT}/V_{DDMEM} = 3.6 V, V_{IN} = 3.6 V			10	µA
I_{IL}[1]	Low Level Input Current	V_{DDEXT}/V_{DDMEM} = 3.6 V, V_{IN} = 0 V			10	µA
I_{IHP}[2]	High Level Input Current JTAG	V_{DDEXT} = 3.6 V, V_{IN} = 3.6 V			75	µA
I_{OZH}[3]	Three-State Leakage Current	V_{DDEXT}/V_{DDMEM} = 3.6 V, V_{IN} = 3.6 V			10	µA
I_{OZHTWI}[4]	Three-State Leakage Current	V_{DDEXT} = 3.0 V, V_{IN} = 5.5 V			10	µA
I_{OZL}[3]	Three-State Leakage Current	V_{DDEXT}/V_{DDMEM} = 3.6 V, V_{IN} = 0 V			10	µA
C_{IN}[5, 6]	Input Capacitance	f_{IN} = 1 MHz, $T_{AMBIENT}$ = 25°C, V_{IN} = 2.5 V		5	8	pF
C_{INTWI}[4, 6]	Input Capacitance	f_{IN} = 1 MHz, $T_{AMBIENT}$ = 25°C, V_{IN} = 2.5 V			15	pF
$I_{DDDEEPSLEEP}$[7]	V_{DDINT} Current in Deep Sleep Mode	V_{DDINT} = 1.3 V, f_{CCLK} = 0 MHz, f_{SCLK} = 0 MHz, T_J = 25°C, ASF = 0.00		2.1		mA
$I_{DDSLEEP}$	V_{DDINT} Current in Sleep Mode	V_{DDINT} = 1.3 V, f_{SCLK} = 25 MHz, T_J = 25°C		5.5		mA
$I_{DD-IDLE}$	V_{DDINT} Current in Idle	V_{DDINT} = 1.3 V, f_{CCLK} = 50 MHz, f_{SCLK} = 25 MHz, T_J = 25°C, ASF = 0.41		12		mA
I_{DD-TYP}	V_{DDINT} Current	V_{DDINT} = 1.3 V, f_{CCLK} = 300 MHz, f_{SCLK} = 25 MHz, T_J = 25°C, ASF = 1.00		77		mA
I_{DD-TYP}	V_{DDINT} Current	V_{DDINT} = 1.4 V, f_{CCLK} = 400 MHz, f_{SCLK} = 25 MHz, T_J = 25°C, ASF = 1.00		108		mA
$I_{DDHIBERNATE}$[8]	Hibernate State Current	V_{DDEXT}=V_{DDMEM}=V_{DDRTC} = 3.3 V V_{DDOTP}=V_{PPOTP}=2.5 V, T_J = 25°C, CLKIN = 0 MHz		40		µA
I_{DDRTC}	V_{DDRTC} Current	V_{DDRTC} = 3.3 V, T_J = 25°C		20		µA
$I_{DDSLEEP}$[8, 9]	V_{DDINT} Current in Sleep Mode	f_{CCLK} = 0 MHz, f_{SCLK} > 0 MHz			Table 14 + (0.20 × V_{DDINT} × f_{SCLK})	mA[10]
$I_{DDDEEPSLEEP}$[8, 10]	V_{DDINT} Current in Deep Sleep Mode	f_{CCLK} = 0 MHz, f_{SCLK} = 0 MHz			Table 14	mA
I_{DDINT}[10, 11]	V_{DDINT} Current	f_{CCLK} > 0 MHz, f_{SCLK} ≥ 0 MHz			Table 14 + (Table 15 × ASF) + (0.20 × V_{DDINT} × f_{SCLK})	mA

Parameter		Test Conditions	Min	Typical	Max	Unit
$I_{DDFLASH1}$	Flash Memory Supply Current 1—Asynchronous Read			6	9	mA
$I_{DDFLASH2}$	Flash Memory Supply Current 2—Standby			15	25	µA
$I_{DDFLASH3}$	Flash Memory Supply Current 3—Program and Erase			20	25	mA
I_{DDOTP}	V_{DDOTP} Current	V_{DDOTP} = 2.5 V, T_J = 25°C, OTP Memory Read		2		mA
I_{DDOTP}	V_{DDOTP} Current	V_{DDOTP} = 2.5 V, T_J = 25°C, OTP Memory Write		2		mA
I_{PPOTP}	V_{PPOTP} Current	V_{PPOTP} = 2.5 V, T_J = 25°C, OTP Memory Read		100		µA
I_{PPOTP}	V_{PPOTP} Current	V_{PPOTP} = Table 20 V, T_J = 25°C, OTP Memory Write		3		mA

[1] Applies to input balls.
[2] Applies to JTAG input balls (TCK, TDI, TMS, $\overline{TRST}$).
[3] Applies to three-statable balls.
[4] Applies to bidirectional balls SCL and SDA.
[5] Applies to all signal balls, except SCL and SDA.
[6] Guaranteed, but not tested.
[7] See the *ADSP-BF51x Blackfin Processor Hardware Reference Manual* for definition of sleep, deep sleep, and hibernate operating modes.
[8] Includes current on V_{DDEXT}, V_{DDMEM}, V_{DDOTP}, and V_{PPOTP} supplies. Clock inputs are tied high or low.
[9] Guaranteed maximum specifications.
[10] Unit for V_{DDINT} is V (Volts). Unit for f_{SCLK} is MHz.
[11] See Table 13 for the list of I_{DDINT} power vectors covered.

Total Power Dissipation

Total power dissipation has two components:

1. Static, including leakage current
2. Dynamic, due to transistor switching characteristics

Many operating conditions can also affect power dissipation, including temperature, voltage, operating frequency, and processor activity. Electrical Characteristics on Page 24 shows the current dissipation for internal circuitry (V_{DDINT}). $I_{DDDEEPSLEEP}$ specifies static power dissipation as a function of voltage (V_{DDINT}) and temperature (see Table 14), and I_{DDINT} specifies the total power specification for the listed test conditions, including the dynamic component as a function of voltage (V_{DDINT}) and frequency (Table 15).

There are two parts to the dynamic component. The first part is due to transistor switching in the core clock (CCLK) domain. This part is subject to an Activity Scaling Factor (ASF) which represents application code running on the processor core and L1 memories (Table 13).

The ASF is combined with the CCLK Frequency and V_{DDINT} dependent data in Table 15 to calculate this part. The second part is due to transistor switching in the system clock (SCLK) domain, which is included in the I_{DDINT} specification equation.

Table 13. Activity Scaling Factors (ASF)[1]

I_{DDINT} Power Vector	Activity Scaling Factor (ASF)
$I_{DD-PEAK}$	1.29
$I_{DD-HIGH}$	1.25
I_{DD-TYP}	1.00
I_{DD-APP}	0.85
I_{DD-NOP}	0.70
$I_{DD-IDLE}$	0.41

[1] See *Estimating Power for ASDP-BF534/BF536/BF537 Blackfin Processors (EE-297)*. The power vector information also applies to the ADSP-BF51x processors.

Table 14. Static Current—$I_{DD-DEEPSLEEP}$ (mA)

	Voltage (V_{DDINT})[1]								
T_J (°C)[1]	1.10 V	1.15 V	1.20 V	1.25 V	1.30 V	1.35 V	1.40 V	1.45 V	1.50 V
–40	0.9	1.0	1.0	1.1	1.1	1.2	1.3	1.7	1.9
–20	1.0	1.1	1.2	1.3	1.4	1.6	1.7	1.9	2.0
0	1.2	1.3	1.4	1.6	1.8	2.0	2.2	2.3	2.5

Table 25. Power-Up Reset Timing

Parameter		Min	Max	Unit
Timing Requirements				
$t_{RST\_IN\_PWR}$	$\overline{\text{RESET}}$ Deasserted after the V_{DDINT}, V_{DDEXT}, V_{DDRTC}, V_{DDMEM}, V_{DDOTP}, and CLKIN Pins are Stable and Within Specification	3500 × t_{CKIN}		ns

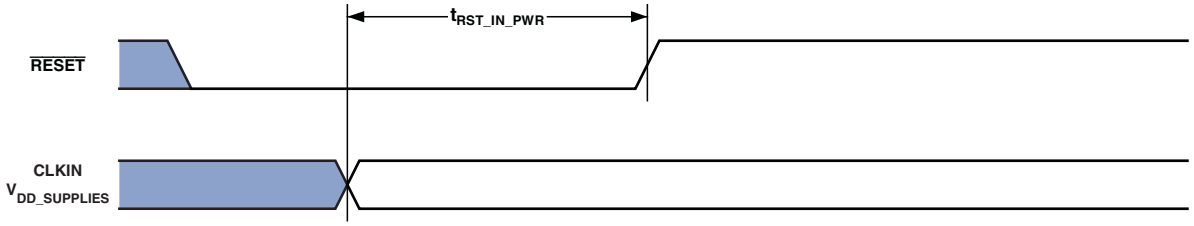


Figure 10. Power-Up Reset Timing

SDRAM Interface Timing

Table 28. SDRAM Interface Timing

Parameter		V_{DDMEM} 1.8 V Nominal Min	V_{DDMEM} 1.8 V Nominal Max	V_{DDMEM} 2.5 V/3.3 V Nominal Min	V_{DDMEM} 2.5 V/3.3 V Nominal Max	Unit
Timing Requirements						
t_{SSDAT}	Data Setup Before CLKOUT	1.5		1.5		ns
t_{HSDAT}	Data Hold After CLKOUT	1.3		0.8		ns
Switching Characteristics						
t_{SCLK}	CLKOUT Period[1]	12.5		10		ns
t_{SCLKH}	CLKOUT Width High	5		4		ns
t_{SCLKL}	CLKOUT Width Low	5		4		ns
t_{DCAD}	Command, Address, Data Delay After CLKOUT[2]		5		4	ns
t_{HCAD}	Command, Address, Data Hold After CLKOUT[2]	1		1		ns
t_{DSDAT}	Data Disable After CLKOUT		5.5		5	ns
t_{ENSDAT}	Data Enable After CLKOUT	0		0		ns

[1] The t_{SCLK} value is the inverse of the f_{SCLK} specification discussed in Table 12 on Page 23. Package type and reduced supply voltages affect the best-case value listed here.
[2] Command pins/balls include: $\overline{SRAS}$, $\overline{SCAS}$, $\overline{SWE}$, SDQM, $\overline{SMS}$, SA10, SCKE.

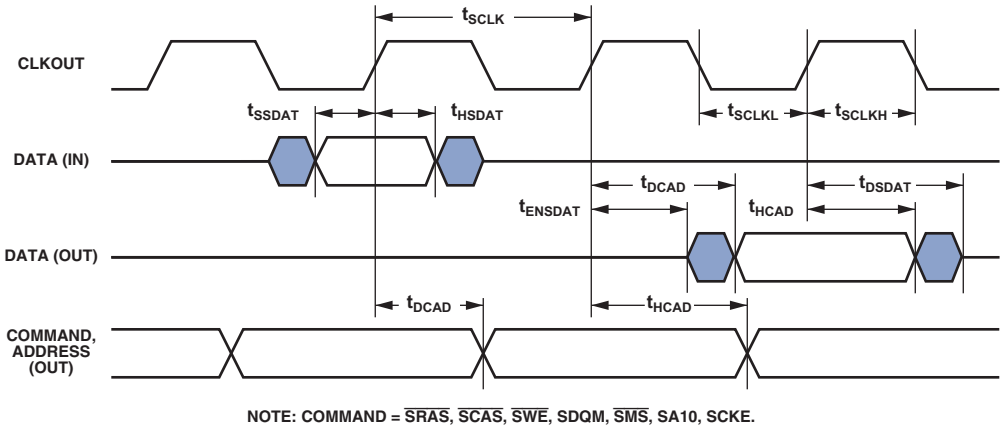


Figure 13. SDRAM Interface Timing

Serial Ports

Table 33 through Table 36 on Page 42 and Figure 22 on Page 40 through Figure 25 on Page 42 describe serial port operations.

Table 33. Serial Ports—External Clock

Parameter		V_{DDEXT} 1.8 V Nominal		V_{DDEXT} 2.5 V/3.3 V Nominal		Unit
		Min	Max	Min	Max	
Timing Requirements						
t_{SFSE}[1]	TFSx/RFSx Setup Before TSCLKx/RSCLKx	3		3		ns
t_{HFSE}[1]	TFSx/RFSx Hold After TSCLKx/RSCLKx	3		3		ns
t_{SDRE}[1]	Receive Data Setup Before RSCLKx	3		3		ns
t_{HDRE}[1]	Receive Data Hold After RSCLKx	3.5		3		ns
t_{SCLKEW}	TSCLKx/RSCLKx Width	7		4.5		ns
t_{SCLKE}	TSCLKx/RSCLKx Period	$2 \times t_{SCLK}$		$2 \times t_{SCLK}$		ns
t_{SUDTE}[2]	Start-Up Delay From SPORT Enable To First External TFSx	$4 \times t_{SCLKE}$		$4 \times t_{SCLKE}$		ns
t_{SUDRE}[2]	Start-Up Delay From SPORT Enable To First External RFSx	$4 \times t_{SCLKE}$		$4 \times t_{SCLKE}$		ns
Switching Characteristics						
t_{DFSE}[3]	TFSx/RFSx Delay After TSCLKx/RSCLKx (Internally Generated TFSx/RFSx)		10		10	ns
t_{HOFSE}[3]	TFSx/RFSx Hold After TSCLKx/RSCLKx (Internally Generated TFSx/RFSx)	0		0		ns
t_{DDTE}[3]	Transmit Data Delay After TSCLKx		10		10	ns
t_{HDTE}[3]	Transmit Data Hold After TSCLKx	0		0		ns

[1] Referenced to sample edge.
[2] Verified in design but untested.
[3] Referenced to drive edge.

Table 34. Serial Ports—Internal Clock

Parameter		V_{DDEXT} 1.8 V Nominal		V_{DDEXT} 2.5 V/3.3 V Nominal		Unit
		Min	Max	Min	Max	
Timing Requirements						
t_{SFSI}[1]	TFSx/RFSx Setup Before TSCLKx/RSCLKx	11		9.6		ns
t_{HFSI}[1]	TFSx/RFSx Hold After TSCLKx/RSCLKx	–1.5		–1.5		ns
t_{SDRI}[1]	Receive Data Setup Before RSCLKx	11		9.6		ns
t_{HDRI}[1]	Receive Data Hold After RSCLKx	–1.5		–1.5		ns
Switching Characteristics						
t_{DFSI}[2]	TFSx/RFSx Delay After TSCLKx/RSCLKx (Internally Generated TFSx/RFSx)		3		3	ns
t_{HOFSI}[2]	TFSx/RFSx Hold After TSCLKx/RSCLKx (Internally Generated TFSx/RFSx)	–2		–1		ns
t_{DDTI}[2]	Transmit Data Delay After TSCLKx		3		3	ns
t_{HDTI}[2]	Transmit Data Hold After TSCLKx	–1.8		–1.5		ns
t_{SCLKIW}	TSCLKx/RSCLKx Width	10		8		ns

[1] Referenced to sample edge.
[2] Referenced to drive edge.

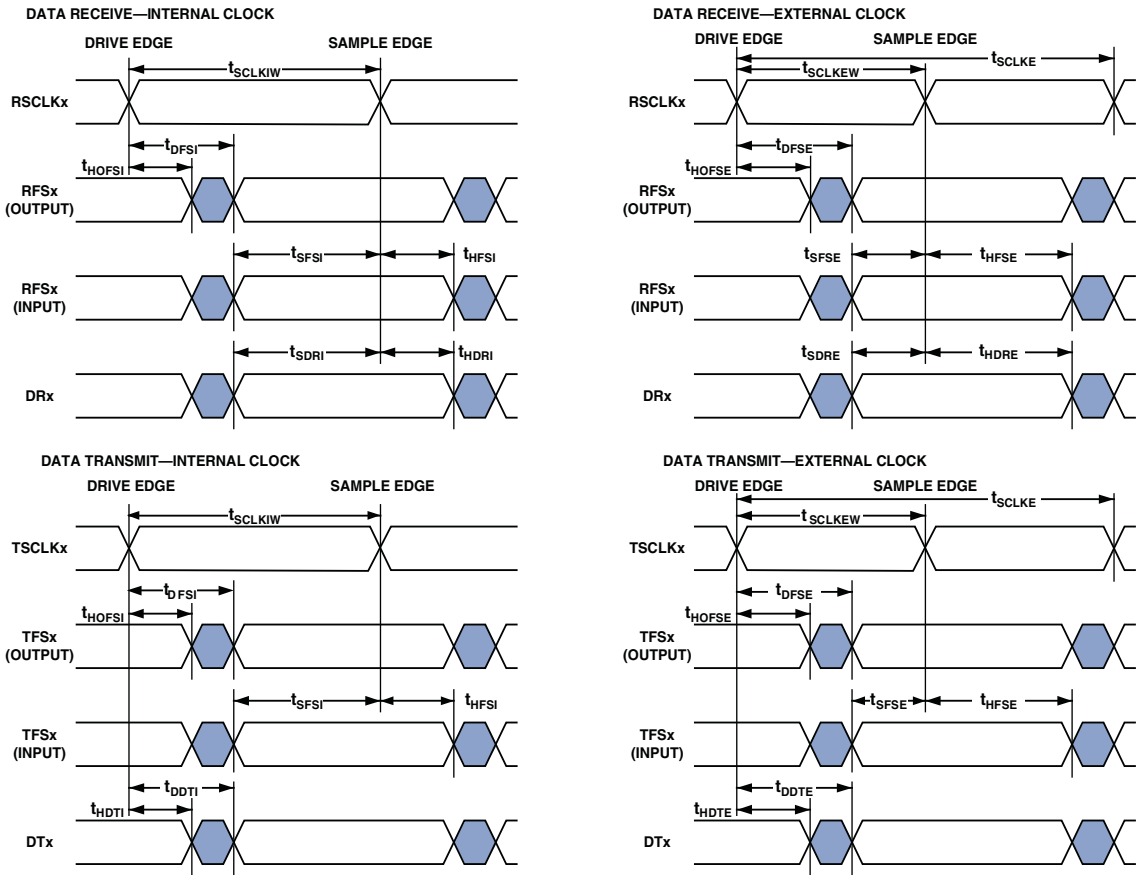


Figure 22. Serial Ports

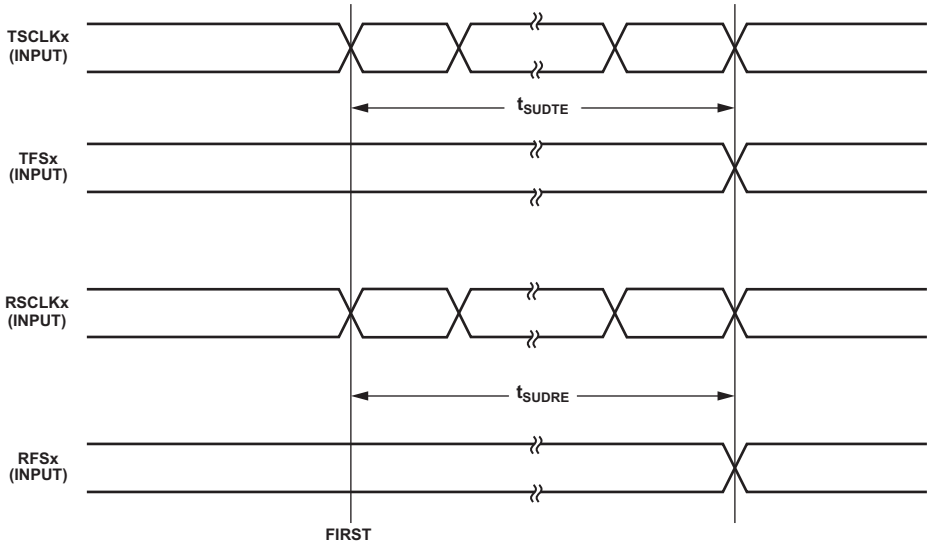


Figure 23. Serial Port Start Up with External Clock and Frame Sync

Serial Peripheral Interface (SPI) Port—Master Timing

Table 37 and Figure 26 describe SPI port master operations.

Table 37. Serial Peripheral Interface (SPI) Port—Master Timing

Parameter		V_{DDEXT} 1.8 V Nominal		V_{DDEXT} 2.5 V/3.3 V Nominal		Unit
		Min	Max	Min	Max	
Timing Requirements						
t_{SSPIDM}	Data Input Valid to SCK Edge (Data Input Setup)	11.6		9.6		ns
t_{HSPIDM}	SCK Sampling Edge to Data Input Invalid	–1.5		–1.5		ns
Switching Characteristics						
t_{SDSCIM}	$\overline{SPISELx}$ low to First SCK Edge	$2 \times t_{SCLK} - 1.5$		$2 \times t_{SCLK} - 1.5$		ns
t_{SPICHM}	Serial Clock High Period	$2 \times t_{SCLK} - 1.5$		$2 \times t_{SCLK} - 1.5$		ns
t_{SPICLM}	Serial Clock Low Period	$2 \times t_{SCLK} - 1.5$		$2 \times t_{SCLK} - 1.5$		ns
t_{SPICLK}	Serial Clock Period	$4 \times t_{SCLK}$		$4 \times t_{SCLK}$		ns
t_{HDSM}	Last SCK Edge to $\overline{SPISELx}$ High	$2 \times t_{SCLK} - 1.5$		$2 \times t_{SCLK} - 1.5$		ns
t_{SPITDM}	Sequential Transfer Delay	$2 \times t_{SCLK} - 1.5$		$2 \times t_{SCLK} - 1.5$		ns
$t_{DDSPIDM}$	SCK Edge to Data Out Valid (Data Out Delay)		6		6	ns
$t_{HDSPIDM}$	SCK Edge to Data Out Invalid (Data Out Hold)	–1		–1		ns

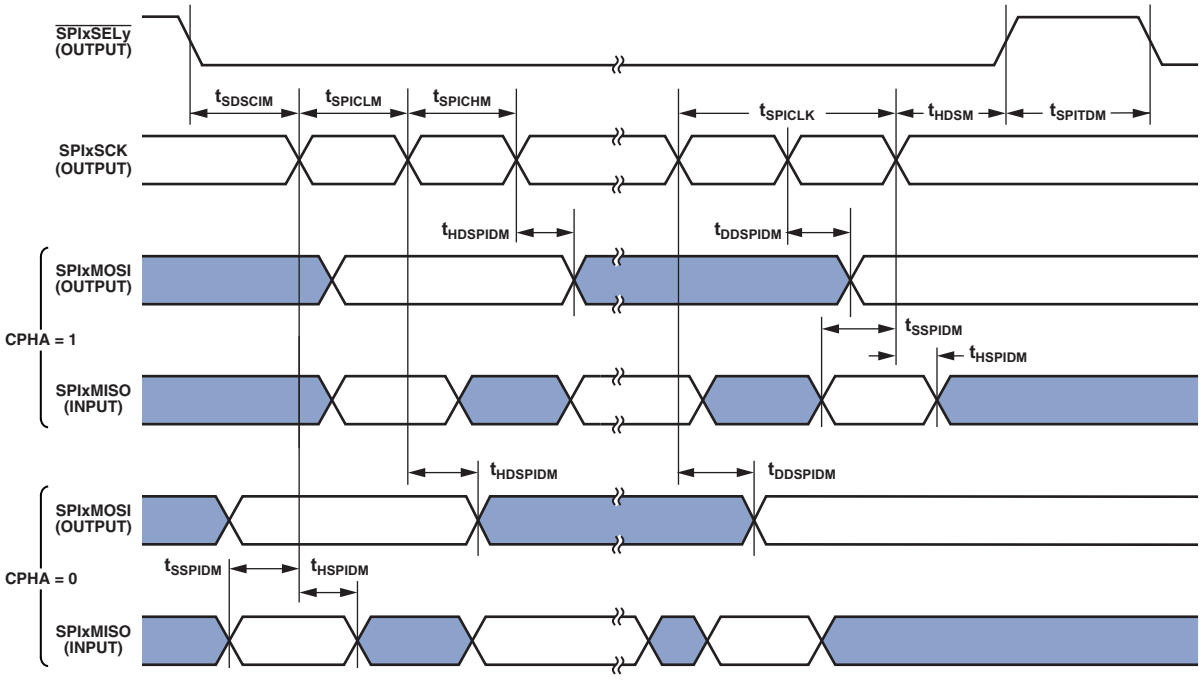


Figure 26. Serial Peripheral Interface (SPI) Port—Master Timing

Timer Cycle Timing

Table 41 and Figure 30 describe timer expired operations. The input signal is asynchronous in "width capture mode" and "external clock mode" and has an absolute maximum input frequency of (f_{SCLK}/2) MHz.

Table 41. Timer Cycle Timing

		V_{DDEXT} 1.8 V Nominal		V_{DDEXT} 2.5 V/3.3 V Nominal		
Parameter		**Min**	**Max**	**Min**	**Max**	**Unit**
Timing Characteristics						
t_{WL}[1]	Timer Pulse Width Input Low (Measured In SCLK Cycles)	t_{SCLK}		t_{SCLK}		ns
t_{WH}[1]	Timer Pulse Width Input High (Measured In SCLK Cycles)	t_{SCLK}		t_{SCLK}		ns
t_{TIS}[2]	Timer Input Setup Time Before CLKOUT Low	10		7		ns
t_{TIH}[2]	Timer Input Hold Time After CLKOUT Low	–2		–2		ns
Switching Characteristics						
t_{HTO}	Timer Pulse Width Output (Measured In SCLK Cycles)	t_{SCLK} – 1.5	$(2^{32}–1)t_{SCLK}$	t_{SCLK} – 1	$(2^{32}–1)t_{SCLK}$	ns
t_{TOD}	Timer Output Update Delay After CLKOUT High		6		6	ns

[1] The minimum pulse widths apply for TMRx signals in width capture and external clock modes. They also apply to the PF15 or PPI_CLK signals in PWM output mode.
[2] Either a valid setup and hold time or a valid pulse width is sufficient. There is no need to resynchronize programmable flag inputs.

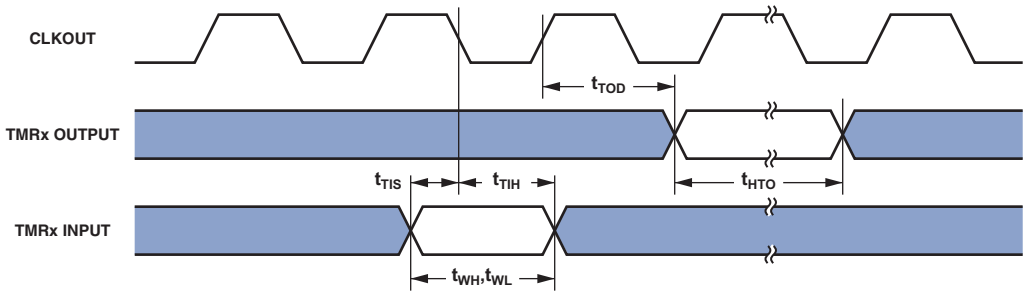


Figure 30. Timer Cycle Timing

JTAG Test And Emulation Port Timing

Table 49 and Figure 38 describe JTAG port operations.

Table 49. JTAG Port Timing

Parameter		Min	Max	Unit
Timing Requirements				
t_{TCK}	TCK Period	20		ns
t_{STAP}	TDI, TMS Setup Before TCK High	4		ns
t_{HTAP}	TDI, TMS Hold After TCK High	4		ns
t_{SSYS}[1]	System Inputs Setup Before TCK High	4		ns
t_{HSYS}[1]	System Inputs Hold After TCK High	5		ns
t_{TRSTW}	$\overline{TRST}$ Pulse Width[2] (measured in TCK cycles)	4		TCK
Switching Characteristics				
t_{DTDO}	TDO Delay from TCK Low		10	ns
t_{DSYS}[3]	System Outputs Delay After TCK Low	0	13	ns

[1] System Inputs = DATA15–0, SCL, SDA, TFS0, TSCLK0, RSCLK0, RFS0, DR0PRI, DR0SEC, PF15–0, PG15–0, PH7–0, MDIO, TD1, TMS, $\overline{RESET}$, $\overline{NMI}$, BMODE2–0.
[2] 50 MHz Maximum.
[3] System Outputs = DATA15–0, ADDR19–1, $\overline{ABE1–0}$, $\overline{ARE}$, $\overline{AWE}$, $\overline{AMS1–0}$, $\overline{SRAS}$, $\overline{SCAS}$, $\overline{SWE}$, SCKE, CLKOUT, SA10, $\overline{SMS}$, SCL, SDA, TSCLK0, TFS0, RFS0, RSCLK0, DT0PRI, DT0SEC, PF15–0, PG15–0, PH7–0, MDC, MDIO.

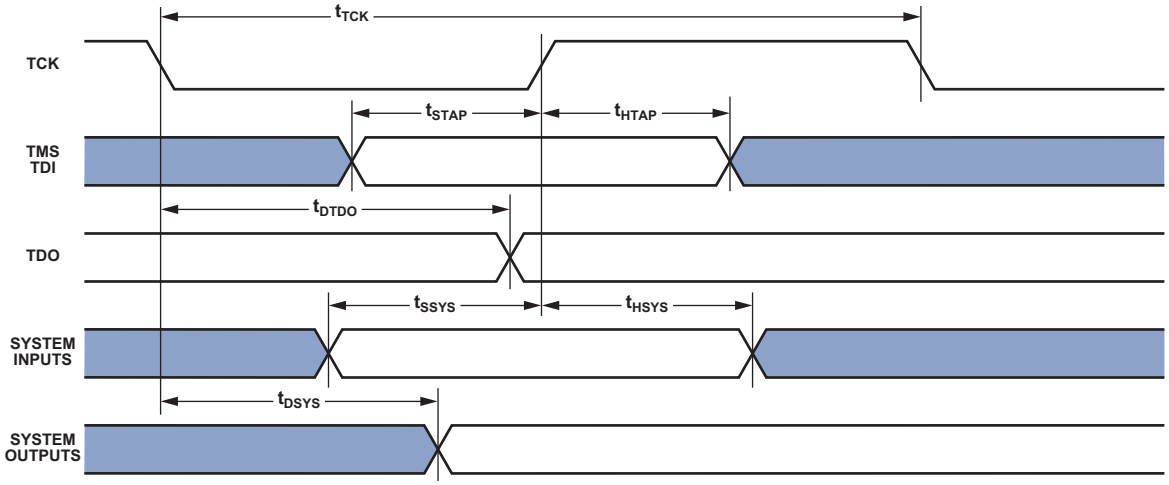


Figure 38. JTAG Port Timing

Output Disable Time Measurement

Output signals are considered to be disabled when they stop driving, go into a high impedance state, and start to decay from their output high or low voltage. The output disable time t_{DIS} is the difference between $t_{DIS\_MEASURED}$ and t_{DECAY} as shown on the left side of Figure 55.

$$t_{DIS} = t_{DIS\_MEASURED} - t_{DECAY}$$

The time for the voltage on the bus to decay by ΔV is dependent on the capacitive load C_L and the load current I_L. This decay time can be approximated by the equation:

$$t_{DECAY} = (C_L \Delta V)/I_L$$

The time t_{DECAY} is calculated with test loads C_L and I_L and with ΔV equal to 0.25 V for V_{DDEXT}/V_{DDMEM} (nominal) = 2.5 V/3.3 V and 0.15 V for V_{DDEXT}/V_{VDDMEM} (nominal) = 1.8 V.

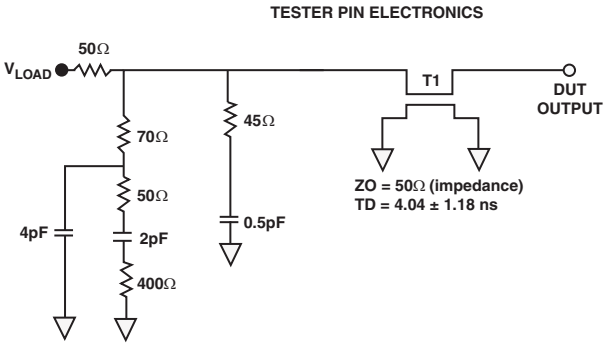
The time $t_{DIS\_MEASURED}$ is the interval from when the reference signal switches to when the output voltage decays ΔV from the measured output high or output low voltage.

Example System Hold Time Calculation

To determine the data output hold time in a particular system, first calculate t_{DECAY} using the equation given above. Choose ΔV to be the difference between the ADSP-BF51x processor's output voltage and the input threshold for the device requiring the hold time. C_L is the total bus capacitance (per data line), and I_L is the total leakage or three-state current (per data line). The hold time is t_{DECAY} plus the various output disable times as specified in the Timing Specifications on Page 29 (for example t_{DSDAT} for an SDRAM write cycle as shown in SDRAM Interface Timing on Page 33).

Capacitive Loading

Output delays and holds are based on standard capacitive loads of an average of 6 pF on all balls (see Figure 56). V_{LOAD} is equal to $(V_{DDEXT}/V_{DDMEM})/2$. The graphs of Figure 57 through Figure 68 show how output rise time varies with capacitance. The delay and hold specifications given should be derated by a factor derived from these figures. The graphs in these figures may not be linear outside the ranges shown.



NOTES:
THE WORST CASE TRANSMISSION LINE DELAY IS SHOWN AND CAN BE USED FOR THE OUTPUT TIMING ANALYSIS TO REFLECT THE TRANSMISSION LINE EFFECT AND MUST BE CONSIDERED. THE TRANSMISSION LINE (TD) IS FOR LOAD ONLY AND DOES NOT AFFECT THE DATA SHEET TIMING SPECIFICATIONS.

ANALOG DEVICES RECOMMENDS USING THE IBIS MODEL TIMING FOR A GIVEN SYSTEM REQUIREMENT. IF NECESSARY, A SYSTEM MAY INCORPORATE EXTERNAL DRIVERS TO COMPENSATE FOR ANY TIMING DIFFERENCES.

Figure 56. Equivalent Device Loading for AC Measurements (Includes All Fixtures)

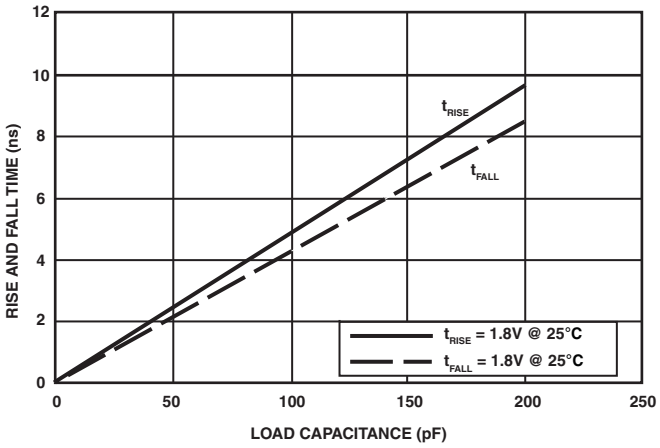


Figure 57. Driver Type A Typical Rise and Fall Times (10%–90%) vs. Load Capacitance (1.8V V_{DDEXT}/V_{DDMEM})

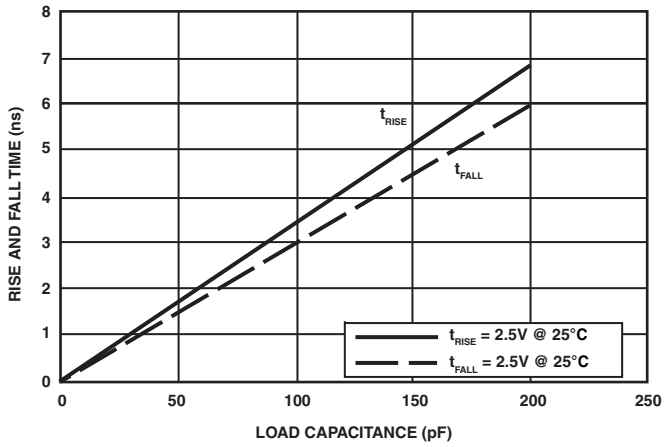


Figure 58. Driver Type A Typical Rise and Fall Times (10%–90%) vs. Load Capacitance (2.5V V_{DDEXT}/V_{DDMEM})

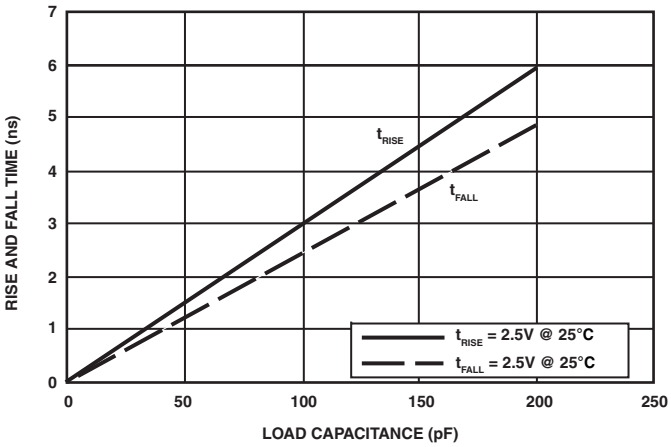


Figure 61. Driver Type B Typical Rise and Fall Times (10%–90%) vs. Load Capacitance (2.5V V_{DDEXT}/V_{DDMEM})

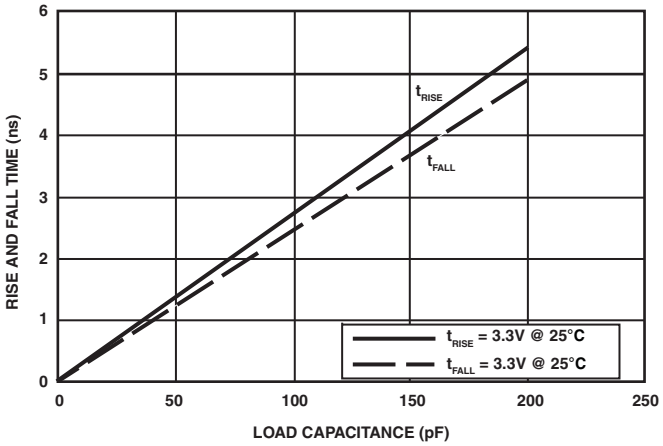


Figure 59. Driver Type A Typical Rise and Fall Times (10%–90%) vs. Load Capacitance (3.3V V_{DDEXT}/V_{DDMEM})

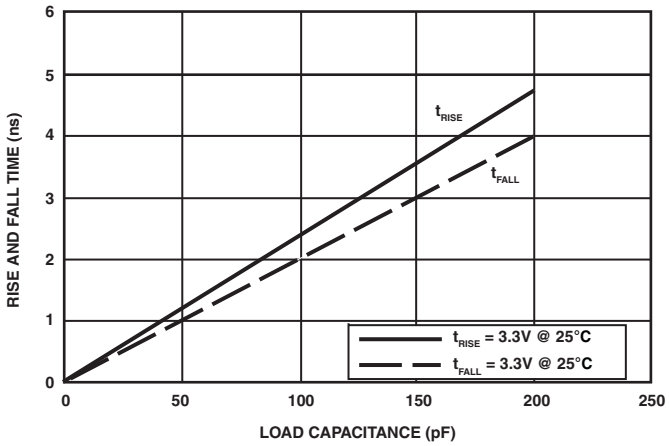


Figure 62. Driver Type B Typical Rise and Fall Times (10%–90%) vs. Load Capacitance (3.3V V_{DDEXT}/V_{DDMEM})

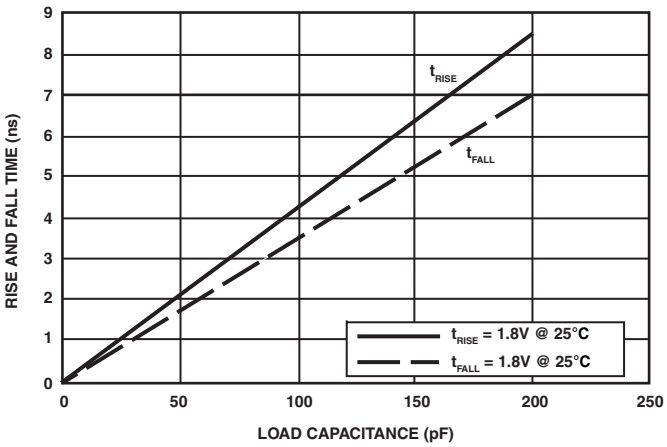


Figure 60. Driver Type B Typical Rise and Fall Times (10%–90%) vs. Load Capacitance (1.8V V_{DDEXT}/V_{DDMEM})

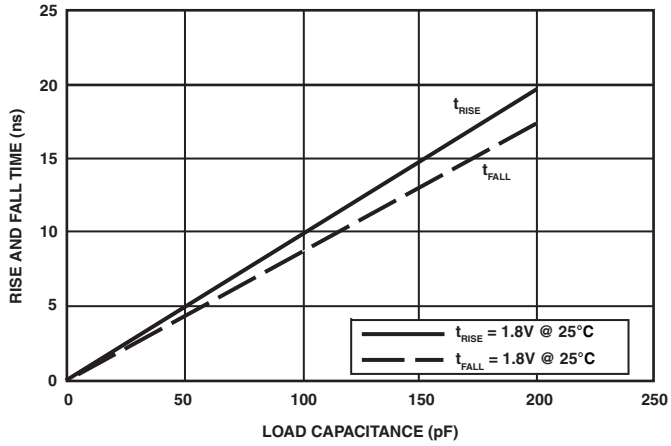


Figure 63. Driver Type C Typical Rise and Fall Times (10%–90%) vs. Load Capacitance (1.8V V_{DDEXT}/V_{DDMEM})

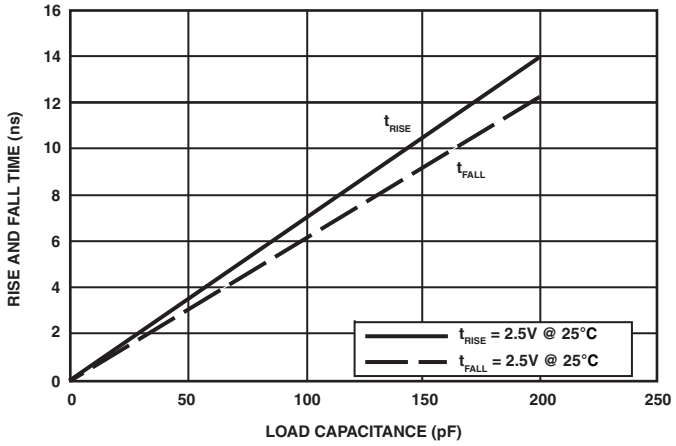


Figure 64. Driver Type C Typical Rise and Fall Times (10%–90%) vs. Load Capacitance (2.5V V_{DDEXT}/V_{DDMEM})

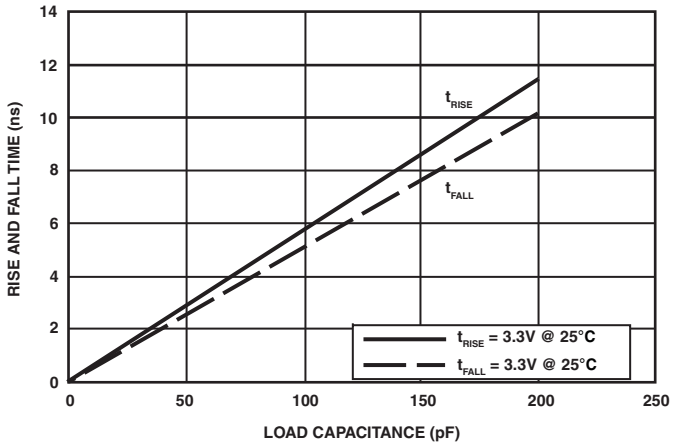


Figure 65. Driver Type C Typical Rise and Fall Times (10%–90%) vs. Load Capacitance (3.3V V_{DDEXT}/V_{DDMEM})

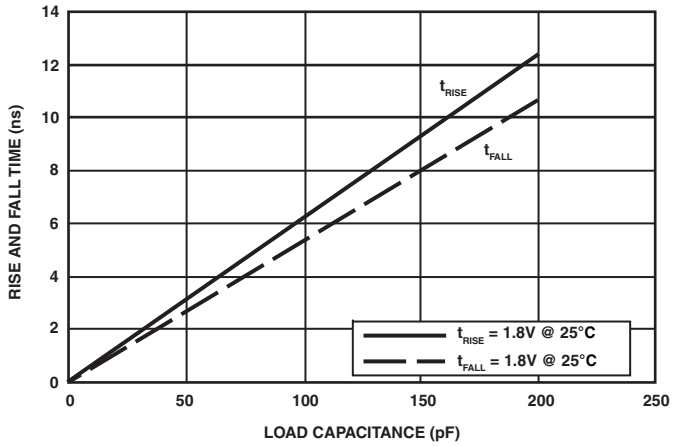


Figure 66. Driver Type D Typical Rise and Fall Times (10%–90%) vs. Load Capacitance (1.8V V_{DDEXT}/V_{DDMEM})

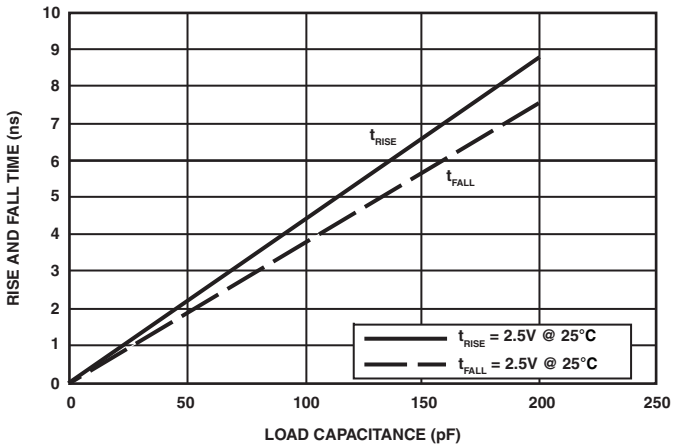


Figure 67. Driver Type D Typical Rise and Fall Times (10%–90%) vs. Load Capacitance (2.5V V_{DDEXT}/V_{DDMEM})

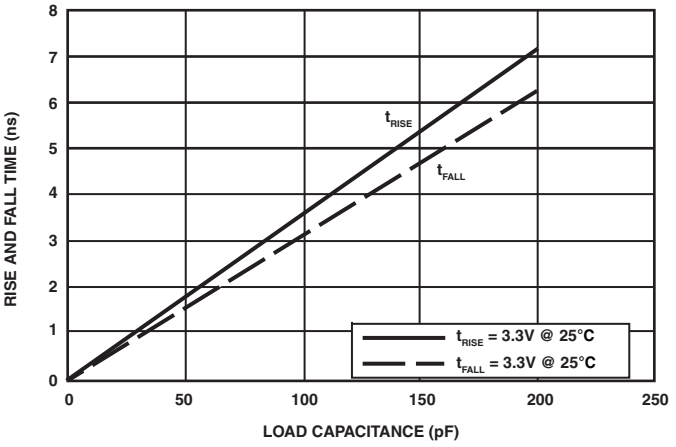


Figure 68. Driver Type D Typical Rise and Fall Times (10%–90%) vs. Load Capacitance (3.3V V_{DDEXT}/V_{DDMEM})

176-LEAD LQFP_EP LEAD ASSIGNMENT

Table 52 lists the LQFP_EP leads by lead number. Table 53 on Page 60 lists the LQFP_EP by signal mnemonic.

Table 52. 176-Lead LQFP_EP Pin Assignment (Numerical by Lead Number)

Lead No.	Signal	Lead No.	Signal	Lead No.	Signal	Lead No.	Signal
1	GND	45	GND	89	GND	133	GND
2	GND	46	GND	90	GND	134	GND
3	PF9	47	PG1	91	A12	135	$\overline{PG}$
4	PF8	48	PG0	92	A11	136	V_{DDEXT}
5	PF7	49	V_{DDEXT}	93	A10	137	GND
6	PF6	50	TDO	94	A9	138	V_{DDINT}
7	V_{DDEXT}	51	$\overline{EMU}$	95	V_{DDMEM}	139	GND
8	V_{PPOTP}	52	TDI	96	A8	140	RTXO
9	V_{DDOTP}	53	TCK	97	A7	141	RTXI
10	PF5	54	$\overline{TRST}$	98	V_{DDINT}	142	V_{DDRTC}
11	PF4	55	TMS	99	GND	143	CLKIN
12	PF3	56	D15	100	V_{DDINT}	144	XTAL
13	PF2	57	D14	101	A6	145	V_{DDEXT}
14	V_{DDINT}	58	D13	102	A5	146	$\overline{RESET}$
15	GND	59	V_{DDMEM}	103	A4	147	$\overline{NMI}$
16	$V_{DDFLASH}$	60	D12	104	V_{DDMEM}	148	V_{DDEXT}
17	$V_{DDFLASH}$	61	D11	105	A3	149	GND
18	PF1	62	D10	106	A2	150	CLKBUF
19	PF0	63	V_{DDINT}	107	A1	151	GND
20	PG15	64	D9	108	$\overline{ABE}$1	152	V_{DDINT}
21	PG14	65	D8	109	$\overline{ABE}$0	153	PH7
22	GND	66	D7	110	SA10	154	PH6
23	V_{DDINT}	67	GND	111	GND	155	PH5
24	V_{DDEXT}	68	V_{DDMEM}	112	V_{DDMEM}	156	PH4
25	PG13	69	D6	113	$\overline{SWE}$	157	GND
26	PG12	70	D5	114	$\overline{SCAS}$	158	V_{DDEXT}
27	PG11	71	D4	115	$\overline{SRAS}$	159	PH3
28	PG10	72	D3	116	V_{DDINT}	160	PH2
29	$V_{DDFLASH}$	73	D2	117	GND	161	PH1
30	V_{DDINT}	74	D1	118	$\overline{SMS}$	162	PH0
31	PG9	75	V_{DDMEM}	119	SCKE	163	GND
32	PG8	76	D0	120	$\overline{AMS}$1	164	V_{DDINT}
33	PG7	77	A19	121	$\overline{ARE}$	165	PF15
34	PG6	78	A18	122	$\overline{AWE}$	166	PF14
35	V_{DDEXT}	79	V_{DDINT}	123	$\overline{AMS}$0	167	PF13
36	PG5	80	A17	124	V_{DDMEM}	168	PF12
37	PG4	81	A16	125	CLKOUT	169	GND
38	PG3	82	V_{DDMEM}	126	$V_{DDFLASH}$	170	V_{DDEXT}
39	PG2	83	GND	127	NC[1]	171	PF11
40	BMODE2	84	A15	128	V_{DDEXT}	172	SDA
41	BMODE1	85	A14	129	V_{DDEXT}	173	SCL
42	BMODE0	86	A13	130	EXT_WAKE	174	PF10
43	GND	87	GND	131	GND	175	GND
44	GND	88	GND	132	GND	176	GND
						GND	177*

* Pin no. 177 is the GND supply (see Figure 70) for the processor; this pad must be **robustly** connected to GND.

[1] This pin must not be connected.

Table 53. 176-Lead LQFP_EP Pin Assignment (Alphabetical by Signal Mnemonic)

Lead No.	Signal	Lead No.	Signal	Lead No.	Signal	Lead No.	Signal
107	A1	58	D13	5	PF7	113	$\overline{SWE}$
106	A2	57	D14	4	PF8	53	TCK
105	A3	56	D15	3	PF9	52	TDI
103	A4	51	$\overline{EMU}$	174	PF10	50	TDO
102	A5	130	EXT_WAKE	171	PF11	55	TMS
101	A6	1	GND	168	PF12	54	$\overline{TRST}$
97	A7	2	GND	167	PF13	7	V_{DDEXT}
96	A8	15	GND	166	PF14	24	V_{DDEXT}
94	A9	22	GND	165	PF15	35	V_{DDEXT}
93	A10	43	GND	135	$\overline{PG}$	49	V_{DDEXT}
92	A11	44	GND	48	PG0	128	V_{DDEXT}
91	A12	45	GND	47	PG1	129	V_{DDEXT}
86	A13	46	GND	39	PG2	136	V_{DDEXT}
85	A14	67	GND	38	PG3	145	V_{DDEXT}
84	A15	83	GND	37	PG4	148	V_{DDEXT}
81	A16	87	GND	36	PG5	158	V_{DDEXT}
80	A17	88	GND	34	PG6	170	V_{DDEXT}
78	A18	89	GND	33	PG7	16	$V_{DDFLASH}$
77	A19	90	GND	32	PG8	17	$V_{DDFLASH}$
109	$\overline{ABE}$0	99	GND	31	PG9	29	$V_{DDFLASH}$
108	$\overline{ABE}$1	111	GND	28	PG10	126	$V_{DDFLASH}$
123	$\overline{AMS}$0	131	GND	27	PG11	14	V_{DDINT}
120	$\overline{AMS}$1	132	GND	26	PG12	23	V_{DDINT}
121	$\overline{ARE}$	133	GND	25	PG13	30	V_{DDINT}
122	$\overline{AWE}$	134	GND	21	PG14	63	V_{DDINT}
42	BMODE0	137	GND	20	PG15	79	V_{DDINT}
41	BMODE1	139	GND	162	PH0	98	V_{DDINT}
40	BMODE2	149	GND	161	PH1	100	V_{DDINT}
150	CLKBUF	151	GND	160	PH2	116	V_{DDINT}
143	CLKIN	157	GND	159	PH3	138	V_{DDINT}
125	CLKOUT	163	GND	156	PH4	152	V_{DDINT}
76	D0	169	GND	155	PH5	164	V_{DDINT}
74	D1	175	GND	154	PH6	59	V_{DDMEM}
73	D2	176	GND	153	PH7	68	V_{DDMEM}
72	D3	117	GND	146	$\overline{RESET}$	75	V_{DDMEM}
71	D4	127	NC[1]	141	RTXI	82	V_{DDMEM}
70	D5	147	$\overline{NMI}$	140	RTXO	95	V_{DDMEM}
69	D6	19	PF0	110	SA10	104	V_{DDMEM}
66	D7	18	PF1	114	$\overline{SCAS}$	112	V_{DDMEM}
65	D8	13	PF2	119	SCKE	124	V_{DDMEM}
64	D9	12	PF3	173	SCL	9	V_{DDOTP}
62	D10	11	PF4	172	SDA	142	V_{DDRTC}
61	D11	10	PF5	118	$\overline{SMS}$	8	V_{PPOTP}
60	D12	6	PF6	115	$\overline{SRAS}$	144	XTAL
						GND	177*

* Pin no. 177 is the GND supply (see Figure 70) for the processor; this pad must be **robustly** connected to GND.

[1] This pin must not be connected.

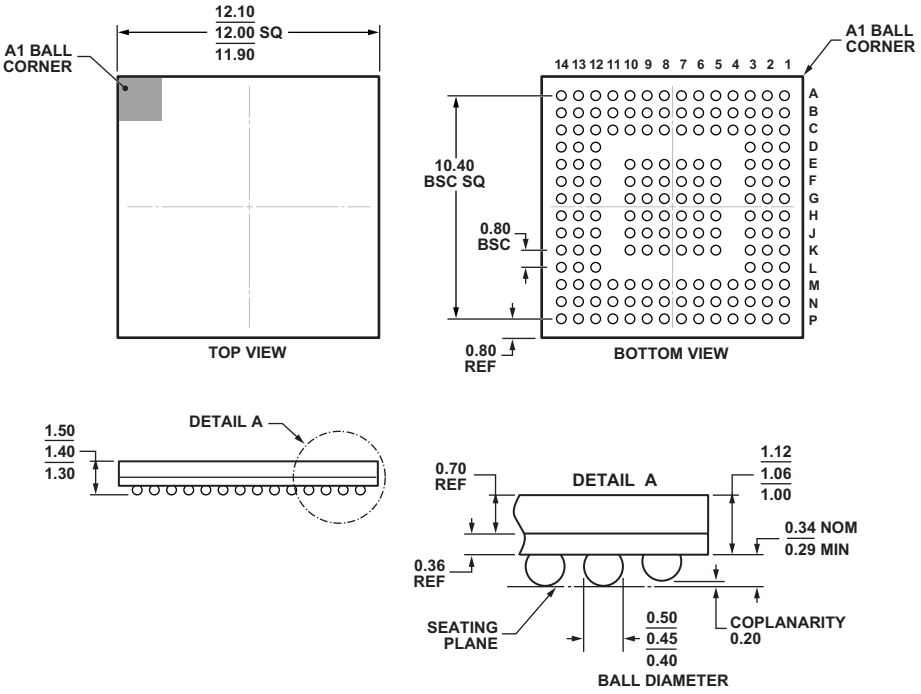


Figure 74. 168-Ball Chip Scale Package Ball Grid Array [CSP_BGA]
(BC-168-1)
Dimensions shown in millimeters

SURFACE-MOUNT DESIGN

Table 56 is provided as an aid to PCB design. For industry standard design recommendations, refer to IPC-7351, *Generic Requirements for Surface Mount Design and Land Pattern Standard.*

Table 56. BGA Data for Use with Surface-Mount Design

Package	Package Ball Attach Type	Package Solder Mask Opening	Package Ball Pad Size
168-Ball CSP_BGA	Solder Mask Defined	0.35 mm diameter	0.48 mm diameter