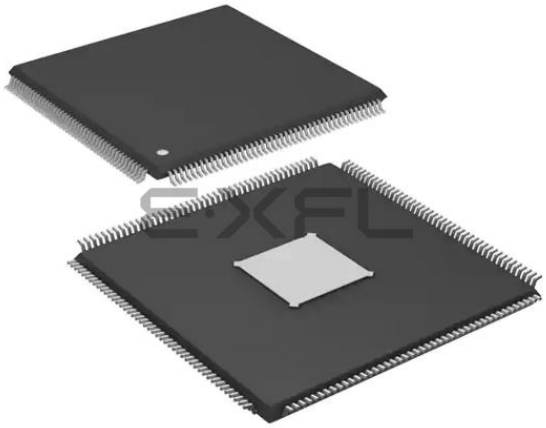

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Obsolete
Type	Fixed Point
Interface	I²C, PPI, RSI, SPI, SPORT, UART/USART
Clock Rate	400MHz
Non-Volatile Memory	FLASH (16Mbit)
On-Chip RAM	116kB
Voltage - I/O	1.8V, 2.5V, 3.3V
Voltage - Core	1.30V
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP Exposed Pad
Supplier Device Package	176-LQFP-EP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-bf514bswz4f16

GENERAL DESCRIPTION

The ADSP-BF512/ADSP-BF514/ADSP-BF514F16/ADSP-BF516/ADSP-BF518/ADSP-BF518F16 processors are members of the Blackfin® family of products, incorporating the Analog Devices/Intel Micro Signal Architecture (MSA). Blackfin processors combine a dual-MAC state-of-the-art signal processing engine, the advantages of a clean, orthogonal RISC-like microprocessor instruction set, and single-instruction, multiple-data (SIMD) multimedia capabilities into a single instruction-set architecture.

The processors are completely code compatible with other Blackfin processors.

Table 1. Processor Comparison

Feature		ADSP-BF512	ADSP-BF514	ADSP-BF514F16	ADSP-BF516	ADSP-BF518	ADSP-BF518F16
IEEE-1588		–	–	–	–	1	1
Ethernet MAC		–	–	–	1	1	1
RSI		–	1	1	1	1	1
TWI		1	1	1	1	1	1
SPORTs		2	2	2	2	2	2
UARTs		2	2	2	2	2	2
SPIs		2	2	2	2	2	2
GP Timers		8	8	8	8	8	8
Watchdog Timers		1	1	1	1	1	1
RTC		1	1	1	1	1	1
PPI		1	1	1	1	1	1
Flash (M bit)		–	–	16	–	–	16
Rotary Counter		1	1	1	1	1	1
3-Phase PWM Pairs		3	3	3	3	3	3
GPIOs		40	40	40	40	40	40
Memory (bytes)	L1 Instruction SRAM	32K					
	L1 Instruction SRAM/Cache	16K					
	L1 Data SRAM	32K					
	L1 Data SRAM/Cache	32K					
	L1 Scratchpad	4K					
	L3 Boot ROM	32K					
Maximum Speed Grade		400 MHz					
Package Options		176-Lead LQFP_EP (with Exposed Pad) 168-Ball CSP_BGA					

By integrating a rich set of industry-leading system peripherals and memory, Blackfin processors are the platform of choice for next-generation applications that require RISC-like programmability, multimedia support, and leading-edge signal processing in one integrated package.

PORTABLE LOW POWER ARCHITECTURE

Blackfin processors provide world-class power management and performance. They are produced with a low power and low voltage design methodology and feature on-chip dynamic power management, which is the ability to vary both the voltage and frequency of operation to significantly lower overall power consumption. This capability can result in a substantial reduction in power consumption, compared with just varying the frequency of operation. This allows longer battery life for portable appliances.

SYSTEM INTEGRATION

The ADSP-BF51x processors are highly integrated system-on-a-chip solutions for the next generation of embedded network connected applications. By combining industry-standard interfaces with a high performance signal processing core, cost-effective applications can be developed quickly, without the need for costly external components. The system peripherals include an IEEE-compliant 802.3 10/100 Ethernet MAC with IEEE-1588 support (ADSP-BF518/ADSP-BF518F16 only), an RSI controller, a TWI controller, two UART ports, two SPI ports, two serial ports (SPORTs), nine general-purpose 32-bit timers (eight with PWM capability), 3-phase PWM for motor control, a real-time clock, a watchdog timer, and a parallel peripheral interface (PPI).

BLACKFIN PROCESSOR CORE

As shown in Figure 2, the Blackfin processor core contains two 16-bit multipliers, two 40-bit accumulators, two 40-bit ALUs, four video ALUs, and a 40-bit shifter. The computation units process 8-, 16-, or 32-bit data from the register file.

The compute register file contains eight 32-bit registers. When performing compute operations on 16-bit operand data, the register file operates as 16 independent 16-bit registers. All operands for compute operations come from the multiported register file and instruction constant fields.

Each MAC can perform a 16-bit by 16-bit multiply in each cycle, accumulating the results into the 40-bit accumulators. Signed and unsigned formats, rounding, and saturation are supported.

The ALUs perform a traditional set of arithmetic and logical operations on 16-bit or 32-bit data. In addition, many special instructions are included to accelerate various signal processing tasks. These include bit operations such as field extract and population count, modulo 2^{32} multiply, divide primitives, saturation and rounding, and sign/exponent detection. The set of video instructions include byte alignment and packing operations, 16-bit and 8-bit adds with clipping, 8-bit average operations, and 8-bit subtract/absolute value/accumulate (SAA) operations. The compare/select and vector search instructions are also provided.

The processors internally connect to the flash memory die with the SPI0SCK, SPI0SEL4 or PH8, SPI0MOSI, and SPI0MISO signals similar to an external SPI flash (for signal descriptions, see Table 2). To further provide a secure processing environment, these internally connected signals are not exposed outside of the package. For this reason, programming the ADSP-BF51xF flash memory is performed by running code on the processor and cannot be programmed from external signals. Data transfers between the SPI flash and the processor cannot be probed externally. The flash memory has the following additional features.

- Serial Interface Architecture—SPI compatible with Mode 0 and Mode 3
- Flexible Erase Capability—Uniform 4K Byte sectors and uniform 64K Byte overlay blocks
- Fast Erase and Byte-Program—Chip-erase time = 11.2 s (typical), Sector-/Block-Erase Time = 70/350 ms (typical) Byte-Program Time = 15 µS (typical)
- Software Write Protection—Write protection through block-protection bits in status register

Combinational Logic Truth Table

SEL4 or PH8	MISO_EXT, SPICLK_EXT, MOSI_EXT
0	Three-state
1	As programmed

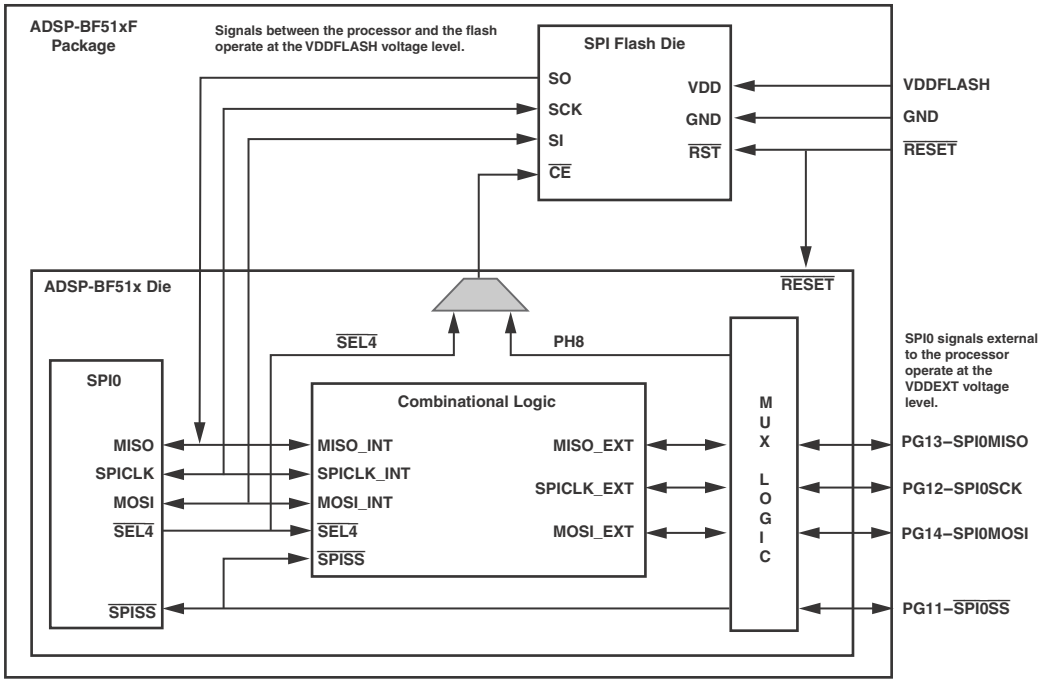

Figure 4. Flash Memory Block Diagram

(EVT), and lists their priorities are described in the *ADSP-BF51x Blackfin Processor Hardware Reference Manual* "System Interrupts" chapter.

System Interrupt Controller (SIC)

The system interrupt controller provides the mapping and routing of events from the many peripheral interrupt sources to the prioritized general-purpose interrupt inputs of the CEC. Although the processors provide a default mapping, the user can alter the mappings and priorities of interrupt events by writing the appropriate values into the interrupt assignment registers (SIC_IARx). See the *ADSP-BF51x Blackfin Processor Hardware Reference Manual* "System Interrupts" chapter for the inputs into the SIC and the default mappings into the CEC.

The SIC allows further control of event processing by providing three pairs of 32-bit interrupt control and status registers. Each register contains a bit corresponding to each of the peripheral interrupt events. For more information, see the *ADSP-BF51x Blackfin Processor Hardware Reference Manual* "System Interrupts" chapter.

DMA CONTROLLERS

The ADSP-BF51x processors have multiple independent DMA channels that support automated data transfers with minimal overhead for the processor core. DMA transfers can occur between the processor's internal memories and any of its DMA-capable peripherals. Additionally, DMA transfers can be accomplished between any of the DMA-capable peripherals and external devices connected to the external memory interfaces, including the SDRAM controller and the asynchronous memory controller. DMA-capable peripherals include the Ethernet MAC, RSI, SPORTs, SPIs, UARTs, and PPI. Each individual DMA-capable peripheral has at least one dedicated DMA channel.

The processors' DMA controller supports both one-dimensional (1-D) and two-dimensional (2-D) DMA transfers. DMA transfer initialization can be implemented from registers or from sets of parameters called descriptor blocks.

The 2-D DMA capability supports arbitrary row and column sizes up to 64K elements by 64K elements, and arbitrary row and column step sizes up to ±32K elements. Furthermore, the column step size can be less than the row step size, allowing implementation of interleaved data streams. This feature is especially useful in video applications where data can be de-interleaved on the fly.

Examples of DMA types supported by the DMA controller include:

- A single, linear buffer that stops upon completion
- A circular, auto-refreshing buffer that interrupts on each full or fractionally full buffer
- 1-D or 2-D DMA using a linked list of descriptors
- 2-D DMA using an array of descriptors, specifying only the base DMA address within a common page

In addition to the dedicated peripheral DMA channels, there are two memory DMA channels that transfer data between the various memories of the processor system. This enables transfers of blocks of data between any of the memories—including external SDRAM, ROM, SRAM, and flash memory—with minimal processor intervention. Memory DMA transfers can be controlled by a very flexible descriptor-based methodology or by a standard register-based autobuffer mechanism.

The processors also have an external DMA controller capability via dual external DMA request signals when used in conjunction with the external bus interface unit (EBIU). This functionality can be used when a high speed interface is required for external FIFOs and high bandwidth communications peripherals. It allows control of the number of data transfers for memory DMA. The number of transfers per edge is programmable. This feature can be programmed to allow memory DMA to have an increased priority on the external bus relative to the core.

PROCESSOR PERIPHERALS

The ADSP-BF51x processors contain a rich set of peripherals connected to the core via several high bandwidth buses, providing flexibility in system configuration as well as excellent overall system performance (see Figure 2). The processors contain dedicated network communication modules and high speed serial and parallel ports, an interrupt controller for flexible management of interrupts from the on-chip peripherals or external sources, and power management control functions to tailor the performance and power characteristics of the processor and system to many application scenarios.

All of the peripherals, except for the general-purpose I/O, rotary counter, TWI, three-phase PWM, real-time clock, and timers, are supported by a flexible DMA structure. There are also separate memory DMA channels dedicated to data transfers between the processor's various memory spaces, including external SDRAM and asynchronous memory. Multiple on-chip buses provide enough bandwidth to keep the processor core running along with activity on all of the on-chip and external peripherals.

Real-Time Clock

The real-time clock (RTC) provides a robust set of digital watch features, including current time, stopwatch, and alarm. The RTC is clocked by a 32.768 kHz crystal external to the processors. The RTC peripheral has a dedicated power supply so that it can remain powered up and clocked even when the rest of the processor is in a low power state. The RTC provides several programmable interrupt options, including interrupt per second, minute, hour, or day clock ticks, interrupt on programmable stopwatch countdown, or interrupt at a programmed alarm time.

The 32.768 kHz input clock frequency is divided down to a 1 Hz signal by a prescaler. The counter function of the timer consists of four counters: a 60-second counter, a 60-minute counter, a 24-hour counter, and an 32,768-day counter.

general-purpose up/down count modes. Then, count direction is either controlled by a level-sensitive input signal or by two edge detectors.

A third input can provide flexible zero marker support and can alternatively be used to input the push-button signal of thumb wheels. All three signals have a programmable debouncing circuit.

An internal signal forwarded to the GP timer unit enables one timer to measure the intervals between count events. Boundary registers enable auto-zero operation or simple system warning by interrupts when programmable count values are exceeded.

Serial Ports

The ADSP-BF51x processors incorporate two dual-channel synchronous serial ports (SPORT0 and SPORT1) for serial and multiprocessor communications. The SPORTs support the following features:

Serial port data can be automatically transferred to and from on-chip memory/external memory via dedicated DMA channels. Each of the serial ports can work in conjunction with another serial port to provide TDM support. In this configuration, one SPORT provides two transmit signals while the other SPORT provides the two receive signals. The frame sync and clock are shared.

Serial ports operate in five modes:

- Standard DSP serial mode
- Multichannel (TDM) mode
- I^2S mode
- Packed I^2S mode
- Left-justified mode

Serial Peripheral Interface (SPI) Ports

The processors have two SPI-compatible ports (SPI0 and SPI1) that enable the processor to communicate with multiple SPI-compatible devices.

The SPI interface uses three signals for transferring data: two data signals (master output-slave input–MOSI, and master input-slave output–MISO) and a clock signal (serial clock–SCK). An SPI chip select input signal ($\overline{\text{SPIxSS}}$) lets other SPI devices select the processor, and multiple SPI chip select output signals let the processor select other SPI devices. The SPI select signals are reconfigured general-purpose I/O signals. Using these signals, the SPI port provides a full-duplex, synchronous serial interface, which supports both master/slave modes and multimaster environments.

The SPI port baud rate and clock phase/polarities are programmable, and it has an integrated DMA channel, configurable to support transmit or receive data streams. The SPI's DMA channel can only service unidirectional accesses at any given time.

UART Ports

The processors provide two full-duplex universal asynchronous receiver/transmitter (UART) ports, which are fully compatible with PC-standard UARTs. Each UART port provides a simplified UART interface to other peripherals or hosts, supporting full-duplex, DMA-supported, asynchronous transfers of serial data. A UART port includes support for five to eight data bits, and none, even, or odd parity. Optionally, an additional address bit can be transferred to interrupt only addressed nodes in multi-drop bus (MDB) systems. A frame is terminates by one, one and a half, two or two and a half stop bits.

The UART ports support automatic hardware flow control through the Clear To Send (CTS) input and Request To Send (RTS) output with programmable assertion FIFO levels.

To help support the Local Interconnect Network (LIN) protocols, a special command causes the transmitter to queue a break command of programmable bit length into the transmit buffer. Similarly, the number of stop bits can be extended by a programmable inter-frame space.

The capabilities of the UARTs are further extended with support for the Infrared Data Association (IrDA®) serial infrared physical layer link specification (SIR) protocol.

2-Wire Interface (TWI)

The processors include a TWI module for providing a simple exchange method of control data between multiple devices. The TWI is compatible with the widely used I^2C® bus standard. The TWI module offers the capabilities of simultaneous master and slave operation, support for both 7-bit addressing and multimedia data arbitration. The TWI interface utilizes two signals for transferring clock (SCL) and data (SDA) and supports the protocol at speeds up to 400k bits/sec. The TWI interface signals are compatible with 5 V logic levels.

Additionally, the processor's TWI module is fully compatible with serial camera control bus (SCCB) functionality for easier control of various CMOS camera sensor devices.

Removable Storage Interface (RSI)

The RSI controller, available on the ADSP-BF514/ADSP-BF514F16/ADSP-BF516/ADSP-BF518/ADSP-BF518F16 processors, acts as the host interface for multi-media cards (MMC), secure digital memory cards (SD Card), secure digital input/output cards (SDIO), and CE-ATA hard disk drives. The following list describes the main features of the RSI controller.

- Support for a single MMC, SD memory, SDIO card or CE-ATA hard disk drive
- Support for 1-bit and 4-bit SD modes
- Support for 1-bit, 4-bit and 8-bit MMC modes
- Support for 4-bit and 8-bit CE-ATA hard disk drives
- A ten-signal external interface with clock, command, and up to eight data lines
- Card detection using one of the data signals
- Card interface clock generation from SCLK
- SDIO interrupt and read wait features
- CE-ATA command completion signal recognition and disable

10/100 Ethernet MAC

The ADSP-BF516 and ADSP-BF518/ADSP-BF518F16 processors offer the capability to directly connect to a network by way of an embedded fast Ethernet media access controller (MAC) that supports both 10-BaseT (10M bits/sec) and 100-BaseT (100M bits/sec) operation. The 10/100 Ethernet MAC peripheral on the processor is fully compliant to the IEEE 802.3-2002 standard and it provides programmable features designed to minimize supervision, bus use, or message processing by the rest of the processor system.

Some standard features are:

- Support of MII and RMII protocols for external PHYs
- Full duplex and half duplex modes
- Data framing and encapsulation: generation and detection of preamble, length padding, and FCS
- Media access management (in half-duplex operation): collision and contention handling, including control of retransmission of collision frames and of back-off timing
- Flow control (in full-duplex operation): generation and detection of pause frames
- Station management: generation of MDC/MDIO frames for read-write access to PHY registers
- Operating range for active and sleep operating modes, see Table 43 on Page 47 and Table 44 on Page 48
- Internal loopback from transmit to receive

Some advanced features are:

- Buffered crystal output to external PHY for support of a single crystal system
- Automatic checksum computation of IP header and IP payload fields of Rx frames
- Independent 32-bit descriptor-driven receive and transmit DMA channels
- Frame status delivery to memory through DMA, including frame completion semaphores for efficient buffer queue management in software
- Tx DMA support for separate descriptors for MAC header and payload to eliminate buffer copy operations
- Convenient frame alignment modes support even 32-bit alignment of encapsulated receive or transmit IP packet data in memory after the 14-byte MAC header
- Programmable Ethernet event interrupt supports any combination of:
  - Selected receive or transmit frame status conditions
  - PHY interrupt condition
  - Wakeup frame detected
  - Selected MAC management counter(s) at half-full
  - DMA descriptor error
- 47 MAC management statistics counters with selectable clear-on-read behavior and programmable interrupts on half maximum value
- Programmable receive address filters, including a 64-bin address hash table for multicast and/or unicast frames, and programmable filter modes for broadcast, multicast, unicast, control, and damaged frames
- Advanced power management supporting unattended transfer of receive and transmit frames and status to/from external memory via DMA during low power sleep mode
- System wakeup from sleep operating mode upon magic packet or any of four user-definable wakeup frame filters
- Support for 802.3Q tagged VLAN frames
- Programmable MDC clock rate and preamble suppression
- In RMII operation, seven unused signals may be configured as GPIO signals for other purposes

IEEE 1588 Support

The IEEE 1588 standard is a precision clock synchronization protocol for networked measurement and control systems. The ADSP-BF518/ADSP-BF518F16 processors include hardware support for IEEE 1588 with an integrated precision time protocol synchronization engine (PTP_TSYNC). This engine provides hardware assisted time stamping to improve the accuracy of clock synchronization between PTP nodes. The main features of the PTP_SYNC engine are:

- Support for both IEEE 1588-2002 and IEEE 1588-2008 protocol standards
- Hardware assisted time stamping capable of up to 12.5 ns resolution
- Lock adjustment
- Programmable PTM message support
- Dedicated interrupts
- Programmable alarm
- Multiple input clock sources (SCLK, MII clock, external clock)
- Programmable pulse per second (PPS) output
- Auxiliary snapshot to time stamp external events

Ports

Because of the rich set of peripherals, the processors group the many peripheral signals to four ports—port F, port G, port H, and port J. Most of the associated pins/balls are shared by multiple signals. The ports function as multiplexer controls.

General-Purpose I/O (GPIO)

The ADSP-BF51x processors have 40 bidirectional, general-purpose I/O (GPIO) signals allocated across three separate GPIO modules—PORTFIO, PORTGIO, and PORTHIO, associated with Port F, Port G, and Port H, respectively. Each GPIO-capable signal shares functionality with other peripherals via a multiplexing scheme; however, the GPIO functionality is the default state of the device upon power-up. Neither GPIO output nor input drivers are active by default. Each general-purpose port signal can be individually controlled by manipulation of the port control, status, and interrupt registers.

All on-chip peripherals are clocked by the system clock (SCLK). The system clock frequency is programmable by means of the SSEL3–0 bits of the PLL_DIV register. The values programmed into the SSEL fields define a divide ratio between the PLL output (VCO) and the system clock. SCLK divider values are 1 through 15. Table 5 illustrates typical system clock ratios.

Table 5. Example System Clock Ratios

Signal Name SSEL3–0	Divider Ratio VCO/SCLK	Example Frequency Ratios (MHz)	
		VCO	SCLK
0010	2:1	100	50
0110	6:1	300	50
1010	10:1	400	40

Note that the divisor ratio must be chosen to limit the system clock frequency to its maximum of f_{SCLK}. The SSEL value can be changed dynamically without any PLL lock latencies by writing the appropriate values to the PLL divisor register (PLL_DIV).

The core clock (CCLK) frequency can also be dynamically changed by means of the CSEL1–0 bits of the PLL_DIV register. Supported CCLK divider ratios are 1, 2, 4, and 8, as shown in Table 6. This programmable core clock capability is useful for fast core frequency modifications.

Table 6. Core Clock Ratios

Signal Name CSEL1–0	Divider Ratio VCO/CCLK	Example Frequency Ratios (MHz)	
		VCO	CCLK
00	1:1	300	300
01	2:1	300	150
10	4:1	400	100
11	8:1	200	25

The maximum CCLK frequency not only depends on the part's speed grade (see Page 67), it also depends on the applied V_{DDINT} voltage. See Table 10 on Page 23 for details. The maximal system clock rate (SCLK) depends on the chip package and the applied V_{DDINT}, V_{DDEXT}, and V_{DDMEM} voltages (see Table 12 on Page 23).

BOOTING MODES

The processor has several mechanisms (listed in Table 7) for automatically loading internal and external memory after a reset. The boot mode is defined by three BMODE input bits dedicated to this purpose. There are two categories of boot modes. In master boot modes the processor actively loads data from parallel or serial memories. In slave boot modes the processor receives data from external host devices.

The boot modes listed in Table 7 provide a number of mechanisms for automatically loading the processor's internal and external memories after a reset. By default, all boot modes use the slowest meaningful configuration settings. Default settings can be altered via the initialization code feature at boot time or by proper OTP programming at pre-boot time. The BMODE bits of the reset configuration register, sampled during power-on resets and software-initiated resets, implement the modes shown in Table 7.

Table 7. Booting Modes

BMODE2–0	Description
000	Idle - No boot
001	Boot from 8- or 16-bit external flash memory
010	Boot from internal SPI memory
011	Boot from external SPI memory (EEPROM or flash)
100	Boot from SPI0 host
101	Boot from OTP memory
110	Boot from SDRAM
111	Boot from UART0 Host

- Idle/no boot mode (BMODE = 0x0)—In this mode, the processor goes into idle. The idle boot mode helps recover from illegal operating modes, such as when the user has mis configured the OTP memory.
- Boot from 8-bit or 16-bit external flash memory (BMODE = 0x1)—In this mode, the boot kernel loads the first block header from address 0x2000 0000 and—depending on instructions containing in the header—the boot kernel performs 8-bit or 16-bit boot or starts program execution at the address provided by the header. By default, all configuration settings are set for the slowest device possible (3-cycle hold time, 15-cycle R/W access times, 4-cycle setup).

  The ARDY is not enabled by default, but it can be enabled by OTP programming. Similarly, all interface behavior and timings can be customized by OTP programming. This includes activation of burst-mode or page-mode operation. In this mode, all signals belonging to the asynchronous interface are enabled at the port muxing level.
- Boot from internal SPI memory (BMODE = 0x2)—The processor uses the internal PH8 GPIO signal to load code previously loaded to the 16M bit internal SPI flash connected to SPI0. Only available on the ADSP-BF51xF processors.
- Boot from external SPI EEPROM or flash (BMODE = 0x3)—8-bit, 16-bit, 24-bit or 32-bit addressable devices are supported. The processor uses the PG15 GPIO signal (at $\overline{\text{SPI0SEL2}}$) to select a single SPI EEPROM/flash device connected to the SPI0 interface; then submits a read command and successive address bytes (0x00) until a valid 8-, 16-, 24-, or 32-bit addressable device is detected. Pull-up resistors are required on the SSEL and MISO signals. By default, a value of 0x85 is written to the SPI0_BAUD register.

The newest IDE, CrossCore Embedded Studio, is based on the Eclipse™ framework. Supporting most Analog Devices processor families, it is the IDE of choice for future processors, including multicore devices. CrossCore Embedded Studio seamlessly integrates available software add-ins to support real time operating systems, file systems, TCP/IP stacks, USB stacks, algorithmic software modules, and evaluation hardware board support packages. For more information visit www.analog.com/cces.

The other Analog Devices IDE, VisualDSP++, supports processor families introduced prior to the release of CrossCore Embedded Studio. This IDE includes the Analog Devices VDK real time operating system and an open source TCP/IP stack. For more information visit www.analog.com/visualdsp. Note that VisualDSP++ will not support future Analog Devices processors.

EZ-KIT Lite Evaluation Board

For processor evaluation, Analog Devices provides wide range of EZ-KIT Lite® evaluation boards. Including the processor and key peripherals, the evaluation board also supports on-chip emulation capabilities and other evaluation and development features. Also available are various EZ-Extenders®, which are daughter cards delivering additional specialized functionality, including audio and video processing. For more information visit www.analog.com and search on “ezkit” or “ezextender”.

EZ-KIT Lite Evaluation Kits

For a cost-effective way to learn more about developing with Analog Devices processors, Analog Devices offer a range of EZ-KIT Lite evaluation kits. Each evaluation kit includes an EZ-KIT Lite evaluation board, directions for downloading an evaluation version of the available IDE(s), a USB cable, and a power supply. The USB controller on the EZ-KIT Lite board connects to the USB port of the user’s PC, enabling the chosen IDE evaluation suite to emulate the on-board processor in-circuit. This permits the customer to download, execute, and debug programs for the EZ-KIT Lite system. It also supports in-circuit programming of the on-board Flash device to store user-specific boot code, enabling standalone operation. With the full version of CrossCore Embedded Studio or VisualDSP++ installed (sold separately), engineers can develop software for supported EZ-KITs or any custom system utilizing supported Analog Devices processors.

Software Add-Ins for CrossCore Embedded Studio

Analog Devices offers software add-ins which seamlessly integrate with CrossCore Embedded Studio to extend its capabilities and reduce development time. Add-ins include board support packages for evaluation hardware, various middleware packages, and algorithmic modules. Documentation, help, configuration dialogs, and coding examples present in these add-ins are viewable through the CrossCore Embedded Studio IDE once the add-in is installed.

Board Support Packages for Evaluation Hardware

Software support for the EZ-KIT Lite evaluation boards and EZ-Extender daughter cards is provided by software add-ins called Board Support Packages (BSPs). The BSPs contain the required drivers, pertinent release notes, and select example code for the given evaluation hardware. A download link for a specific BSP is located on the web page for the associated EZ-KIT or EZ-Extender product. The link is found in the *Product Download* area of the product web page.

Middleware Packages

Analog Devices separately offers middleware add-ins such as real time operating systems, file systems, USB stacks, and TCP/IP stacks. For more information see the following web pages:

- www.analog.com/ucos3
- www.analog.com/ucfs
- www.analog.com/ucusbd
- www.analog.com/lwip

Algorithmic Modules

To speed development, Analog Devices offers add-ins that perform popular audio and video processing algorithms. These are available for use with both CrossCore Embedded Studio and VisualDSP++. For more information visit www.analog.com and search on “Blackfin software modules” or “SHARC software modules”.

Designing an Emulator-Compatible DSP Board (Target)

For embedded system test and debug, Analog Devices provides a family of emulators. On each JTAG DSP, Analog Devices supplies an IEEE 1149.1 JTAG Test Access Port (TAP). In-circuit emulation is facilitated by use of this JTAG interface. The emulator accesses the processor’s internal features via the processor’s TAP, allowing the developer to load code, set breakpoints, and view variables, memory, and registers. The processor must be halted to send data and commands, but once an operation is completed by the emulator, the DSP system is set to run at full speed with no impact on system timing. The emulators require the target board to include a header that supports connection of the DSP’s JTAG port to the emulator.

For details on target board design issues including mechanical layout, single processor connections, signal buffering, signal termination, and emulator pod logic, see the *EE-68: Analog Devices JTAG Emulation Technical Reference* on the Analog Devices website (www.analog.com)—use site search on “EE-68.” This document is updated regularly to keep pace with improvements to emulator support.

SIGNAL DESCRIPTIONS

The processors' signal definitions are listed in Table 8. In order to maintain maximum function and reduce package size and signal count, some signals have dual, multiplexed functions. In cases where signal function is reconfigurable, the default state is shown in plain text, while the alternate function is shown in italics.

All pins are three-stated during and immediately after reset, with the exception of the external memory interface, asynchronous and synchronous memory control, and the buffered XTAL output pin (CLKBUF). On the external memory interface, the control and address lines are driven high, with the exception of CLKOUT, which toggles at the system clock rate. During hibernate all outputs are three-stated unless otherwise noted in Table 8.

All I/O signals have their input buffers disabled with the exception of the signals noted in the data sheet that need pull-ups or pull downs if unused.

The SDA (serial data) and SCL (serial clock) pins/balls are open drain and therefore require a pullup resistor. Consult version 2.1 of the I^2C specification for the proper resistor value.

It is strongly advised to use the available IBIS models to ensure that a given board design meets overshoot/undershoot and signal integrity requirements. If no IBIS simulation is performed, it is strongly recommended to add series resistor terminations for all Driver Types A, C and D. The termination resistors should be placed near the processor to reduce transients and improve signal integrity. The resistance value, typically 33 Ω or 47 Ω, should be chosen to match the average board trace impedance. Additionally, adding a parallel termination to CLKOUT may prove useful in further enhancing signal integrity. Be sure to verify overshoot/undershoot and signal integrity specifications on actual hardware.

Table 8. Signal Descriptions

Signal Name	Type	Function	Driver Type[1]
EBIU			
ADDR19–1	O	Address Bus	A
DATA15–0	I/O	Data Bus	A
$\overline{\text{ABE1–0}}$/*SDQM1–0*	O	Byte Enable or Data Mask	A
$\overline{\text{AMS1–0}}$	O	Asynchronous Memory Bank Selects (Require pull-ups if hibernate is used)	A
$\overline{\text{ARE}}$	O	Asynchronous Memory Read Enable	A
$\overline{\text{AWE}}$	O	Asynchronous Memory Write Enable	A
$\overline{\text{SRAS}}$	O	SDRAM Row Address Strobe	A
$\overline{\text{SCAS}}$	O	SDRAM Column Address Strobe	A
$\overline{\text{SWE}}$	O	SDRAM Write Enable	A
SCKE	O	SDRAM Clock Enable (Requires a pull-down if hibernate with SDRAM self-refresh is used)	A
CLKOUT	O	SDRAM Clock Output	B
SA10	O	SDRAM A10 Signal	A
$\overline{\text{SMS}}$	O	SDRAM Bank Select	A
Port F: GPIO and Multiplexed Peripherals			
PF0/*ETxD2/PPI D0/*$\overline{\textit{SPI1SEL2}}$*/TACLK6*	I/O	GPIO/*Ethernet MII Transmit D2/PPI Data 0/SPI1 Slave Select 2/Timer6 Alternate Clock*	C
PF1/*ERxD2/PPI D1/PWM AH/TACLK7*	I/O	GPIO/*Ethernet MII Receive D2/PPI Data 1/PWM AH Output/Timer7 Alternate Clock*	C
PF2/*ETxD3/PPI D2/PWM AL*	I/O	GPIO/*Ethernet Transmit D3/PPI Data 2/PWM AL Output*	C
PF3/*ERxD3/PPI D3/PWM BH/TACLK0*	I/O	GPIO/*Ethernet MII Data Receive D3/PPI Data 3/PWM BH Output/Timer0 Alternate Clock*	C
PF4/*ERxCLK/PPI D4/PWM BL/TACLK1*	I/O	GPIO/*Ethernet MII Receive Clock/PPI Data 4/PWM BL Out/Timer1 Alternate CLK*	C
PF5/*ERxDV/PPI D5/PWM CH/TACI0*	I/O	GPIO/*Ethernet MII Receive Data Valid/PPI Data 5/PWM CH Out /Timer0 Alternate Capture Input*	C
PF6/*COL/PPI D6/PWM CL/TACI1*	I/O	GPIO/*Ethernet MII Collision/PPI Data 6/PWM CL Out/Timer1 Alternate Capture Input*	C
PF7/$\overline{\textit{SPI0SEL1}}$*/PPI D7/PWMSYNC*	I/O	GPIO/*SPI0 Slave Select 1/PPI Data 7/PWM Sync*	C

TIMING SPECIFICATIONS

Clock and Reset Timing

Table 24 and Figure 9 describe clock and reset operations. Per the CCLK and SCLK timing specifications in Table 10, Table 11, and Table 12 on Page 23, combinations of CLKIN and clock multipliers must not select core/peripheral clocks in excess of the processor's speed grade.

Table 24. Clock and Reset Timing

Parameter		Min	Max	Unit
Timing Requirements				
f_{CKIN}	CLKIN Frequency (Commercial/Industrial Models[1, 2, 3, 4]	12	50	MHz
f_{CKIN}	CLKIN Frequency (Automotive Models)[1, 2, 3, 4]	14	50	MHz
t_{CKINL}	CLKIN Low Pulse[1]	10		ns
t_{CKINH}	CLKIN High Pulse[1]	10		ns
t_{WRST}	$\overline{\text{RESET}}$ Asserted Pulse Width Low[5]	11 × t_{CKIN}		ns
Switching Characteristic				
$t_{BUFDLAY}$	CLKIN to CLKBUF Delay		11	ns

[1] Applies to PLL bypass mode and PLL nonbypass mode.
[2] Combinations of the CLKIN frequency and the PLL clock multiplier must not exceed the allowed f_{VCO}, f_{CCLK}, and f_{SCLK} settings discussed in Table 10 through Table 12 on Page 23.
[3] The t_{CKIN} period (see Figure 9) equals $1/f_{CKIN}$.
[4] If the DF bit in the PLL_CTL register is set, the minimum f_{CKIN} specification is 24 MHz for commercial/industrial models and 28 MHz for automotive models.
[5] Applies after power-up sequence is complete. See Table 25 and Figure 10 for power-up reset timing.

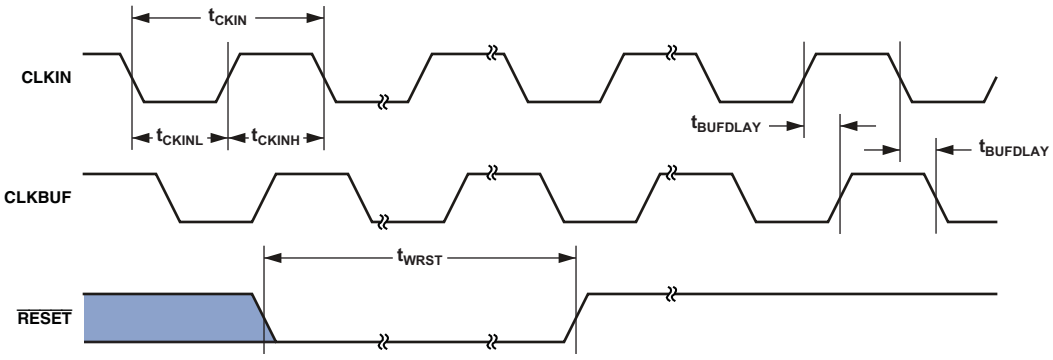

Figure 9. Clock and Reset Timing

Asynchronous Memory Read Cycle Timing

Table 26. Asynchronous Memory Read Cycle Timing

Parameter		V_{DDMEM} 1.8 V Nominal Min	V_{DDMEM} 1.8 V Nominal Max	V_{DDMEM} 2.5 V/3.3 V Nominal Min	V_{DDMEM} 2.5 V/3.3 V Nominal Max	Unit
Timing Requirements						
t_{SDAT}	DATA15–0 Setup Before CLKOUT	2.1		2.1		ns
t_{HDAT}	DATA15–0 Hold After CLKOUT	1.2		0.8		ns
t_{SARDY}	ARDY Setup Before CLKOUT	4		4		ns
t_{HARDY}	ARDY Hold After CLKOUT	0.2		0.2		ns
Switching Characteristics						
t_{DO}	Output Delay After CLKOUT[1]		6		6	ns
t_{HO}	Output Hold After CLKOUT [1]	0.8		0.8		ns

[1] Output pins/balls include $\overline{AMS3-0}$, $\overline{ABE1-0}$, ADDR19–1, $\overline{AOE}$, $\overline{ARE}$.

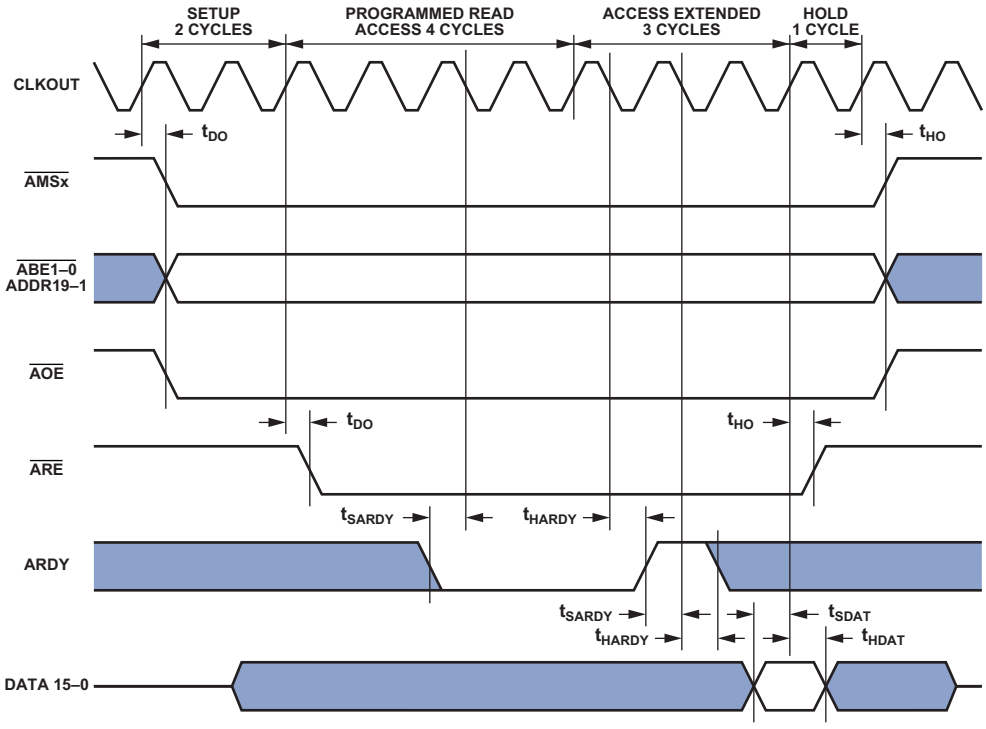

Figure 11. Asynchronous Memory Read Cycle Timing

Table 32. RSI Controller Timing (High Speed Mode)

Parameter		Min	Max	Unit
Timing Requirements				
t_{ISU}	Input Setup Time	5.6		ns
t_{IH}	Input Hold Time	2		ns
Switching Characteristics				
f_{PP}[1]	Clock Frequency Data Transfer Mode	0	50	MHz
t_{WL}	Clock Low Time	7		ns
t_{WH}	Clock High Time	7		ns
t_{TLH}	Clock Rise Time		3	ns
t_{THL}	Clock Fall Time		3	ns
t_{ODLY}	Output Delay Time During Data Transfer Mode		4	ns
t_{OH}	Output Hold Time	2.75		ns

[1] $t_{PP} = 1/f_{PP}$

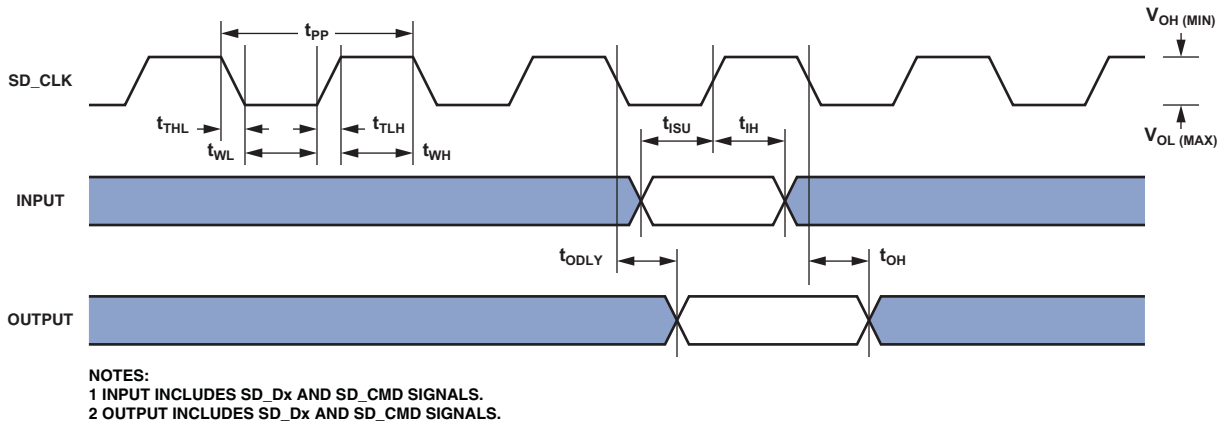

Figure 21. RSI Controller Timing (High Speed Mode)

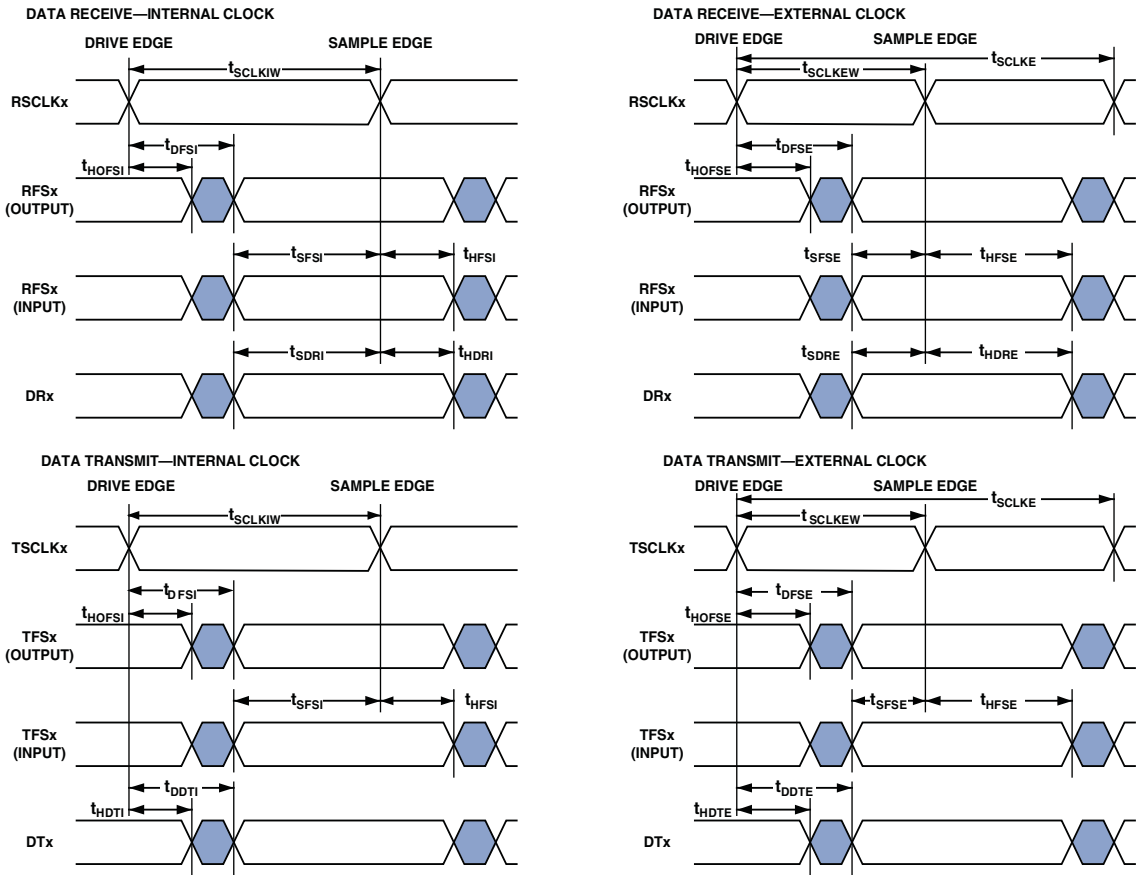

Figure 22. Serial Ports

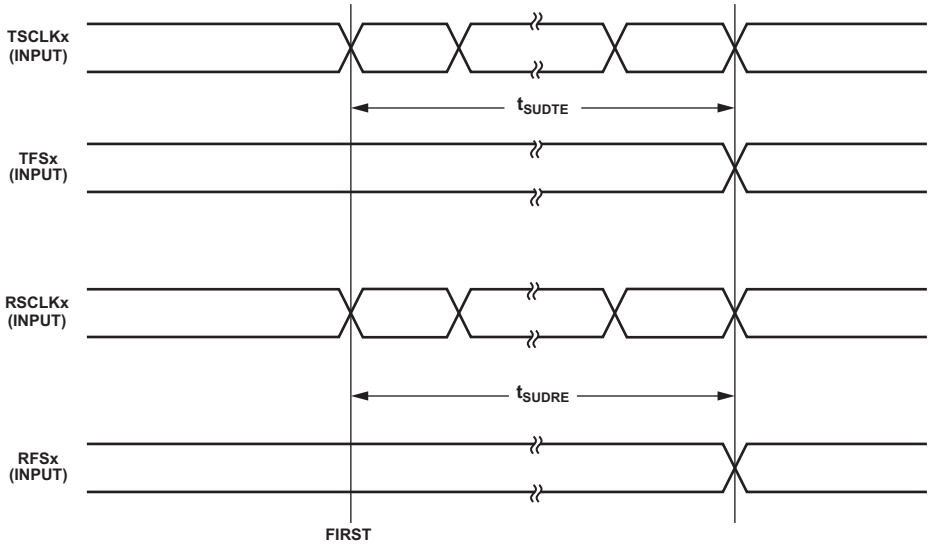

Figure 23. Serial Port Start Up with External Clock and Frame Sync

Table 36. External Late Frame Sync

Parameter		V_{DDEXT} 1.8 V Nominal Min	V_{DDEXT} 1.8 V Nominal Max	V_{DDEXT} 2.5 V/3.3 V Nominal Min	V_{DDEXT} 2.5 V/3.3 V Nominal Max	Unit
Switching Characteristics						
$t_{DDTLFSE}$[1, 2]	Data Delay from Late External TFSx or External RFSx with MCE = 1, MFD = 0		12		10	ns
$t_{DTENLFSE}$[1, 2]	Data Enable from Late FS or MCE = 1, MFD = 0	0		0		ns

[1] MCE = 1, TFSx enable and TFSx valid follow $t_{DDTENFS}$ and $t_{DDTLFSE}$.
[2] If external RFSx/TFSx setup to RSCLKx/TSCLKx > $t_{SCLKE}/2$ then $t_{DDTTE/I}$ and $t_{DTENE/I}$ apply, otherwise $t_{DDTLFSE}$ and $t_{DTENLFS}$ apply.

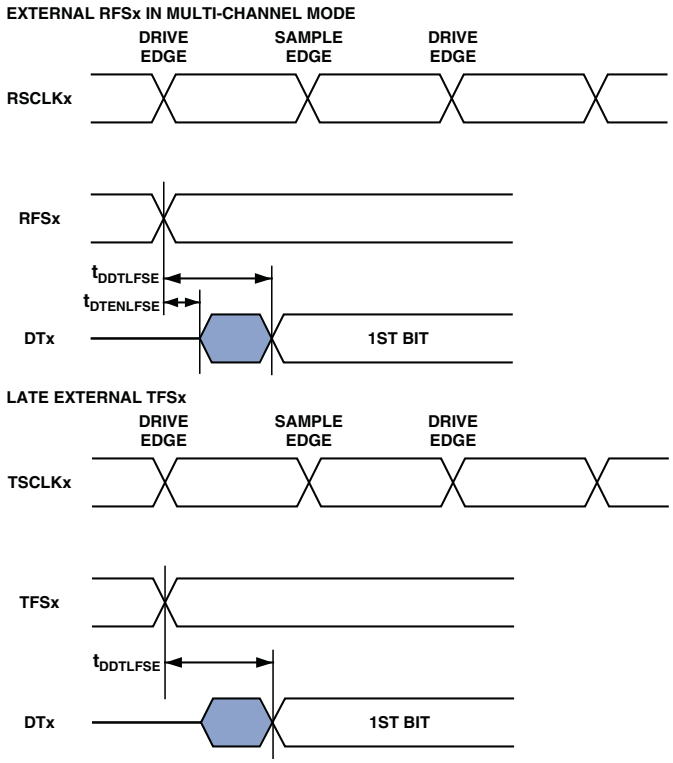

Figure 25. External Late Frame Sync

Serial Peripheral Interface (SPI) Port—Slave Timing

Table 38 and Figure 27 describe SPI port slave operations.

Table 38. Serial Peripheral Interface (SPI) Port—Slave Timing

Parameter		V_{DDEXT} 1.8 V Nominal		V_{DDEXT} 2.5 V/3.3 V Nominal		Unit
		Min	Max	Min	Max	
Timing Requirements						
t_{SPICHS}	Serial Clock High Period	$2 \times t_{SCLK} - 1.5$		$2 \times t_{SCLK} - 1.5$		ns
t_{SPICLS}	Serial Clock Low Period	$2 \times t_{SCLK} - 1.5$		$2 \times t_{SCLK} - 1.5$		ns
t_{SPICLK}	Serial Clock Period	$4 \times t_{SCLK} - 1.5$		$4 \times t_{SCLK} - 1.5$		ns
t_{HDS}	Last SCK Edge to $\overline{SPISS}$ Not Asserted	$2 \times t_{SCLK} - 1.5$		$2 \times t_{SCLK} - 1.5$		ns
t_{SPITDS}	Sequential Transfer Delay	$2 \times t_{SCLK} - 1.5$		$2 \times t_{SCLK} - 1.5$		ns
t_{SDSCI}	$\overline{SPISS}$ Assertion to First SCK Edge	$2 \times t_{SCLK} - 1.5$		$2 \times t_{SCLK} - 1.5$		ns
t_{SSPID}	Data Input Valid to SCK Edge (Data Input Setup)	1.6		1.6		ns
t_{HSPID}	SCK Sampling Edge to Data Input Invalid	2		1.6		ns
Switching Characteristics						
t_{DSOE}	$\overline{SPISS}$ Assertion to Data Out Active	0	12	0	10.3	ns
t_{DSDHI}	$\overline{SPISS}$ Deassertion to Data High Impedance	0	11	0	9	ns
t_{DDSPID}	SCK Edge to Data Out Valid (Data Out Delay)		10		10	ns
t_{HDSPID}	SCK Edge to Data Out Invalid (Data Out Hold)	0		0		ns

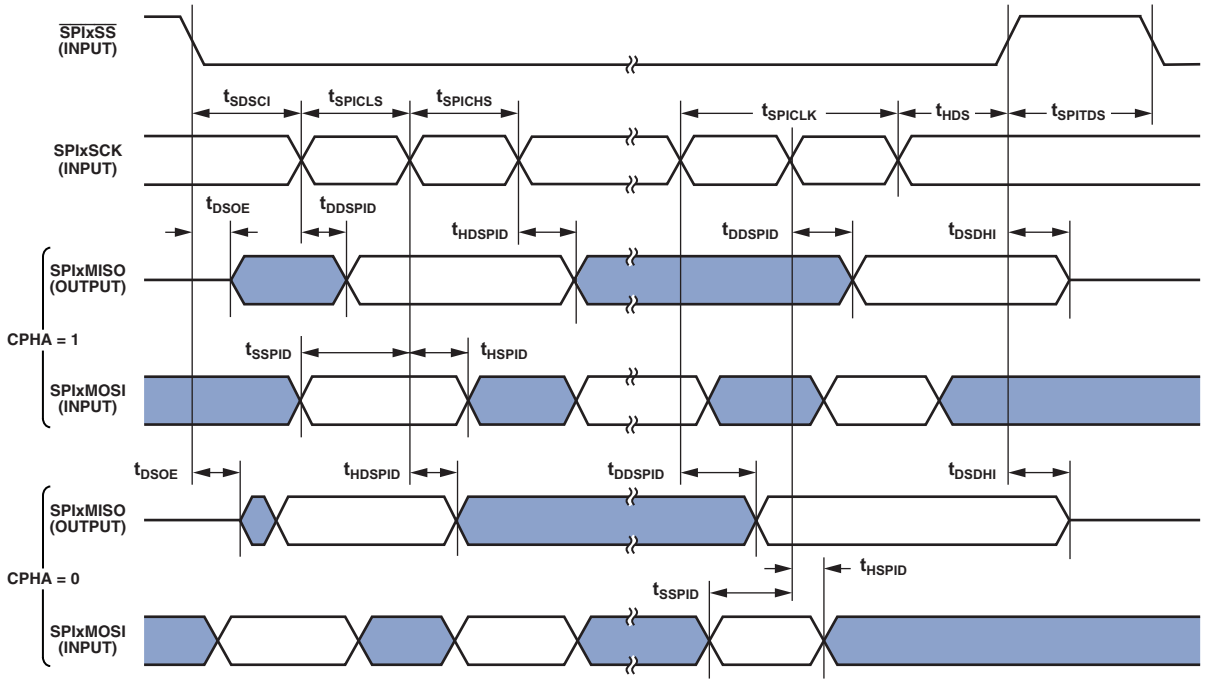

Figure 27. Serial Peripheral Interface (SPI) Port—Slave Timing

Universal Asynchronous Receiver-Transmitter (UART) Ports—Receive and Transmit Timing

The UART ports receive and transmit operations are described in the *ADSP-BF51x Hardware Reference Manual*.

General-Purpose Port Timing

Table 39 and Figure 28 describe general-purpose port operations.

Table 39. General-Purpose Port Timing

Parameter		V_{DDEXT} 1.8 V Nominal		V_{DDEXT} 2.5 V/3.3 V Nominal		Unit
		Min	Max	Min	Max	
Timing Requirement						
t_{WFI}	General-Purpose Port Signal Input Pulse Width	t_{SCLK} + 1		t_{SCLK} + 1		ns
Switching Characteristic						
t_{GPOD}	General-Purpose Port Signal Output Delay from CLKOUT Low	0	11	0	8.5	ns

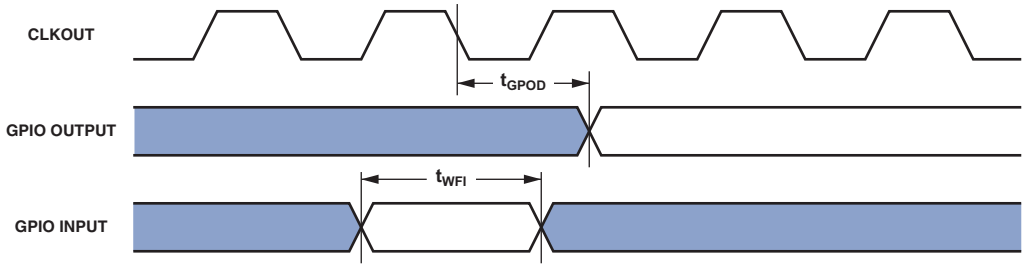

Figure 28. General-Purpose Port Timing

Timer Clock Timing

Table 40 and Figure 29 describe timer clock timing.

Table 40. Timer Clock Timing

Parameter		Min	Max	Unit
Switching Characteristic				
t_{TODP}	Timer Output Update Delay After PPICLK High		12	ns

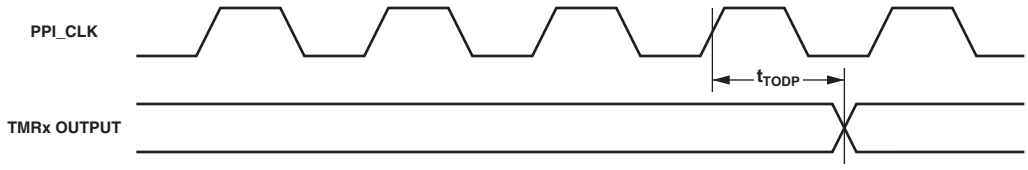

Figure 29. Timer Clock Timing

Table 46. 10/100 Ethernet MAC Controller Timing: RMII Transmit Signal

Parameter[1]		Min	Max	Unit
Switching Characteristics				
$t_{EREFCLKOV}$	RMII REF_CLK Rising Edge to Tx Output Valid (Data Out Valid)		8.1	ns
$t_{EREFCLKOH}$	RMII REF_CLK Rising Edge to Tx Output Invalid (Data Out Hold)	2		ns

[1] RMII outputs synchronous to RMII REF_CLK are ETxD1–0.

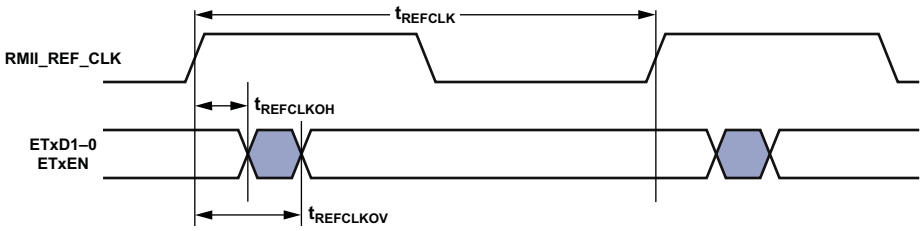

Figure 35. 10/100 Ethernet MAC Controller Timing: RMII Transmit Signal

OUTPUT DRIVE CURRENTS

Figure 39 through Figure 53 show typical current-voltage characteristics for the output drivers of the ADSP-BF51xF processors.

The curves represent the current drive capability of the output drivers. See Table 8 on Page 19 for information about which driver type corresponds to a particular ball.

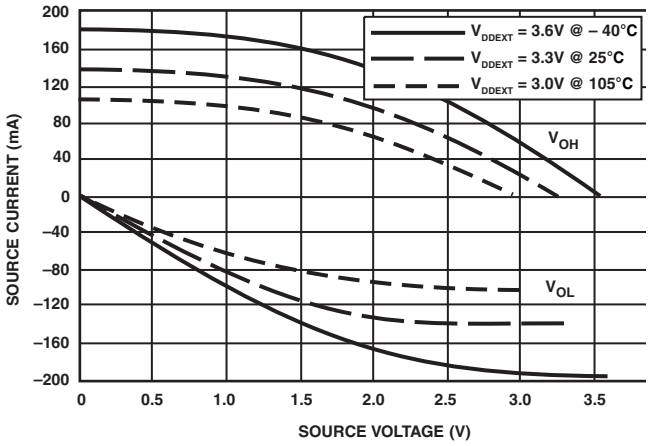

Figure 39. Driver Type A Current (3.3V V_{DDEXT}/V_{DDMEM})

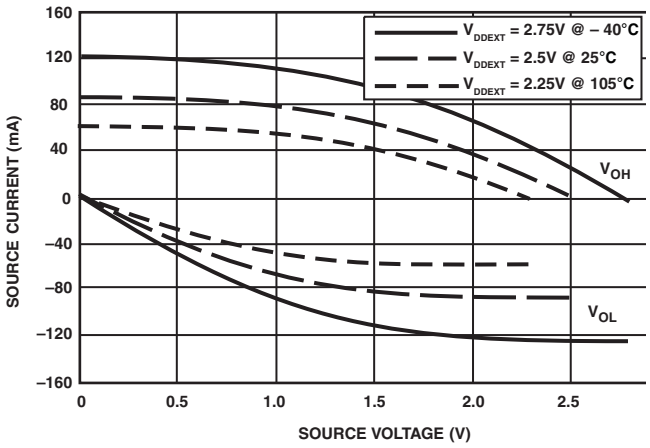

Figure 40. Driver Type A Current (2.5V V_{DDEXT}/V_{DDMEM})

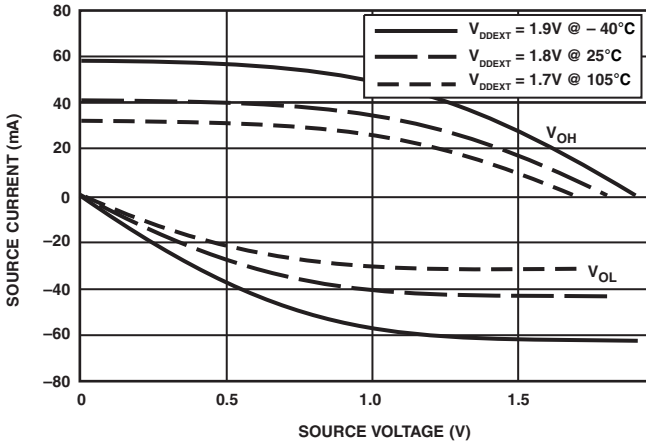

Figure 41. Driver Type A Current (1.8V V_{DDEXT}/V_{DDMEM})

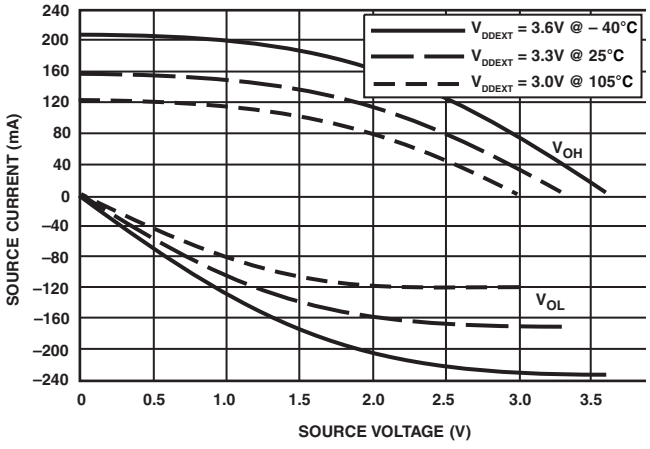

Figure 42. Driver Type B Current (3.3V V_{DDEXT}/V_{DDMEM})

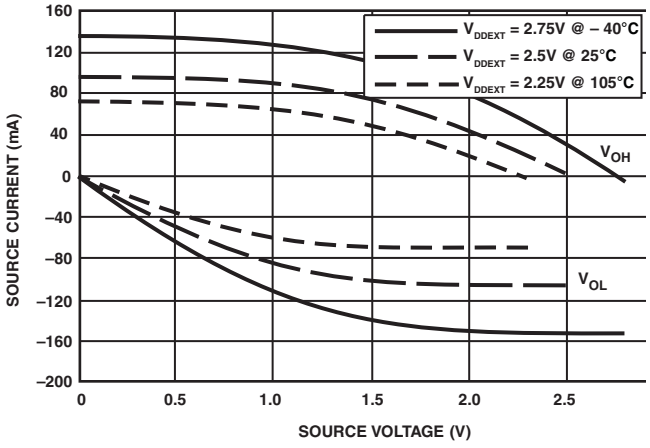

Figure 43. Driver Type B Current (2.5V V_{DDEXT}/V_{DDMEM})

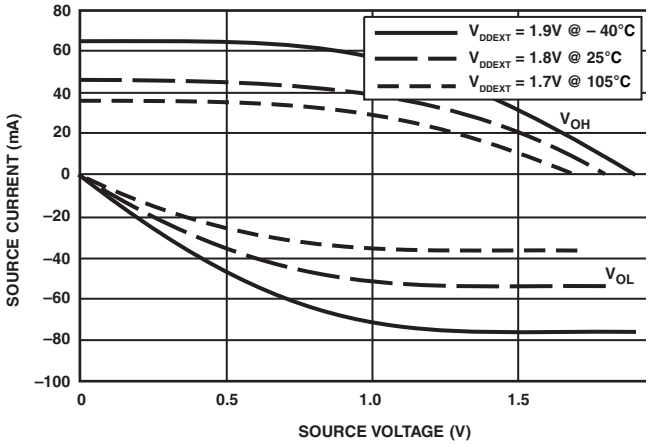

Figure 44. Driver Type B Current (1.8V V_{DDEXT}/V_{DDMEM})

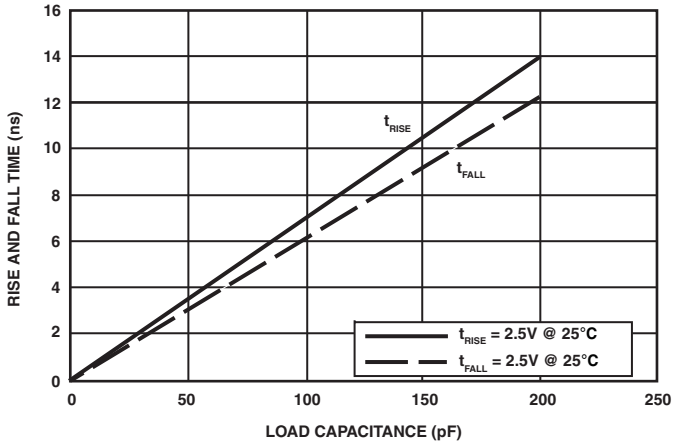

Figure 64. Driver Type C Typical Rise and Fall Times (10%–90%) vs. Load Capacitance (2.5V V_{DDEXT}/V_{DDMEM})

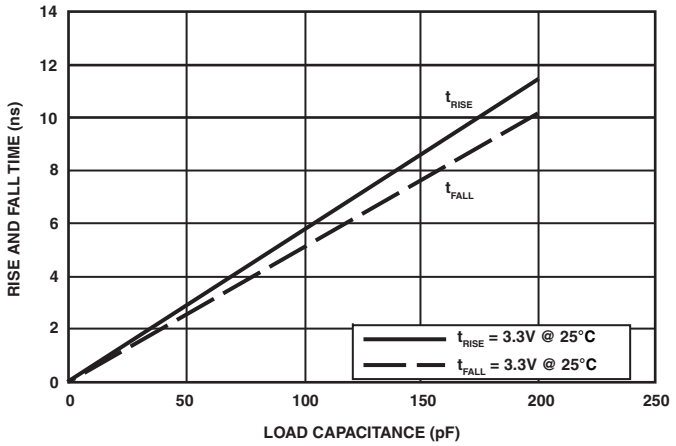

Figure 65. Driver Type C Typical Rise and Fall Times (10%–90%) vs. Load Capacitance (3.3V V_{DDEXT}/V_{DDMEM})

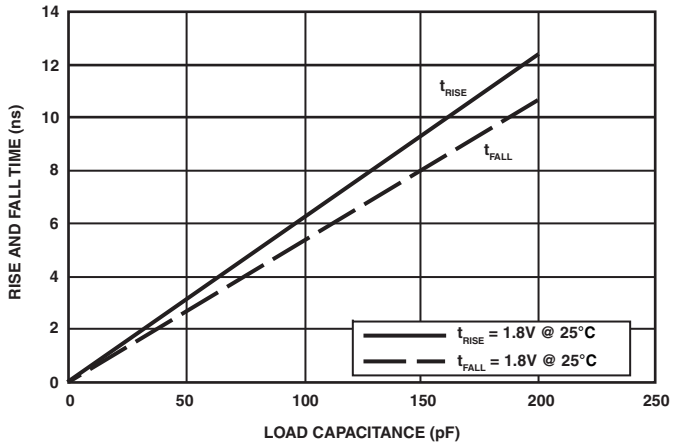

Figure 66. Driver Type D Typical Rise and Fall Times (10%–90%) vs. Load Capacitance (1.8V V_{DDEXT}/V_{DDMEM})

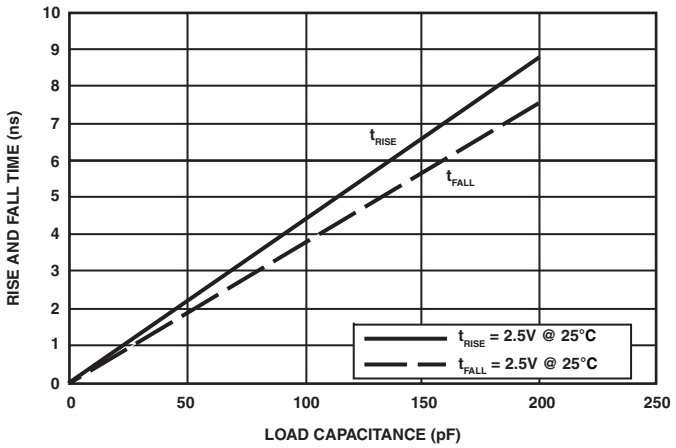

Figure 67. Driver Type D Typical Rise and Fall Times (10%–90%) vs. Load Capacitance (2.5V V_{DDEXT}/V_{DDMEM})

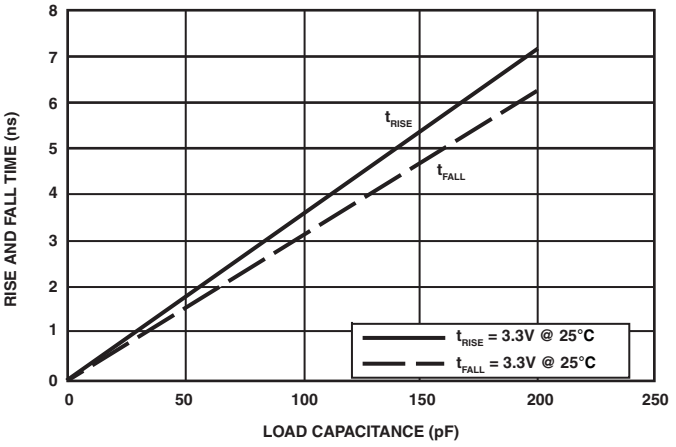

Figure 68. Driver Type D Typical Rise and Fall Times (10%–90%) vs. Load Capacitance (3.3V V_{DDEXT}/V_{DDMEM})

THERMAL CHARACTERISTICS

To determine the junction temperature on the application printed circuit board use:

$$T_J = T_{CASE} + (\Psi_{JT} \times P_D)$$

where:

T_J = Junction temperature (°C)

T_{CASE} = Case temperature (°C) measured by customer at top center of package.

Ψ_{JT} = From Table 51

P_D = Power dissipation (see Total Power Dissipation on Page 25 for the method to calculate P_D)

Values of θ_{JA} are provided for package comparison and printed circuit board design considerations. θ_{JA} can be used for a first order approximation of T_J by the equation:

$$T_J = T_A + (\theta_{JA} \times P_D)$$

where:

T_A = Ambient temperature (°C)

Values of θ_{JC} are provided for package comparison and printed circuit board design considerations when an external heat sink is required.

Values of θ_{JB} are provided for package comparison and printed circuit board design considerations.

In Table 51, airflow measurements comply with JEDEC standards JESD51-2 and JESD51-6, and the junction-to-board measurement complies with JESD51-8. The junction-to-case measurement complies with MIL-STD-883 (Method 1012.1). All measurements use a 2S2P JEDEC test board.

The LQFP_EP package requires thermal trace squares and thermal vias to an embedded ground plane in the PCB. The paddle must be connected to ground for proper operation to data sheet specifications. Refer to JEDEC standard JESD51-5 for more information.

Table 50. Thermal Characteristics for SQ-176-2 Package

Parameter	Condition	Typical	Unit
θ_{JA}	0 Linear m/s Airflow	17.4	°C/W
θ_{JMA}	1 Linear m/s Airflow	14.8	°C/W
θ_{JMA}	2 Linear m/s Airflow	14.0	°C/W
θ_{JC}	Not Applicable	7.8	°C/W
Ψ_{JT}	0 Linear m/s Airflow	0.28	°C/W
Ψ_{JT}	1 Linear m/s Airflow	0.39	°C/W
Ψ_{JT}	2 Linear m/s Airflow	0.48	°C/W

Table 51. Thermal Characteristics for BC-168-1 Package

Parameter	Condition	Typical	Unit
θ_{JA}	0 Linear m/s Airflow	30.5	°C/W
θ_{JMA}	1 Linear m/s Airflow	27.6	°C/W
θ_{JMA}	2 Linear m/s Airflow	26.3	°C/W
θ_{JC}	Not Applicable	11.1	°C/W
Ψ_{JT}	0 Linear m/s Airflow	0.20	°C/W
Ψ_{JT}	1 Linear m/s Airflow	0.35	°C/W
Ψ_{JT}	2 Linear m/s Airflow	0.45	°C/W

Figure 71 shows the top view of the CSP_BGA ball configuration. Figure 72 shows the bottom view of the CSP_BGA ball configuration.

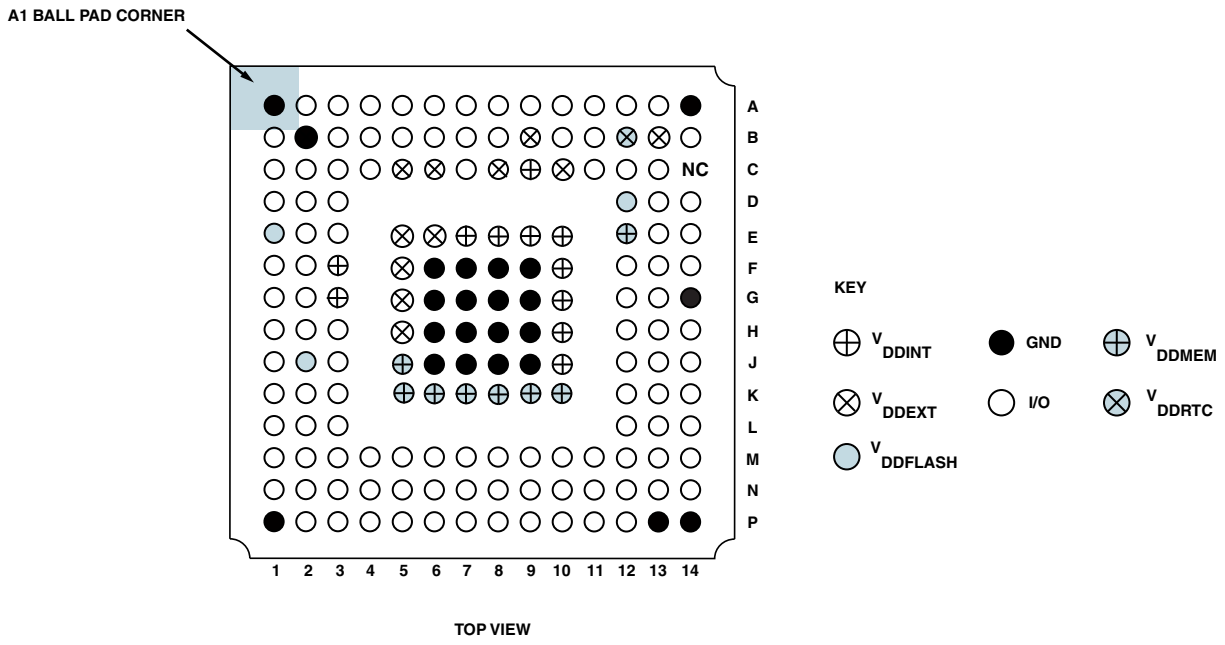

Figure 71. 168-Ball CSP_BGA Ball Configuration (Top View)

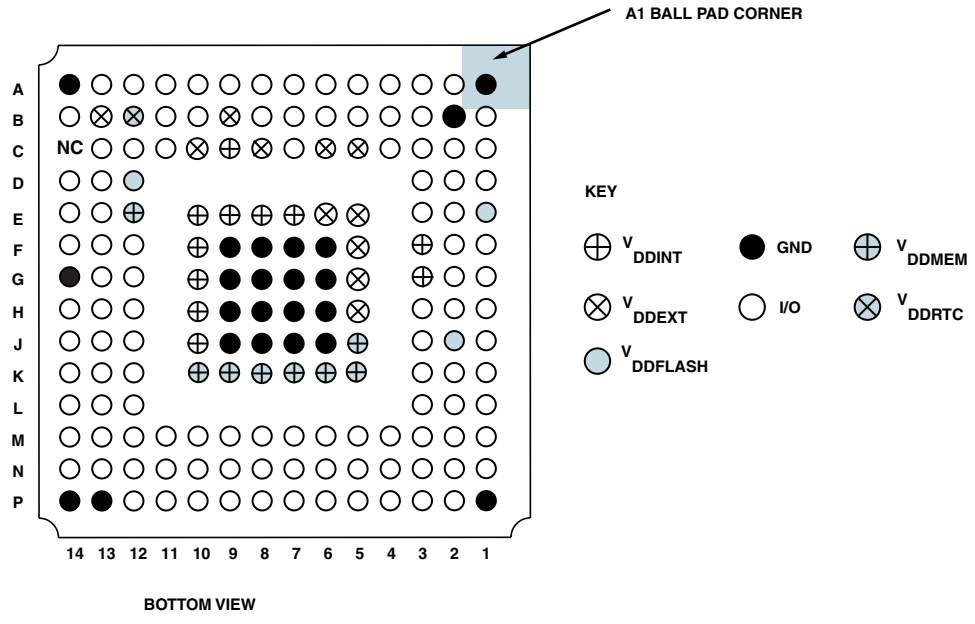

Figure 72. 168-Ball CSP_BGA Ball Configuration (Bottom View)