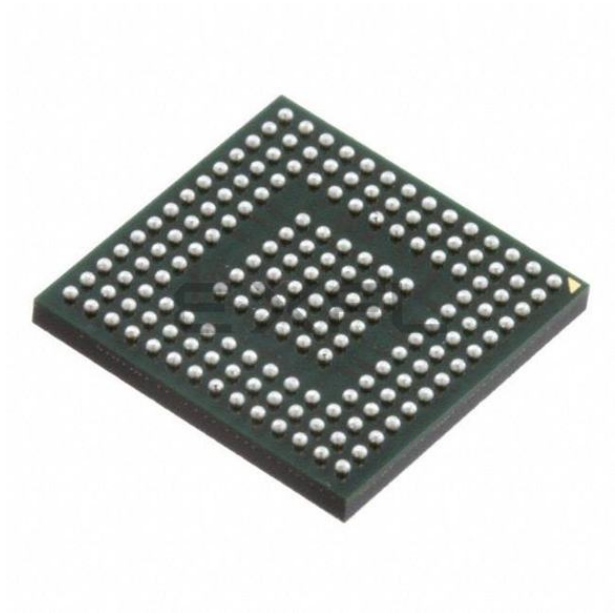


Welcome to E-XFL.COM

Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Obsolete
Type	Fixed Point
Interface	Ethernet, I²C, PPI, RSI, SPI, SPORT, UART/USART
Clock Rate	400MHz
Non-Volatile Memory	FLASH (16Mbit)
On-Chip RAM	116kB
Voltage - I/O	1.8V, 2.5V, 3.3V
Voltage - Core	1.30V
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	168-LFBGA, CSPBGA
Supplier Device Package	168-CSPBGA (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-bf518bbcz4f16

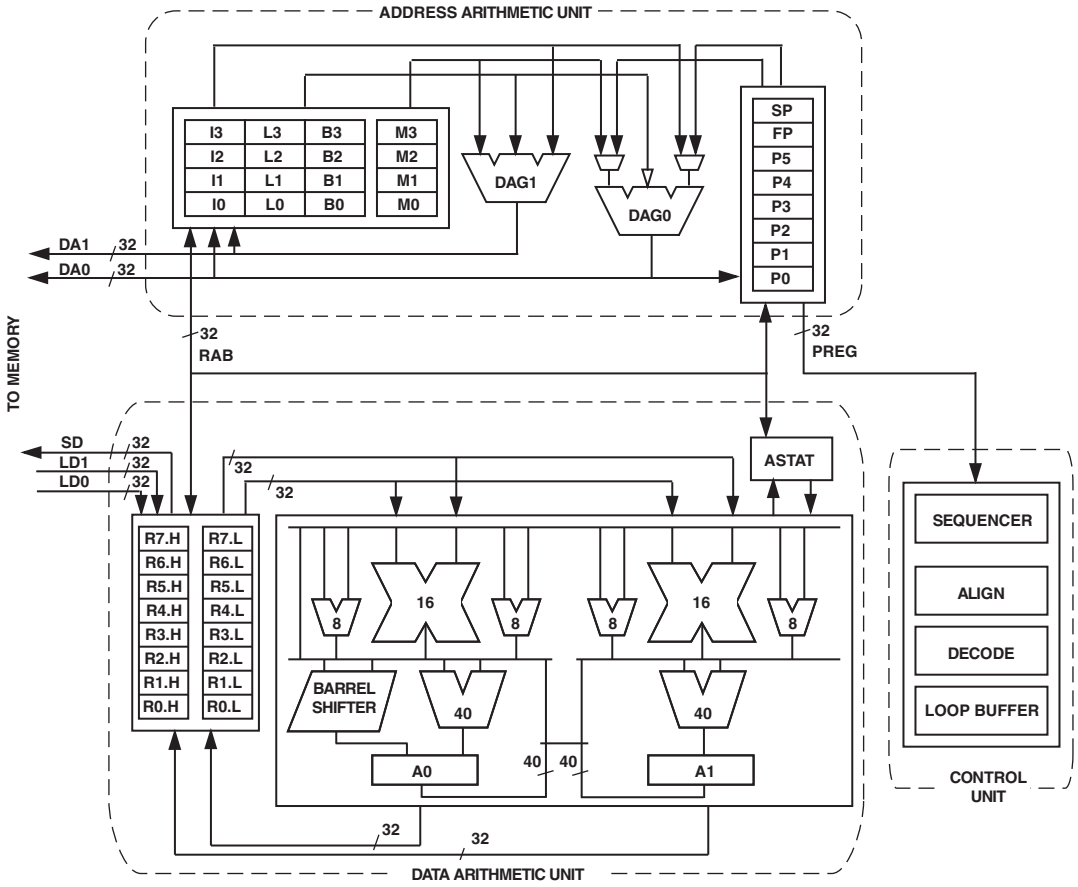


Figure 2. Blackfin Processor Core

For certain instructions, two 16-bit ALU operations can be performed simultaneously on register pairs (a 16-bit high half and 16-bit low half of a compute register). If the second ALU is used, quad 16-bit operations are possible.

The 40-bit shifter can perform shifts and rotates and is used to support normalization, field extract, and field deposit instructions.

The program sequencer controls the flow of instruction execution, including instruction alignment and decoding. For program flow control, the sequencer supports PC relative and indirect conditional jumps (with static branch prediction), and subroutine calls. Hardware is provided to support zero-overhead looping. The architecture is fully interlocked, meaning that the programmer need not manage the pipeline when executing instructions with data dependencies.

The address arithmetic unit provides two addresses for simultaneous dual fetches from memory. It contains a multiported register file consisting of four sets of 32-bit index, modify, length, and base registers (for circular buffering), and eight additional 32-bit pointer registers (for C-style indexed stack manipulation).

Blackfin processors support a modified Harvard architecture in combination with a hierarchical memory structure. Level 1 (L1) memories are those that typically operate at the full processor speed with little or no latency. At the L1 level, the instruction memory holds instructions only. The two data memories hold data, and a dedicated scratchpad data memory stores stack and local variable information.

In addition, multiple L1 memory blocks are provided, offering a configurable mix of SRAM and cache. The memory management unit (MMU) provides memory protection for individual tasks that may be operating on the core and can protect system registers from unintended access.

The architecture provides three modes of operation: user mode, supervisor mode, and emulation mode. User mode has restricted access to certain system resources, thus providing a protected software environment, while supervisor mode has unrestricted access to the system and core resources.

The Blackfin processor instruction set has been optimized so that 16-bit opcodes represent the most frequently used instructions, resulting in excellent compiled code density. Complex DSP instructions are encoded into 32-bit opcodes, representing fully featured multifunction instructions. Blackfin processors support a limited multi-issue capability, where a 32-bit

(EVT), and lists their priorities are described in the *ADSP-BF51x Blackfin Processor Hardware Reference Manual* "System Interrupts" chapter.

System Interrupt Controller (SIC)

The system interrupt controller provides the mapping and routing of events from the many peripheral interrupt sources to the prioritized general-purpose interrupt inputs of the CEC. Although the processors provide a default mapping, the user can alter the mappings and priorities of interrupt events by writing the appropriate values into the interrupt assignment registers (SIC_IARx). See the *ADSP-BF51x Blackfin Processor Hardware Reference Manual* "System Interrupts" chapter for the inputs into the SIC and the default mappings into the CEC.

The SIC allows further control of event processing by providing three pairs of 32-bit interrupt control and status registers. Each register contains a bit corresponding to each of the peripheral interrupt events. For more information, see the *ADSP-BF51x Blackfin Processor Hardware Reference Manual* "System Interrupts" chapter.

DMA CONTROLLERS

The ADSP-BF51x processors have multiple independent DMA channels that support automated data transfers with minimal overhead for the processor core. DMA transfers can occur between the processor's internal memories and any of its DMA-capable peripherals. Additionally, DMA transfers can be accomplished between any of the DMA-capable peripherals and external devices connected to the external memory interfaces, including the SDRAM controller and the asynchronous memory controller. DMA-capable peripherals include the Ethernet MAC, RSI, SPORTs, SPIs, UARTs, and PPI. Each individual DMA-capable peripheral has at least one dedicated DMA channel.

The processors' DMA controller supports both one-dimensional (1-D) and two-dimensional (2-D) DMA transfers. DMA transfer initialization can be implemented from registers or from sets of parameters called descriptor blocks.

The 2-D DMA capability supports arbitrary row and column sizes up to 64K elements by 64K elements, and arbitrary row and column step sizes up to ±32K elements. Furthermore, the column step size can be less than the row step size, allowing implementation of interleaved data streams. This feature is especially useful in video applications where data can be de-interleaved on the fly.

Examples of DMA types supported by the DMA controller include:

- A single, linear buffer that stops upon completion
- A circular, auto-refreshing buffer that interrupts on each full or fractionally full buffer
- 1-D or 2-D DMA using a linked list of descriptors
- 2-D DMA using an array of descriptors, specifying only the base DMA address within a common page

In addition to the dedicated peripheral DMA channels, there are two memory DMA channels that transfer data between the various memories of the processor system. This enables transfers of blocks of data between any of the memories—including external SDRAM, ROM, SRAM, and flash memory—with minimal processor intervention. Memory DMA transfers can be controlled by a very flexible descriptor-based methodology or by a standard register-based autobuffer mechanism.

The processors also have an external DMA controller capability via dual external DMA request signals when used in conjunction with the external bus interface unit (EBIU). This functionality can be used when a high speed interface is required for external FIFOs and high bandwidth communications peripherals. It allows control of the number of data transfers for memory DMA. The number of transfers per edge is programmable. This feature can be programmed to allow memory DMA to have an increased priority on the external bus relative to the core.

PROCESSOR PERIPHERALS

The ADSP-BF51x processors contain a rich set of peripherals connected to the core via several high bandwidth buses, providing flexibility in system configuration as well as excellent overall system performance (see Figure 2). The processors contain dedicated network communication modules and high speed serial and parallel ports, an interrupt controller for flexible management of interrupts from the on-chip peripherals or external sources, and power management control functions to tailor the performance and power characteristics of the processor and system to many application scenarios.

All of the peripherals, except for the general-purpose I/O, rotary counter, TWI, three-phase PWM, real-time clock, and timers, are supported by a flexible DMA structure. There are also separate memory DMA channels dedicated to data transfers between the processor's various memory spaces, including external SDRAM and asynchronous memory. Multiple on-chip buses provide enough bandwidth to keep the processor core running along with activity on all of the on-chip and external peripherals.

Real-Time Clock

The real-time clock (RTC) provides a robust set of digital watch features, including current time, stopwatch, and alarm. The RTC is clocked by a 32.768 kHz crystal external to the processors. The RTC peripheral has a dedicated power supply so that it can remain powered up and clocked even when the rest of the processor is in a low power state. The RTC provides several programmable interrupt options, including interrupt per second, minute, hour, or day clock ticks, interrupt on programmable stopwatch countdown, or interrupt at a programmed alarm time.

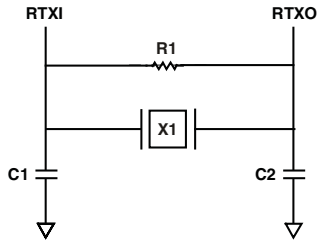
The 32.768 kHz input clock frequency is divided down to a 1 Hz signal by a prescaler. The counter function of the timer consists of four counters: a 60-second counter, a 60-minute counter, a 24-hour counter, and an 32,768-day counter.

When enabled, the alarm function generates an interrupt when the output of the timer matches the programmed value in the alarm control register. There are two alarms: The first alarm is for a time of day. The second alarm is for a day and time of that day.

The stopwatch function counts down from a programmed value, with one-second resolution. When the stopwatch is enabled and the counter underflows, an interrupt is generated.

Like the other peripherals, the RTC can wake up the processor from sleep mode upon generation of any RTC wakeup event. Additionally, an RTC wakeup event can wake up the processor from deep sleep mode or cause a transition from the hibernate state.

Connect RTC signals RTXI and RTXO with external components as shown in Figure 5.



SUGGESTED COMPONENTS:
X1 = ECLIPTEK EC38J (THROUGH-HOLE PACKAGE) OR
EPSON MC405 12 pF LOAD (SURFACE-MOUNT PACKAGE)
C1 = 22 pF
C2 = 22 pF
R1 = 10 MΩ
NOTE: C1 AND C2 ARE SPECIFIC TO CRYSTAL SPECIFIED FOR X1. CONTACT CRYSTAL MANUFACTURER FOR DETAILS. C1 AND C2 SPECIFICATIONS ASSUME BOARD TRACE CAPACITANCE OF 3 pF.

Figure 5. External Components for RTC

Watchdog Timer

The ADSP-BF51x processors include a 32-bit timer that can be used to implement a software watchdog function. A software watchdog can improve system availability by forcing the processor to a known state through generation of a hardware reset, nonmaskable interrupt (NMI), or general-purpose interrupt, if the timer expires before being reset by software. The programmer initializes the count value of the timer, enables the appropriate interrupt, then enables the timer. Thereafter, the software must reload the counter before it counts to zero from the programmed value. This protects the system from remaining in an unknown state where software, which would normally reset the timer, has stopped running due to an external noise condition or software error.

If configured to generate a hardware reset, the watchdog timer resets both the core and the processor peripherals. After a reset, software can determine if the watchdog was the source of the hardware reset by interrogating a status bit in the watchdog timer control register.

The timer is clocked by the system clock (SCLK) at a maximum frequency of f_{SCLK}.

Timers

There are nine general-purpose programmable timer units in the ADSP-BF51x processors. Eight timers have an external signal that can be configured either as a pulse width modulator (PWM) or timer output, as an input to clock the timer, or as a mechanism for measuring pulse widths and periods of external events. These timers can be synchronized to an external clock input to the several other associated PF signals, an external clock input to the PPI_CLK input signal, or to the internal SCLK.

The timer units can be used in conjunction with the two UARTs to measure the width of the pulses in the data stream to provide a software auto-baud detect function for the respective serial channels.

The timers can generate interrupts to the processor core providing periodic events for synchronization, either to the system clock or to a count of external signals.

In addition to the eight general-purpose programmable timers, a ninth timer is also provided. This extra timer is clocked by the internal processor clock and is typically used as a system tick clock for generation of operating system periodic interrupts.

3-Phase PWM

The processors integrate a flexible and programmable 3-phase PWM waveform generator that can be programmed to generate the required switching patterns to drive a 3-phase voltage source inverter for ac induction (ACIM) or permanent magnet synchronous (PMSM) motor control. In addition, the PWM block contains special functions that considerably simplify the generation of the required PWM switching patterns for control of the electronically commutated motor (ECM) or brushless dc motor (BDCM). Software can enable a special mode for switched reluctance motors (SRM).

Features of the 3-phase PWM generation unit are:

- 16-bit center-based PWM generation unit
- Programmable PWM pulse width
- Single/double update modes
- Programmable dead time and switching frequency
- Twos-complement implementation which permits smooth transition to full ON and full OFF states
- Possibility to synchronize the PWM generation to an external synchronization
- Special provisions for BDCM operation (crossover and output enable functions)
- Wide variety of special switched reluctance (SR) operating modes
- Output polarity and clock gating control
- Dedicated asynchronous PWM shutdown signal

General-Purpose (GP) Counter

A 32-bit GP counter is provided that can sense 2-bit quadrature or binary codes as typically emitted by industrial drives or manual thumb wheels. The counter can also operate in

general-purpose up/down count modes. Then, count direction is either controlled by a level-sensitive input signal or by two edge detectors.

A third input can provide flexible zero marker support and can alternatively be used to input the push-button signal of thumb wheels. All three signals have a programmable debouncing circuit.

An internal signal forwarded to the GP timer unit enables one timer to measure the intervals between count events. Boundary registers enable auto-zero operation or simple system warning by interrupts when programmable count values are exceeded.

Serial Ports

The ADSP-BF51x processors incorporate two dual-channel synchronous serial ports (SPORT0 and SPORT1) for serial and multiprocessor communications. The SPORTs support the following features:

Serial port data can be automatically transferred to and from on-chip memory/external memory via dedicated DMA channels. Each of the serial ports can work in conjunction with another serial port to provide TDM support. In this configuration, one SPORT provides two transmit signals while the other SPORT provides the two receive signals. The frame sync and clock are shared.

Serial ports operate in five modes:

- Standard DSP serial mode
- Multichannel (TDM) mode
- I^2S mode
- Packed I^2S mode
- Left-justified mode

Serial Peripheral Interface (SPI) Ports

The processors have two SPI-compatible ports (SPI0 and SPI1) that enable the processor to communicate with multiple SPI-compatible devices.

The SPI interface uses three signals for transferring data: two data signals (master output-slave input–MOSI, and master input-slave output–MISO) and a clock signal (serial clock–SCK). An SPI chip select input signal ($\overline{\text{SPIxSS}}$) lets other SPI devices select the processor, and multiple SPI chip select output signals let the processor select other SPI devices. The SPI select signals are reconfigured general-purpose I/O signals. Using these signals, the SPI port provides a full-duplex, synchronous serial interface, which supports both master/slave modes and multimaster environments.

The SPI port baud rate and clock phase/polarities are programmable, and it has an integrated DMA channel, configurable to support transmit or receive data streams. The SPI's DMA channel can only service unidirectional accesses at any given time.

UART Ports

The processors provide two full-duplex universal asynchronous receiver/transmitter (UART) ports, which are fully compatible with PC-standard UARTs. Each UART port provides a simplified UART interface to other peripherals or hosts, supporting full-duplex, DMA-supported, asynchronous transfers of serial data. A UART port includes support for five to eight data bits, and none, even, or odd parity. Optionally, an additional address bit can be transferred to interrupt only addressed nodes in multi-drop bus (MDB) systems. A frame is terminates by one, one and a half, two or two and a half stop bits.

The UART ports support automatic hardware flow control through the Clear To Send (CTS) input and Request To Send (RTS) output with programmable assertion FIFO levels.

To help support the Local Interconnect Network (LIN) protocols, a special command causes the transmitter to queue a break command of programmable bit length into the transmit buffer. Similarly, the number of stop bits can be extended by a programmable inter-frame space.

The capabilities of the UARTs are further extended with support for the Infrared Data Association (IrDA®) serial infrared physical layer link specification (SIR) protocol.

2-Wire Interface (TWI)

The processors include a TWI module for providing a simple exchange method of control data between multiple devices. The TWI is compatible with the widely used I^2C® bus standard. The TWI module offers the capabilities of simultaneous master and slave operation, support for both 7-bit addressing and multimedia data arbitration. The TWI interface utilizes two signals for transferring clock (SCL) and data (SDA) and supports the protocol at speeds up to 400k bits/sec. The TWI interface signals are compatible with 5 V logic levels.

Additionally, the processor's TWI module is fully compatible with serial camera control bus (SCCB) functionality for easier control of various CMOS camera sensor devices.

Removable Storage Interface (RSI)

The RSI controller, available on the ADSP-BF514/ADSP-BF514F16/ADSP-BF516/ADSP-BF518/ADSP-BF518F16 processors, acts as the host interface for multi-media cards (MMC), secure digital memory cards (SD Card), secure digital input/output cards (SDIO), and CE-ATA hard disk drives. The following list describes the main features of the RSI controller.

- Support for a single MMC, SD memory, SDIO card or CE-ATA hard disk drive
- Support for 1-bit and 4-bit SD modes
- Support for 1-bit, 4-bit and 8-bit MMC modes
- Support for 4-bit and 8-bit CE-ATA hard disk drives
- A ten-signal external interface with clock, command, and up to eight data lines
- Card detection using one of the data signals
- Card interface clock generation from SCLK
- SDIO interrupt and read wait features
- CE-ATA command completion signal recognition and disable

T_{NOM} is the duration running at $f_{CCLKNOM}$

T_{RED} is the duration running at $f_{CCLKRED}$

VOLTAGE REGULATION INTERFACE

The ADSP-BF51x processors require an external voltage regulator to power the V_{DDINT} domain. To reduce standby power consumption in the hibernate state, the external voltage regulator can be signaled through EXT_WAKE to remove power from the processor core. The EXT_WAKE signal is high-true for power-up and may be connected directly to the low-true shut down input of many common regulators.

The Power Good ($\overline{PG}$) input signal allows the processor to start only after the internal voltage has reached a chosen level. In this way, the startup time of the external regulator is detected after hibernation. For a complete description of the $\overline{PG}$ functionality, refer to the *ADSP-BF51x Blackfin Processor Hardware Reference*.

CLOCK SIGNALS

The ADSP-BF51x processors can be clocked by an external crystal, a sine wave input, or a buffered, shaped clock derived from an external clock oscillator.

If an external clock is used, it should be a TTL compatible signal and must not be halted, changed, or operated below the specified frequency during normal operation. This signal is connected to the processor CLKIN signal. When an external clock is used, the XTAL pin/ball must be left unconnected.

Alternatively, because the processor includes an on-chip oscillator circuit, an external crystal may be used. For fundamental frequency operation, use the circuit shown in Figure 6. A parallel-resonant, fundamental frequency, microprocessor-grade crystal is connected across the CLKIN and XTAL pins/balls. The on-chip resistance between the CLKIN pin/ball and the XTAL pin/ball is in the 500 kΩ range. Further parallel resistors are typically not recommended. The two capacitors and the series resistor shown in Figure 6 fine tune phase and amplitude of the sine frequency.

The capacitor and resistor values shown in Figure 6 are typical values only. The capacitor values are dependent upon the crystal manufacturers' load capacitance recommendations and the PCB physical layout. The resistor value depends on the drive level specified by the crystal manufacturer. The user should verify the customized values based on careful investigations on multiple devices over temperature range.

A third-overtone crystal can be used for frequencies above 25 MHz. The circuit is then modified to ensure crystal operation only at the third overtone, by adding a tuned inductor circuit as shown in Figure 6. A design procedure for third-overtone operation is discussed in detail in application note *(EE-168) Using Third Overtone Crystals with the ADSP-218x DSP* on the Analog Devices website (www.analog.com)—use site search on "EE-168."

The CLKBUF signal is an output signal, which is a buffered version of the input clock. This signal is particularly useful in Ethernet applications to limit the number of required clock sources in the system. In this type of application, a single

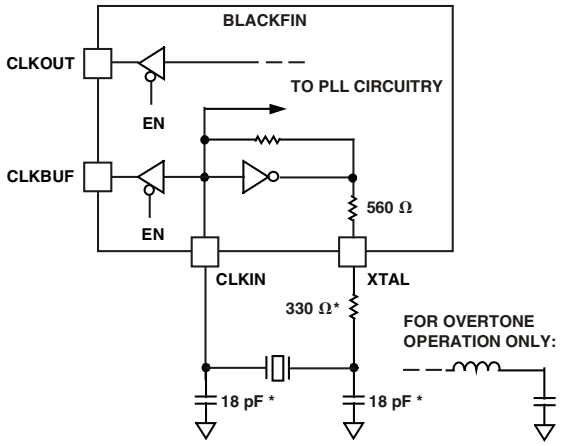


Figure 6. External Crystal Connections

25 MHz or 50 MHz crystal may be applied directly to the processor. The 25 MHz or 50 MHz output of CLKBUF can then be connected to an external Ethernet MII or RMII PHY device.

The Blackfin core runs at a different clock rate than the on-chip peripherals. As shown in Figure 7, the core clock (CCLK) and system peripheral clock (SCLK) are derived from the input clock (CLKIN) signal. An on-chip PLL is capable of multiplying the CLKIN signal by a programmable 5× to 64× multiplication factor (bounded by specified minimum and maximum VCO frequencies). The default multiplier is 6×, but it can be modified by a software instruction sequence.

On-the-fly frequency changes can be done simply by writing to the PLL_DIV register. The maximum allowed CCLK and SCLK rates depend on the applied voltages V_{DDINT}, V_{DDEXT}, and V_{DDMEM}, and the VCO is always permitted to run up to the frequency specified by the part's speed grade. The CLKOUT signal reflects the SCLK frequency to the off-chip world. It belongs to the SDRAM interface, but it functions as a reference signal in other timing specifications as well. While active by default, it can be disabled using the EBIU_SDGCTL and EBIU_AMGCTL registers.

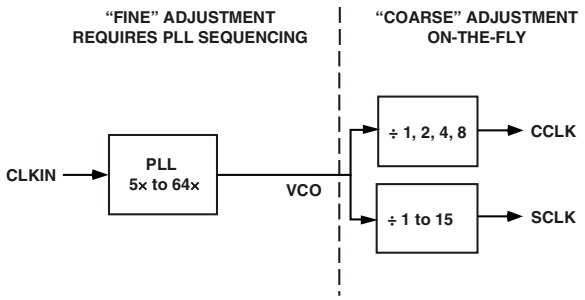


Figure 7. Frequency Modification Methods

All on-chip peripherals are clocked by the system clock (SCLK). The system clock frequency is programmable by means of the SSEL3–0 bits of the PLL_DIV register. The values programmed into the SSEL fields define a divide ratio between the PLL output (VCO) and the system clock. SCLK divider values are 1 through 15. Table 5 illustrates typical system clock ratios.

Table 5. Example System Clock Ratios

Signal Name SSEL3–0	Divider Ratio VCO/SCLK	Example Frequency Ratios (MHz)	
		VCO	SCLK
0010	2:1	100	50
0110	6:1	300	50
1010	10:1	400	40

Note that the divisor ratio must be chosen to limit the system clock frequency to its maximum of f_{SCLK}. The SSEL value can be changed dynamically without any PLL lock latencies by writing the appropriate values to the PLL divisor register (PLL_DIV).

The core clock (CCLK) frequency can also be dynamically changed by means of the CSEL1–0 bits of the PLL_DIV register. Supported CCLK divider ratios are 1, 2, 4, and 8, as shown in Table 6. This programmable core clock capability is useful for fast core frequency modifications.

Table 6. Core Clock Ratios

Signal Name CSEL1–0	Divider Ratio VCO/CCLK	Example Frequency Ratios (MHz)	
		VCO	CCLK
00	1:1	300	300
01	2:1	300	150
10	4:1	400	100
11	8:1	200	25

The maximum CCLK frequency not only depends on the part's speed grade (see Page 67), it also depends on the applied V_{DDINT} voltage. See Table 10 on Page 23 for details. The maximal system clock rate (SCLK) depends on the chip package and the applied V_{DDINT}, V_{DDEXT}, and V_{DDMEM} voltages (see Table 12 on Page 23).

BOOTING MODES

The processor has several mechanisms (listed in Table 7) for automatically loading internal and external memory after a reset. The boot mode is defined by three BMODE input bits dedicated to this purpose. There are two categories of boot modes. In master boot modes the processor actively loads data from parallel or serial memories. In slave boot modes the processor receives data from external host devices.

The boot modes listed in Table 7 provide a number of mechanisms for automatically loading the processor's internal and external memories after a reset. By default, all boot modes use the slowest meaningful configuration settings. Default settings can be altered via the initialization code feature at boot time or by proper OTP programming at pre-boot time. The BMODE bits of the reset configuration register, sampled during power-on resets and software-initiated resets, implement the modes shown in Table 7.

Table 7. Booting Modes

BMODE2–0	Description
000	Idle - No boot
001	Boot from 8- or 16-bit external flash memory
010	Boot from internal SPI memory
011	Boot from external SPI memory (EEPROM or flash)
100	Boot from SPI0 host
101	Boot from OTP memory
110	Boot from SDRAM
111	Boot from UART0 Host

- Idle/no boot mode (BMODE = 0x0)—In this mode, the processor goes into idle. The idle boot mode helps recover from illegal operating modes, such as when the user has mis configured the OTP memory.
- Boot from 8-bit or 16-bit external flash memory (BMODE = 0x1)—In this mode, the boot kernel loads the first block header from address 0x2000 0000 and—depending on instructions containing in the header—the boot kernel performs 8-bit or 16-bit boot or starts program execution at the address provided by the header. By default, all configuration settings are set for the slowest device possible (3-cycle hold time, 15-cycle R/W access times, 4-cycle setup).

  The ARDY is not enabled by default, but it can be enabled by OTP programming. Similarly, all interface behavior and timings can be customized by OTP programming. This includes activation of burst-mode or page-mode operation. In this mode, all signals belonging to the asynchronous interface are enabled at the port muxing level.
- Boot from internal SPI memory (BMODE = 0x2)—The processor uses the internal PH8 GPIO signal to load code previously loaded to the 16M bit internal SPI flash connected to SPI0. Only available on the ADSP-BF51xF processors.
- Boot from external SPI EEPROM or flash (BMODE = 0x3)—8-bit, 16-bit, 24-bit or 32-bit addressable devices are supported. The processor uses the PG15 GPIO signal (at $\overline{\text{SPI0SEL2}}$) to select a single SPI EEPROM/flash device connected to the SPI0 interface; then submits a read command and successive address bytes (0x00) until a valid 8-, 16-, 24-, or 32-bit addressable device is detected. Pull-up resistors are required on the SSEL and MISO signals. By default, a value of 0x85 is written to the SPI0_BAUD register.

SPECIFICATIONS

Note that component specifications are subject to change without notice.

OPERATING CONDITIONS

Parameter		Conditions	Min	Nominal	Max	Unit
V_{DDINT}	Internal Supply Voltage	Industrial Models	1.14		1.47	V
	Internal Supply Voltage	Commercial Models	1.10		1.47	V
	Internal Supply Voltage	Automotive Models	1.33		1.47	V
V_{DDEXT}[1, 2]	External Supply Voltage	1.8 V I/O, Nonautomotive Models	1.7	1.8	1.9	V
	External Supply Voltage	2.5 V I/O, Nonautomotive Models	2.25	2.5	2.75	V
	External Supply Voltage	3.3 V I/O, All Models	3.0	3.3	3.6	V
V_{DDMEM}[3]	MEM Supply Voltage	1.8 V I/O, Nonautomotive Models	1.7	1.8	1.9	V
	MEM Supply Voltage	2.5 V I/O, Nonautomotive Models	2.25	2.5	2.75	V
	MEM Supply Voltage	3.3 V I/O, All Models	3.0	3.3	3.6	V
V_{DDRTC}[4]	RTC Power Supply Voltage		2.25		3.6	V
$V_{DDFLASH}$[4]	Internal SPI Flash Supply Voltage		2.7	3.3	3.6	V
V_{DDOTP}[1]	OTP Supply Voltage		2.25	2.5	2.75	V
V_{PPOTP}	OTP Programming Voltage					
	For Reads[1]		2.25	2.5	2.75	V
	For Writes[5]		6.9	7.0	7.1	V
V_{IH}	High Level Input Voltage[6, 7]	V_{DDEXT}/V_{DDMEM} = 1.90 V	1.2			V
	High Level Input Voltage[6, 8]	V_{DDEXT}/V_{DDMEM} = 2.75 V	1.7			V
	High Level Input Voltage[6, 8]	V_{DDEXT}/V_{DDMEM} = 3.6 V	2			V
V_{IHTWI}	High Level Input Voltage	V_{DDEXT} = 1.90 V/2.75 V/3.6 V	0.7 × V_{BUSTWI}		V_{BUSTWI}[9]	V
V_{IL}	Low Level Input Voltage[6, 7]	V_{DDEXT}/V_{DDMEM} = 1.7 V			0.6	V
	Low Level Input Voltage[6, 8]	V_{DDEXT}/V_{DDMEM} = 2.25 V			0.7	V
	Low Level Input Voltage[6, 8]	V_{DDEXT}/V_{DDMEM} = 3.0 V			0.8	V
V_{ILTWI}	Low Level Input Voltage	V_{DDEXT} = Minimum			0.3 × V_{BUSTWI}[10]	V
	Junction Temperature	168-Ball CSP_BGA @ $T_{AMBIENT}$ = 0°C to +70°C	0		+95	°C
	Junction Temperature	168-Ball CSP_BGA @ $T_{AMBIENT}$ = –40°C to +85°C	–40		+105	°C
	Junction Temperature	176-Lead LQFP_EP @ $T_{AMBIENT}$ = 0°C to +70°C	0		+95	°C
	Junction Temperature	176-Lead LQFP_EP @ $T_{AMBIENT}$ = –40°C to +85°C	–40		+105	°C

[1] Must remain powered (even if the associated function is not used).

[2] V_{DDEXT} is the supply to the GPIO.

[3] Pins/balls that use V_{DDMEM} are DATA15–0, ADDR19–1, $\overline{ABE1–0}$, $\overline{ARE}$, $\overline{AWE}$, $\overline{AMS1–0}$, SA10, $\overline{SWE}$, $\overline{SCAS}$, CLKOUT, $\overline{SRAS}$, $\overline{SMS}$, SCKE. These pins/balls are not tolerant to voltages higher than V_{DDMEM}. When using any of the asynchronous memory signals $\overline{AMS3–2}$, ARDY, or $\overline{AOE}$ V_{DDMEM} and V_{DDEXT} must be shorted externally.

[4] If not used, power with V_{DDEXT}.

[5] The V_{PPOTP} voltage for writes must only be applied when programming OTP memory. There is a finite amount of cumulative time that this voltage may be applied (dependent on voltage and junction temperature) over the lifetime of the part.

[6] Parameter value applies to all input and bidirectional pins/balls except SDA and SCL.

[7] Bidirectional balls (PF15–0, PG15–0, PH15–0) and input balls (RTXI, TCK, TDI, TMS, $\overline{TRST}$, CLKIN, $\overline{RESET}$, $\overline{NMI}$, and BMODE3–0) of the ADSP-BF51x processors are 2.5 V tolerant (always accept up to 2.7 V maximum V_{IH}). Voltage compliance (on outputs, V_{OH}) is limited by the V_{DDEXT} supply voltage.

[8] Bidirectional pins/balls (PF15–0, PG15–0, PH7–0) and input pins/balls (RTXI, TCK, TDI, TMS, $\overline{TRST}$, CLKIN, $\overline{RESET}$, $\overline{NMI}$, and BMODE2–0) of the ADSP-BF51x are 3.3 V tolerant (always accept up to 3.6 V maximum V_{IH}). Voltage compliance (on outputs, V_{OH}) is limited by the V_{DDEXT} supply voltage.

[9] The V_{IHTWI} min and max value vary with the selection in the TWI_DT field of the NONGPIO_DRIVE register. See V_{BUSTWI} min and max values in Table 9.

[10] SDA and SCL are pulled up to V_{BUSTWI}. See Table 9.

ABSOLUTE MAXIMUM RATINGS

Stresses greater than those listed in Table 18 may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 18. Absolute Maximum Ratings

Parameter	Rating
Internal Supply Voltage (V_{DDINT})	–0.3 V to +1.50 V
External (I/O) Supply Voltage (V_{DDEXT}/V_{DDMEM})	–0.3 V to +3.8 V
Input Voltage[1, 2]	–0.5 V to +3.6 V
Input Voltage[1, 3]	–0.5 V to +5.5 V
Output Voltage Swing	–0.5 V to V_{DDEXT}/V_{DDMEM} + 0.5 V
I_{OH}/I_{OL} Current per Pin Group[4]	80 mA (max)
Storage Temperature Range	–65°C to +150°C
Junction Temperature While biased	+110°C

[1] Applies to 100% transient duty cycle. For other duty cycles see Table 19.
[2] Applies only when V_{DDEXT} is within specifications. When V_{DDEXT} is outside specifications, the range is V_{DDEXT} ± 0.2.
[3] Applies to signals SCL, SDA.
[4] For more information, see the information preceding Table 21 and Table 22.

Table 19. Maximum Duty Cycle for Input Transient Voltage[1]

V_{IN} Min (V)[2]	V_{IN} Max (V)[2]	Maximum Duty Cycle[3]
–0.50	+3.80	100%
–0.70	+4.00	40%
–0.80	+4.10	25%
–0.90	+4.20	15%
–1.00	+4.30	10%

[1] Applies to all signal pins/balls with the exception of CLKIN, XTAL.
[2] The individual values cannot be combined for analysis of a single instance of overshoot or undershoot. The worst case observed value must fall within one of the voltages specified and the total duration of the overshoot or undershoot (exceeding the 100% case) must be less than or equal to the corresponding duty cycle.
[3] Duty cycle refers to the percentage of time the signal exceeds the value for the 100% case. It is equivalent to the measured duration of a single instance of overshoot or undershoot as a percentage of the period of occurrence.

When programming OTP memory on the ADSP-BF51x processor, the V_{PPOTP} pin/ball must be set to the write value specified in the Operating Conditions on Page 22. There is a finite amount of cumulative time that the write voltage may be applied (dependent on voltage and junction temperature) to V_{PPOTP} over the lifetime of the part. Therefore, maximum OTP memory programming time for the processor is shown in Table 20.

Table 20. Maximum OTP Memory Programming Time

VPPOTP Voltage (V)	Temperature		
	25°C	85°C	110°C
6.9	6000 sec	100 sec	25 sec
7.0	2400 sec	44 sec	12 sec
7.1	1000 sec	18 sec	4.5 sec

Table 21 and Table 22 specify the maximum total source/sink (I_{OH}/I_{OL}) current for a group of pins. Permanent damage can occur if this value is exceeded. To understand this specification, if pins PF9, PF8, PF7, PF6, and PF5 from Group 1 in Table 22 table were sourcing or sinking 2 mA each, the total current for those pins would be 10 mA. This would allow up to 70 mA total that could be sourced or sunk by the remaining pins in the group without damaging the device. Note that the V_{OH} and V_{OL} specifications have separate per-pin maximum current requirements as shown in the Electrical Characteristics table.

Table 21. Total Current Pin Groups–V_{DDMEM} Groups

Group	Pins in Group
1	DATA15, DATA14, DATA13, DATA12, DATA11, DATA10
2	DATA9, DATA8, DATA7, DATA6, DATA5, DATA4
3	DATA3, DATA2, DATA1, DATA0, ADDR19, ADDR18
4	ADDR17, ADDR16, ADDR15, ADDR14, ADDR13
5	ADDR12, ADDR11, ADDR10, ADDR9, ADDR8, ADDR7
6	ADDR6, ADDR5, ADDR4, ADDR3, ADDR2, ADDR1
7	$\overline{ABE1}$, $\overline{ABE0}$, SA10, $\overline{SWE}$, $\overline{SCAS}$, $\overline{SRAS}$
8	$\overline{SMS}$, SCKE, $\overline{AMS1}$, $\overline{ARE}$, $\overline{AWE}$, $\overline{AMS0}$, CLKOUT

Table 22. Total Current Pin Groups–V_{DDEXT} Groups

Group	Pins in Group
1	PF9, PF8, PF7, PF6, PF5, PF4, PF3, PF2
2	PF1, PF0, PG15, PG14, PG13, PG12, PG11, PG10
3	PG9, PG8, PG7, PG6, PG5, PG4, PG3, PG2, BMODE0, BMODE1, BMODE2
4	PG1, PG0, TDO, $\overline{EMU}$, TDI, TCK, $\overline{TRST}$, TMS
5	$\overline{RESET}$, $\overline{NMI}$, CLKBUF
6	PH7, PH6, PH5, PH4, PH3, PH2, PH1, PH0
7	PF15, PF14, PF13, PF12, PF11, SDA, SCL, PF10

TIMING SPECIFICATIONS

Clock and Reset Timing

Table 24 and Figure 9 describe clock and reset operations. Per the CCLK and SCLK timing specifications in Table 10, Table 11, and Table 12 on Page 23, combinations of CLKIN and clock multipliers must not select core/peripheral clocks in excess of the processor's speed grade.

Table 24. Clock and Reset Timing

Parameter		Min	Max	Unit
Timing Requirements				
f_{CKIN}	CLKIN Frequency (Commercial/Industrial Models[1, 2, 3, 4]	12	50	MHz
f_{CKIN}	CLKIN Frequency (Automotive Models)[1, 2, 3, 4]	14	50	MHz
t_{CKINL}	CLKIN Low Pulse[1]	10		ns
t_{CKINH}	CLKIN High Pulse[1]	10		ns
t_{WRST}	$\overline{\text{RESET}}$ Asserted Pulse Width Low[5]	11 × t_{CKIN}		ns
Switching Characteristic				
$t_{BUFDLAY}$	CLKIN to CLKBUF Delay		11	ns

[1] Applies to PLL bypass mode and PLL nonbypass mode.
[2] Combinations of the CLKIN frequency and the PLL clock multiplier must not exceed the allowed f_{VCO}, f_{CCLK}, and f_{SCLK} settings discussed in Table 10 through Table 12 on Page 23.
[3] The t_{CKIN} period (see Figure 9) equals $1/f_{CKIN}$.
[4] If the DF bit in the PLL_CTL register is set, the minimum f_{CKIN} specification is 24 MHz for commercial/industrial models and 28 MHz for automotive models.
[5] Applies after power-up sequence is complete. See Table 25 and Figure 10 for power-up reset timing.

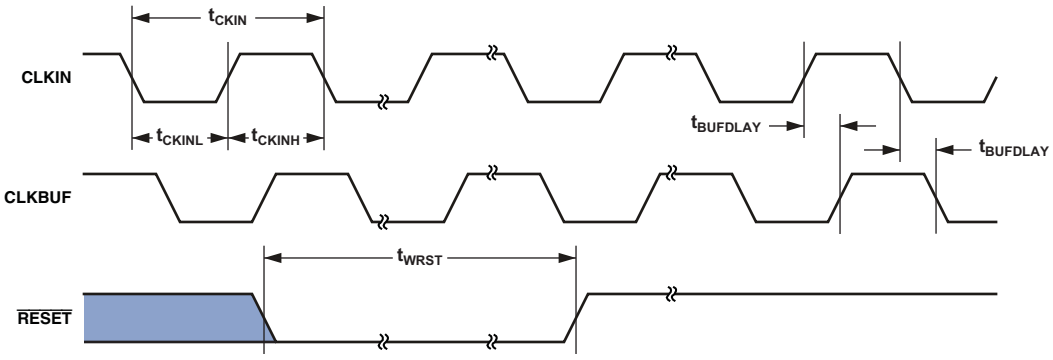


Figure 9. Clock and Reset Timing

External DMA Request Timing

Table 29 and Figure 14 describe the External DMA Request operations.

Table 29. External DMA Request Timing[1]

Parameter		V_{DDMEM}/V_{DDEXT} 1.8 V Nominal		V_{DDMEM}/V_{DDEXT} 2.5 V/3.3 V Nominal		Unit
		Min	Max	Min	Max	
Timing Requirements						
t_{DS}	DMARx Asserted to CLKOUT High Setup	9		7.2		ns
t_{DH}	CLKOUT High to DMARx Deasserted Hold Time	0		0		ns
$t_{DMARACT}$	DMARx Active Pulse Width	$t_{SCLK} + 1$		$t_{SCLK} + 1$		ns
$t_{DMARINACT}$	DMARx Inactive Pulse Width	$1.75 \times t_{SCLK}$		$1.75 \times t_{SCLK}$		ns

[1] Because the external DMA control pins are part of the V_{DDEXT} power domain and the CLKOUT signal is part of the V_{DDMEM} power domain, systems in which V_{DDEXT} and V_{DDMEM} are NOT equal may require level shifting logic for correct operation.

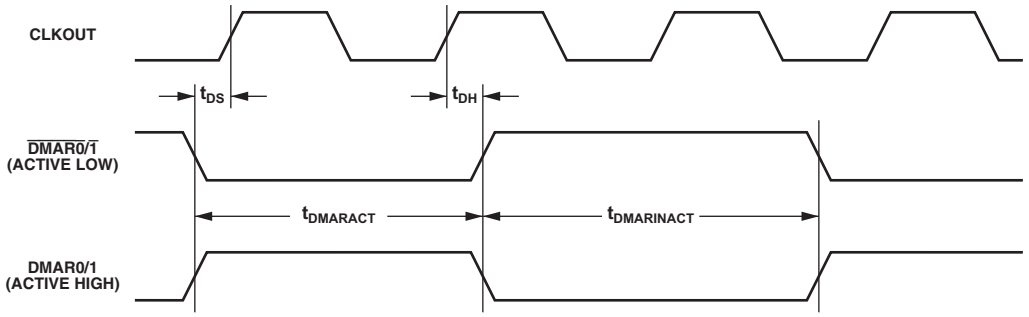


Figure 14. External DMA Request Timing

Parallel Peripheral Interface Timing

Table 30 and Figure 16 on Page 35, Figure 22 on Page 40, and Figure 25 on Page 42 describe parallel peripheral interface operations.

Table 30. Parallel Peripheral Interface Timing

Parameter		V_{DDEXT} 1.8 V Nominal Min	V_{DDEXT} 1.8 V Nominal Max	V_{DDEXT} 2.5 V/3.3 V Nominal Min	V_{DDEXT} 2.5 V/3.3 V Nominal Max	Unit
Timing Requirements						
t_{PCLKW}	PPI_CLK Width	$t_{SCLK} - 1.5$		$t_{SCLK} - 1.5$		ns
t_{PCLK}	PPI_CLK Period	$2 \times t_{SCLK} - 1.5$		$2 \times t_{SCLK} - 1.5$		ns
Timing Requirements - GP Input and Frame Capture Modes						
t_{PSUD}	External Frame Sync Startup Delay[1]	$4 \times t_{PCLK}$		$4 \times t_{PCLK}$		ns
t_{SFSPE}	External Frame Sync Setup Before PPI_CLK (Nonsampling Edge for Rx, Sampling Edge for Tx)	6.7		6.7		ns
t_{HFSPE}	External Frame Sync Hold After PPI_CLK	1.75		1.75		ns
t_{SDRPE}	Receive Data Setup Before PPI_CLK	4.1		3.5		ns
t_{HDRPE}	Receive Data Hold After PPI_CLK	2		1.6		ns
Switching Characteristics - GP Output and Frame Capture Modes						
t_{DFSPE}	Internal Frame Sync Delay After PPI_CLK		8		8	ns
t_{HOFSPE}	Internal Frame Sync Hold After PPI_CLK	1.7		1.7		ns
t_{DDTPE}	Transmit Data Delay After PPI_CLK		8.2		8	ns
t_{HDTPE}	Transmit Data Hold After PPI_CLK	2.3		1.9		ns

[1] The PPI port is fully enabled 4 PPI clock cycles after the PAB write to the PPI port enable bit. Only after the PPI port is fully enabled are external frame syncs and data words guaranteed to be received correctly by the PPI peripheral.

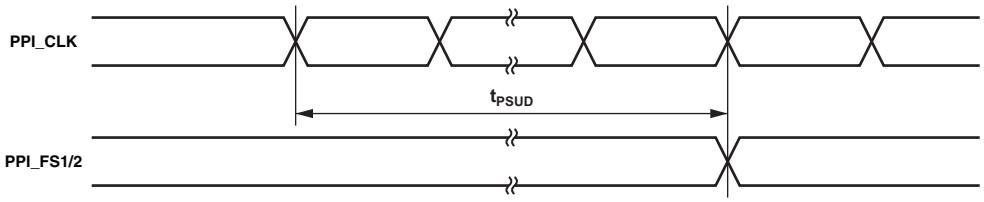


Figure 15. PPI with External Frame Sync Timing

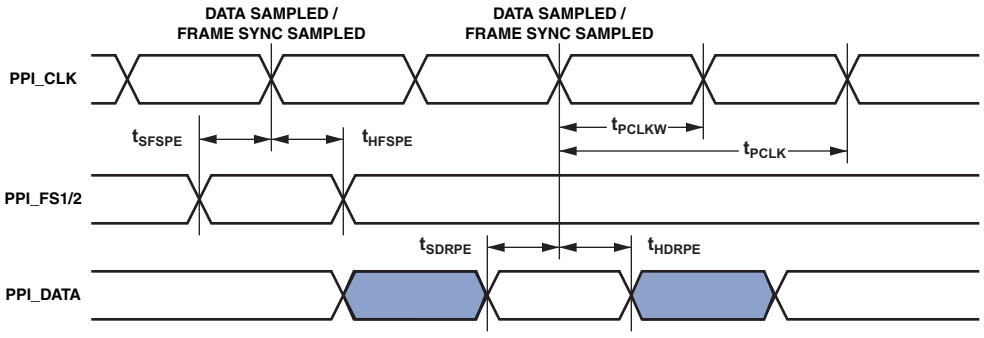


Figure 16. PPI GP Rx Mode with External Frame Sync Timing

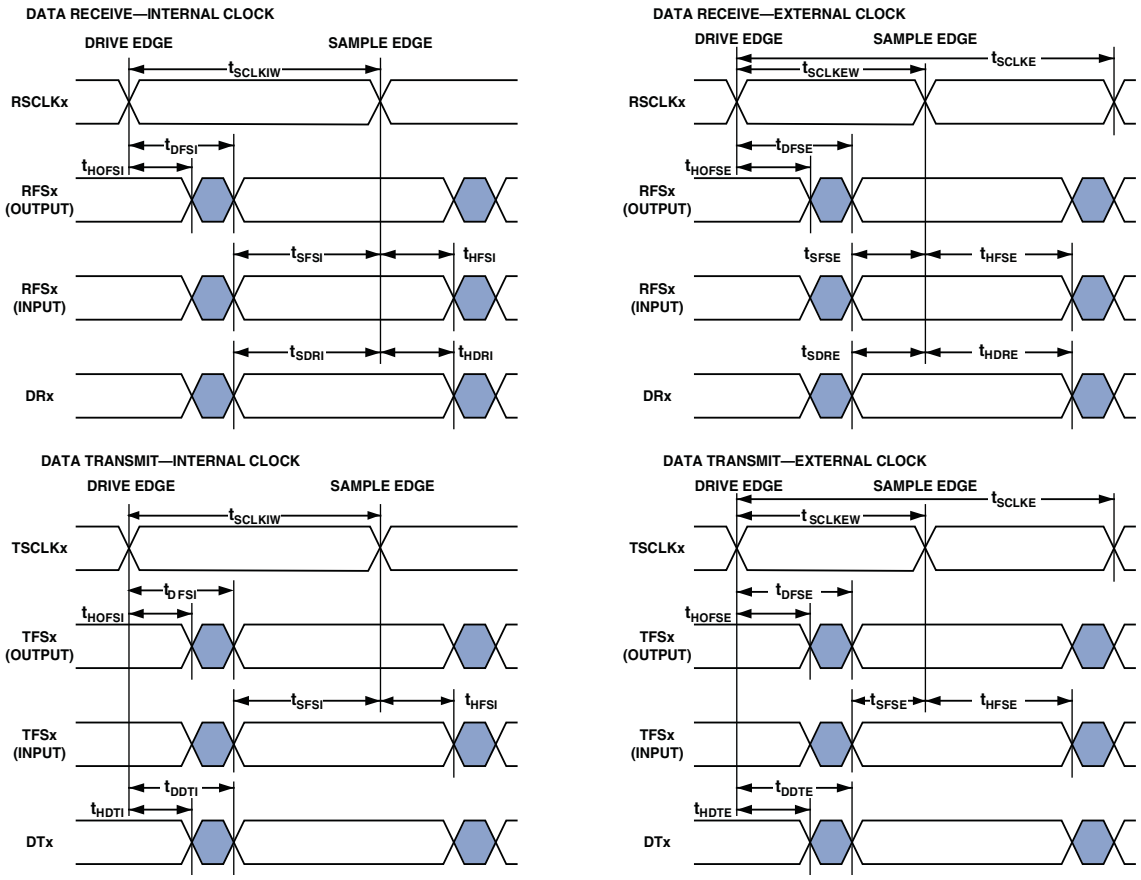


Figure 22. Serial Ports

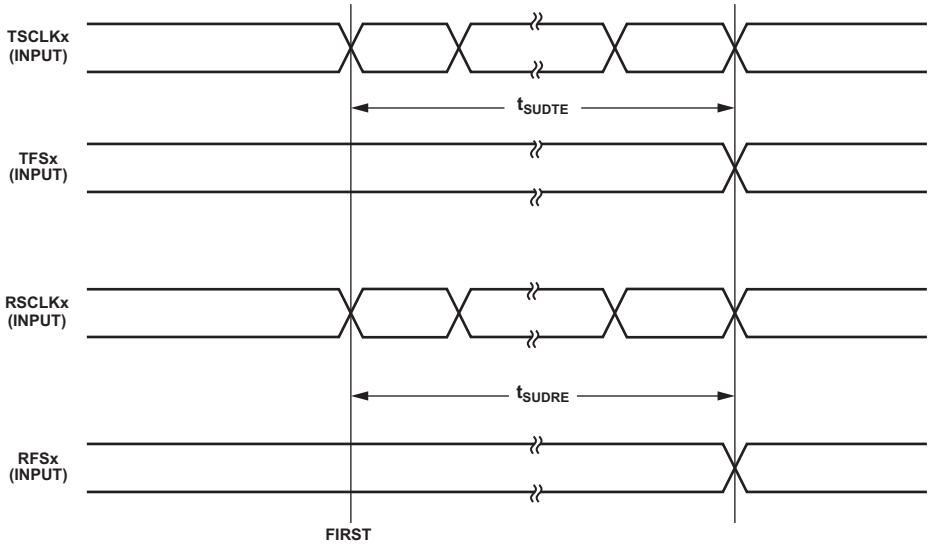


Figure 23. Serial Port Start Up with External Clock and Frame Sync

Table 36. External Late Frame Sync

Parameter		V_{DDEXT} 1.8 V Nominal Min	V_{DDEXT} 1.8 V Nominal Max	V_{DDEXT} 2.5 V/3.3 V Nominal Min	V_{DDEXT} 2.5 V/3.3 V Nominal Max	Unit
Switching Characteristics						
$t_{DDTLFSE}$[1, 2]	Data Delay from Late External TFSx or External RFSx with MCE = 1, MFD = 0		12		10	ns
$t_{DTENLFSE}$[1, 2]	Data Enable from Late FS or MCE = 1, MFD = 0	0		0		ns

[1] MCE = 1, TFSx enable and TFSx valid follow $t_{DDTENFS}$ and $t_{DDTLFSE}$.
[2] If external RFSx/TFSx setup to RSCLKx/TSCLKx > $t_{SCLKE}/2$ then $t_{DDTTE/I}$ and $t_{DTENE/I}$ apply, otherwise $t_{DDTLFSE}$ and $t_{DTENLFS}$ apply.

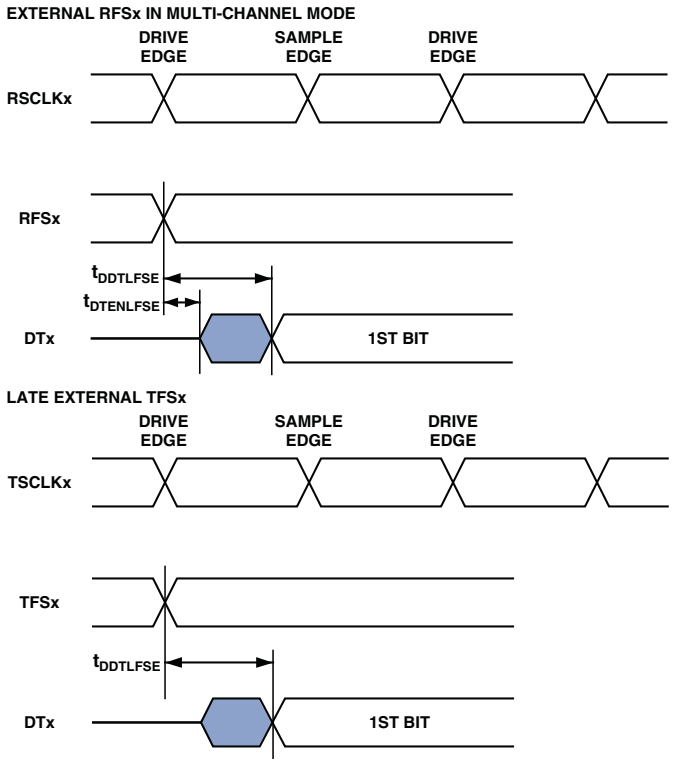


Figure 25. External Late Frame Sync

Table 47. 10/100 Ethernet MAC Controller Timing: MII/RMII Asynchronous Signal

Parameter		Min	Max	Unit
Timing Requirements				
t_{ECOLH}	COL Pulse Width High[1]	$t_{ETxCLK} \times 1.5$		ns
		$t_{ERxCLK} \times 1.5$		ns
t_{ECOLL}	COL Pulse Width Low[1]	$t_{ETxCLK} \times 1.5$		ns
		$t_{ERxCLK} \times 1.5$		ns
t_{ECRSH}	CRS Pulse Width High[2]	$t_{ETxCLK} \times 1.5$		ns
t_{ECRSL}	CRS Pulse Width Low[2]	$t_{ETxCLK} \times 1.5$		ns

[1] MII/RMII asynchronous signals are COL, CRS. These signals are applicable in both MII and RMII modes. The asynchronous COL input is synchronized separately to both the ETxCLK and the ERxCLK, and must have a minimum pulse width high or low at least 1.5 times the period of the slower of the two clocks.
[2] The asynchronous CRS input is synchronized to the ETxCLK, and must have a minimum pulse width high or low at least 1.5 times the period of ETxCLK.

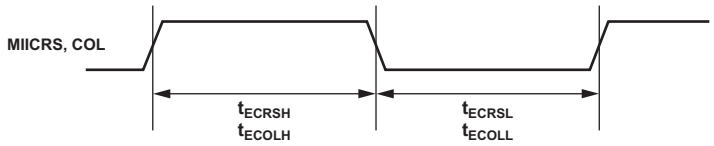


Figure 36. 10/100 Ethernet MAC Controller Timing: Asynchronous Signal

Table 48. 10/100 Ethernet MAC Controller Timing: MII Station Management

Parameter[1]		Min	Max	Unit
Timing Requirements				
t_{MDIOS}	MDIO Input Valid to MDC Rising Edge (Setup)	11.5		ns
t_{MDCIH}	MDC Rising Edge to MDIO Input Invalid (Hold)	0		ns
Switching Characteristics				
t_{MDCOV}	MDC Falling Edge to MDIO Output Valid		25	ns
t_{MDCOH}	MDC Falling Edge to MDIO Output Invalid (Hold)	–1.25		ns

[1] MDC/MDIO is a 2-wire serial bidirectional port for controlling one or more external PHYs. MDC is an output clock whose minimum period is programmable as a multiple of the system clock SCLK. MDIO is a bidirectional data line.

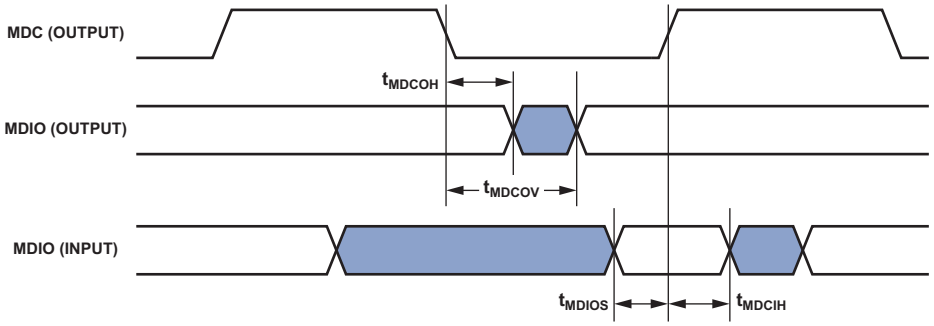


Figure 37. 10/100 Ethernet MAC Controller Timing: MII Station Management

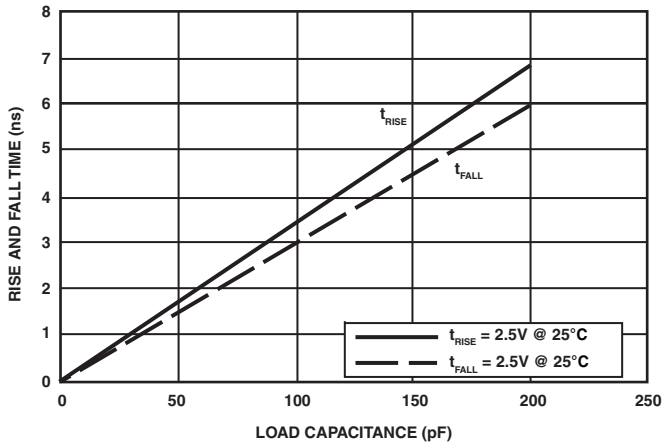


Figure 58. Driver Type A Typical Rise and Fall Times (10%–90%) vs. Load Capacitance (2.5V V_{DDEXT}/V_{DDMEM})

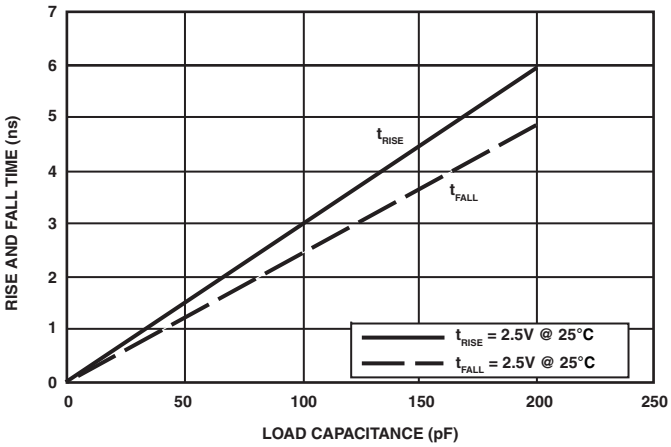


Figure 61. Driver Type B Typical Rise and Fall Times (10%–90%) vs. Load Capacitance (2.5V V_{DDEXT}/V_{DDMEM})

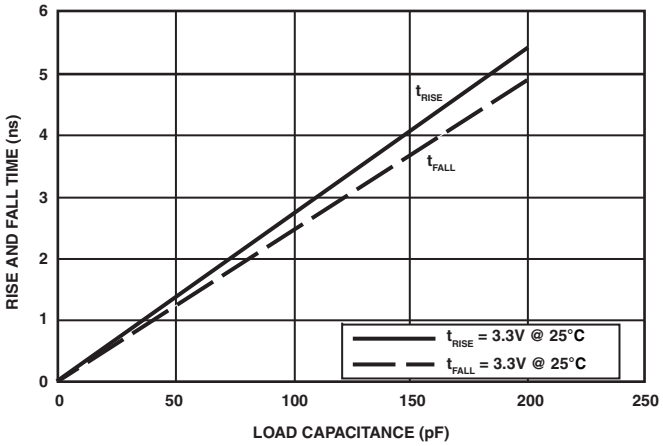


Figure 59. Driver Type A Typical Rise and Fall Times (10%–90%) vs. Load Capacitance (3.3V V_{DDEXT}/V_{DDMEM})

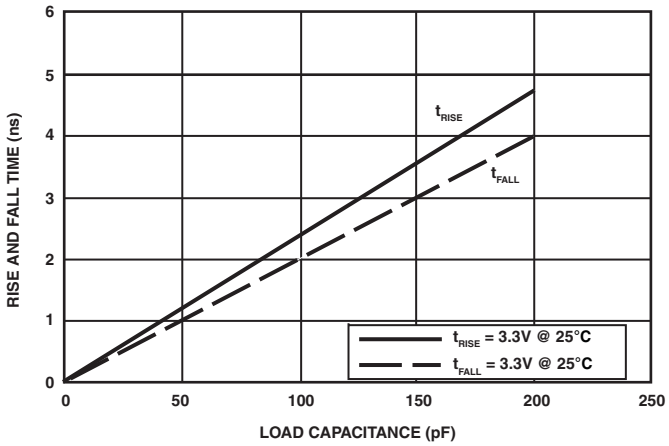


Figure 62. Driver Type B Typical Rise and Fall Times (10%–90%) vs. Load Capacitance (3.3V V_{DDEXT}/V_{DDMEM})

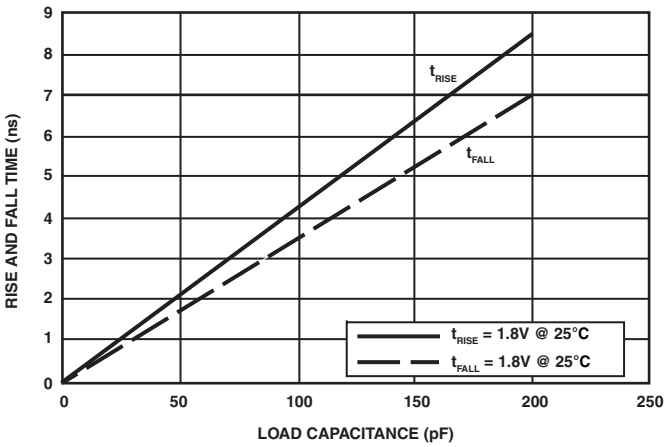


Figure 60. Driver Type B Typical Rise and Fall Times (10%–90%) vs. Load Capacitance (1.8V V_{DDEXT}/V_{DDMEM})

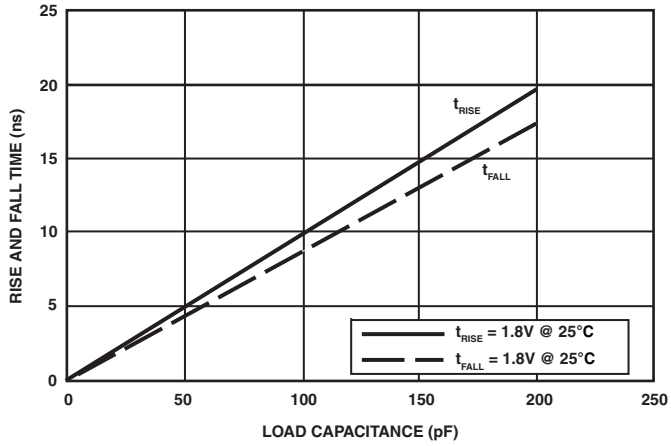


Figure 63. Driver Type C Typical Rise and Fall Times (10%–90%) vs. Load Capacitance (1.8V V_{DDEXT}/V_{DDMEM})

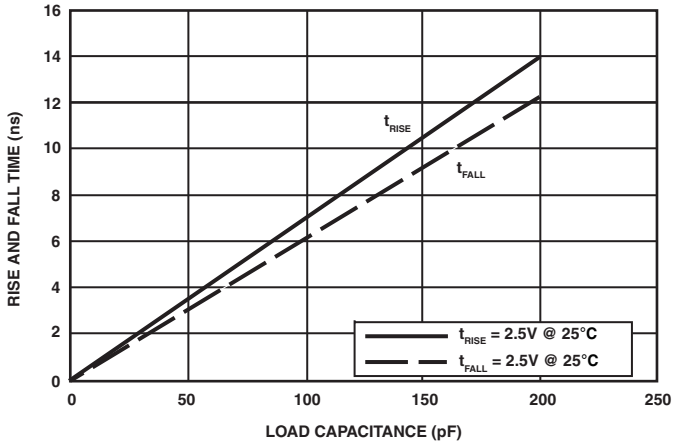


Figure 64. Driver Type C Typical Rise and Fall Times (10%–90%) vs. Load Capacitance (2.5V V_{DDEXT}/V_{DDMEM})

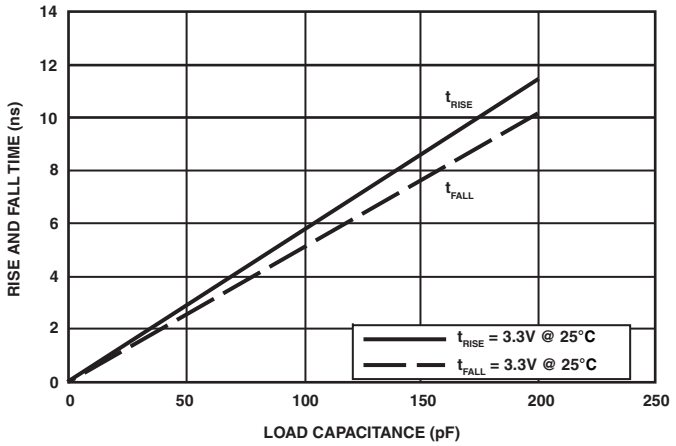


Figure 65. Driver Type C Typical Rise and Fall Times (10%–90%) vs. Load Capacitance (3.3V V_{DDEXT}/V_{DDMEM})

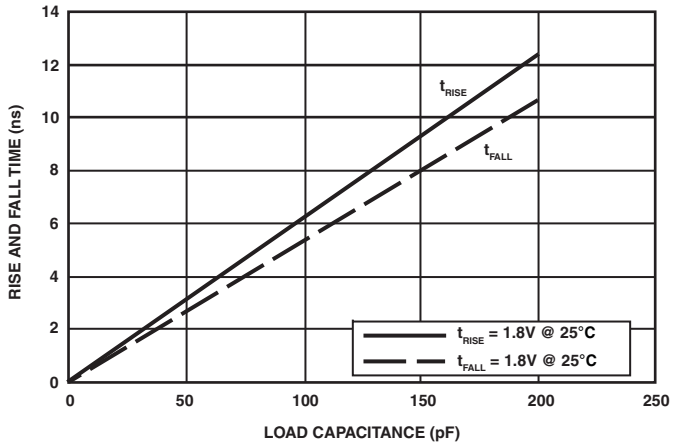


Figure 66. Driver Type D Typical Rise and Fall Times (10%–90%) vs. Load Capacitance (1.8V V_{DDEXT}/V_{DDMEM})

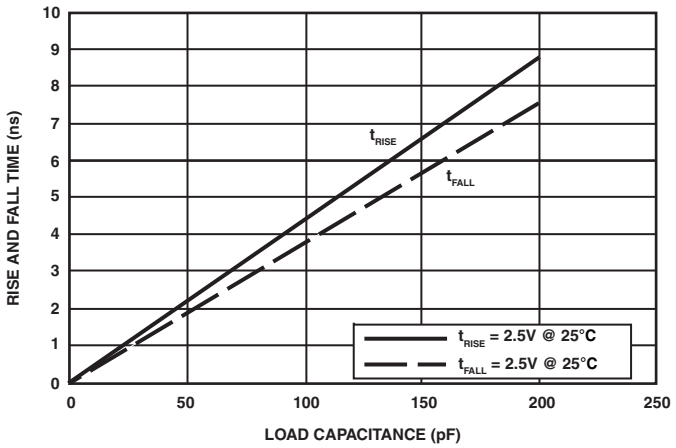


Figure 67. Driver Type D Typical Rise and Fall Times (10%–90%) vs. Load Capacitance (2.5V V_{DDEXT}/V_{DDMEM})

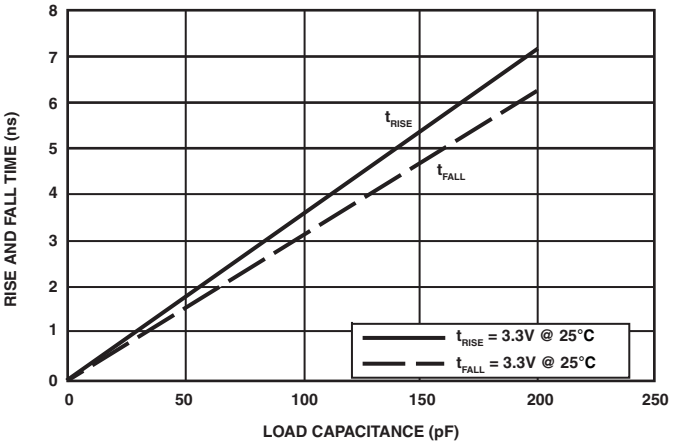


Figure 68. Driver Type D Typical Rise and Fall Times (10%–90%) vs. Load Capacitance (3.3V V_{DDEXT}/V_{DDMEM})

176-LEAD LQFP_EP LEAD ASSIGNMENT

Table 52 lists the LQFP_EP leads by lead number. Table 53 on Page 60 lists the LQFP_EP by signal mnemonic.

Table 52. 176-Lead LQFP_EP Pin Assignment (Numerical by Lead Number)

Lead No.	Signal	Lead No.	Signal	Lead No.	Signal	Lead No.	Signal
1	GND	45	GND	89	GND	133	GND
2	GND	46	GND	90	GND	134	GND
3	PF9	47	PG1	91	A12	135	$\overline{PG}$
4	PF8	48	PG0	92	A11	136	V_{DDEXT}
5	PF7	49	V_{DDEXT}	93	A10	137	GND
6	PF6	50	TDO	94	A9	138	V_{DDINT}
7	V_{DDEXT}	51	$\overline{EMU}$	95	V_{DDMEM}	139	GND
8	V_{PPOTP}	52	TDI	96	A8	140	RTXO
9	V_{DDOTP}	53	TCK	97	A7	141	RTXI
10	PF5	54	$\overline{TRST}$	98	V_{DDINT}	142	V_{DDRTC}
11	PF4	55	TMS	99	GND	143	CLKIN
12	PF3	56	D15	100	V_{DDINT}	144	XTAL
13	PF2	57	D14	101	A6	145	V_{DDEXT}
14	V_{DDINT}	58	D13	102	A5	146	$\overline{RESET}$
15	GND	59	V_{DDMEM}	103	A4	147	$\overline{NMI}$
16	$V_{DDFLASH}$	60	D12	104	V_{DDMEM}	148	V_{DDEXT}
17	$V_{DDFLASH}$	61	D11	105	A3	149	GND
18	PF1	62	D10	106	A2	150	CLKBUF
19	PF0	63	V_{DDINT}	107	A1	151	GND
20	PG15	64	D9	108	$\overline{ABE}$1	152	V_{DDINT}
21	PG14	65	D8	109	$\overline{ABE}$0	153	PH7
22	GND	66	D7	110	SA10	154	PH6
23	V_{DDINT}	67	GND	111	GND	155	PH5
24	V_{DDEXT}	68	V_{DDMEM}	112	V_{DDMEM}	156	PH4
25	PG13	69	D6	113	$\overline{SWE}$	157	GND
26	PG12	70	D5	114	$\overline{SCAS}$	158	V_{DDEXT}
27	PG11	71	D4	115	$\overline{SRAS}$	159	PH3
28	PG10	72	D3	116	V_{DDINT}	160	PH2
29	$V_{DDFLASH}$	73	D2	117	GND	161	PH1
30	V_{DDINT}	74	D1	118	$\overline{SMS}$	162	PH0
31	PG9	75	V_{DDMEM}	119	SCKE	163	GND
32	PG8	76	D0	120	$\overline{AMS}$1	164	V_{DDINT}
33	PG7	77	A19	121	$\overline{ARE}$	165	PF15
34	PG6	78	A18	122	$\overline{AWE}$	166	PF14
35	V_{DDEXT}	79	V_{DDINT}	123	$\overline{AMS}$0	167	PF13
36	PG5	80	A17	124	V_{DDMEM}	168	PF12
37	PG4	81	A16	125	CLKOUT	169	GND
38	PG3	82	V_{DDMEM}	126	$V_{DDFLASH}$	170	V_{DDEXT}
39	PG2	83	GND	127	NC[1]	171	PF11
40	BMODE2	84	A15	128	V_{DDEXT}	172	SDA
41	BMODE1	85	A14	129	V_{DDEXT}	173	SCL
42	BMODE0	86	A13	130	EXT_WAKE	174	PF10
43	GND	87	GND	131	GND	175	GND
44	GND	88	GND	132	GND	176	GND
						GND	177*

* Pin no. 177 is the GND supply (see Figure 70) for the processor; this pad must be **robustly** connected to GND.

[1] This pin must not be connected.

Figure 69 shows the top view of the LQFP_EP lead configuration. Figure 70 shows the bottom view of the LQFP_EP lead configuration.

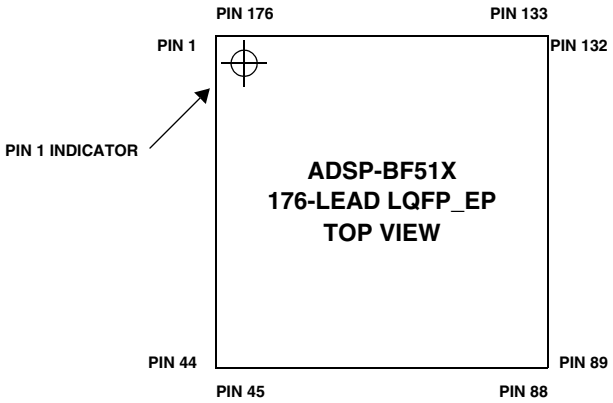


Figure 69. 176-Lead LQFP_EP Lead Configuration (Top View)

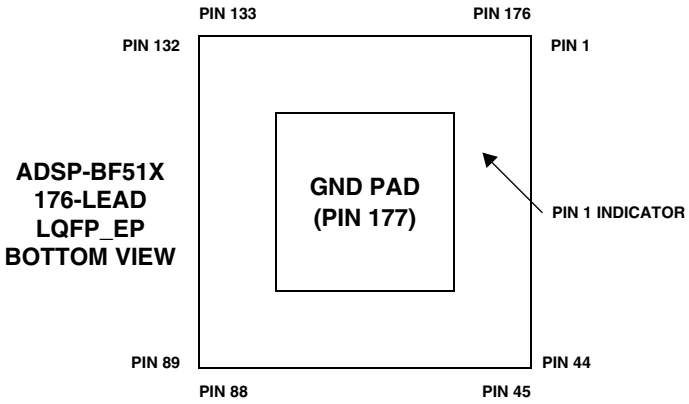


Figure 70. 176-Lead LQFP_EP Lead Configuration (Bottom View)

168-BALL CSP_BGA BALL ASSIGNMENT

Table 54 lists the CSP_BGA by ball number. Table 55 on Page 63 lists the CSP_BGA balls by signal mnemonic.

Table 54. 168-Ball CSP_BGA Ball Assignment (Numerical by Ball Number)

Ball No.	Signal Name	Ball No.	Signal Name	Ball No.	Signal Name	Ball No.	Signal Name	Ball No.	Signal Name	Ball No.	Signal Name
A1	GND	C1	PF4	E10	V_{DDINT}	H1	PG12	K6	V_{DDMEM}	N1	BMODE1
A2	SCL	C2	PF7	E12	V_{DDMEM}	H2	PG13	K7	V_{DDMEM}	N2	PG1
A3	SDA	C3	PF8	E13	$\overline{ARE}$	H3	PG11	K8	V_{DDMEM}	N3	TDO
A4	PF13	C4	PF10	E14	$\overline{AWE}$	H5	V_{DDEXT}	K9	V_{DDMEM}	N4	$\overline{TRST}$
A5	PF15	C5	V_{DDEXT}	F1	PF0	H6	GND	K10	V_{DDMEM}	N5	TMS
A6	PH2	C6	V_{DDEXT}	F2	PF1	H7	GND	K12	A8	N6	D13
A7	PH1	C7	PF11	F3	V_{DDINT}	H8	GND	K13	A2	N7	D9
A8	PH5	C8	V_{DDEXT}	F5	V_{DDEXT}	H9	GND	K14	A1	N8	D5
A9	PH6	C9	V_{DDINT}	F6	GND	H10	V_{DDINT}	L1	PG5	N9	D1
A10	PH7	C10	V_{DDEXT}	F7	GND	H12	A3	L2	PG3	N10	A18
A11	CLKBUF	C11	RTXI	F8	GND	H13	$\overline{ABE}$0	L3	PG2	N11	A16
A12	XTAL	C12	RTXO	F9	GND	H14	$\overline{SCAS}$	L12	A9	N12	A14
A13	CLKIN	C13	$\overline{PG}$	F10	V_{DDINT}	J1	PG10	L13	A6	N13	A11
A14	GND	C14	NC[1]	F12	$\overline{SMS}$	J2	$V_{DDFLASH}$	L14	A4	N14	A7
B1	V_{DDOTP}	D1	PF3	F13	SCKE	J3	PG9	M1	PG4	P1	GND
B2	GND	D2	PF5	F14	$\overline{AMS}$1	J5	V_{DDMEM}	M2	BMODE2	P2	TDI
B3	PF9	D3	VPPOTP	G1	PG15	J6	GND	M3	BMODE0	P3	TCK
B4	PF12	D12	$V_{DDFLASH}$	G2	PG14	J7	GND	M4	PG0	P4	D15
B5	PF14	D13	CLKOUT	G3	V_{DDINT}	J8	GND	M5	$\overline{EMU}$	P5	D14
B6	PH0	D14	$\overline{AMS}$0	G5	V_{DDEXT}	J9	GND	M6	D12	P6	D11
B7	PH3	E1	$V_{DDFLASH}$	G6	GND	J10	V_{DDINT}	M7	D10	P7	D8
B8	PH4	E2	PF2	G7	GND	J12	A15	M8	D2	P8	D7
B9	V_{DDEXT}	E3	PF6	G8	GND	J13	$\overline{ABE}$1	M9	D0	P9	D6
B10	$\overline{RESET}$	E5	V_{DDEXT}	G9	GND	J14	SA10	M10	A17	P10	D4
B11	$\overline{NMI}$	E6	V_{DDEXT}	G10	V_{DDINT}	K1	PG6	M11	A13	P11	D3
B12	V_{DDRTC}	E7	V_{DDINT}	G12	$\overline{SWE}$	K2	PG8	M12	A12	P12	A19
B13	V_{DDEXT}	E8	V_{DDINT}	G13	$\overline{SRAS}$	K3	PG7	M13	A10	P13	GND
B14	EXT_WAKE	E9	V_{DDINT}	G14	GND	K5	V_{DDMEM}	M14	A5	P14	GND

[1] This pin must not be connected.

AUTOMOTIVE PRODUCTS

The ADBF512W and ADBF518 models are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. Note that these automotive models may have specifications that differ from the commercial models and designers should review the product Specifications section of this data sheet carefully. Only the automotive grade products shown in Table 57 are available for use in automotive applications. Contact your local ADI account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.

Table 57. Automotive Products

Automotive Models[1,2]	Temperature Range[3]	Instruction Rate (Max)	Package Description	Package Option
ADBF512WBBCZ4xx	–40°C to +85°C	400 MHz	168-Ball CSP_BGA	BC-168-1
ADBF518WBBCZ4xx	–40°C to +85°C	400 MHz	168-Ball CSP_BGA	BC-168-1
ADBF512WBSWZ4xx	–40°C to +85°C	400 MHz	176-Lead LQFP_EP	SQ-176-2
ADBF518WBSWZ4xx	–40°C to +85°C	400 MHz	176-Lead LQFP_EP	SQ-176-2

[1] Z = RoHS Compliant Part.
[2] The use of xx designates silicon revision.
[3] Referenced temperature is ambient temperature. The ambient temperature is not a specification. Please see Operating Conditions on Page 22 for junction temperature (T_J) specification which is the only temperature specification.

ORDERING GUIDE

Model[1]	Temperature Range[2]	Processor Instruction Rate (Max)	Flash Memory	Package Description	Package Option
ADSP-BF512BBCZ-3	–40°C to +85°C	300 MHz	N/A	168-Ball CSP_BGA	BC-168-1
ADSP-BF512BBCZ-4	–40°C to +85°C	400 MHz	N/A	168-Ball CSP_BGA	BC-168-1
ADSP-BF512BSWZ-3	–40°C to +85°C	300 MHz	N/A	176-Lead LQFP_EP	SQ-176-2
ADSP-BF512BSWZ-4	–40°C to +85°C	400 MHz	N/A	176-Lead LQFP_EP	SQ-176-2
ADSP-BF512KBCZ-3	0°C to +70°C	300 MHz	N/A	168-Ball CSP_BGA	BC-168-1
ADSP-BF512KBCZ-4	0°C to +70°C	400 MHz	N/A	168-Ball CSP_BGA	BC-168-1
ADSP-BF512KSWZ-3	0°C to +70°C	300 MHz	N/A	176-Lead LQFP_EP	SQ-176-2
ADSP-BF512KSWZ-4	0°C to +70°C	400 MHz	N/A	176-Lead LQFP_EP	SQ-176-2
ADSP-BF514BBCZ-3	–40°C to +85°C	300 MHz	N/A	168-Ball CSP_BGA	BC-168-1
ADSP-BF514BBCZ-4	–40°C to +85°C	400 MHz	N/A	168-Ball CSP_BGA	BC-168-1
ADSP-BF514BBCZ4F16	–40°C to +85°C	400 MHz	16M bit	168-Ball CSP_BGA	BC-168-1
ADSP-BF514BSWZ-3	–40°C to +85°C	300 MHz	N/A	176-Lead LQFP_EP	SQ-176-2
ADSP-BF514BSWZ-4	–40°C to +85°C	400 MHz	N/A	176-Lead LQFP_EP	SQ-176-2
ADSP-BF514BSWZ4F16	–40°C to +85°C	400 MHz	16M bit	176-Lead LQFP_EP	SQ-176-2
ADSP-BF514KBCZ-3	0°C to +70°C	300 MHz	N/A	168-Ball CSP_BGA	BC-168-1
ADSP-BF514KBCZ-4	0°C to +70°C	400 MHz	N/A	168-Ball CSP_BGA	BC-168-1
ADSP-BF514KSWZ-3	0°C to +70°C	300 MHz	N/A	176-Lead LQFP_EP	SQ-176-2
ADSP-BF514KSWZ-4	0°C to +70°C	400 MHz	N/A	176-Lead LQFP_EP	SQ-176-2
ADSP-BF516KSWZ-3	0°C to +70°C	300 MHz	N/A	176-Lead LQFP_EP	SQ-176-2
ADSP-BF516KBCZ-3	0°C to +70°C	300 MHz	N/A	168-Ball CSP_BGA	BC-168-1
ADSP-BF516KSWZ-4	0°C to +70°C	400 MHz	N/A	176-Lead LQFP_EP	SQ-176-2
ADSP-BF516KBCZ-4	0°C to +70°C	400 MHz	N/A	168-Ball CSP_BGA	BC-168-1