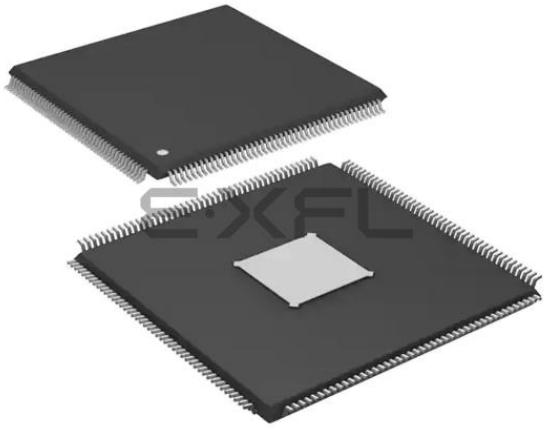

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Obsolete
Type	Fixed Point
Interface	Ethernet, I²C, PPI, RSI, SPI, SPORT, UART/USART
Clock Rate	400MHz
Non-Volatile Memory	FLASH (16Mbit)
On-Chip RAM	116kB
Voltage - I/O	1.8V, 2.5V, 3.3V
Voltage - Core	1.30V
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP Exposed Pad
Supplier Device Package	176-LQFP-EP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-bf518bswz4f16

instruction can be issued in parallel with two 16-bit instructions, allowing the programmer to use many of the core resources in a single instruction cycle.

The Blackfin processor assembly language uses an algebraic syntax for ease of coding and readability. The architecture has been optimized for use in conjunction with the C/C++ compiler, resulting in fast and efficient software implementations.

MEMORY ARCHITECTURE

The ADSP-BF51x processors view memory as a single unified 4G byte address space, using 32-bit addresses. All resources, including internal memory, external memory, and I/O control registers, occupy separate sections of this common address space. The memory portions of this address space are arranged in a hierarchical structure to provide a good cost/performance balance of some very fast, low-latency on-chip memory as cache or SRAM, and larger, lower-cost and performance off-chip memory systems. The memory map for both internal and external memory space is shown in Figure 3.

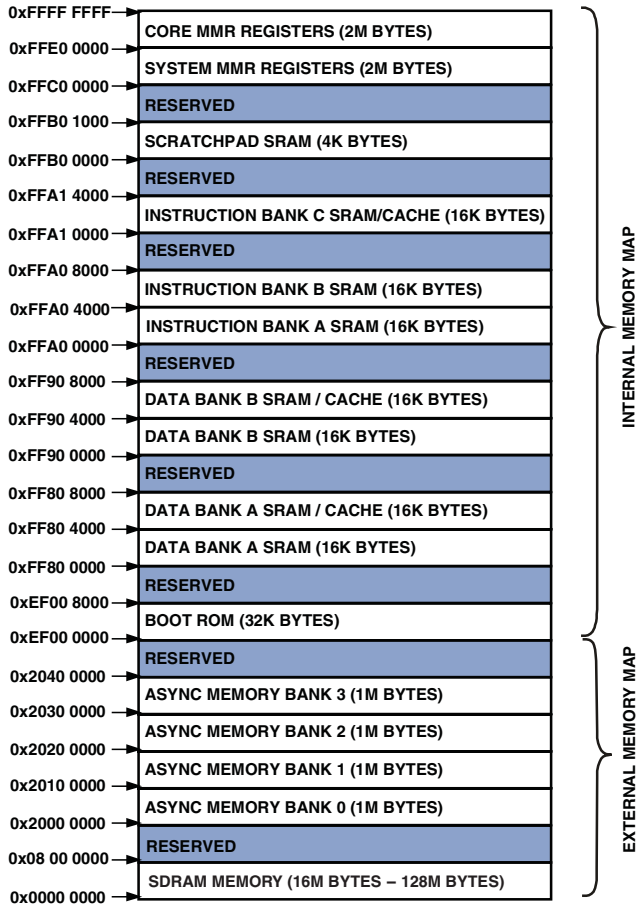


Figure 3. ADSP-BF51x Internal/External Memory Map

The on-chip L1 memory system is the highest-performance memory available to the Blackfin processor. The off-chip memory system, accessed through the external bus interface unit (EBIU), provides expansion with SDRAM, flash memory, and SRAM, optionally accessing up to 132M bytes of physical memory.

The memory DMA controller provides high bandwidth data-movement capability. It can perform block transfers of code or data between the internal memory and the external memory spaces.

Internal (On-Chip) Memory

The ADSP-BF51x processors have three blocks of on-chip memory that provide high bandwidth access to the core.

The first block is the L1 instruction memory, consisting of 48K bytes SRAM, of which 16K bytes can be configured as a four-way set-associative cache. This memory is accessed at full processor speed.

The second on-chip memory block is the L1 data memory, consisting of up to two banks of up to 32K bytes each. Each memory bank is configurable, offering both cache and SRAM functionality. This memory block is accessed at full processor speed.

The third memory block is a 4K byte scratchpad SRAM which runs at the same speed as the L1 memories, but is only accessible as data SRAM and cannot be configured as cache memory.

External (Off-Chip) Memory

External memory is accessed via the EBIU. This 16-bit interface provides a glueless connection to a bank of synchronous DRAM (SDRAM) as well as up to four banks of asynchronous memory devices including flash, EPROM, ROM, SRAM, and memory mapped I/O devices.

The SDRAM controller can be programmed to interface to up to 128M bytes of SDRAM. A separate row can be open for each SDRAM internal bank, and the SDRAM controller supports up to four internal SDRAM banks, improving overall performance.

The asynchronous memory controller can be programmed to control up to four banks of devices with very flexible timing parameters for a wide variety of devices. Each bank occupies a 1M byte segment regardless of the size of the devices used, so that these banks are only contiguous if each is fully populated with 1M byte of memory.

Flash Memory

The ADSP-BF51xF processors contain an SPI flash memory within the package of the processor connected to SPI0 (Figure 4).

The SPI flash memory has a 16M bit capacity. Also included are support for software write protection and for fast erase and byte-program.

Table 2. Internal Flash Memory Signal Descriptions

Symbol	Pin Name	Function
SCK	Serial Clock	Provides the timing of the serial interface. Commands, addresses, or input data are latched on the rising edge of the clock input, while output data is shifted out on the falling edge of the clock input.
SI	Serial Data Input	Transfers commands, addresses, or data serially into the device. Inputs are latched on the rising edge of the serial clock.
SO	Serial Data Output	Transfers data serially out of the device. Data is shifted out on the falling edge of the serial clock. Flash busy status pin in AAI mode if SO is configured as a hardware RY/$\overline{BY}$ pin.
$\overline{CE}$	Chip Enable	The device is enabled by a high to low transition on $\overline{CE}$. $\overline{CE}$ must remain low for the duration of any command sequence.
$\overline{RST}$	Reset	Resets the operation of the device and the internal logic. This signal is tied to the ADSP-BF51x $\overline{RESET}$ signal.

One-Time Programmable Memory

The processors have 64K bits of one-time programmable non-volatile memory that can be programmed by the developer only once. It includes the array and logic to support read access and programming. Additionally, its pages can be write protected.

The OTP memory allows both public and private data to be stored on-chip. In addition to storing public and private key data for applications requiring security, OTP allows developers to store completely user-definable data such as customer ID, product ID, and MAC address. Therefore, generic parts can be supplied which are then programmed and protected by the developer within this non-volatile memory.

I/O Memory Space

The processors do not define a separate I/O space. All resources are mapped through the flat 32-bit address space. On-chip I/O devices have their control registers mapped into memory-mapped registers (MMRs) at addresses near the top of the 4G byte address space. These are separated into two smaller blocks, one which contains the control MMRs for all core functions, and the other which contains the registers needed for setup and control of the on-chip peripherals outside of the core. The MMRs are accessible only in supervisor mode and appear as reserved space to on-chip peripherals.

Booting from ROM

The processors contain a small on-chip boot kernel, which configures the appropriate peripheral for booting. If the processors are configured to boot from boot ROM memory space, the processor starts executing from the on-chip boot ROM. For more information, see Booting Modes on Page 15.

EVENT HANDLING

The event controller handles all asynchronous and synchronous events to the processor. The processors provide event handling that supports both nesting and prioritization. Nesting allows multiple event service routines to be active simultaneously. Prioritization ensures that servicing of a higher priority event takes precedence over servicing of a lower priority event.

The controller provides support for five different types of events:

- Emulation—An emulation event causes the processor to enter emulation mode, allowing command and control of the processor through the JTAG interface.
- Reset—This event resets the processor.
- Nonmaskable Interrupt (NMI)—The NMI event can be generated by the software watchdog timer or by the NMI input signal to the processor. The NMI event is frequently used as a power-down indicator to initiate an orderly shut-down of the system.
- Exceptions—Events that occur synchronously to program flow; that is, the exception is taken before the instruction is allowed to complete. Conditions such as data alignment violations and undefined instructions cause exceptions.
- Interrupts—Events that occur asynchronously to program flow. They are caused by input signals, timers, and other peripherals, as well as by an explicit software instruction.

Each event type has an associated register to hold the return address and an associated return-from-event instruction. When an event is triggered, the state of the processor is saved on the supervisor stack.

The event controller consists of two stages, the core event controller (CEC) and the system interrupt controller (SIC). The core event controller works with the system interrupt controller to prioritize and control all system events. Conceptually, interrupts from the peripherals enter into the SIC, and are then routed directly into the general-purpose interrupts of the CEC.

Core Event Controller (CEC)

The CEC supports nine general-purpose interrupts (IVG15–7), in addition to the dedicated interrupt and exception events. Of these general-purpose interrupts, the two lowest priority interrupts (IVG15–14) are recommended to be reserved for software interrupt handlers, leaving seven prioritized interrupt inputs to support the peripherals of the processors. The inputs to the CEC, identifies their names in the event vector table

In the active mode, it is possible to disable the PLL through the PLL control register (PLL_CTL). If disabled, the PLL must be re-enabled before transitioning to the full-on or sleep modes.

Sleep Operating Mode—High Dynamic Power Savings

The sleep mode reduces dynamic power dissipation by disabling the clock to the processor core (CCLK). The PLL and system clock (SCLK), however, continue to operate in this mode. Typically an external event or RTC activity wakes up the processor. When in the sleep mode, asserting wakeup causes the processor to sense the value of the BYPASS bit in the PLL control register (PLL_CTL). If BYPASS is disabled, the processor transitions to the full on mode. If BYPASS is enabled, the processor transitions to the active mode.

System DMA access to L1 memory is not supported in sleep mode.

Deep Sleep Operating Mode—Maximum Dynamic Power Savings

The deep sleep mode maximizes dynamic power savings by disabling the clocks to the processor core (CCLK) and to all synchronous peripherals (SCLK). Asynchronous peripherals, such as the RTC, may still be running but cannot access internal resources or external memory. This powered-down mode can only be exited by assertion of the reset interrupt ($\overline{\text{RESET}}$) or by an asynchronous interrupt generated by the RTC. When in deep sleep mode, an RTC asynchronous interrupt causes the processor to transition to the Active mode. Assertion of $\overline{\text{RESET}}$ while in deep sleep mode causes the processor to transition to the full on mode.

Hibernate State—Maximum Static Power Savings

The hibernate state maximizes static power savings by disabling the voltage and clocks to the processor core (CCLK) and system blocks (SCLK). Any critical information stored internally (for example memory contents, register contents) must be written to a non-volatile storage device prior to removing power if the processor state is to be preserved. Writing b#00 to the FREQ bits in the VR_CTL register also causes the EXT_WAKE signal to transition low, which can be used to signal an external voltage regulator to shut down.

Since V_{DDEXT} is still supplied in this mode, all of the external signals three-state, unless otherwise specified. This allows other devices that may be connected to the processor to still have power applied without drawing unwanted current.

The Ethernet module can signal an external regulator to wake up using the EXT_WAKE signal. If PF15 does not connect as a $\overline{\text{PHYINT}}$ signal to an external PHY device, it can be pulled low by any other device to wake the processor up. The processor can also be woken up by a real-time clock wakeup event or by asserting the $\overline{\text{RESET}}$ pin. All hibernate wakeup events initiate the hardware reset sequence. Individual sources are enabled by the VR_CTL register. The EXT_WAKE signal is provided to indicate the occurrence of wakeup events.

With the exception of the VR_CTL and the RTC registers, all internal registers and memories lose their content in the hibernate state. State variables may be held in external SRAM or SDRAM. The SCKELOW bit in the VR_CTL register controls whether or not SDRAM operates in self-refresh mode, which allows it to retain its content while the processor is in hibernation and through the subsequent reset sequence.

Power Savings

As shown in Table 4, the processors support up to six different power domains, which maximizes flexibility while maintaining compliance with industry standards and conventions. By isolating the internal logic of the processor into its own power domain, separate from the RTC and other I/O, the processor can take advantage of dynamic power management without affecting the RTC or other I/O devices. There are no sequencing requirements for the various power domains, but all domains must be powered according to the appropriate Specifications table for processor Operating Conditions; even if the feature/peripheral is not used.

Table 4. Power Domains

Power Domain	V_{DD} Range
All internal logic, except RTC, Memory, OTP	V_{DDINT}
RTC internal logic and crystal I/O	V_{DDRTC}
Memory logic	V_{DDMEM}
OTP logic	V_{DDOTP}
Optional internal flash	$V_{DDFLASH}$
All other I/O	V_{DDEXT}

The dynamic power management feature of the processor allows both the processor's input voltage (V_{DDINT}) and clock frequency (f_{CCLK}) to be dynamically controlled.

The power dissipated by a processor is largely a function of its clock frequency and the square of the operating voltage. For example, reducing the clock frequency by 25% results in a 25% reduction in dynamic power dissipation, while reducing the voltage by 25% reduces dynamic power dissipation by more than 40%. Further, these power savings are additive, in that if the clock frequency and supply voltage are both reduced, the power savings can be dramatic, as shown in the following equations.

$$\text{Power Savings Factor} = \frac{f_{CCLKRED}}{f_{CCLKNOM}} \times \left(\frac{V_{DDINTRED}}{V_{DDINTNOM}}\right)^2 \times \left(\frac{T_{RED}}{T_{NOM}}\right)$$

$$\%\ \text{Power Savings} = (1 - \text{Power Savings Factor}) \times 100\%$$

where the variables in the equations are:

$f_{CCLKNOM}$ is the nominal core clock frequency

$f_{CCLKRED}$ is the reduced core clock frequency

$V_{DDINTNOM}$ is the nominal internal supply voltage

$V_{DDINTRED}$ is the reduced internal supply voltage

The newest IDE, CrossCore Embedded Studio, is based on the Eclipse™ framework. Supporting most Analog Devices processor families, it is the IDE of choice for future processors, including multicore devices. CrossCore Embedded Studio seamlessly integrates available software add-ins to support real time operating systems, file systems, TCP/IP stacks, USB stacks, algorithmic software modules, and evaluation hardware board support packages. For more information visit www.analog.com/cces.

The other Analog Devices IDE, VisualDSP++, supports processor families introduced prior to the release of CrossCore Embedded Studio. This IDE includes the Analog Devices VDK real time operating system and an open source TCP/IP stack. For more information visit www.analog.com/visualdsp. Note that VisualDSP++ will not support future Analog Devices processors.

EZ-KIT Lite Evaluation Board

For processor evaluation, Analog Devices provides wide range of EZ-KIT Lite® evaluation boards. Including the processor and key peripherals, the evaluation board also supports on-chip emulation capabilities and other evaluation and development features. Also available are various EZ-Extenders®, which are daughter cards delivering additional specialized functionality, including audio and video processing. For more information visit www.analog.com and search on “ezkit” or “ezextender”.

EZ-KIT Lite Evaluation Kits

For a cost-effective way to learn more about developing with Analog Devices processors, Analog Devices offer a range of EZ-KIT Lite evaluation kits. Each evaluation kit includes an EZ-KIT Lite evaluation board, directions for downloading an evaluation version of the available IDE(s), a USB cable, and a power supply. The USB controller on the EZ-KIT Lite board connects to the USB port of the user’s PC, enabling the chosen IDE evaluation suite to emulate the on-board processor in-circuit. This permits the customer to download, execute, and debug programs for the EZ-KIT Lite system. It also supports in-circuit programming of the on-board Flash device to store user-specific boot code, enabling standalone operation. With the full version of CrossCore Embedded Studio or VisualDSP++ installed (sold separately), engineers can develop software for supported EZ-KITs or any custom system utilizing supported Analog Devices processors.

Software Add-Ins for CrossCore Embedded Studio

Analog Devices offers software add-ins which seamlessly integrate with CrossCore Embedded Studio to extend its capabilities and reduce development time. Add-ins include board support packages for evaluation hardware, various middleware packages, and algorithmic modules. Documentation, help, configuration dialogs, and coding examples present in these add-ins are viewable through the CrossCore Embedded Studio IDE once the add-in is installed.

Board Support Packages for Evaluation Hardware

Software support for the EZ-KIT Lite evaluation boards and EZ-Extender daughter cards is provided by software add-ins called Board Support Packages (BSPs). The BSPs contain the required drivers, pertinent release notes, and select example code for the given evaluation hardware. A download link for a specific BSP is located on the web page for the associated EZ-KIT or EZ-Extender product. The link is found in the *Product Download* area of the product web page.

Middleware Packages

Analog Devices separately offers middleware add-ins such as real time operating systems, file systems, USB stacks, and TCP/IP stacks. For more information see the following web pages:

- www.analog.com/ucos3
- www.analog.com/ucfs
- www.analog.com/ucusbd
- www.analog.com/lwip

Algorithmic Modules

To speed development, Analog Devices offers add-ins that perform popular audio and video processing algorithms. These are available for use with both CrossCore Embedded Studio and VisualDSP++. For more information visit www.analog.com and search on “Blackfin software modules” or “SHARC software modules”.

Designing an Emulator-Compatible DSP Board (Target)

For embedded system test and debug, Analog Devices provides a family of emulators. On each JTAG DSP, Analog Devices supplies an IEEE 1149.1 JTAG Test Access Port (TAP). In-circuit emulation is facilitated by use of this JTAG interface. The emulator accesses the processor’s internal features via the processor’s TAP, allowing the developer to load code, set breakpoints, and view variables, memory, and registers. The processor must be halted to send data and commands, but once an operation is completed by the emulator, the DSP system is set to run at full speed with no impact on system timing. The emulators require the target board to include a header that supports connection of the DSP’s JTAG port to the emulator.

For details on target board design issues including mechanical layout, single processor connections, signal buffering, signal termination, and emulator pod logic, see the *EE-68: Analog Devices JTAG Emulation Technical Reference* on the Analog Devices website (www.analog.com)—use site search on “EE-68.” This document is updated regularly to keep pace with improvements to emulator support.

Table 9 shows settings for TWI_DT in the NONGPIO_DRIVE register. Set this register prior to using the TWI port.

Table 9. TWI_DT Field Selections and V_{DDEXT}/V_{BUSTWI}

TWI_DT	V_{DDEXT} Nominal	V_{BUSTWI} Minimum	V_{BUSTWI} Nominal	V_{BUSTWI} Maximum	Unit
000 (default)	3.3	2.97	3.3	3.63	V
001	1.8	1.7	1.8	1.98	V
010	2.5	2.97	3.3	3.63	V
011	1.8	2.97	3.3	3.63	V
100	3.3	4.5	5	5.5	V
101	1.8	2.25	2.5	2.75	V
110	2.5	2.25	2.5	2.75	V
111 (reserved)	—	—	—	—	—

Clock Related Operating Conditions

Table 10 describes the timing requirements for the processor clocks. Take care in selecting MSEL, SSEL, and CSEL ratios so as not to exceed the maximum core clock and system clock. Table 11 describes phase-locked loop operating conditions.

Table 10. Core Clock (CCLK) Requirements

Parameter		Nominal Voltage Setting	Maximum	Unit
f_{CCLK}	Core Clock Frequency (V_{DDINT} = 1.33 V Minimum, All Models)	1.400 V	400	MHz
	Core Clock Frequency (V_{DDINT} = 1.23 V Minimum, Industrial/Commercial Models)	1.300 V	300	MHz
	Core Clock Frequency (V_{DDINT} = 1.14 V Minimum, Industrial Models Only)	1.200 V	200	MHz
	Core Clock Frequency (V_{DDINT} = 1.10 V Minimum, Commercial Models Only)	1.150 V	200	MHz

Table 11. Phase-Locked Loop Operating Conditions

Parameter		Min	Max	Unit
f_{VCO}	Voltage Controlled Oscillator (VCO) Frequency (Commercial/Industrial Models)	72	Instruction Rate[1]	MHz
	Voltage Controlled Oscillator (VCO) Frequency (Automotive Models)	84	Instruction Rate[1]	MHz

[1] For more information, see Ordering Guide on Page 67.

Table 12. SCLK Conditions

Parameter[1]		V_{DDEXT}/V_{DDMEM} 1.8 V Nominal Max	V_{DDEXT}/V_{DDMEM} 2.5 V or 3.3 V Nominal Max	Unit
f_{SCLK}	CLKOUT/SCLK Frequency (V_{DDINT} ≥ 1.230 V Minimum)	80	100	MHz
f_{SCLK}	CLKOUT/SCLK Frequency (V_{DDINT} < 1.230 V)	80	80	MHz

[1] f_{SCLK} must be less than or equal to f_{CCLK} and is subject to additional restrictions for SDRAM interface operation. See Table 28 on Page 33.

Parameter		Test Conditions	Min	Typical	Max	Unit
$I_{DDFLASH1}$	Flash Memory Supply Current 1—Asynchronous Read			6	9	mA
$I_{DDFLASH2}$	Flash Memory Supply Current 2—Standby			15	25	µA
$I_{DDFLASH3}$	Flash Memory Supply Current 3—Program and Erase			20	25	mA
I_{DDOTP}	V_{DDOTP} Current	V_{DDOTP} = 2.5 V, T_J = 25°C, OTP Memory Read		2		mA
I_{DDOTP}	V_{DDOTP} Current	V_{DDOTP} = 2.5 V, T_J = 25°C, OTP Memory Write		2		mA
I_{PPOTP}	V_{PPOTP} Current	V_{PPOTP} = 2.5 V, T_J = 25°C, OTP Memory Read		100		µA
I_{PPOTP}	V_{PPOTP} Current	V_{PPOTP} = Table 20 V, T_J = 25°C, OTP Memory Write		3		mA

[1] Applies to input balls.
[2] Applies to JTAG input balls (TCK, TDI, TMS, $\overline{TRST}$).
[3] Applies to three-statable balls.
[4] Applies to bidirectional balls SCL and SDA.
[5] Applies to all signal balls, except SCL and SDA.
[6] Guaranteed, but not tested.
[7] See the *ADSP-BF51x Blackfin Processor Hardware Reference Manual* for definition of sleep, deep sleep, and hibernate operating modes.
[8] Includes current on V_{DDEXT}, V_{DDMEM}, V_{DDOTP}, and V_{PPOTP} supplies. Clock inputs are tied high or low.
[9] Guaranteed maximum specifications.
[10] Unit for V_{DDINT} is V (Volts). Unit for f_{SCLK} is MHz.
[11] See Table 13 for the list of I_{DDINT} power vectors covered.

Total Power Dissipation

Total power dissipation has two components:

1. Static, including leakage current
2. Dynamic, due to transistor switching characteristics

Many operating conditions can also affect power dissipation, including temperature, voltage, operating frequency, and processor activity. Electrical Characteristics on Page 24 shows the current dissipation for internal circuitry (V_{DDINT}). $I_{DDDEEPSLEEP}$ specifies static power dissipation as a function of voltage (V_{DDINT}) and temperature (see Table 14), and I_{DDINT} specifies the total power specification for the listed test conditions, including the dynamic component as a function of voltage (V_{DDINT}) and frequency (Table 15).

There are two parts to the dynamic component. The first part is due to transistor switching in the core clock (CCLK) domain. This part is subject to an Activity Scaling Factor (ASF) which represents application code running on the processor core and L1 memories (Table 13).

The ASF is combined with the CCLK Frequency and V_{DDINT} dependent data in Table 15 to calculate this part. The second part is due to transistor switching in the system clock (SCLK) domain, which is included in the I_{DDINT} specification equation.

Table 13. Activity Scaling Factors (ASF)[1]

I_{DDINT} Power Vector	Activity Scaling Factor (ASF)
$I_{DD-PEAK}$	1.29
$I_{DD-HIGH}$	1.25
I_{DD-TYP}	1.00
I_{DD-APP}	0.85
I_{DD-NOP}	0.70
$I_{DD-IDLE}$	0.41

[1] See *Estimating Power for ASDP-BF534/BF536/BF537 Blackfin Processors (EE-297)*. The power vector information also applies to the ADSP-BF51x processors.

Table 14. Static Current—$I_{DD-DEEPSLEEP}$ (mA)

	Voltage (V_{DDINT})[1]								
T_J (°C)[1]	1.10 V	1.15 V	1.20 V	1.25 V	1.30 V	1.35 V	1.40 V	1.45 V	1.50 V
–40	0.9	1.0	1.0	1.1	1.1	1.2	1.3	1.7	1.9
–20	1.0	1.1	1.2	1.3	1.4	1.6	1.7	1.9	2.0
0	1.2	1.3	1.4	1.6	1.8	2.0	2.2	2.3	2.5

Table 25. Power-Up Reset Timing

Parameter		Min	Max	Unit
Timing Requirements				
$t_{RST\_IN\_PWR}$	$\overline{\text{RESET}}$ Deasserted after the V_{DDINT}, V_{DDEXT}, V_{DDRTC}, V_{DDMEM}, V_{DDOTP}, and CLKIN Pins are Stable and Within Specification	3500 × t_{CKIN}		ns

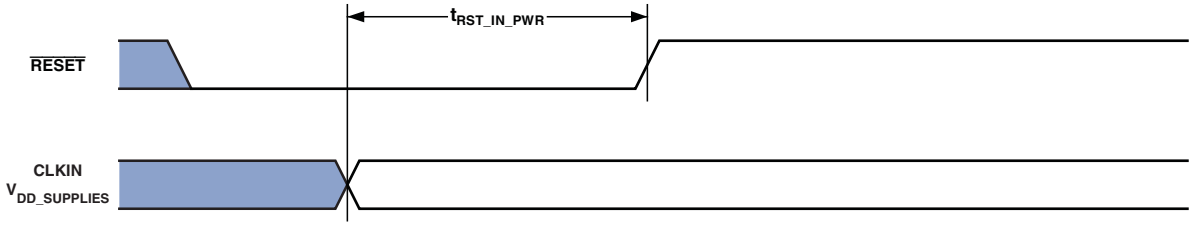


Figure 10. Power-Up Reset Timing

Asynchronous Memory Write Cycle Timing

Table 27. Asynchronous Memory Write Cycle Timing

Parameter		Min	Max	Unit
Timing Requirements				
t_{SARDY}	ARDY Setup Before CLKOUT	4		ns
t_{HARDY}	ARDY Hold After CLKOUT	0.2		ns
Switching Characteristics				
t_{DDAT}	DATA15–0 Disable After CLKOUT		6	ns
t_{ENDAT}	DATA15–0 Enable After CLKOUT	0		ns
t_{DO}	Output Delay After CLKOUT[1]		6	ns
t_{HO}	Output Hold After CLKOUT [1]	0.8		ns

[1] Output pins/balls include $\overline{AMS3-0}$, $\overline{ABE1-0}$, ADDR19–1, DATA15–0, $\overline{AOE}$, $\overline{AWE}$.

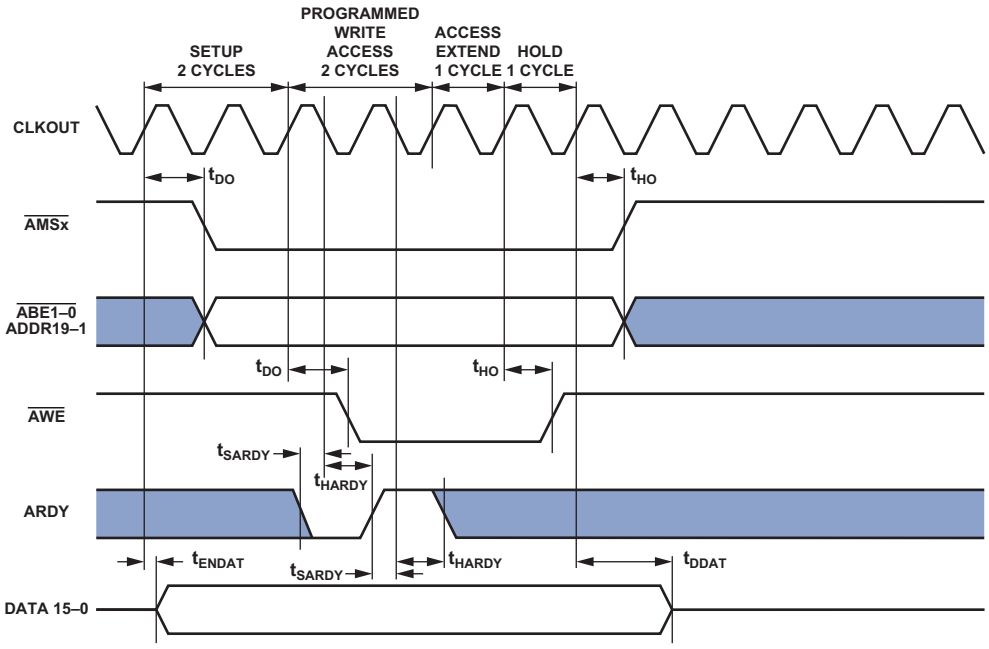


Figure 12. Asynchronous Memory Write Cycle Timing

SDRAM Interface Timing

Table 28. SDRAM Interface Timing

Parameter		V_{DDMEM} 1.8 V Nominal Min	V_{DDMEM} 1.8 V Nominal Max	V_{DDMEM} 2.5 V/3.3 V Nominal Min	V_{DDMEM} 2.5 V/3.3 V Nominal Max	Unit
Timing Requirements						
t_{SSDAT}	Data Setup Before CLKOUT	1.5		1.5		ns
t_{HSDAT}	Data Hold After CLKOUT	1.3		0.8		ns
Switching Characteristics						
t_{SCLK}	CLKOUT Period[1]	12.5		10		ns
t_{SCLKH}	CLKOUT Width High	5		4		ns
t_{SCLKL}	CLKOUT Width Low	5		4		ns
t_{DCAD}	Command, Address, Data Delay After CLKOUT[2]		5		4	ns
t_{HCAD}	Command, Address, Data Hold After CLKOUT[2]	1		1		ns
t_{DSDAT}	Data Disable After CLKOUT		5.5		5	ns
t_{ENSDAT}	Data Enable After CLKOUT	0		0		ns

[1] The t_{SCLK} value is the inverse of the f_{SCLK} specification discussed in Table 12 on Page 23. Package type and reduced supply voltages affect the best-case value listed here.
[2] Command pins/balls include: $\overline{SRAS}$, $\overline{SCAS}$, $\overline{SWE}$, SDQM, $\overline{SMS}$, SA10, SCKE.

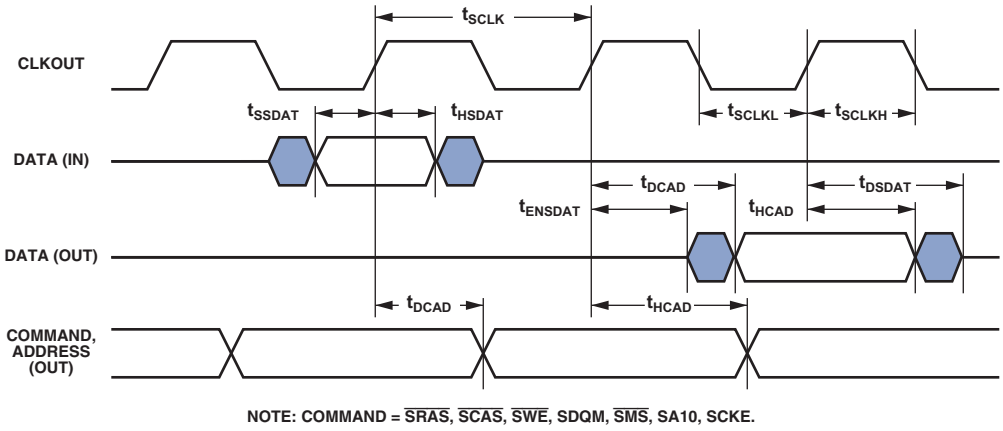


Figure 13. SDRAM Interface Timing

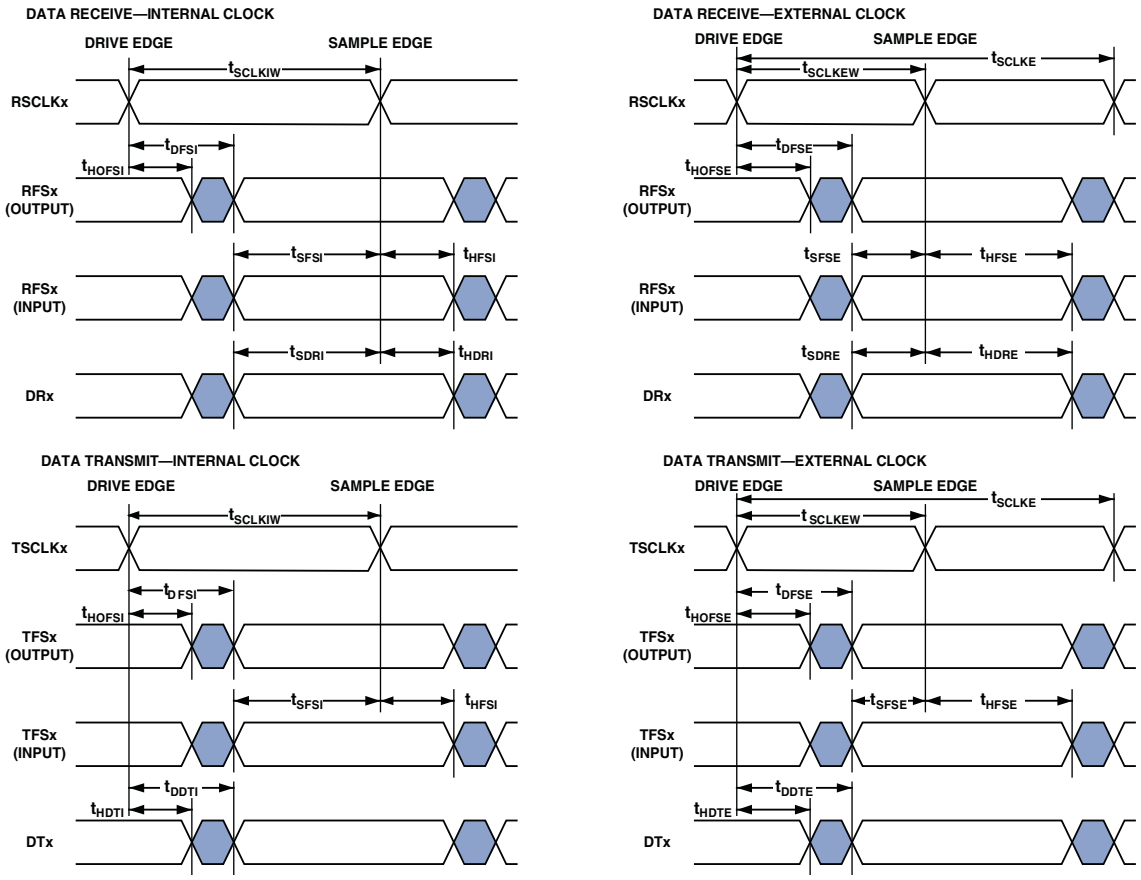


Figure 22. Serial Ports

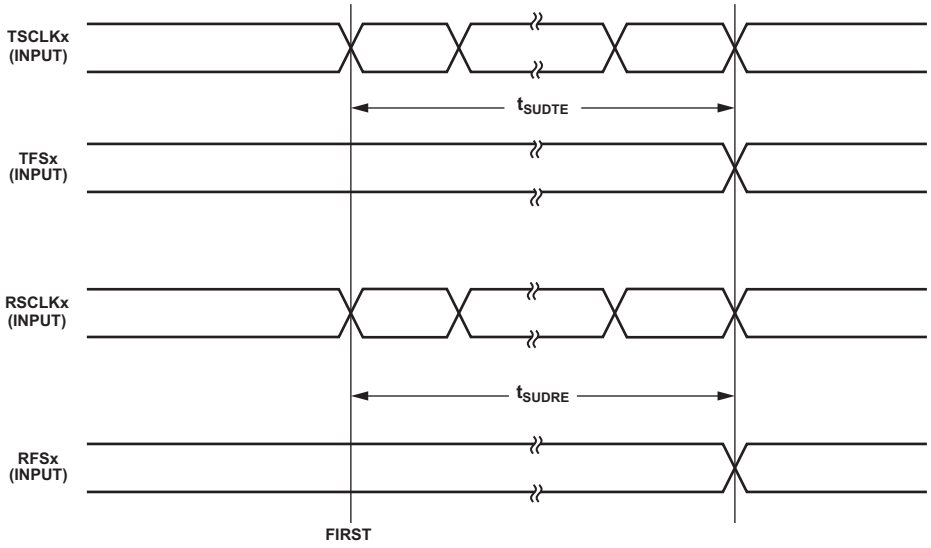


Figure 23. Serial Port Start Up with External Clock and Frame Sync

Table 36. External Late Frame Sync

Parameter		V_{DDEXT} 1.8 V Nominal Min	V_{DDEXT} 1.8 V Nominal Max	V_{DDEXT} 2.5 V/3.3 V Nominal Min	V_{DDEXT} 2.5 V/3.3 V Nominal Max	Unit
Switching Characteristics						
$t_{DDTLFSE}$[1, 2]	Data Delay from Late External TFSx or External RFSx with MCE = 1, MFD = 0		12		10	ns
$t_{DTENLFSE}$[1, 2]	Data Enable from Late FS or MCE = 1, MFD = 0	0		0		ns

[1] MCE = 1, TFSx enable and TFSx valid follow $t_{DDTENFS}$ and $t_{DDTLFSE}$.
[2] If external RFSx/TFSx setup to RSCLKx/TSCLKx > $t_{SCLKE}/2$ then $t_{DDTTE/I}$ and $t_{DTENE/I}$ apply, otherwise $t_{DDTLFSE}$ and $t_{DTENLFS}$ apply.

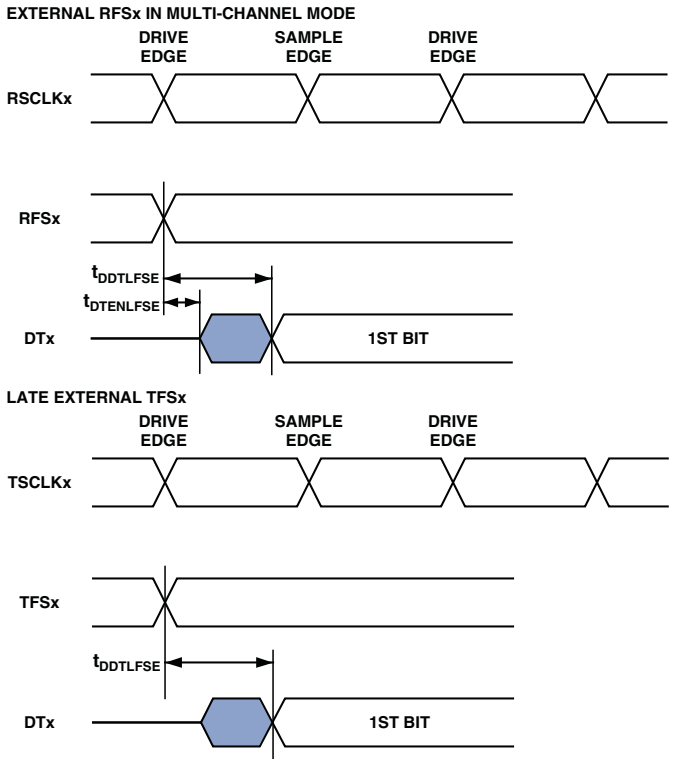


Figure 25. External Late Frame Sync

General-Purpose Port Timing

Table 39 and Figure 28 describe general-purpose port operations.

Table 39. General-Purpose Port Timing

Parameter		V_{DDEXT} 1.8 V Nominal		V_{DDEXT} 2.5 V/3.3 V Nominal		Unit
		Min	Max	Min	Max	
Timing Requirement						
t_{WFI}	General-Purpose Port Signal Input Pulse Width	t_{SCLK} + 1		t_{SCLK} + 1		ns
Switching Characteristic						
t_{GPOD}	General-Purpose Port Signal Output Delay from CLKOUT Low	0	11	0	8.5	ns

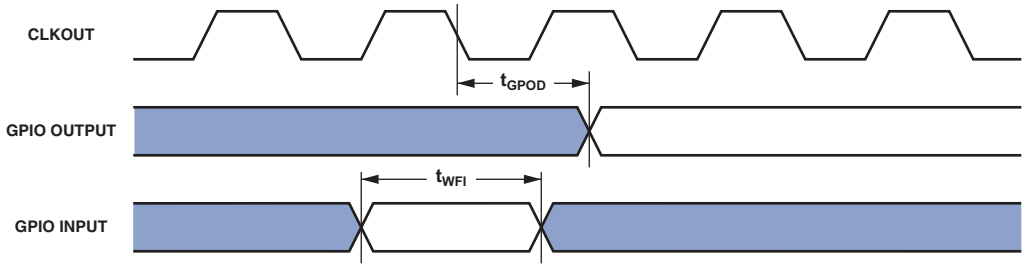


Figure 28. General-Purpose Port Timing

Timer Clock Timing

Table 40 and Figure 29 describe timer clock timing.

Table 40. Timer Clock Timing

Parameter		Min	Max	Unit
Switching Characteristic				
t_{TODP}	Timer Output Update Delay After PPICLK High		12	ns

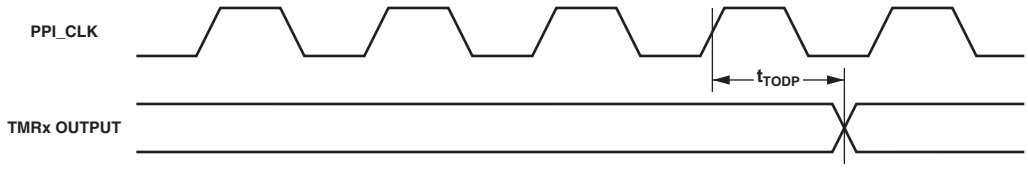


Figure 29. Timer Clock Timing

Table 47. 10/100 Ethernet MAC Controller Timing: MII/RMII Asynchronous Signal

Parameter		Min	Max	Unit
Timing Requirements				
t_{ECOLH}	COL Pulse Width High[1]	$t_{ETxCLK} \times 1.5$		ns
		$t_{ERxCLK} \times 1.5$		ns
t_{ECOLL}	COL Pulse Width Low[1]	$t_{ETxCLK} \times 1.5$		ns
		$t_{ERxCLK} \times 1.5$		ns
t_{ECRSH}	CRS Pulse Width High[2]	$t_{ETxCLK} \times 1.5$		ns
t_{ECRSL}	CRS Pulse Width Low[2]	$t_{ETxCLK} \times 1.5$		ns

[1] MII/RMII asynchronous signals are COL, CRS. These signals are applicable in both MII and RMII modes. The asynchronous COL input is synchronized separately to both the ETxCLK and the ERxCLK, and must have a minimum pulse width high or low at least 1.5 times the period of the slower of the two clocks.
[2] The asynchronous CRS input is synchronized to the ETxCLK, and must have a minimum pulse width high or low at least 1.5 times the period of ETxCLK.

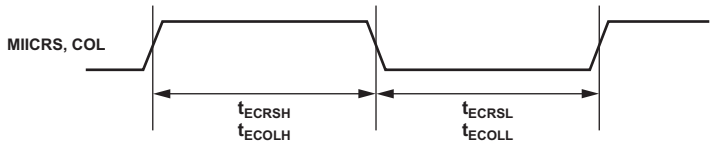


Figure 36. 10/100 Ethernet MAC Controller Timing: Asynchronous Signal

Table 48. 10/100 Ethernet MAC Controller Timing: MII Station Management

Parameter[1]		Min	Max	Unit
Timing Requirements				
t_{MDIOS}	MDIO Input Valid to MDC Rising Edge (Setup)	11.5		ns
t_{MDCIH}	MDC Rising Edge to MDIO Input Invalid (Hold)	0		ns
Switching Characteristics				
t_{MDCOV}	MDC Falling Edge to MDIO Output Valid		25	ns
t_{MDCOH}	MDC Falling Edge to MDIO Output Invalid (Hold)	–1.25		ns

[1] MDC/MDIO is a 2-wire serial bidirectional port for controlling one or more external PHYs. MDC is an output clock whose minimum period is programmable as a multiple of the system clock SCLK. MDIO is a bidirectional data line.

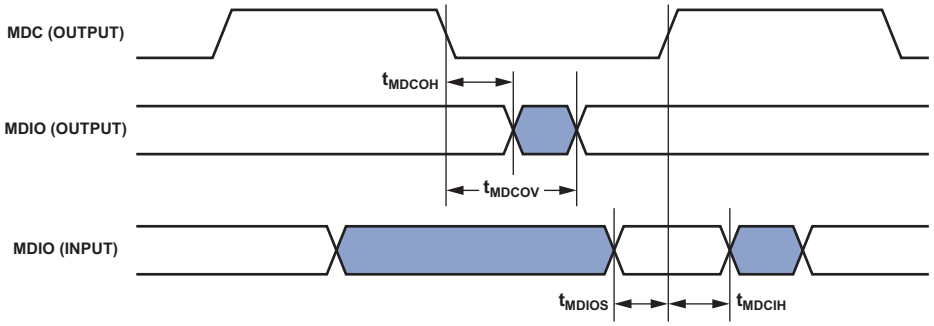


Figure 37. 10/100 Ethernet MAC Controller Timing: MII Station Management

OUTPUT DRIVE CURRENTS

Figure 39 through Figure 53 show typical current-voltage characteristics for the output drivers of the ADSP-BF51xF processors.

The curves represent the current drive capability of the output drivers. See Table 8 on Page 19 for information about which driver type corresponds to a particular ball.

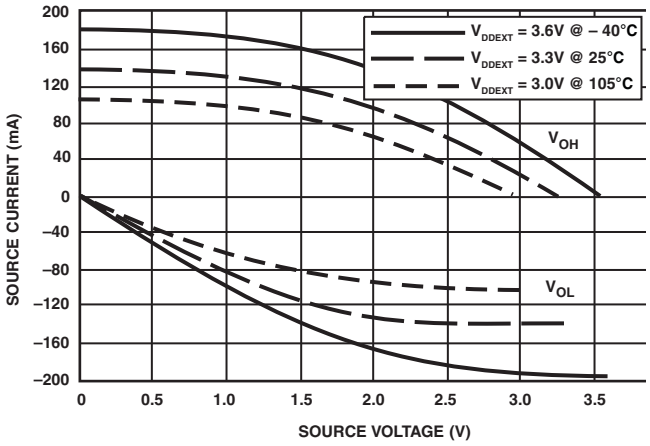


Figure 39. Driver Type A Current (3.3V V_{DDEXT}/V_{DDMEM})

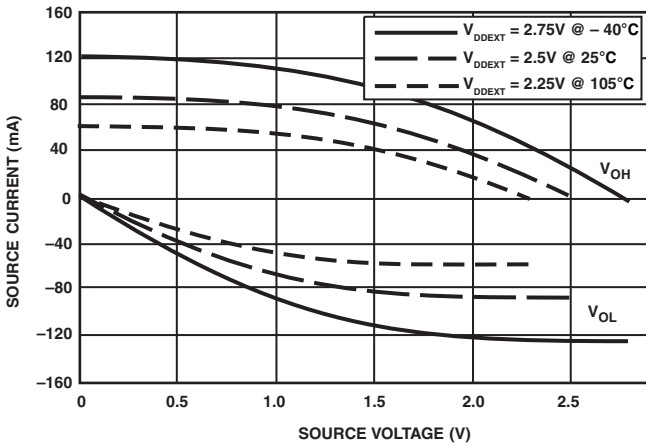


Figure 40. Driver Type A Current (2.5V V_{DDEXT}/V_{DDMEM})

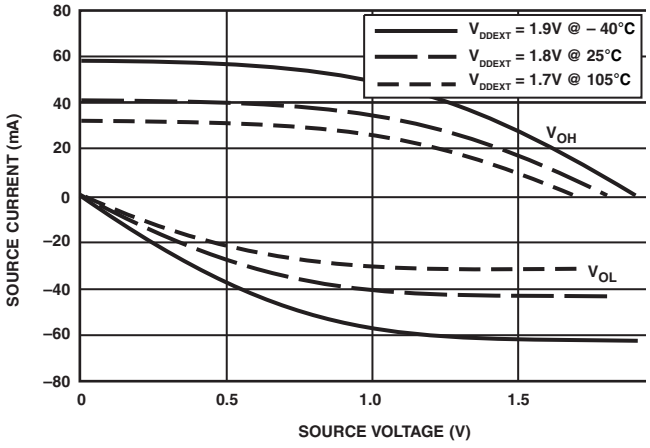


Figure 41. Driver Type A Current (1.8V V_{DDEXT}/V_{DDMEM})

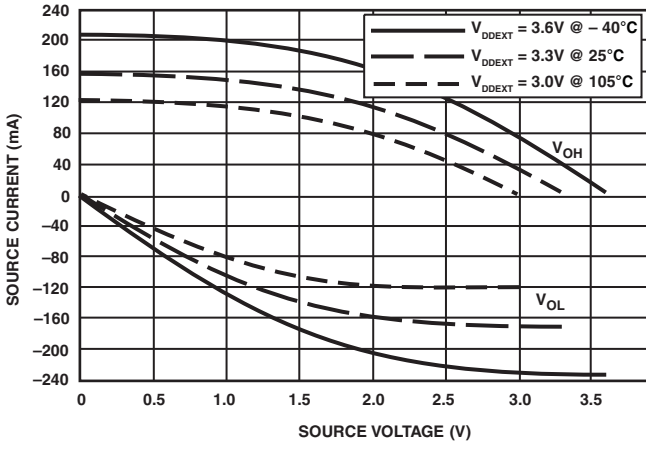


Figure 42. Driver Type B Current (3.3V V_{DDEXT}/V_{DDMEM})

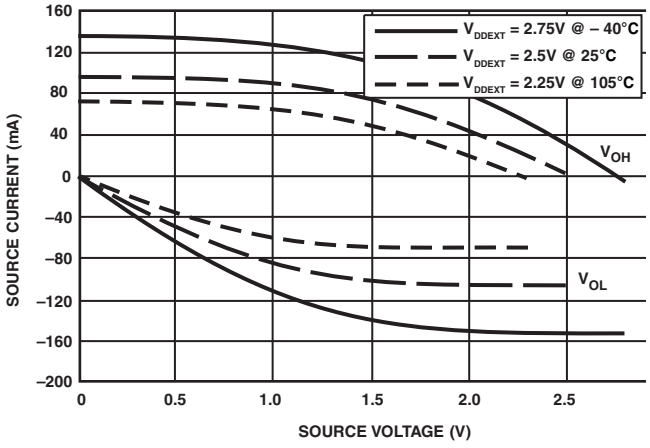


Figure 43. Driver Type B Current (2.5V V_{DDEXT}/V_{DDMEM})

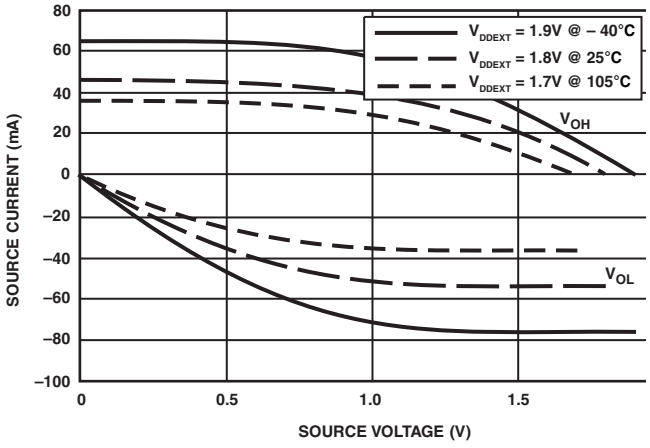


Figure 44. Driver Type B Current (1.8V V_{DDEXT}/V_{DDMEM})

Output Disable Time Measurement

Output signals are considered to be disabled when they stop driving, go into a high impedance state, and start to decay from their output high or low voltage. The output disable time t_{DIS} is the difference between $t_{DIS\_MEASURED}$ and t_{DECAY} as shown on the left side of Figure 55.

$$t_{DIS} = t_{DIS\_MEASURED} - t_{DECAY}$$

The time for the voltage on the bus to decay by ΔV is dependent on the capacitive load C_L and the load current I_L. This decay time can be approximated by the equation:

$$t_{DECAY} = (C_L \Delta V)/I_L$$

The time t_{DECAY} is calculated with test loads C_L and I_L and with ΔV equal to 0.25 V for V_{DDEXT}/V_{DDMEM} (nominal) = 2.5 V/3.3 V and 0.15 V for V_{DDEXT}/V_{VDDMEM} (nominal) = 1.8 V.

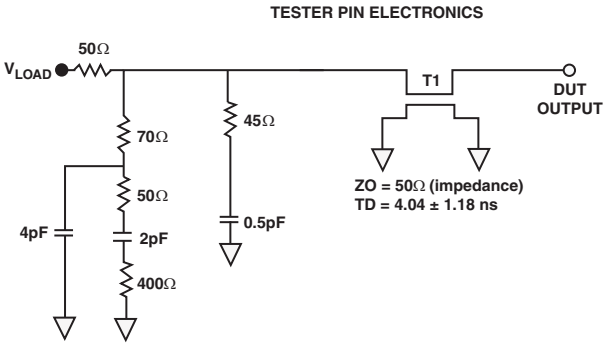
The time $t_{DIS\_MEASURED}$ is the interval from when the reference signal switches to when the output voltage decays ΔV from the measured output high or output low voltage.

Example System Hold Time Calculation

To determine the data output hold time in a particular system, first calculate t_{DECAY} using the equation given above. Choose ΔV to be the difference between the ADSP-BF51x processor's output voltage and the input threshold for the device requiring the hold time. C_L is the total bus capacitance (per data line), and I_L is the total leakage or three-state current (per data line). The hold time is t_{DECAY} plus the various output disable times as specified in the Timing Specifications on Page 29 (for example t_{DSDAT} for an SDRAM write cycle as shown in SDRAM Interface Timing on Page 33).

Capacitive Loading

Output delays and holds are based on standard capacitive loads of an average of 6 pF on all balls (see Figure 56). V_{LOAD} is equal to $(V_{DDEXT}/V_{DDMEM})/2$. The graphs of Figure 57 through Figure 68 show how output rise time varies with capacitance. The delay and hold specifications given should be derated by a factor derived from these figures. The graphs in these figures may not be linear outside the ranges shown.



NOTES:
THE WORST CASE TRANSMISSION LINE DELAY IS SHOWN AND CAN BE USED FOR THE OUTPUT TIMING ANALYSIS TO REFLECT THE TRANSMISSION LINE EFFECT AND MUST BE CONSIDERED. THE TRANSMISSION LINE (TD) IS FOR LOAD ONLY AND DOES NOT AFFECT THE DATA SHEET TIMING SPECIFICATIONS.

ANALOG DEVICES RECOMMENDS USING THE IBIS MODEL TIMING FOR A GIVEN SYSTEM REQUIREMENT. IF NECESSARY, A SYSTEM MAY INCORPORATE EXTERNAL DRIVERS TO COMPENSATE FOR ANY TIMING DIFFERENCES.

Figure 56. Equivalent Device Loading for AC Measurements (Includes All Fixtures)

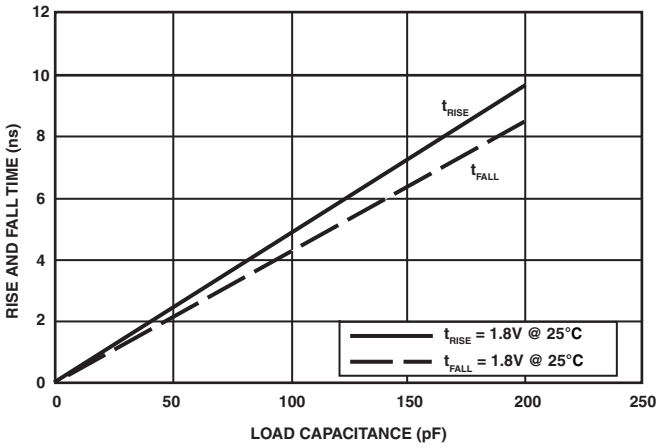


Figure 57. Driver Type A Typical Rise and Fall Times (10%–90%) vs. Load Capacitance (1.8V V_{DDEXT}/V_{DDMEM})

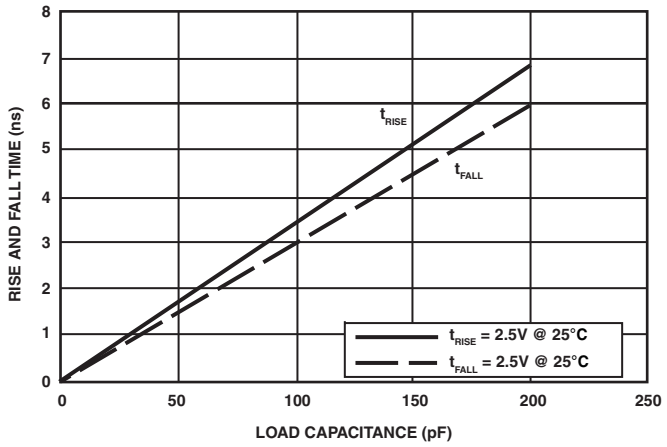


Figure 58. Driver Type A Typical Rise and Fall Times (10%–90%) vs. Load Capacitance (2.5V V_{DDEXT}/V_{DDMEM})

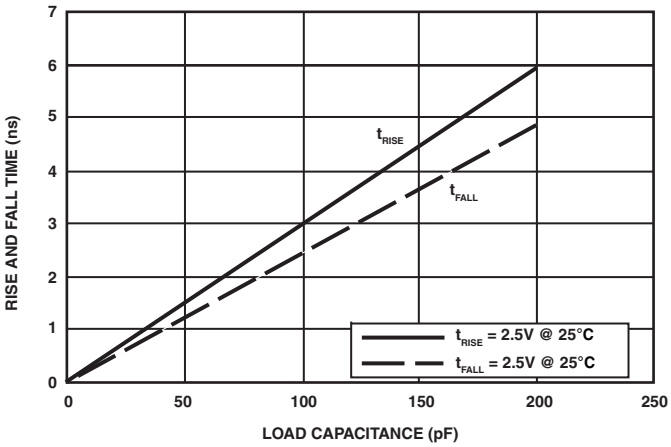


Figure 61. Driver Type B Typical Rise and Fall Times (10%–90%) vs. Load Capacitance (2.5V V_{DDEXT}/V_{DDMEM})

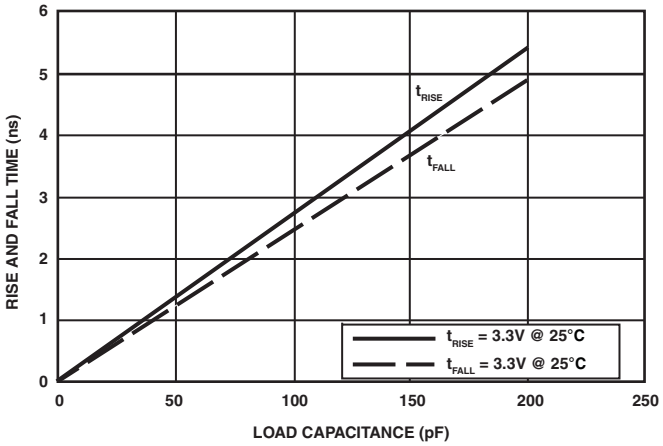


Figure 59. Driver Type A Typical Rise and Fall Times (10%–90%) vs. Load Capacitance (3.3V V_{DDEXT}/V_{DDMEM})

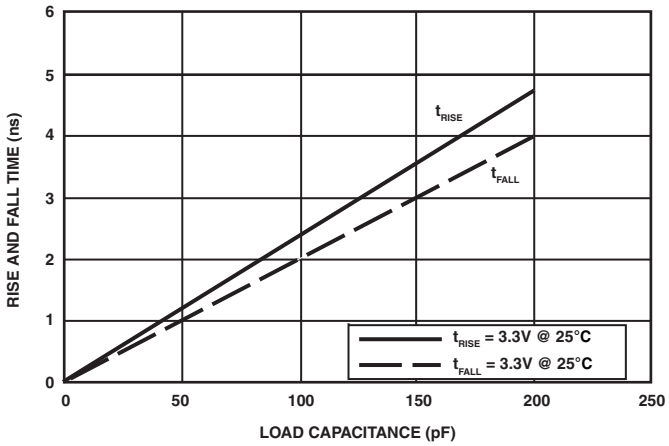


Figure 62. Driver Type B Typical Rise and Fall Times (10%–90%) vs. Load Capacitance (3.3V V_{DDEXT}/V_{DDMEM})

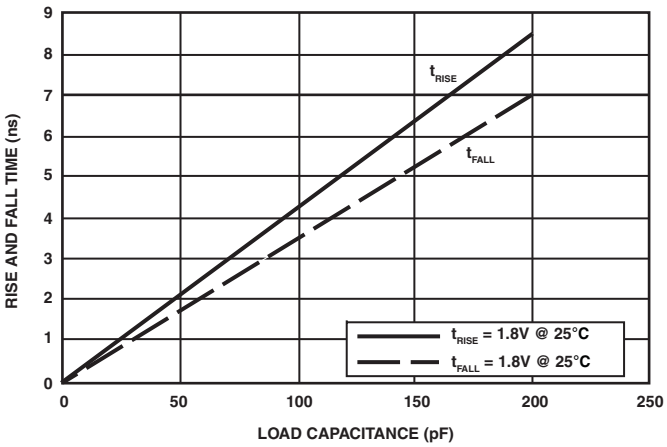


Figure 60. Driver Type B Typical Rise and Fall Times (10%–90%) vs. Load Capacitance (1.8V V_{DDEXT}/V_{DDMEM})

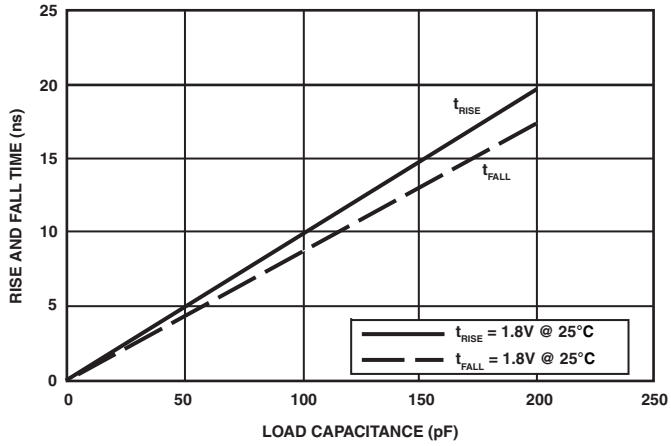


Figure 63. Driver Type C Typical Rise and Fall Times (10%–90%) vs. Load Capacitance (1.8V V_{DDEXT}/V_{DDMEM})

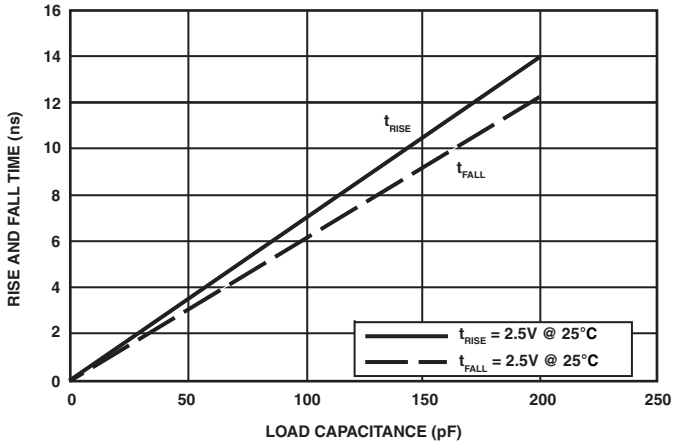


Figure 64. Driver Type C Typical Rise and Fall Times (10%–90%) vs. Load Capacitance (2.5V V_{DDEXT}/V_{DDMEM})

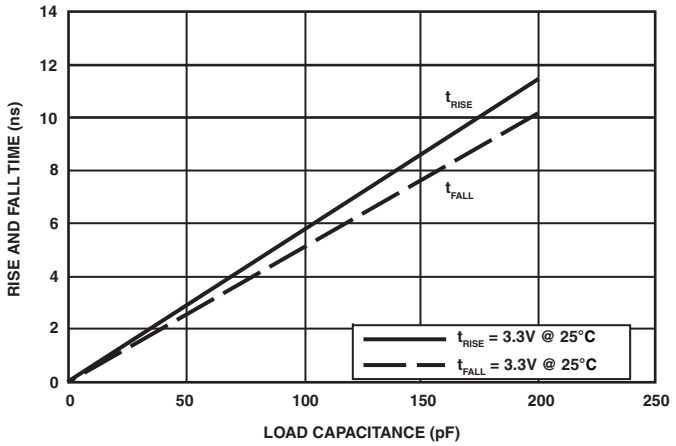


Figure 65. Driver Type C Typical Rise and Fall Times (10%–90%) vs. Load Capacitance (3.3V V_{DDEXT}/V_{DDMEM})

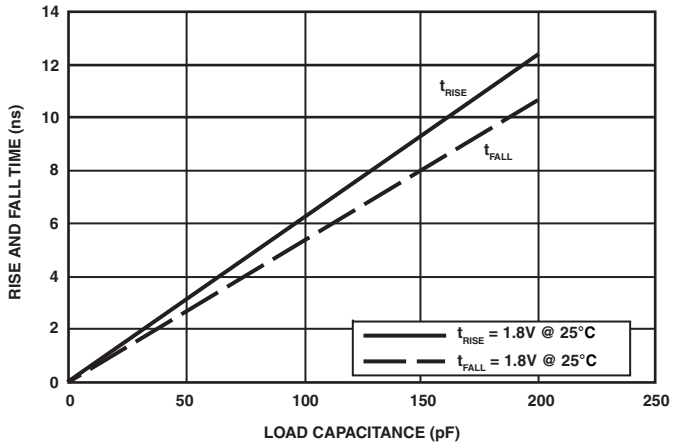


Figure 66. Driver Type D Typical Rise and Fall Times (10%–90%) vs. Load Capacitance (1.8V V_{DDEXT}/V_{DDMEM})

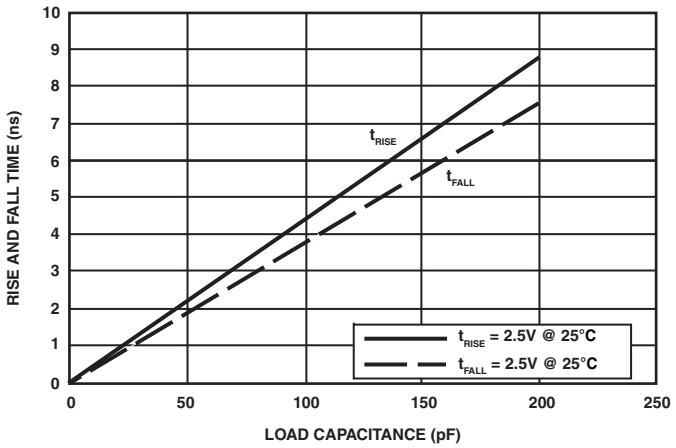


Figure 67. Driver Type D Typical Rise and Fall Times (10%–90%) vs. Load Capacitance (2.5V V_{DDEXT}/V_{DDMEM})

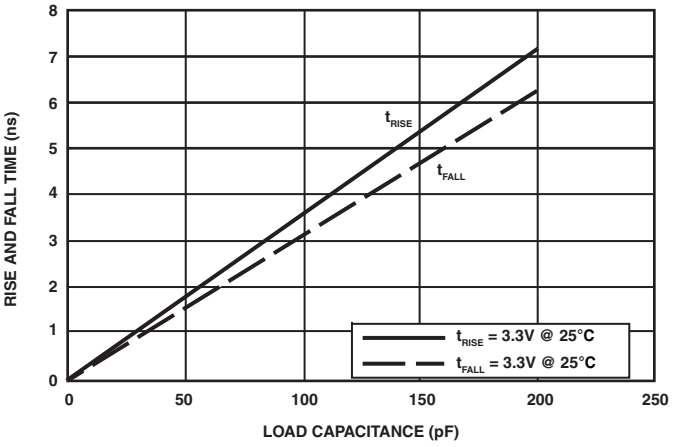


Figure 68. Driver Type D Typical Rise and Fall Times (10%–90%) vs. Load Capacitance (3.3V V_{DDEXT}/V_{DDMEM})

THERMAL CHARACTERISTICS

To determine the junction temperature on the application printed circuit board use:

$$T_J = T_{CASE} + (\Psi_{JT} \times P_D)$$

where:

T_J = Junction temperature (°C)

T_{CASE} = Case temperature (°C) measured by customer at top center of package.

Ψ_{JT} = From Table 51

P_D = Power dissipation (see Total Power Dissipation on Page 25 for the method to calculate P_D)

Values of θ_{JA} are provided for package comparison and printed circuit board design considerations. θ_{JA} can be used for a first order approximation of T_J by the equation:

$$T_J = T_A + (\theta_{JA} \times P_D)$$

where:

T_A = Ambient temperature (°C)

Values of θ_{JC} are provided for package comparison and printed circuit board design considerations when an external heat sink is required.

Values of θ_{JB} are provided for package comparison and printed circuit board design considerations.

In Table 51, airflow measurements comply with JEDEC standards JESD51-2 and JESD51-6, and the junction-to-board measurement complies with JESD51-8. The junction-to-case measurement complies with MIL-STD-883 (Method 1012.1). All measurements use a 2S2P JEDEC test board.

The LQFP_EP package requires thermal trace squares and thermal vias to an embedded ground plane in the PCB. The paddle must be connected to ground for proper operation to data sheet specifications. Refer to JEDEC standard JESD51-5 for more information.

Table 50. Thermal Characteristics for SQ-176-2 Package

Parameter	Condition	Typical	Unit
θ_{JA}	0 Linear m/s Airflow	17.4	°C/W
θ_{JMA}	1 Linear m/s Airflow	14.8	°C/W
θ_{JMA}	2 Linear m/s Airflow	14.0	°C/W
θ_{JC}	Not Applicable	7.8	°C/W
Ψ_{JT}	0 Linear m/s Airflow	0.28	°C/W
Ψ_{JT}	1 Linear m/s Airflow	0.39	°C/W
Ψ_{JT}	2 Linear m/s Airflow	0.48	°C/W

Table 51. Thermal Characteristics for BC-168-1 Package

Parameter	Condition	Typical	Unit
θ_{JA}	0 Linear m/s Airflow	30.5	°C/W
θ_{JMA}	1 Linear m/s Airflow	27.6	°C/W
θ_{JMA}	2 Linear m/s Airflow	26.3	°C/W
θ_{JC}	Not Applicable	11.1	°C/W
Ψ_{JT}	0 Linear m/s Airflow	0.20	°C/W
Ψ_{JT}	1 Linear m/s Airflow	0.35	°C/W
Ψ_{JT}	2 Linear m/s Airflow	0.45	°C/W

168-BALL CSP_BGA BALL ASSIGNMENT

Table 54 lists the CSP_BGA by ball number. Table 55 on Page 63 lists the CSP_BGA balls by signal mnemonic.

Table 54. 168-Ball CSP_BGA Ball Assignment (Numerical by Ball Number)

Ball No.	Signal Name	Ball No.	Signal Name	Ball No.	Signal Name	Ball No.	Signal Name	Ball No.	Signal Name	Ball No.	Signal Name
A1	GND	C1	PF4	E10	V_{DDINT}	H1	PG12	K6	V_{DDMEM}	N1	BMODE1
A2	SCL	C2	PF7	E12	V_{DDMEM}	H2	PG13	K7	V_{DDMEM}	N2	PG1
A3	SDA	C3	PF8	E13	$\overline{ARE}$	H3	PG11	K8	V_{DDMEM}	N3	TDO
A4	PF13	C4	PF10	E14	$\overline{AWE}$	H5	V_{DDEXT}	K9	V_{DDMEM}	N4	$\overline{TRST}$
A5	PF15	C5	V_{DDEXT}	F1	PF0	H6	GND	K10	V_{DDMEM}	N5	TMS
A6	PH2	C6	V_{DDEXT}	F2	PF1	H7	GND	K12	A8	N6	D13
A7	PH1	C7	PF11	F3	V_{DDINT}	H8	GND	K13	A2	N7	D9
A8	PH5	C8	V_{DDEXT}	F5	V_{DDEXT}	H9	GND	K14	A1	N8	D5
A9	PH6	C9	V_{DDINT}	F6	GND	H10	V_{DDINT}	L1	PG5	N9	D1
A10	PH7	C10	V_{DDEXT}	F7	GND	H12	A3	L2	PG3	N10	A18
A11	CLKBUF	C11	RTXI	F8	GND	H13	$\overline{ABE}$0	L3	PG2	N11	A16
A12	XTAL	C12	RTXO	F9	GND	H14	$\overline{SCAS}$	L12	A9	N12	A14
A13	CLKIN	C13	$\overline{PG}$	F10	V_{DDINT}	J1	PG10	L13	A6	N13	A11
A14	GND	C14	NC[1]	F12	$\overline{SMS}$	J2	$V_{DDFLASH}$	L14	A4	N14	A7
B1	V_{DDOTP}	D1	PF3	F13	SCKE	J3	PG9	M1	PG4	P1	GND
B2	GND	D2	PF5	F14	$\overline{AMS}$1	J5	V_{DDMEM}	M2	BMODE2	P2	TDI
B3	PF9	D3	VPPOTP	G1	PG15	J6	GND	M3	BMODE0	P3	TCK
B4	PF12	D12	$V_{DDFLASH}$	G2	PG14	J7	GND	M4	PG0	P4	D15
B5	PF14	D13	CLKOUT	G3	V_{DDINT}	J8	GND	M5	$\overline{EMU}$	P5	D14
B6	PH0	D14	$\overline{AMS}$0	G5	V_{DDEXT}	J9	GND	M6	D12	P6	D11
B7	PH3	E1	$V_{DDFLASH}$	G6	GND	J10	V_{DDINT}	M7	D10	P7	D8
B8	PH4	E2	PF2	G7	GND	J12	A15	M8	D2	P8	D7
B9	V_{DDEXT}	E3	PF6	G8	GND	J13	$\overline{ABE}$1	M9	D0	P9	D6
B10	$\overline{RESET}$	E5	V_{DDEXT}	G9	GND	J14	SA10	M10	A17	P10	D4
B11	$\overline{NMI}$	E6	V_{DDEXT}	G10	V_{DDINT}	K1	PG6	M11	A13	P11	D3
B12	V_{DDRTC}	E7	V_{DDINT}	G12	$\overline{SWE}$	K2	PG8	M12	A12	P12	A19
B13	V_{DDEXT}	E8	V_{DDINT}	G13	$\overline{SRAS}$	K3	PG7	M13	A10	P13	GND
B14	EXT_WAKE	E9	V_{DDINT}	G14	GND	K5	V_{DDMEM}	M14	A5	P14	GND

[1] This pin must not be connected.

Model[1]	Temperature Range[2]	Processor Instruction Rate (Max)	Flash Memory	Package Description	Package Option
ADSP-BF516BBCZ-3	–40°C to +85°C	300 MHz	N/A	168-Ball CSP_BGA	BC-168-1
ADSP-BF516BBCZ-4	–40°C to +85°C	400 MHz	N/A	168-Ball CSP_BGA	BC-168-1
ADSP-BF516BSWZ-3	–40°C to +85°C	300 MHz	N/A	176-Lead LQFP_EP	SQ-176-2
ADSP-BF516BSWZ-4	–40°C to +85°C	400 MHz	N/A	176-Lead LQFP_EP	SQ-176-2
ADSP-BF518BBCZ-4	–40°C to +85°C	400 MHz	N/A	168-Ball CSP_BGA	BC-168-1
ADSP-BF518BBCZ4F16	–40°C to +85°C	400 MHz	16M bit	168-Ball CSP_BGA	BC-168-1
ADSP-BF518BSWZ-4	–40°C to +85°C	400 MHz	N/A	176-Lead LQFP_EP	SQ-176-2
ADSP-BF518BSWZ4F16	–40°C to +85°C	400 MHz	16M bit	176-Lead LQFP_EP	SQ-176-2

[1] Z = RoHS compliant part.

[2] Referenced temperature is ambient temperature. The ambient temperature is not a specification. Please see Operating Conditions on Page 22 for junction temperature (T_J) specification which is the only temperature specification.

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