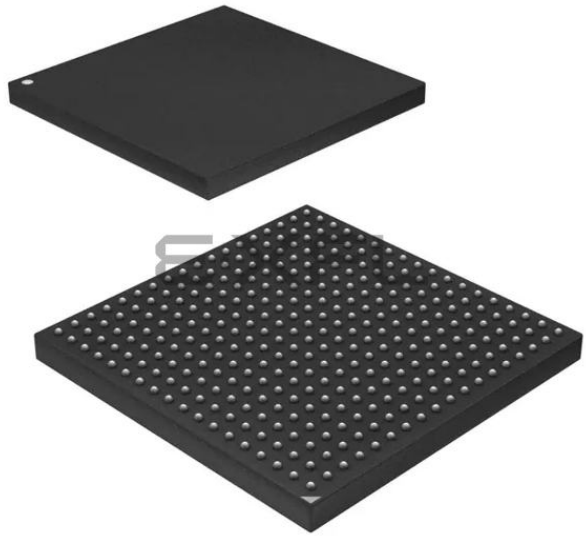

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM926EJ-S
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	400MHz
Co-Processors/DSP	-
RAM Controllers	LPDDR, LPSDR, DDR2, SDR, SRAM
Graphics Acceleration	No
Display & Interface Controllers	LCD, Touchscreen, Video Decoder
Ethernet	10/100Mbps
SATA	-
USB	USB 2.0 (3)
Voltage - I/O	1.8V, 3.3V
Operating Temperature	-40°C ~ 85°C (TA)
Security Features	-
Package / Case	324-TFBGA
Supplier Device Package	324-TFBGA (15x15)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/at91sam9m10c-cu-999

Table 3-1. Signal Description List (Continued)

Signal Name	Function	Type	Active Level	Reference Voltage	Comments
Shutdown, Wakeup Logic					
SHDN	Shut-Down Control	Output		VDDBU	Driven at 0V only. 0: The device is in backup mode 1: The device is running (not in backup mode).
WKUP	Wake-Up Input	Input		VDDBU	Accept between 0V and VDDBU.
ICE and JTAG					
TCK	Test Clock	Input		VDDIOP0	No pull-up resistor, Schmitt trigger
TDI	Test Data In	Input		VDDIOP0	No pull-up resistor, Schmitt trigger
TDO	Test Data Out	Output		VDDIOP0	
TMS	Test Mode Select	Input		VDDIOP0	No pull-up resistor, Schmitt trigger
JTAGSEL	JTAG Selection	Input		VDDBU	Pull-down resistor (15 kΩ).
RTCK	Return Test Clock	Output		VDDIOP0	
Reset/Test					
NRST	Microcontroller Reset[2]	I/O	Low	VDDIOP0	Open drain output Pull-Up resistor (100 kΩ), Schmitt trigger
TST	Test Mode Select	Input		VDDBU	Pull-down resistor (15 kΩ), Schmitt trigger
NTRST	Test Reset Signal	Input		VDDIOP0	Pull-Up resistor (100 kΩ), Schmitt trigger
BMS	Boot Mode Select	**Input**		VDDIOP0	must be connected to GND or VDDIOP0.
Debug Unit - DBGU					
DRXD	Debug Receive Data	Input		[1]	
DTXD	Debug Transmit Data	Output		[1]	
Advanced Interrupt Controller - AIC					
IRQ	External Interrupt Input	Input		[1]	
FIQ	Fast Interrupt Input	Input		[1]	
PIO Controller - PIOA- PIOB - PIOC - PIOD - PIOE					
PA0 - PA31	Parallel IO Controller A	I/O		[1]	Pulled-up input at reset (100kΩ)[3], Schmitt trigger
PB0 - PB31	Parallel IO Controller B	I/O		[1]	Pulled-up input at reset (100kΩ)[3], Schmitt trigger
PC0 - PC31	Parallel IO Controller C	I/O		[1]	Pulled-up input at reset (100kΩ)[3], Schmitt trigger

Table 3-1. Signal Description List (Continued)

Signal Name	Function	Type	Active Level	Reference Voltage	Comments
Ethernet 10/100					
ETXCK	Transmit Clock or Reference Clock	Input		(1)	MII only, REFCK in RMII
ERXCK	Receive Clock	Input		(1)	MII only
ETXEN	Transmit Enable	Output		(1)	
ETX0-ETX3	Transmit Data	Output		(1)	ETX0-ETX1 only in RMII
ETXER	Transmit Coding Error	Output		(1)	MII only
ERXDV	Receive Data Valid	Input		(1)	RXDV in MII, CRSDV in RMII
ERX0-ERX3	Receive Data	Input		(1)	ERX0-ERX1 only in RMII
ERXER	Receive Error	Input		(1)	
ECRS	Carrier Sense and Data Valid	Input		(1)	MII only
ECOL	Collision Detect	Input		(1)	MII only
EMDC	Management Data Clock	Output		(1)	
EMDIO	Management Data Input/Output	I/O		(1)	
Image Sensor Interface					
ISI_D0-ISI_D11	Image Sensor Data	Input		VDDIOP2	
ISI_MCK	Image sensor Reference clock	output		VDDIOP2	
ISI_HSYNC	Image Sensor Horizontal Synchro	input		VDDIOP2	
ISI_VSYNC	Image Sensor Vertical Synchro	input		VDDIOP2	
ISI_PCK	Image Sensor Data clock	input		VDDIOP2	
LCD Controller - LCDC					
LCDD0 - LCDD23	LCD Data Bus	Output		VDDIOP1	
LCDVSYNC	LCD Vertical Synchronization	Output		VDDIOP1	
LCDHSYNC	LCD Horizontal Synchronization	Output		VDDIOP1	
LCDDOTCK	LCD Dot Clock	Output		VDDIOP1	
LCDDEN	LCD Data Enable	Output		VDDIOP1	
LCDCC	LCD Contrast Control	Output		VDDIOP1	
LCDPWR	LCD panel Power enable control	Output		VDDIOP1	
LCDMOD	LCD Modulation signal	Output		VDDIOP1	
Touch Screen Analog-to-Digital Converter					
$AD0X_P$	Analog input channel 0 or Touch Screen Top channel	Analog		VDDANA	Multiplexed with AD0
$AD1X_M$	Analog input channel 1 or Touch Screen Bottom channel	Analog		VDDANA	Multiplexed with AD1
$AD2Y_P$	Analog input channel 2 or Touch Screen Right channel	Analog		VDDANA	Multiplexed with AD2
$AD3Y_M$	Analog input channel 3 or Touch Screen Left channel	Analog		VDDANA	Multiplexed with AD3

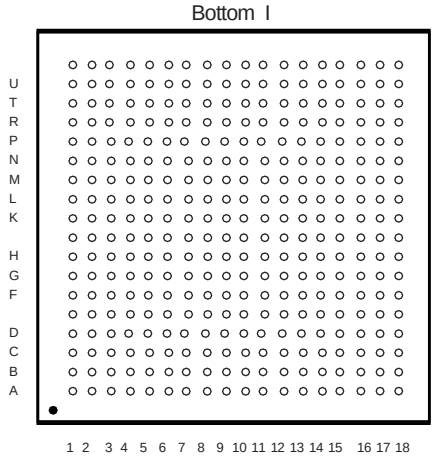
4. Package and Pinout

The SAM9M10 is delivered in a 324-ball TFBGA package.

4.1 Mechanical Overview of the 324-ball TFBGA Package

Figure 4-1 shows the orientation of the 324-ball TFBGA Package

Figure 4-1. Orientation of the 324-ball TFBGA Package



4.2 324-ball TFBGA Package Pinout

Table 4-1. SAM9M10 Pinout for 324-ball BGA Package

Pin	Signal Name
A1	PC27
A2	PC28
A3	PC25
A4	PC20
A5	PC12
A6	PC7
A7	PC5
A8	PC0
A9	NWR3/NBS3
A10	NCS0
A11	DQS0
A12	RAS
A13	SDCK
A14	NSDCK
A15	D7
A16	DDR_VREF
A17	D0
A18	A14
B1	PC31
B2	PC29
B3	PC30
B4	PC22
B5	PC17
B6	PC10
B7	PC11
B8	PC2
B9	SDA10
B10	A17/BA1
B11	DQM0
B12	SDCKE
B13	D12
B14	D8
B15	D4
B16	D3
B17	A15
B18	A13
C1	XIN32

Pin	Signal Name
E10	NANDWE
E11	DQS1
E12	D13
E13	D11
E14	A4
E15	A8
E16	A9
E17	A7
E18	VDDCORE
F1	PD22
F2	PD24
F3	SHDN
F4	PE1
F5	PE3
F6	VDDIOM1
F7	PC19
F8	PC14
F9	PC4
F10	NCS1/SDCS
F11	NRD
F12	SDWE
F13	A0/NBS0
F14	A1/NBS2/NWR2
F15	A3
F16	A6
F17	A5
F18	A2
G1	PD25
G2	PD23
G3	PE6
G4	PE0
G5	PE2
G6	PE8
G7	PE4
G8	PE11
G9	GNDCORE
G10	VDDIOM1

Pin	Signal Name
K1	PE21
K2	PE23
K3	PE26
K4	PE22
K5	PE24
K6	PE25
K7	PE27
K8	PE28
K9	VDDIOP0
K10	VDDIOP0
K11	GNDIOM
K12	GNDIOM
K13	VDDIOM0
K14	DDR_A7
K15	DDR_A8
K16	DDR_A9
K17	DDR_A11
K18	DDR_A10
L1	PA0
L2	PE30
L3	PE29
L4	PE31
L5	PA2
L6	PA4
L7	PA8
L8	PD2
L9	PD13
L10	PD29
L11	PD31
L12	VDDIOM0
L13	VDDIOM0
L14	DDR_A1
L15	DDR_A3
L16	DDR_A4
L17	DDR_A6
L18	DDR_A5
M1	PA1

Pin	Signal Name
P10	TMS
P11	VDDPLLA
P12	PB20
P13	PB31
P14	DDR_D7
P15	DDR_D3
P16	DDR_D4
P17	DDR_D5
P18	DDR_D10
R1	PA18
R2	PA20
R3	PA24
R4	PA30
R5	PB4
R6	PB13
R7	PD0
R8	PD9
R9	PD18
R10	TDI
R11	RTCK
R12	PB22
R13	PB29
R14	DDR_D6
R15	DDR_D1
R16	DDR_D0
R17	HHSDMA
R18	HFSDMA
T1	PA22
T2	PA25
T3	PA26
T4	PB0
T5	PB6
T6	PB16
T7	PD1
T8	PD11
T9	PD19
T10	PD30

Figure 6-1. Video Mode Configuration

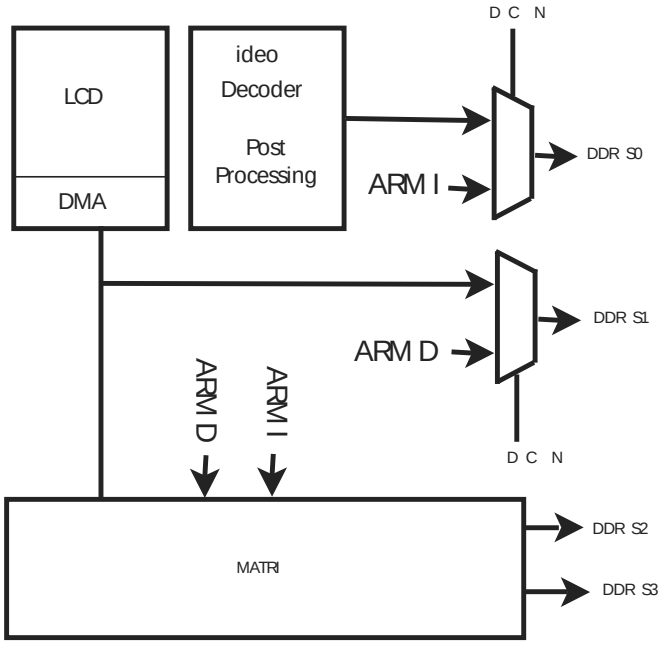


Table 6-3. SAM9M10 Masters to Slaves Access with VDEC_SEL = 0

Master		0	1	2	3	4 & 5	6	7	8	9	10	11
Slave		ARM 926 Instr.	ARM 926 Data	PDC	USB Host OHCI	DMA	ISI DMA	LCD DMA	Etherne t MAC	USB Device HS	USB Host EHCI	VDEC
0	Internal SRAM 0	X	X	X	X	X	X	-	X	X	X	-
	Internal ROM	X	X	X	-	-	-	-	-	X	-	-
	UHP OHCI	X	X	-	-	-	-	-	-	-	-	-
	UHP EHCI	X	X	-	-	-	-	-	-	-	-	-
	LCD User Int.	X	X	-	-	-	-	-	-	-	-	-
	UDPHS RAM	X	X	-	-	-	-	-	-	-	-	-
1	VDEC	X	X	-	-	-	-	-	-	-	-	-
2	DDR Port 0	X	-	-	-	-	-	-	-	-	-	-
3	DDR Port 1	-	X	-	-	-	-	-	-	-	-	-
4	DDR Port 2	-	-	X	X	X	X	-	X	X	X	X
5	DDR Port 3	-	-	X	X	X	X	X	X	X	X	-
6	EBI	X	X	X	X	X	X	X	X	X	X	X
7	Internal Periph.	X	X	X	-	X	-	-	-	-	-	-

Table 6-4. SAM9M10 Masters to Slaves Access with VDEC_SEL = 1 (default)

Master		0	1	2	3	4 & 5	6	7	8	9	10	11
Slave		ARM 926 Instr.	ARM 926 Data	PDC	USB HOST OHCI	DMA	ISI DMA	LCD DMA	Ethernet MAC	USB Device HS	USB Host EHCI	VDEC
0	Internal SRAM 0	X	X	X	X	X	X	-	X	X	X	-
1	Internal ROM	X	X	X	-	-	-	-	-	X	-	-
	UHP OHCI	X	X	-	-	-	-	-	-	-	-	-
	UHP EHCI	X	X	-	-	-	-	-	-	-	-	-
	LCD User Int.	X	X	-	-	-	-	-	-	-	-	-
	UDPHS RAM	X	X	-	-	-	-	-	-	-	-	-
	VDEC	X	X	-	-	-	-	-	-	-	-	-
2	DDR Port 0	-	-	-	-	-	-	-	-	-	-	X
3	DDR Port 1	-	-	-	-	-	-	X	-	-	-	-
4	DDR Port 2	X	-	X	X	X	X	-	X	X	X	-
5	DDR Port 3	-	X	X	X	X	X	-	X	X	X	-
6	EBI	X	X	X	X	X	X	X	X	X	X	X
7	Internal Periph.	X	X	X	-	X	-	-	-	-	-	-

Table 6-5 summarizes the Slave Memory Mapping for each connected Master, depending on the Remap status (RCBx bit in Bus Matrix Master Remap Control Register MATRIX_MRCR) and the BMS state at reset.

Table 6-5. Internal Memory Mapping

	Master		
Slave Base Address	RCBx = 0		RCBx = 1
	BMS = 1	BMS = 0	
0x0000 0000	Internal ROM	EBI NCS0	Internal SRAM

6.3 Peripheral DMA Controller (PDC)

- Acting as one AHB Bus Matrix Master
- Allows data transfers from/to peripheral to/from any memory space without any intervention of the processor.
- Next Pointer support, prevents strong real-time constraints on buffer management.

The Peripheral DMA Controller handles transfer requests from the channel according to the following priorities (Low to High priorities):

Table 6-6. Peripheral DMA Controller

Instance name	Channel T/R
DBGU	Transmit
USART3	Transmit
USART2	Transmit
USART1	Transmit
USART0	Transmit
AC97C	Transmit
SPI1	Transmit

Table 6-6. Peripheral DMA Controller

Instance name	Channel T/R
SPI0	Transmit
SSC1	Transmit
SSC0	Transmit
TSADCC	Receive
DBGU	Receive
USART3	Receive
USART2	Receive
USART1	Receive
USART0	Receive
AC97C	Receive
SPI1	Receive
SPI0	Receive
SSC1	Receive
SSC0	Receive

6.4 USB

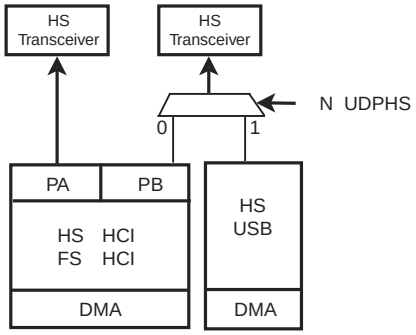
The SAM9M10 features USB communication ports as follows:

- 2 Ports USB Host full speed OHCI and High speed EHCI
- 1 Device High speed

USB Host Port A is directly connected to the first UTMI transceiver.

The Host Port B is multiplexed with the USB device High speed and connected to the second UTMI port. The selection between Host Port B and USB device high speed is controlled by a the bit UDPHS enable bit located in the UDPHS_CTRL control register.

Figure 6-2. USB Selection



6.5 DMA Controller

- Two Masters
- Embeds 8 channels
- 64 bytes/FIFO for Channel Buffering
- Linked List support with Status Write Back operation at End of Transfer
- Word, HalfWord, Byte transfer support.

- Internal SRAM C is only accessible by all the AHB Masters. After reset and until the Remap Command is performed, this SRAM block is accessible through the AHB bus at address 0x0030 0000 by all the AHB Masters. After Remap, this SRAM block also becomes accessible through the AHB bus at address 0x0 by the ARM926 Instruction and the ARM926 Data Masters.

Within the 64 Kbyte SRAM size available, the amount of memory assigned to each block is software programmable according to Table 7-1.

Table 7-1. ITCM and DTCM Memory Configuration

SRAM A ITCM size (KBytes) seen at 0x100000 through AHB	SRAM B DTCM size (KBytes) seen at 0x200000 through AHB	SRAM C (KBytes) seen at 0x300000 through AHB
0	0	64
0	64	0
32	32	0

7.2.3 Internal ROM

The SAM9M10 embeds an Internal ROM, which contains the bootrom and SAM-BA program.

At any time, the ROM is mapped at address 0x0040 0000. It is also accessible at address 0x0 (BMS =1) after the reset and before the Remap Command.

7.2.4 Boot Strategies

The system always boots at address 0x0. To ensure maximum boot possibilities the memory layout can be changed with two parameters.

REMAP allows the user to layout the internal SRAM bank to 0x0 to ease the development. This is done by software once the system has boot.

BMS allows the user to lay out to 0x0, when convenient, the ROM or an external memory. This is done by a hardware way at reset.

Note: All the memory blocks can always be seen at their specified base addresses that are not concerned by these parameters.

The SAM9M10 Bus Matrix manages a boot memory that depends on the level on the pin BMS at reset. The internal memory area mapped between address 0x0 and 0x000F FFFF is reserved to this effect.

If BMS is detected at 1, the boot memory is the embedded ROM.

If BMS is detected at 0, the boot memory is the memory connected on the Chip Select 0 of the External Bus Interface.

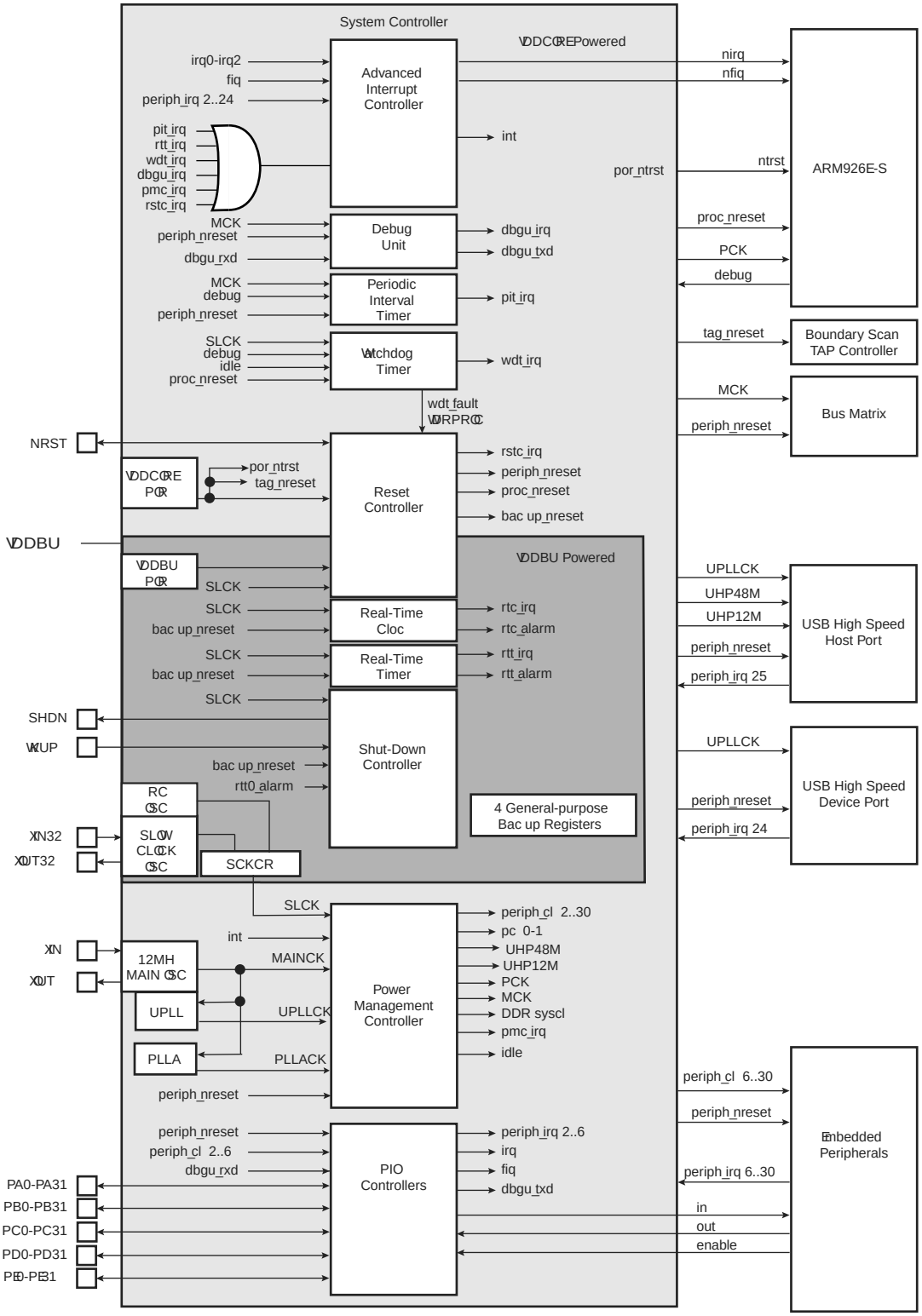
7.2.4.1 BMS = 1, boot on embedded ROM

The system boots on Boot Program.

- Boot on on-chip RC
- Enable the 32768 Hz oscillator
- Auto baudrate detection
- Downloads and runs an application from external storage media into internal SRAM
- Downloaded code size depends on embedded SRAM size
- Automatic detection of valid application
- Bootloader on a non-volatile memory
  - SPI DataFlash/SerialFlash connected on NPCS0 of the SPI0
  - SDCard
  - NandFlash
  - EEPROM connected on TWI0

8.2 System Controller Block Diagram

Figure 8-1. SAM9M10 System Controller Block Diagram



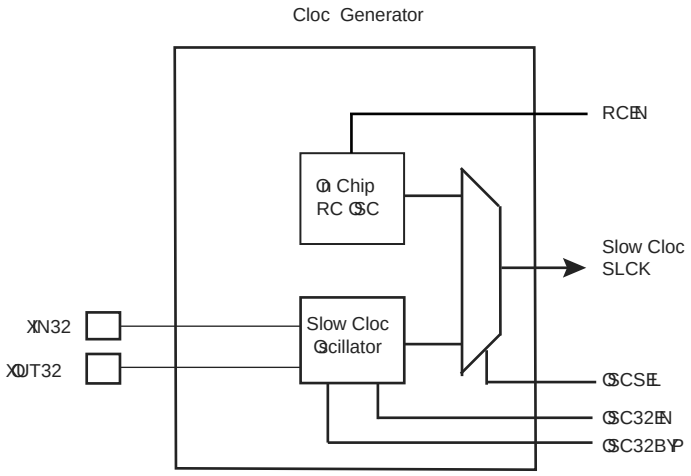
8.6 Slow Clock Selection

The SAM9M10 slow clock can be generated either by an external 32768Hz crystal or the on-chip RC oscillator. The 32768 Hz crystal oscillator can be bypassed, by setting the bit OSC32BYP, to accept an external slow clock on XIN32.

The internal RC oscillator and the 32768 Hz oscillator can be enabled by setting to 1 respectively RCEN bit and OSC32EN bit in the system controller user interface. OSCSEL command selects the slow clock source.

RCEN, OSC32EN,OSCSEL and OSC32BYP bits are located in the slow clock control register (SCKCR) located at address 0xFFFFFD50 in the backup part of the system controller and so are preserved while VDDBU is present.

Figure 8-3. Slow Clock



After a VDDBU power on reset, the default configuration is RCEN = 1, OSC32EN = 0 and OSCSEL = 0 allowing the system to start on the internal RC oscillator.

The programmer controls by software the slow clock switching and so must take precautions during the switching phase.

8.6.1 Switch from Internal RC Oscillator to the 32768 Hz Crystal

To switch from internal RC oscillator to the 32768 Hz crystal, the programmer must execute the following sequence:

- Switch the master clock to a source different from slow clock (PLLA or PLLB or Main Oscillator) through the Power Management Controller.
- Enable the 32768 Hz oscillator by setting the bit OSCEN to 1.
- Wait 32768 Hz startup time for clock stabilization (software loop).
- Switch from internal RC to 32768 Hz by setting the bit OSCSEL to 1.
- Wait 5 slow clock cycles for internal resynchronization.
- Disable the RC oscillator by setting the bit RCEN to 0.

8.6.2 Bypass the 32768 Hz Oscillator

The following step must be added to bypass the 32768 Hz Oscillator.

- An external clock must be connected on XIN32.
- Enable the bypass path OSC32BYP bit set to 1.
- Disable the 32768 Hz oscillator by setting the bit OSC32EN to 0.

8.6.3 Switch from 32768 Hz Crystal to the Internal RC Oscillator

The same procedure must be followed to switch from 32768 Hz crystal to the internal RC oscillator.

- Switch the master clock to a source different from slow clock (PLLA or PLLB or Main Oscillator).
- Enable the internal RC oscillator by setting the bit RCEN to 1.

- Wait internal RC Startup Time for clock stabilization (software loop).
- Switch from 32768 Hz oscillator to internal RC oscillator by setting the bit OSCSEL to 0.
- Wait 5 slow clock cycles for internal resynchronization.
- Disable the 32768Hz oscillator by setting the bit OSC32EN to 0.

8.7 Power Management Controller

The Power Management Controller provides all the clock signals to the system.

PMC input clocks:

- UPLLCK: From UTMI PLL
- PLLACK From PLLA
- SLCK: slow clock from OSC32K or internal RC OSC
- MAINCK: from 12 MHz external oscillator

PMC output clocks

- Processor Clock PCK
- Master Clock MCK, in particular to the Matrix and the memory interfaces. The divider can be 1,2,3 or 4
- DDR system clock equal to 2xMCK

Note: DDR system clock is not available when Master Clock (MCK) equals Processor Clock (PCK).

- USB Host EHCI High speed clock (UPLLCK)
- USB OHCI clocks (UHP48M and UHP12M)
- Independent peripheral clocks, typically at the frequency of MCK
- Two programmable clock outputs: PCK0 and PCK1

This allows the software control of five flexible operating modes:

- Normal Mode, processor and peripherals running at a programmable frequency
- Idle Mode, processor stopped waiting for an interrupt
- Slow Clock Mode, processor and peripherals running at low frequency
- Standby Mode, mix of Idle and Backup Mode, peripheral running at low frequency, processor stopped waiting for an interrupt
- Backup Mode, Main Power Supplies off, VDDBU powered by a battery

- USB Device High Speed and Host EHCI High Speed operations are NOT allowed
- Full Speed OHCI input clock is PLLACK, USBDIV is 7 (division by 8)
- System Input clock is PLLACK, PCK is 384 MHz
- MDIV is ‘11’, MCK is 128 MHz
- DDR2 can be used at up to 128 MHz

8.8 Periodic Interval Timer

- Includes a 20-bit Periodic Counter, with less than 1µs accuracy
- Includes a 12-bit Interval Overlay Counter
- Real Time OS or Linux/WinCE compliant tick generator

8.9 Watchdog Timer

- 16-bit key-protected only-once-Programmable Counter
- Windowed, prevents the processor to be in a dead-lock on the watchdog access

8.10 Real-Time Timer

- Real-Time Timer, allowing backup of time with different accuracies
  - 32-bit Free-running back-up Counter
  - Integrates a 16-bit programmable prescaler running on slow clock
  - Alarm Register capable to generate a wake-up of the system through the Shut Down Controller

8.11 Real Time Clock

- Low power consumption
- Full asynchronous design
- Two hundred year calendar
- Programmable Periodic Interrupt
- Alarm and update parallel load
- Control of alarm and update Time/Calendar Data In

8.12 General-Purpose Backup Registers

- Four 32-bit backup general-purpose registers

8.13 Advanced Interrupt Controller

- Controls the interrupt lines (nIRQ and nFIQ) of the ARM Processor
- Thirty-two individually maskable and vectored interrupt sources
  - Source 0 is reserved for the Fast Interrupt Input (FIQ)
  - Source 1 is reserved for system peripherals (PIT, RTT, PMC, DBGU, etc.)
  - Programmable Edge-triggered or Level-sensitive Internal Sources
  - Programmable Positive/Negative Edge-triggered or High/Low Level-sensitive
- One External Sources plus the Fast Interrupt signal
- 8-level Priority Controller
  - Drives the Normal Interrupt of the processor
  - Handles priority of the interrupt sources 1 to 31
  - Higher priority interrupts can be served during service of lower priority interrupt
- Vectoring
  - Optimizes Interrupt Service Routine Branch and Execution

9. Peripherals

9.1 Peripheral Mapping

As shown in Figure 7-1, the Peripherals are mapped in the upper 256 Mbytes of the address space between the addresses 0xFFF7 8000 and 0xFFFC FFFF.

Each User Peripheral is allocated 16K bytes of address space.

9.2 Peripheral Identifiers

Table 9-1 defines the Peripheral Identifiers of the SAM9M10. A peripheral identifier is required for the control of the peripheral interrupt with the Advanced Interrupt Controller and for the control of the peripheral clock with the Power Management Controller.

Table 9-1. SAM9M10 Peripheral Identifiers

Peripheral ID	Peripheral Mnemonic	Peripheral Name	External Interrupt
0	**AIC**	Advanced Interrupt Controller	FIQ
1	**SYSC**	System Controller Interrupt	
2	**PIOA**	Parallel I/O Controller A,	
3	**PIOB**	Parallel I/O Controller B	
4	**PIOC**	Parallel I/O Controller C	
5	**PIOD/PIOE**	Parallel I/O Controller D/E	
6	**TRNG**	True Random Number Generator	
7	**US0**	USART 0	
8	**US1**	USART 1	
9	**US2**	USART 2	
10	**US3**	USART 3	
11	**MCI0**	High Speed Multimedia Card Interface 0	
12	**TWI0**	Two-Wire Interface 0	
13	**TWI1**	Two-Wire Interface 1	
14	**SPI0**	Serial Peripheral Interface	
15	**SPI1**	Serial Peripheral Interface	
16	**SSC0**	Synchronous Serial Controller 0	
17	**SSC1**	Synchronous Serial Controller 1	
18	**TC0..TC5**	Timer Counter 0,1,2,3,4,5	
19	**PWM**	Pulse Width Modulation Controller	
20	**TSADCC**	Touch Screen ADC Controller	
21	**DMA**	DMA Controller	
22	**UHPHS**	USB Host High Speed	
23	**LCDC**	LCD Controller	
24	**AC97C**	AC97 Controller	
25	**EMAC**	Ethernet MAC	
26	**ISI**	Image Sensor Interface	
27	**UDPHS**	USB Device High Speed	
29	**MCI1**	High Speed Multimedia Card Interface 1	
30	**VDEC**	Video Decoder	
31	**AIC**	Advanced Interrupt Controller	IRQ

9.4.3 PIO Controller C Multiplexing

Table 9-4. Multiplexing on PIO Controller C (PIOC)

I/O Line	Peripheral A	Peripheral B	Reset State	Power Supply	Function	Comments
PC0	DQM2		DQM2	VDDIOM1		
PC1	DQM3		DQM3	VDDIOM1		
PC2	A19		A19	VDDIOM1		
PC3	A20		A20	VDDIOM1		
PC4	A21/NANDALE		A21	VDDIOM1		
PC5	A22/NANDCLE		A22	VDDIOM1		
PC6	A23		A23	VDDIOM1		
PC7	A24		A24	VDDIOM1		
PC8	CFCE1		I/O	VDDIOM1		
PC9	CFCE2	RTS2	I/O	VDDIOM1		
PC10	NCS4/CFCS0	TCLK2	I/O	VDDIOM1		
PC11	NCS5/CFCS1	CTS2	I/O	VDDIOM1		
PC12	A25/CFRNW		A25	VDDIOM1		
PC13	NCS2		I/O	VDDIOM1		
PC14	NCS3/NANDCS		I/O	VDDIOM1		
PC15	NWAIT		I/O	VDDIOM1		
PC16	D16		I/O	VDDIOM1		
PC17	D17		I/O	VDDIOM1		
PC18	D18		I/O	VDDIOM1		
PC19	D19		I/O	VDDIOM1		
PC20	D20		I/O	VDDIOM1		
PC21	D21		I/O	VDDIOM1		
PC22	D22		I/O	VDDIOM1		
PC23	D23		I/O	VDDIOM1		
PC24	D24		I/O	VDDIOM1		
PC25	D25		I/O	VDDIOM1		
PC26	D26		I/O	VDDIOM1		
PC27	D27		I/O	VDDIOM1		
PC28	D28		I/O	VDDIOM1		
PC29	D29		I/O	VDDIOM1		
PC30	D30		I/O	VDDIOM1		
PC31	D31		I/O	VDDIOM1		

9.4.4 PIO Controller D Multiplexing

Table 9-5. Multiplexing on PIO Controller D (PIOD)

I/O Line	Peripheral A	Peripheral B	Reset State	Power Supply	Function	Comments
PD0	TK0	PWM3	I/O	VDDIOP0		
PD1	TF0		I/O	VDDIOP0		
PD2	TD0		I/O	VDDIOP0		
PD3	RD0		I/O	VDDIOP0		
PD4	RK0		I/O	VDDIOP0		
PD5	RF0		I/O	VDDIOP0		
PD6	AC97RX		I/O	VDDIOP0		
PD7	AC97TX	TIOA5	I/O	VDDIOP0		
PD8	AC97FS	TIOB5	I/O	VDDIOP0		
PD9	AC97CK	TCLK5	I/O	VDDIOP0		
PD10	TD1		I/O	VDDIOP0		
PD11	RD1		I/O	VDDIOP0		
PD12	TK1	PCK0	I/O	VDDIOP0		
PD13	RK1		I/O	VDDIOP0		
PD14	TF1		I/O	VDDIOP0		
PD15	RF1		I/O	VDDIOP0		
PD16	RTS1		I/O	VDDIOP0		
PD17	CTS1		I/O	VDDIOP0		
PD18	SPI1_NPCS2	IRQ	I/O	VDDIOP0		
PD19	SPI1_NPCS3	FIQ	I/O	VDDIOP0		
PD20	TIOA0		I/O	VDDANA		TSAD0
PD21	TIOA1		I/O	VDDANA		TSAD1
PD22	TIOA2		I/O	VDDANA		TSAD2
PD23	TCLK0		I/O	VDDANA		TSAD3
PD24	SPI0_NPCS1	PWM0	I/O	VDDANA		GPAD4
PD25	SPI0_NPCS2	PWM1	I/O	VDDANA		GPAD5
PD26	PCK0	PWM2	I/O	VDDANA		GPAD6
PD27	PCK1	SPI0_NPCS3	I/O	VDDANA		GPAD7
PD28	TSADTRG	SPI1_NPCS1	I/O	VDDIOP0		
PD29	TCLK1	SCK1	I/O	VDDIOP0		
PD30	TIOB0	SCK2	I/O	VDDIOP0		
PD31	TIOB1	PWM1	I/O	VDDIOP0		

9.4.5 PIO Controller E Multiplexing

Table 9-6. Multiplexing on PIO Controller E (PIOE)

I/O Line	Peripheral A	Peripheral B	Reset State	Power Supply	Function	Comments
PE0	LCDPWR	PCK0	I/O	VDDIOP1		
PE1	LCDMOD		I/O	VDDIOP1		
PE2	LCDCC		I/O	VDDIOP1		
PE3	LCDVSYNC		I/O	VDDIOP1		
PE4	LCDHSYNC		I/O	VDDIOP1		
PE5	LCDDOTCK		I/O	VDDIOP1		
PE6	LCDDEN		I/O	VDDIOP1		
PE7	LCDD0	LCDD2	I/O	VDDIOP1		
PE8	LCDD1	LCDD3	I/O	VDDIOP1		
PE9	LCDD2	LCDD4	I/O	VDDIOP1		
PE10	LCDD3	LCDD5	I/O	VDDIOP1		
PE11	LCDD4	LCDD6	I/O	VDDIOP1		
PE12	LCDD5	LCDD7	I/O	VDDIOP1		
PE13	LCDD6	LCDD10	I/O	VDDIOP1		
PE14	LCDD7	LCDD11	I/O	VDDIOP1		
PE15	LCDD8	LCDD12	I/O	VDDIOP1		
PE16	LCDD9	LCDD13	I/O	VDDIOP1		
PE17	LCDD10	LCDD14	I/O	VDDIOP1		
PE18	LCDD11	LCDD15	I/O	VDDIOP1		
PE19	LCDD12	LCDD18	I/O	VDDIOP1		
PE20	LCDD13	LCDD19	I/O	VDDIOP1		
PE21	LCDD14	LCDD20	I/O	VDDIOP1		
PE22	LCDD15	LCDD21	I/O	VDDIOP1		
PE23	LCDD16	LCDD22	I/O	VDDIOP1		
PE24	LCDD17	LCDD23	I/O	VDDIOP1		
PE25	LCDD18		I/O	VDDIOP1		
PE26	LCDD19		I/O	VDDIOP1		
PE27	LCDD20		I/O	VDDIOP1		
PE28	LCDD21		I/O	VDDIOP1		
PE29	LCDD22		I/O	VDDIOP1		
PE30	LCDD23		I/O	VDDIOP1		
PE31	PWM2	PCK1	I/O	VDDIOP1		

10. Embedded Peripherals

10.1 Serial Peripheral Interface (SPI)

- Supports communication with serial external devices
  - Four chip selects with external decoder support allow communication with up to 15 peripherals
  - Serial memories, such as DataFlash and 3-wire EEPROMs
  - Serial peripherals, such as ADCs, DACs, LCD Controllers, CAN Controllers and Sensors
  - External co-processors
- Master or slave serial peripheral bus interface
  - 8- to 16-bit programmable data length per chip select
  - Programmable phase and polarity per chip select
  - Programmable transfer delays between consecutive transfers and between clock and data per chip select
  - Programmable delay between consecutive transfers
  - Selectable mode fault detection
- Very fast transfers supported
  - Transfers with baud rates up to MCK
  - The chip select line may be left active to speed up transfers on the same device

10.2 Two Wire Interface (TWI)

- Compatibility with standard two-wire serial memory
- One, two or three bytes for slave address
- Sequential read/write operations
- Supports either master or slave modes
- Compatible with Standard Two-wire Serial Memories
- Master, Multi-master and Slave Mode Operation
- Bit Rate: Up to 400 Kbits
- General Call Supported in Slave mode
- Connection to Peripheral DMA Controller (PDC) Channel Capabilities Optimizes Data Transfers in Master Mode Only
  - One Channel for the Receiver, One Channel for the Transmitter
  - Next Buffer Support

10.3 Universal Synchronous Asynchronous Receiver Transmitter (USART)

- Programmable Baud Rate Generator
- 5- to 9-bit full-duplex synchronous or asynchronous serial communications
  - 1, 1.5 or 2 stop bits in Asynchronous Mode or 1 or 2 stop bits in Synchronous Mode
  - Parity generation and error detection
  - Framing error detection, overrun error detection
  - MSB- or LSB-first
  - Optional break generation and detection
  - By 8 or by-16 over-sampling receiver frequency
  - Hardware handshaking RTS-CTS
  - Receiver time-out and transmitter timeguard
  - Optional Multi-drop Mode with address generation and detection
  - Optional Manchester Encoding

- 4-bit single scan, 8-bit single or dual scan, 16-bit dual scan STN interfaces supported
- Up to 24-bit single scan TFT interfaces supported
- Up to 16 gray levels for mono STN and up to 4096 colors for color STN displays
- 1, 2 bits per pixel (palletized), 4 bits per pixel (non-palletized) for mono STN
- 1, 2, 4, 8 bits per pixel (palletized), 16 bits per pixel (non-palletized) for color STN
- 1, 2, 4, 8 bits per pixel (palletized), 16, 24 bits per pixel (non-palletized) for TFT
- Single clock domain architecture
- Resolution supported up to 2048 x 2048

10.12 Touch Screen Analog-to-Digital Converter (TSADC)

- 8-channel ADC
- Support 4-wire resistive Touch Screen
- 10-bit 384 Ksamples/sec. Successive Approximation Register ADC
- -3/+3 LSB Integral Non Linearity, -2/+2 LSB Differential Non Linearity
- Integrated 8-to-1 multiplexer, offering eight independent 3.3V analog inputs
- External voltage reference for better accuracy on low voltage inputs
- Individual enable and disable of each channel
- Multiple trigger sources
  - Hardware or software trigger
  - External trigger pin
- Sleep Mode and conversion sequencer
  - Automatic wakeup on trigger and back to sleep mode after conversions of all enabled channels

10.13 Ethernet 10/100 MAC (EMAC)

- Compatibility with IEEE Standard 802.3
- 10 and 100 MBits per second data throughput capability
- Full- and half-duplex operations
- MII or RMII interface to the physical layer
- Register Interface to address, data, status and control registers
- DMA Interface, operating as a master on the Memory Controller
- Interrupt generation to signal receive and transmit completion
- 128-byte transmit and 128-byte receive FIFOs
- Automatic pad and CRC generation on transmitted frames
- Address checking logic to recognize four 48-bit addresses
- Supports promiscuous mode where all valid frames are copied to memory
- Supports physical layer management through MDIO interface
- Supports Wake On Lan. The receiver supports Wake on LAN by detecting the following events on incoming receive frames:
  - Magic packet
  - ARP request to the device IP address
  - Specific address 1 filter match
  - Multicast hash filter match

10.14 Image Sensor Interface (ISI)

- ITU-R BT. 601/656 8-bit mode external interface support
- Support for ITU-R BT.656-4 SAV and EAV synchronization

- H.263 Profile 0, levels 10-70
- VC-1
    - Simple Profile, Low and Medium Levels
    - Main Profile, Low, Medium and High Levels
    - Advanced Profile, Levels 0-3
- MPEG-2 Main Profile, Low, Medium and High Levels
- JPEG Profile Baseline DCT (sequential) and JFIF 1.02 file form

Post-processor features:

- Image up-scaling
- Image down-scaling
- YCbCr to RGB conversion
- Dithering
- Deinterlacing
- Programmable alpha channel
- Alpha blending
- De-blocking filter for MPEG-4 simple profile/H.263
- Image cropping / digital zoom
- Picture in picture
- Supported display size for picture in picture
- Image rotation

Revision History

In the tables that follow, the most recent version appears first. The initials “rfo” indicate changes requested by product experts, or made during proof reading as part of the approval process.

Table 12-2.

Doc. Rev	Comments	Change Request Ref.
6355ES	Product Overview: Section 1. “Features”, under “Peripherals” , added DBGU to USART... AT91 removed from SAM9M10 product name in headers, text and images.	 rfo rfo
	Ordering Codes: Table 12-1, “AT91SAM9M10 Ordering Information”, added AT91SAM9M10C-CU and MRL C	8551
6355DS	Section 11.3 “Marking” added at the end of Section 11. “Mechanical Characteristics”. Section 12. “SAM9M10 Ordering Information”, a second ordering code added: AT91SAM9M10B-CU. An MRL column added too.	7979
	LFBGA changed to TFBGA in Section 4. “Package and Pinout”.	7883
6355CS	Product Line/Product naming convention changed - **AT91SAM ARM-based MPU / SAM9M10** Section 5.1 “Power Supplies”, replaced ground pin names by GNDIOM, GNDCORE, GNDANA, GNDIOP, GNDBU, GNDOSC, GNDUTMI. Reorganized text describing GND association to power supply pins	rfo 7332 rfo
6355BS	Section 10.17 “Video Decoder (VDEC)” added.	RFO
	Section 10.16 “True Random Number Generator (TRNG)” added.	7172
	‘11-layer --> ‘12-layer’ in Section 6.2 “Bus Matrix”	7171
	New Figure 11-1 “324-ball TFBGA Package Drawing” .	6954
	Section 7.3 “External Memories” reorganized.	RFO
6355AS	First issue	