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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

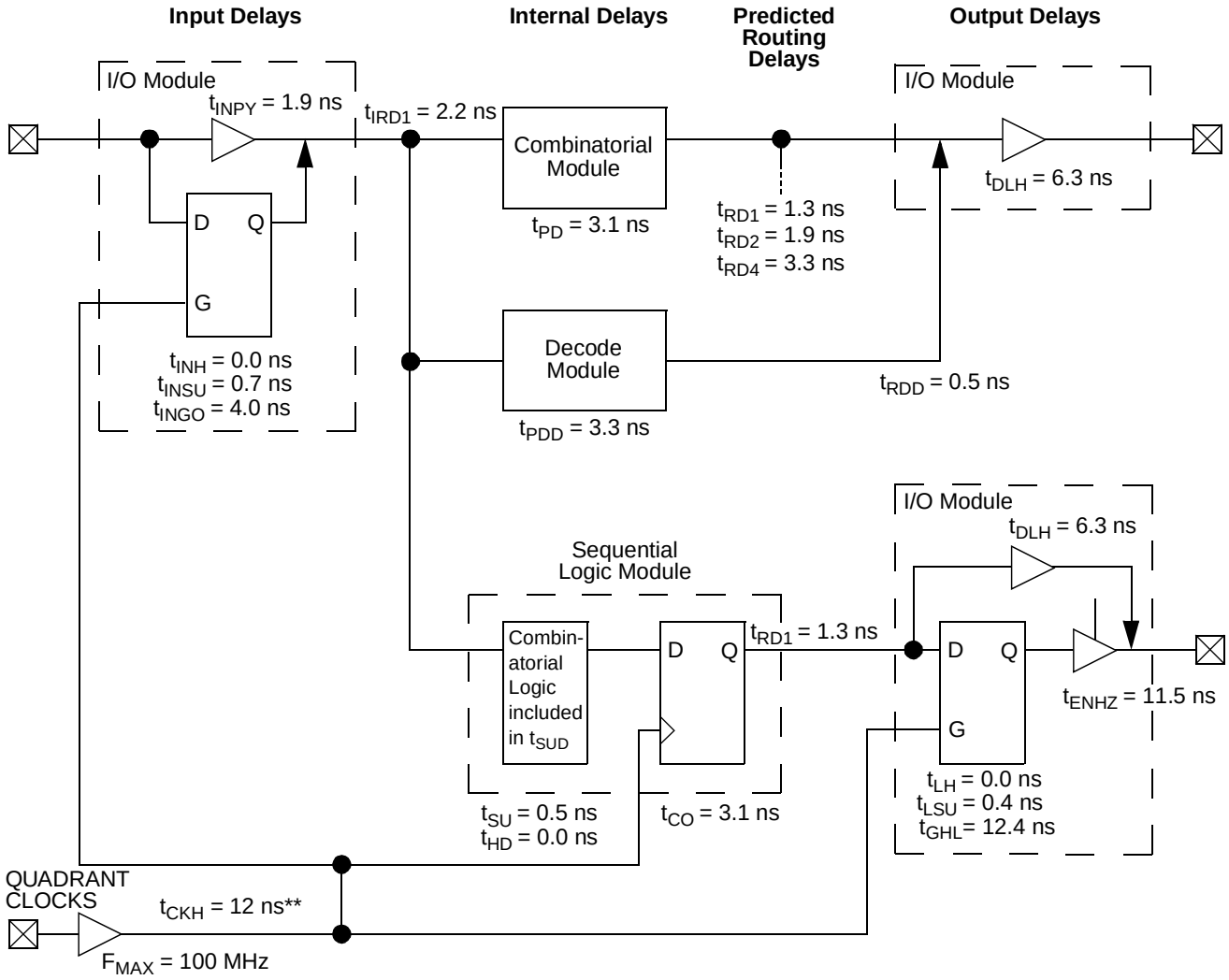
The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	295
Number of Logic Elements/Cells	-
Total RAM Bits	-
Number of I/O	57
Number of Gates	1200
Voltage - Supply	4.5V ~ 5.5V
Mounting Type	Through Hole
Operating Temperature	-55°C ~ 125°C (TJ)
Package / Case	84-BCPGA
Supplier Device Package	84-CPGA (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/microsemi/a1010b-1pg84b

DESC SMD/Actel Part Number Cross Reference

Actel Part Number (Gold Leads)	DSCC SMD (Gold Leads)	DSCC SMD (Solder Dipped)
A1010B-PG84B	5962-9096403MXC	5962-9096403MXA
A1010B-1PG84B	5962-9096404MXC	5962-9096404MXA
A1020B-PG84B	5962-9096503MUC	5962-9096503MUA
A1020B-1PG84B	5962-9096504MUC	5962-9096504MUA
A1020B-CQ84B	5962-9096503MTC	5962-9096503MTA
A1020B-1CQ84B	5962-9096504MTC	5962-9096504MTA
A1240A-PG132B	5962-9322101MXC	5962-9322101MXA
A1240A-1PG132B	5962-9322102MXC	5962-9322102MXA
A1280A-PG176B	5962-9215601MXC	5962-9215601MXA
A1280A-1PG176B	5962-9215602MXC	5962-9215602MXA
A1280A-CQ172B	5962-9215601MYC	5962-9215601MYA
A1280A-1CQ172B	5962-9215602MYC	5962-9215602MYA
A1425A-PG133B	5962-9552001MXC	N/A
A1425A-1PG133B	5962-9552002MXC	N/A
A1425A-CQ132B	5962-9552001MYC	N/A
A1425A-1CQ132B	5962-9552002MYC	N/A
A1460A-PG207B	5962-9550801MXC	N/A
A1460A-1PG207B	5962-9550802MXC	N/A
A1460A-CQ196B	5962-9550801MYC	N/A
A1460A-1CQ196B	5962-9550802MYC	N/A
A14100A-PG257B	5962-9552101MXC	N/A
A14100A-1PG257B	5962-9552102MXC	N/A
A14100A-CQ256B	5962-9552101MYC	N/A
A14100A-1CQ256B	5962-9552102MYC	N/A
A32100DX-CQ84B	5962-9875901QXC	N/A
A32100DX-1CQ84B	5962-9857902QXC	N/A
A32200DX-CQ256B	5962-9952701QXC	N/A
A32200DX-1CQ256B	5962-9952702QXC	N/A
A32200DX-CQ208B	5962-9952701QYC	N/A
A32200DX-1CQ208B	5962-9952702QYC	N/A

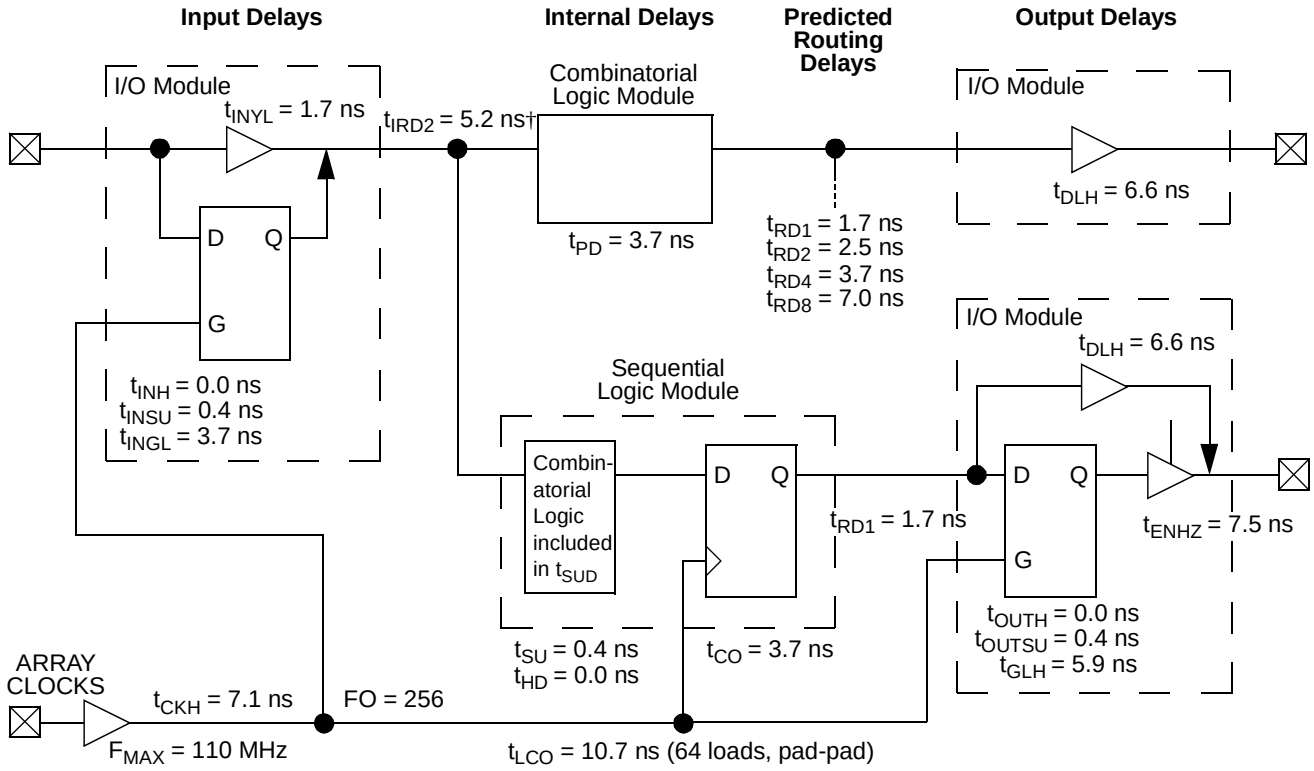
3200DX Timing Model (Logic Functions using Quadrant Clocks)*



** Values shown for A32100DX–1 at worst-case military conditions.*

*** Load dependent.*

1200XL Timing Model*

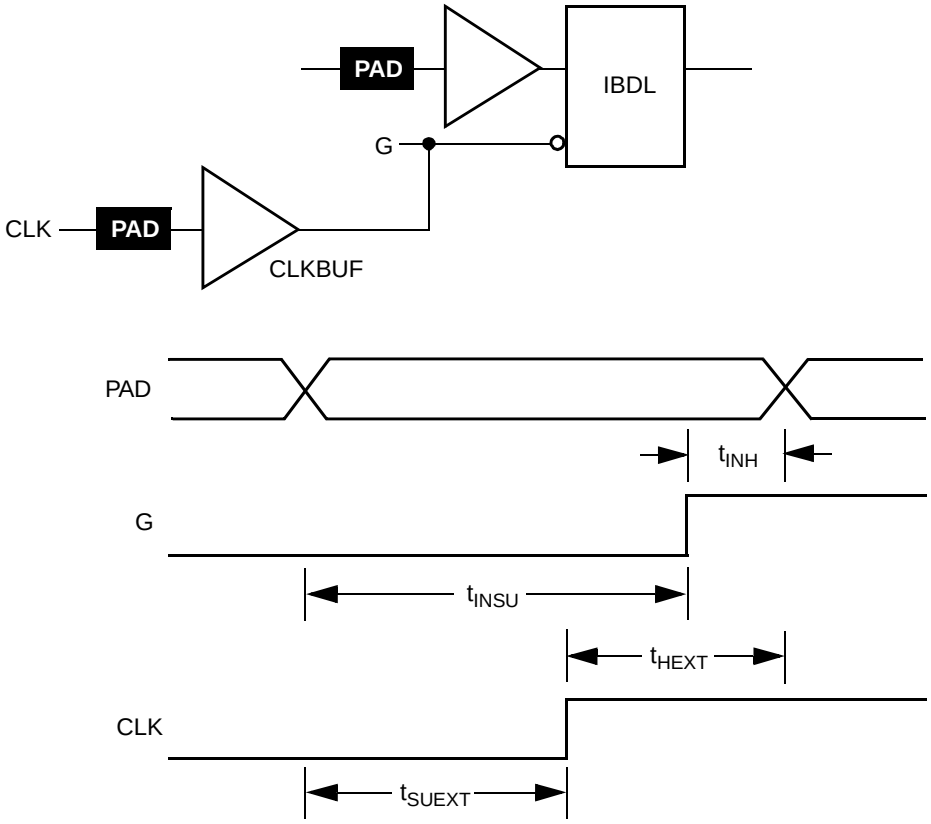


**Values shown for A1280XL–1 at worst-case military conditions.*

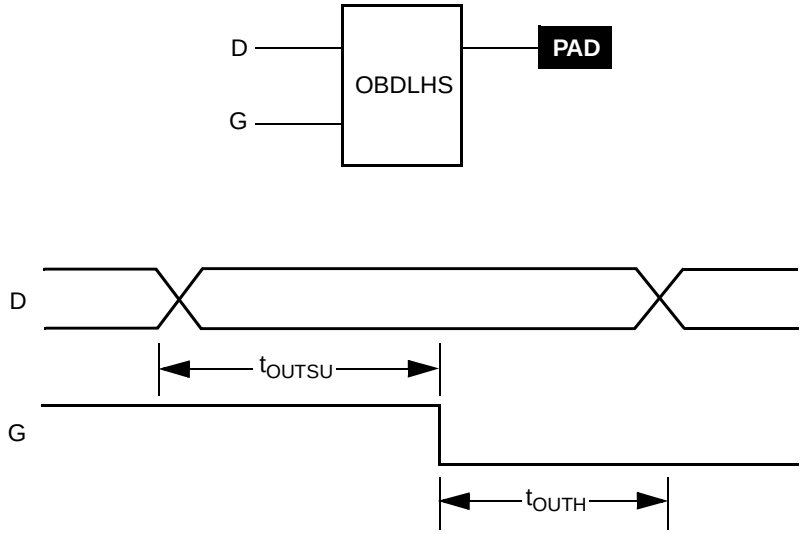
† Input module predicted routing delay.

Sequential Timing Characteristics (continued)

Input Buffer Latches (ACT 2 and 1200XL/3200DX)



Output Buffer Latches (ACT 2 and 1200XL/3200DX)



A1240A Timing Characteristics (continued)

(Worst-Case Military Conditions, V_{CC} = 4.5V, T_J = 125°C)

		'–1' Speed		'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
TTL Output Module Timing[1]						
t_{DLH}	Data to Pad High		11.0		13.0	ns
t_{DHL}	Data to Pad Low		13.9		16.4	ns
t_{ENZH}	Enable Pad Z to High		12.3		14.4	ns
t_{ENZL}	Enable Pad Z to Low		16.1		19.0	ns
t_{ENHZ}	Enable Pad High to Z		9.8		11.5	ns
t_{ENLZ}	Enable Pad Low to Z		11.5		13.6	ns
t_{GLH}	G to Pad High		12.4		14.6	ns
t_{GHL}	G to Pad Low		15.5		18.2	ns
d_{TLH}	Delta Low to High		0.09		0.11	ns/pF
d_{THL}	Delta High to Low		0.17		0.20	ns/pF
CMOS Output Module Timing[1]						
t_{DLH}	Data to Pad High		14.0		16.5	ns
t_{DHL}	Data to Pad Low		11.7		13.7	ns
t_{ENZH}	Enable Pad Z to High		12.3		14.4	ns
t_{ENZL}	Enable Pad Z to Low		16.1		19.0	ns
t_{ENHZ}	Enable Pad High to Z		9.8		11.5	ns
t_{ENLZ}	Enable Pad Low to Z		11.5		13.6	ns
t_{GLH}	G to Pad High		12.4		14.6	ns
t_{GHL}	G to Pad Low		15.5		18.2	ns
d_{TLH}	Delta Low to High		0.17		0.20	ns/pF
d_{THL}	Delta High to Low		0.12		0.15	ns/pF

Notes:

1. *Delays based on 50 pF loading.*
2. *SSO information can be found in the* Simultaneously Switching Output Limits for Actel FPGAs *application note at http://www.actel.com/appnotes.*

A1280XL Timing Characteristics

(Worst-Case Military Conditions, V_{CC} = 4.5V, T_J = 125°C)

		'–1' Speed		'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
Logic Module Propagation Delays[1]						
t_{PD1}	Single Module		3.7		4.3	ns
t_{CO}	Sequential Clk to Q		3.7		4.3	ns
t_{GO}	Latch G to Q		3.7		4.3	ns
t_{RS}	Flip-Flop (Latch) Reset to Q		3.7		4.3	ns
Logic Module Predicted Routing Delays[2]						
t_{RD1}	FO=1 Routing Delay		1.7		2.1	ns
t_{RD2}	FO=2 Routing Delay		2.5		3.0	ns
t_{RD3}	FO=3 Routing Delay		3.1		3.6	ns
t_{RD4}	FO=4 Routing Delay		3.7		4.3	ns
t_{RD8}	FO=8 Routing Delay		7.0		8.3	ns
Logic Module Sequential Timing[3, 4]						
t_{SUD}	Flip-Flop (Latch) Data Input Setup	0.4		0.5		ns
t_{HD}	Flip-Flop (Latch) Data Input Hold	0.0		0.0		ns
t_{SUENA}	Flip-Flop (Latch) Enable Setup	1.1		1.2		ns
t_{HENA}	Flip-Flop (Latch) Enable Hold	0.0		0.0		ns
t_{WCLKA}	Flip-Flop (Latch) Clock Active Pulse Width	5.3		6.1		ns
t_{WASYN}	Flip-Flop (Latch) Asynchronous Pulse Width	5.3		6.1		ns
t_A	Flip-Flop Clock Input Period	10.7		12.3		ns
t_{INH}	Input Buffer Latch Hold	0.0		0.0		ns
t_{INSU}	Input Buffer Latch Setup	0.4		0.4		ns
t_{OUTH}	Output Buffer Latch Hold	0.0		0.0		ns
t_{OUTSU}	Output Buffer Latch Setup	0.4		0.4		ns
f_{MAX}	Flip-Flop (Latch) Clock Frequency		90		75	MHz

Notes:

1. *For dual-module macros, use $t_{PD1} + t_{RD1} + t_{PDn}$, $t_{CO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.*
2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*
3. *Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the DirectTime Analyzer utility.*
4. *Setup and hold timing parameters for the input buffer latch are defined with respect to the PAD and the D input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.*

A1460A Timing Characteristics (continued)

(Worst-Case Military Conditions, V_{CC} = 4.5V, T_J = 125°C)

		'–1' Speed		'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
CMOS Output Module Timing[1]						
t_{DHS}	Data to Pad, High Slew		9.2		10.8	ns
t_{DLS}	Data to Pad, Low Slew		17.3		20.3	ns
t_{ENZHS}	Enable to Pad, Z to H/L, High Slew		7.7		9.1	ns
t_{ENZLS}	Enable to Pad, Z to H/L, Low Slew		13.1		15.5	ns
t_{ENHSZ}	Enable to Pad, H/L to Z, High Slew		10.9		12.8	ns
t_{ENLSZ}	Enable to Pad, H/L to Z, Low Slew		10.9		12.8	ns
t_{CKHS}	IOCLK Pad to Pad H/L, High Slew		14.1		16.0	ns
t_{CKLS}	IOCLK Pad to Pad H/L, Low Slew		20.2		22.4	ns
d_{TLHHS}	Delta Low to High, High Slew		0.06		0.07	ns/pF
d_{TLHLS}	Delta Low to High, Low Slew		0.11		0.13	ns/pF
d_{THLHS}	Delta High to Low, High Slew		0.04		0.05	ns/pF
d_{THLLS}	Delta High to Low, Low Slew		0.05		0.06	ns/pF
Dedicated (Hard-Wired) I/O Clock Network						
t_{IOCKH}	Input Low to High (Pad to I/O Module Input)		3.5		4.1	ns
t_{IOPWH}	Minimum Pulse Width High	4.8		5.7		ns
t_{IOPWL}	Minimum Pulse Width Low	4.8		5.7		ns
t_{IOSAPW}	Minimum Asynchronous Pulse Width	3.9		4.4		ns
t_{IOCKSW}	Maximum Skew		0.9		1.0	ns
t_{IOP}	Minimum Period	9.9		11.6		ns
f_{IOMAX}	Maximum Frequency		100		85	MHz
Dedicated (Hard-Wired) Array Clock Network						
t_{HCKH}	Input Low to High (Pad to S-Module Input)		5.5		6.4	ns
t_{HCKL}	Input High to Low (Pad to S-Module Input)		5.5		6.4	ns
t_{HPWH}	Minimum Pulse Width High	4.8		5.7		ns
t_{HPWL}	Minimum Pulse Width Low	4.8		5.7		ns
t_{HCKSW}	Maximum Skew		0.9		1.0	ns
t_{HP}	Minimum Period	9.9		11.6		ns
f_{HMAX}	Maximum Frequency		100		85	MHz

Notes:

1. *Delays based on 35 pF loading.*
2. *SSO information can be found in the* Simultaneously Switching Output Limits for Actel FPGAs *application note at http://www.actel.com/appnotes.*

A14100A Timing Characteristics (continued)

(Worst-Case Military Conditions, V_{CC} = 4.5V, T_J = 125°C)

		'–1' Speed		'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
I/O Module Sequential Timing						
t_{INH}	Input F-F Data Hold (w.r.t. IOCLK Pad)	0.0		0.0		ns
t_{INSU}	Input F-F Data Setup (w.r.t. IOCLK Pad)	2.1		2.4		ns
t_{IDEH}	Input Data Enable Hold (w.r.t. IOCLK Pad)	0.0		0.0		ns
t_{IDESU}	Input Data Enable Setup (w.r.t. IOCLK Pad)	8.7		10.0		ns
t_{OUTH}	Output F-F Data Hold (w.r.t. IOCLK Pad)	1.2		1.2		ns
t_{OUTSU}	Output F-F Data Setup (w.r.t. IOCLK Pad)	1.2		1.2		ns
t_{ODEH}	Output Data Enable Hold (w.r.t. IOCLK Pad)	0.6		0.6		ns
t_{ODESU}	Output Data Enable Setup (w.r.t. IOCLK Pad)	2.4		2.4		ns
TTL Output Module Timing[1]						
t_{DHS}	Data to Pad, High Slew		7.5		8.9	ns
t_{DLS}	Data to Pad, Low Slew		11.9		14.0	ns
t_{ENZHS}	Enable to Pad, Z to H/L, High Slew		6.0		7.0	ns
t_{ENZLS}	Enable to Pad, Z to H/L, Low Slew		10.9		12.8	ns
t_{ENHSZ}	Enable to Pad, H/L to Z, High Slew		11.9		14.0	ns
t_{ENLSZ}	Enable to Pad, H/L to Z, Low Slew		10.9		12.8	ns
t_{CKHS}	IOCLK Pad to Pad H/L, High Slew		12.2		14.0	ns
t_{CKLS}	IOCLK Pad to Pad H/L, Low Slew		17.8		17.8	ns
d_{TLHHS}	Delta Low to High, High Slew		0.04		0.04	ns/pF
d_{TLHLS}	Delta Low to High, Low Slew		0.07		0.08	ns/pF
d_{THLHS}	Delta High to Low, High Slew		0.05		0.06	ns/pF
d_{THLLS}	Delta High to Low, Low Slew		0.07		0.08	ns/pF

Note:

1. Delays based on 35 pF loading.

A32100DX Timing Characteristics (continued)

(Worst-Case Military Conditions, V_{CC} = 4.5V, T_J = 125°C)

			'–1' Speed		'Std' Speed		
Parameter	**Description**		**Min.**	**Max.**	**Min.**	**Max.**	**Units**
Input Module Propagation Delays							
t_{INPY}	Input Data Pad to Y			1.9		2.6	ns
t_{INGO}	Input Latch Gate-to-Output			4.0		5.3	ns
t_{INH}	Input Latch Hold		0.0		0.0		ns
t_{INSU}	Input Latch Setup		0.7		0.9		ns
t_{ILA}	Latch Active Pulse Width		6.1		8.1		ns
Input Module Predicted Routing Delays[1]							
t_{IRD1}	FO=1 Routing Delay			2.2		2.9	ns
t_{IRD2}	FO=2 Routing Delay			2.8		3.8	ns
t_{IRD3}	FO=3 Routing Delay			3.5		4.7	ns
t_{IRD4}	FO=4 Routing Delay			3.5		4.7	ns
t_{IRD8}	FO=8 Routing Delay			5.6		7.5	ns
Global Clock Network							
t_{CKH}	Input Low to High	FO=32 FO=635		6.5 7.9		8.7 10.6	ns ns
t_{CKL}	Input High to Low	FO=32 FO=635		6.6 8.8		8.8 11.8	ns ns
t_{PWH}	Minimum Pulse Width High	FO=32 FO=635	4.1 4.6		5.5 6.1		ns ns
t_{PWL}	Minimum Pulse Width Low	FO=32 FO=635	4.1 4.6		5.5 6.1		ns ns
t_{CKSW}	Maximum Skew	FO=32 FO=635		1.8 1.8		2.4 2.4	ns ns
t_{SUEXT}	Input Latch External Setup	FO=32 FO=635	0.0 0.0		0.0 0.0		ns ns
t_{HEXT}	Input Latch External Hold	FO=32 FO=635	3.0 3.8		4.0 5.1		ns ns
t_P	Minimum Period (1/fmax)	FO=32 FO=635	7.1 7.9		9.5 10.5		ns ns
f_{HMAX}	Maximum Datapath Frequency	FO=32 FO=635		140 126		105 95	MHz MHz

Note:

1. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment. Optimization techniques may further reduce delays by 0 to 4 ns.

A32200DX Timing Characteristics (continued)

(Worst-Case Military Conditions, V_{CC} = 4.5V, T_J = 125°C)

		'–1' Speed		'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
Synchronous SRAM Operations						
t_{RC}	Read Cycle Time	8.8		11.8		ns
t_{WC}	Write Cycle Time	8.8		11.8		ns
t_{RCKHL}	Clock High/Low Time	4.4		5.9		ns
t_{RCO}	Data Valid After Clock High/Low		4.4		5.9	ns
t_{ADSU}	Address/Data Setup Time	2.1		2.8		ns
t_{ADH}	Address/Data Hold Time	0.0		0.0		ns
t_{RENSU}	Read Enable Setup	0.8		1.1		ns
t_{RENH}	Read Enable Hold	4.4		5.9		ns
t_{WENSU}	Write Enable Setup	3.5		4.7		ns
t_{WENH}	Write Enable Hold	0.0		0.0		ns
t_{BENS}	Block Enable Setup	3.6		4.8		ns
t_{BENH}	Block Enable Hold	0.0		0.0		ns
Asynchronous SRAM Operations						
t_{RPD}	Asynchronous Access Time		10.6		14.1	ns
t_{RDADV}	Read Address Valid	11.5		15.3		ns
t_{ADSU}	Address/Data Setup Time	2.1		2.8		ns
t_{ADH}	Address/Data Hold Time	0.0		0.0		ns
t_{RENSUA}	Read Enable Setup to Address Valid	0.8		1.1		ns
t_{RENHA}	Read Enable Hold	4.4		5.9		ns
t_{WENSU}	Write Enable Setup	3.5		4.7		ns
t_{WENH}	Write Enable Hold	0.0		0.0		ns
t_{DOH}	Data Out Hold Time		1.6		2.1	ns

A32200DX Timing Characteristics (continued)

(Worst-Case Military Conditions, V_{CC} = 4.5V, T_J = 125°C)

			‘–1’ Speed		‘Std’ Speed		
Parameter	**Description**		**Min.**	**Max.**	**Min.**	**Max.**	**Units**
Input Module Propagation Delays							
t_{INPY}	Input Data Pad to Y			1.9		2.6	ns
t_{INGO}	Input Latch Gate-to-Output			4.6		6.0	ns
t_{INH}	Input Latch Hold		0.0		0.0		ns
t_{INSU}	Input Latch Setup		0.7		0.9		ns
t_{ILA}	Latch Active Pulse Width		6.1		8.1		ns
Input Module Predicted Routing Delays[1]							
t_{IRD1}	FO=1 Routing Delay			2.6		3.5	ns
t_{IRD2}	FO=2 Routing Delay			3.4		4.6	ns
t_{IRD3}	FO=3 Routing Delay			4.6		6.1	ns
t_{IRD4}	FO=4 Routing Delay			5.4		7.2	ns
t_{IRD5}	FO=8 Routing Delay			7.0		9.3	ns
Global Clock Network							
t_{CKH}	Input Low to High	FO=32		7.3		9.8	ns
		FO=635		8.5		11.3	ns
t_{CKL}	Input High to Low	FO=32		7.2		9.6	ns
		FO=635		9.3		12.5	ns
t_{PWH}	Minimum Pulse Width High	FO=32	3.2		4.3		ns
		FO=635	3.9		5.2		ns
t_{PWL}	Minimum Pulse Width Low	FO=32	3.2		4.3		ns
		FO=635	3.9		5.2		ns
t_{CKSW}	Maximum Skew	FO=32		1.8		2.4	ns
		FO=635		1.8		2.4	ns
t_{SUEXT}	Input Latch External Setup	FO=32	0.0		0.0		ns
		FO=635	0.0		0.0		ns
t_{HEXT}	Input Latch External Hold	FO=32	3.0		4.0		ns
		FO=635	3.8		5.1		ns
t_P	Minimum Period (1/fmax)	FO=32	5.8		7.7		ns
		FO=635	6.8		9.1		ns
f_{HMAX}	Maximum Datapath Frequency	FO=32		172		130	MHz
		FO=635		147		110	MHz

Note:

1. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment. Optimization techniques may further reduce delays by 0 to 4 ns.

Pin Description

CLK Clock (Input)

ACT 1 only. TTL Clock input for global clock distribution network. The Clock input is buffered prior to clocking the logic modules. This pin can also be used as an I/O.

CLKA Clock A (Input)

ACT 2, 1200XL, 3200DX, and ACT 3 only. TTL Clock input for global clock distribution networks. The Clock input is buffered prior to clocking the logic modules. This pin can also be used as an I/O.

CLKB Clock B (Input)

ACT 2, 1200XL, 3200DX, and ACT 3 only. TTL Clock input for global clock distribution networks. The Clock input is buffered prior to clocking the logic modules. This pin can also be used as an I/O.

DCLK Diagnostic Clock (Input)

TTL Clock input for diagnostic probe and device programming. DCLK is active when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

GND Ground

LOW supply voltage.

HCLK Dedicated (Hard-wired) Array Clock (Input)

ACT 3 only. TTL Clock input for sequential modules. This input is directly wired to each S-module and offers clock speeds independent of the number of S-modules being driven. This pin can also be used as an I/O.

I/O Input/Output (Input, Output)

I/O pin functions as an input, output, tristate, or bi-directional buffer. Input and output levels are compatible with standard TTL and CMOS specifications. In the ACT 3 and 3200DX families, unused I/Os are automatically tri-stated. With this configuration, the input buffer internal to the I/O module is disabled. In the ACT 1, ACT 2 and 1200XL families, unused I/Os are automatically configured as bi-directional buffers where each buffer is configured as a LOW driver.

IOCLK Dedicated (Hard-wired) I/O Clock (Input)

ACT 3 only. TTL Clock input for I/O modules. This input is directly wired to each I/O module and offers clock speeds independent of the number of I/O modules being driven. This pin can also be used as an I/O.

IOPCL Dedicated (Hard-wired) I/O Preset/Clear (Input)

ACT 3 only. TTL input for I/O preset or clear. This global input is directly wired to the preset and clear inputs of all I/O registers. This pin functions as an I/O when no I/O preset or clear macros are used.

MODE Mode (Input)

The MODE pin controls the use of diagnostic pins (DCLK, PRA, PRB, SDI). When the MODE pin is HIGH, the special functions are active. When the MODE pin is LOW, the pins function as I/Os. To provide debugging capability, the MODE pin should be terminated to GND through a 10 kΩ resistor so that the MODE pin can be pulled high when required.

NC No Connection

This pin is not connected to circuitry within the device.

PRA, I/O Probe A (Output)

The Probe A pin is used to output data from any user-defined design node within the device. This independent diagnostic pin can be used in conjunction with the Probe B pin to allow real-time diagnostic output of any signal path within the device. The Probe A pin can be used as a user-defined I/O when debugging has been completed. The pin's probe capabilities can be permanently disabled to protect programmed design confidentiality. PRA is accessible when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

PRB, I/O Probe B (Output)

The Probe B pin is used to output data from any user-defined design node within the device. This independent diagnostic pin can be used in conjunction with the Probe A pin to allow real-time diagnostic output of any signal path within the device. The Probe B pin can be used as a user-defined I/O when verification has been completed. The pin's probe capabilities can be permanently disabled to protect programmed design confidentiality. PRB is accessible when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

SDI Serial Data Input (Input)

Serial data input for diagnostic probe and device programming. SDI is active when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

V_{CC} 5.0V Supply Voltage

HIGH supply voltage.

QCLKA/B,C,D Quadrant Clock (Input/Output)

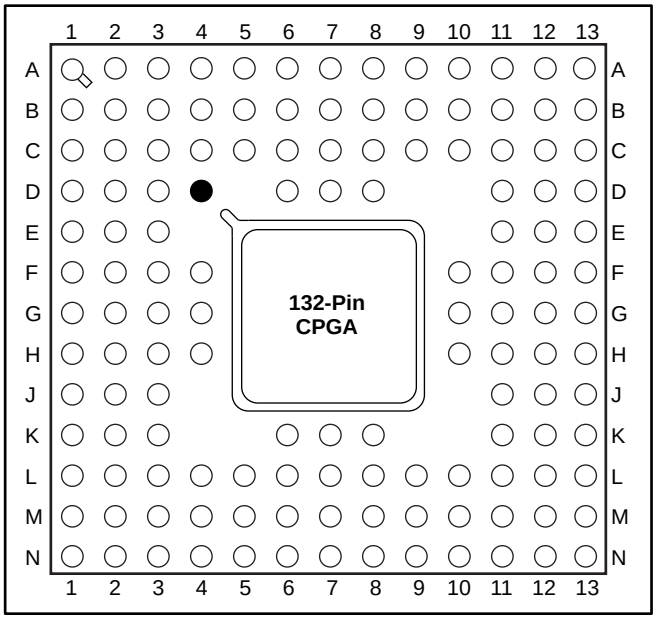
3200DX only. These four pins are the quadrant clock inputs. When not used as a register control signal, these pins can function as general purpose I/O.

TCK Test Clock

Clock signal to shift the JTAG data into the device. This pin functions as an I/O when the JTAG fuse is not programmed. JTAG pins are only available in the 3200DX device.

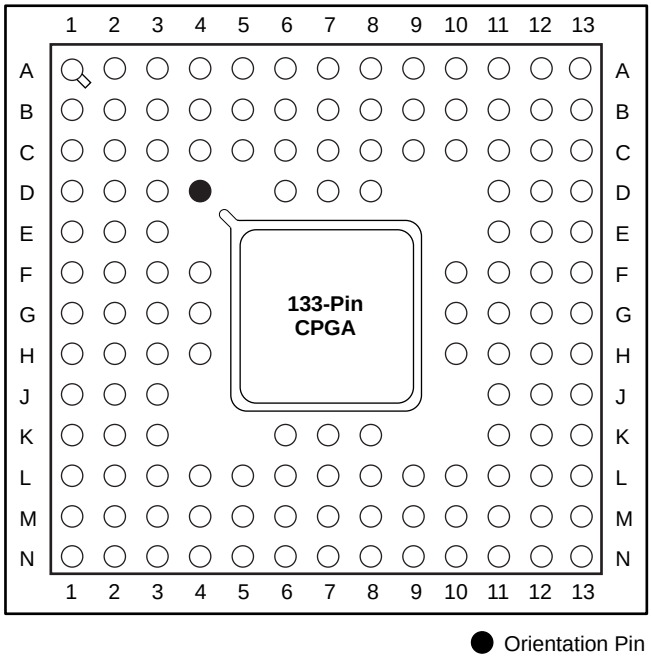
Package Pin Assignments (continued)

132-Pin CPGA (Top View)



Package Pin Assignments (continued)

133-Pin CPGA (Top View)



133-Pin CPGA

Pin Number	A1425A Function
A1	NC
A2	GND
A3	I/O
A4	I/O
A5	I/O
A6	PRA, I/O
A7	NC
A8	I/O
A9	I/O
A10	I/O
A11	I/O
A12	I/O
A13	NC
B1	I/O
B2	V_{CC}
B3	I/O
B4	I/O
B5	I/O
B6	CLKB, I/O
B7	V_{CC}
B8	I/O
B9	I/O
B10	I/O
B11	I/O
B12	V_{CC}
B13	I/O
C1	I/O
C2	SDI, I/O
C3	GND
C4	I/O
C5	I/O
C6	I/O
C7	GND
C8	I/O
C9	I/O
C10	IOCLK, I/O
C11	GND
C12	GND
C13	I/O
D1	I/O
D2	I/O
D3	I/O
D4	DCLK, I/O
D6	CLKA, I/O
D7	I/O
D8	I/O
D11	I/O
D12	I/O
D13	I/O
E1	I/O
E2	I/O
E3	MODE
E11	V_{CC}
E12	I/O
E13	I/O
F1	I/O
F2	I/O
F3	I/O
F4	I/O
F10	GND
F11	I/O
F12	I/O
F13	I/O
G1	NC
G2	V_{CC}
G3	GND
G4	I/O
G10	I/O
G11	GND
G12	V_{CC}
G13	NC
H1	I/O
H2	I/O
H3	I/O
H4	I/O
H10	I/O
H11	I/O
H12	I/O
H13	I/O
J1	I/O
J2	V_{CC}
J3	I/O
J11	I/O
J12	V_{CC}
J13	I/O
K1	I/O
K2	I/O
K3	I/O
K6	I/O
K7	HCLKA, I/O
K8	I/O
K11	I/O
K12	I/O
K13	I/O
L1	I/O
L2	I/O
L3	GND
L4	I/O
L5	I/O
L6	PRB, I/O
L7	GND
L8	I/O
L9	I/O
L10	IOPCL, I/O
L11	GND
L12	I/O
L13	I/O
M1	I/O
M2	V_{CC}
M3	GND
M4	I/O
M5	I/O
M6	I/O
M7	V_{CC}
M8	I/O
M9	I/O
M10	I/O
M11	I/O
M12	V_{CC}
M13	I/O
N1	NC
N2	I/O
N3	I/O
N4	I/O
N5	I/O
N6	I/O
N7	NC
N8	I/O
N9	I/O
N10	I/O
N11	I/O
N12	GND
N13	NC

257-Pin CPGA

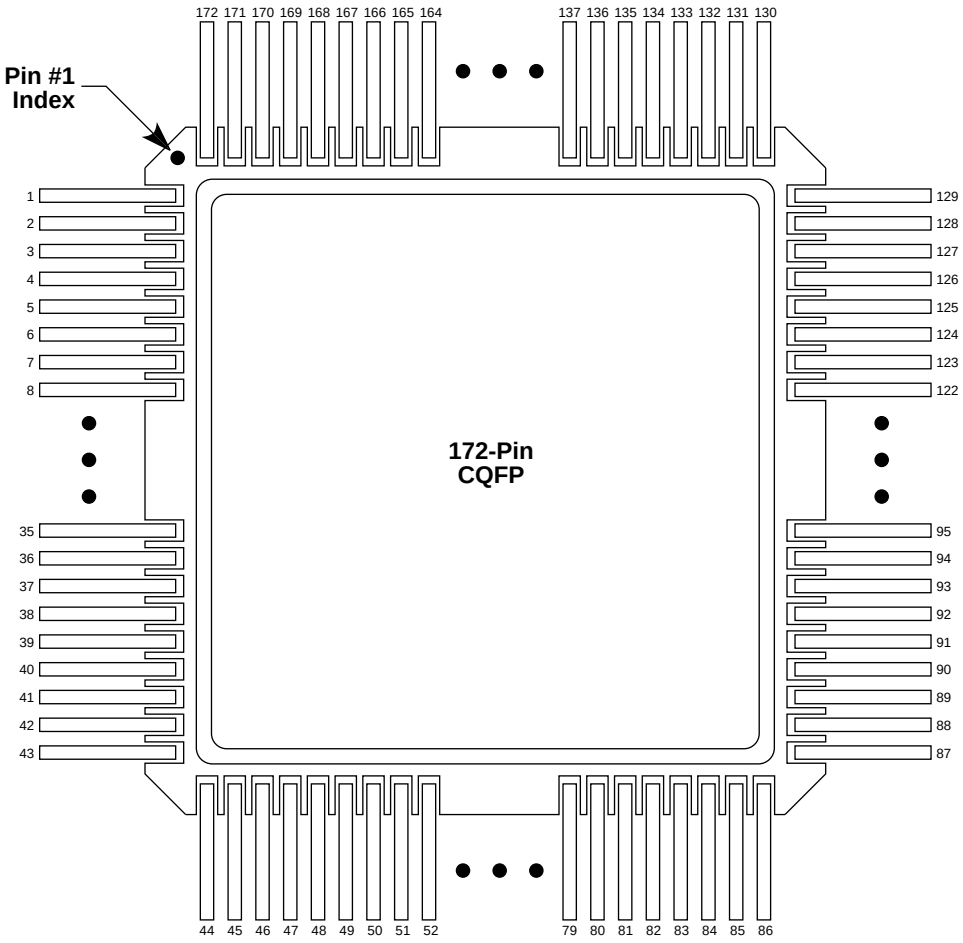
Pin Number	A14100A Function
A1	I/O
A2	I/O
A3	I/O
A4	I/O
A5	MODE
A6	I/O
A7	I/O
A8	I/O
A9	I/O
A10	I/O
A11	I/O
A12	I/O
A13	I/O
A14	I/O
A15	I/O
A16	I/O
A17	I/O
A18	I/O
A19	I/O
B1	I/O
B2	I/O
B3	I/O
B4	SDI, I/O
B5	I/O
B6	I/O
B7	I/O
B8	I/O
B9	I/O
B10	I/O
B11	I/O
B12	I/O
B13	I/O
B14	I/O
B15	I/O
B16	GND
B17	I/O
B18	I/O
B19	I/O
C1	I/O
C2	I/O
C3	V_{CC}
C4	GND
C5	I/O
C6	I/O

Pin Number	A14100A Function
C7	I/O
C8	I/O
C9	I/O
C10	V_{CC}
C11	I/O
C12	I/O
C13	V_{CC}
C14	I/O
C15	I/O
C16	I/O
C17	V_{CC}
C18	I/O
C19	I/O
D1	I/O
D2	I/O
D3	I/O
D4	GND
D5	I/O
D6	I/O
D7	I/O
D8	I/O
D9	I/O
D10	GND
D11	I/O
D12	I/O
D13	I/O
D14	I/O
D15	I/O
D16	GND
D17	I/O
D18	I/O
D19	I/O
E1	I/O
E2	I/O
E3	I/O
E4	DCLK, I/O
E5	NC
E7	I/O
E9	I/O
E11	GND
E13	I/O
E16	I/O
E17	I/O
E18	I/O

Pin Number	A14100A Function
E19	I/O
F1	I/O
F2	I/O
F3	I/O
F4	I/O
F16	I/O
F17	I/O
F18	I/O
F19	I/O
G1	I/O
G2	I/O
G3	I/O
G4	I/O
G5	I/O
G15	I/O
G16	I/O
G17	I/O
G18	I/O
G19	I/O
H1	I/O
H2	I/O
H3	I/O
H4	I/O
H16	I/O
H17	I/O
H18	I/O
H19	I/O
J1	PRA, I/O
J2	I/O
J3	I/O
J4	I/O
J5	GND
J15	I/O
J16	HCLK, I/O
J17	PRB, I/O
J18	I/O
J19	I/O
K1	I/O
K2	I/O
K3	V_{CC}
K4	GND
K16	GND
K17	V_{CC}
K18	I/O

Package Pin Assignments (continued)

172-Pin CQFP (Top View)



208-Pin CQFP (Continued)

Pin Number	A32100DX Function
130	V_{CC}
131	GND
132	V_{CC}
133	V_{CC}
134	I/O
135	I/O
136	V_{CC}
137	I/O
138	I/O
139	I/O
140	I/O
141	I/O
142	I/O
143	I/O
144	I/O
145	I/O
146	I/O
147	I/O
148	I/O
149	I/O
150	GND
151	I/O
152	I/O
153	I/O
154	I/O
155	I/O
156	I/O

Pin Number	A32100DX Function
157	GND
158	I/O
159	SDI, I/O
160	I/O
161	I/O (WD)
162	I/O (WD)
163	I/O
164	V_{CC}
165	I/O
166	I/O
167	I/O
168	I/O (WD)
169	I/O (WD)
170	I/O
171	QCLKD, I/O
172	I/O
173	I/O
174	I/O
175	I/O
176	I/O (WD)
177	I/O (WD)
178	PRA, I/O
179	I/O
180	CLKA, I/O
181	I/O
182	V_{CC}
183	V_{CC}

Pin Number	A32100DX Function
184	GND
185	I/O
186	CLKB, I/O
187	I/O
188	PRB, I/O
189	I/O
190	I/O (WD)
191	I/O (WD)
192	I/O
193	I/O
194	I/O (WD)
195	I/O (WD)
196	QCLKC, I/O
197	I/O
198	I/O
199	I/O
200	I/O
201	I/O
202	V_{CC}
203	I/O (WD)
204	I/O (WD)
205	I/O
206	I/O
207	DCLK, I/O
208	I/O

256-Pin CQFP (Continued)

Pin Number	A14100A Function	A32200DX Function
133	I/O	I/O
134	I/O	I/O
135	I/O	I/O
136	I/O	I/O
137	I/O	I/O
138	I/O	I/O
139	I/O	GND
140	I/O	I/O
141	V_{CC}	I/O
142	I/O	I/O
143	I/O	I/O
144	I/O	I/O
145	I/O	I/O
146	I/O	I/O
147	I/O	I/O
148	I/O	I/O
149	I/O	I/O
150	I/O	I/O
151	I/O	I/O
152	I/O	I/O
153	I/O	I/O
154	I/O	I/O
155	I/O	V_{CC}
156	I/O	I/O
157	I/O	I/O
158	GND	V_{CC}
159	V_{CC}	V_{CC}
160	GND	GND
161	V_{CC}	I/O
162	I/O	I/O
163	I/O	I/O
164	I/O	I/O
165	I/O	GND
166	I/O	I/O
167	I/O	I/O
168	I/O	I/O
169	I/O	I/O
170	I/O	V_{CC}
171	I/O	I/O
172	I/O	I/O
173	I/O	I/O
174	V_{CC}	I/O
175	GND	I/O
176	GND	I/O
177	I/O	I/O
178	I/O	I/O
179	I/O	I/O
180	I/O	GND
181	I/O	I/O
182	I/O	I/O
183	I/O	I/O
184	I/O	I/O
185	I/O	I/O
186	I/O	I/O
187	I/O	I/O
188	IOCLK, I/O	MODE
189	GND	V_{CC}
190	I/O	GND
191	I/O	NC
192	I/O	NC
193	I/O	NC
194	I/O	I/O
195	I/O	DCLK, I/O
196	I/O	I/O
197	I/O	I/O
198	I/O	I/O
199	I/O	I/O (WD)
200	I/O	I/O (WD)
201	I/O	V_{CC}
202	I/O	I/O
203	I/O	I/O
204	I/O	I/O
205	I/O	I/O
206	I/O	GND
207	I/O	I/O
208	I/O	I/O
209	I/O	QCLKC, I/O
210	I/O	I/O
211	I/O	I/O (WD)
212	I/O	I/O (WD)
213	I/O	I/O
214	I/O	I/O
215	I/O	I/O (WD)
216	I/O	I/O (WD)
217	I/O	I/O
218	I/O	PRB, I/O
219	CLKA, I/O	I/O
220	CLKB, I/O	CLKB, I/O
221	V_{CC}	I/O
222	GND	GND
223	V_{CC}	GND
224	GND	V_{CC}
225	PRA, I/O	V_{CC}
226	I/O	I/O
227	I/O	CLKA, I/O
228	I/O	I/O
229	I/O	PRA, I/O
230	I/O	I/O
231	I/O	I/O
232	I/O	I/O (WD)
233	I/O	I/O (WD)
234	I/O	I/O
235	I/O	I/O
236	I/O	I/O
237	I/O	I/O
238	I/O	I/O
239	I/O	I/O
240	GND	QCLKD, I/O
241	I/O	I/O
242	I/O	I/O (WD)
243	I/O	GND
244	I/O	I/O (WD)
245	I/O	I/O
246	I/O	I/O
247	I/O	I/O
248	I/O	V_{CC}
249	I/O	I/O
250	I/O	I/O (WD)
251	I/O	I/O (WD)
252	I/O	I/O
253	I/O	SDI, I/O
254	I/O	I/O
255	I/O	GND
256	DCLK, I/O	NC

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