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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

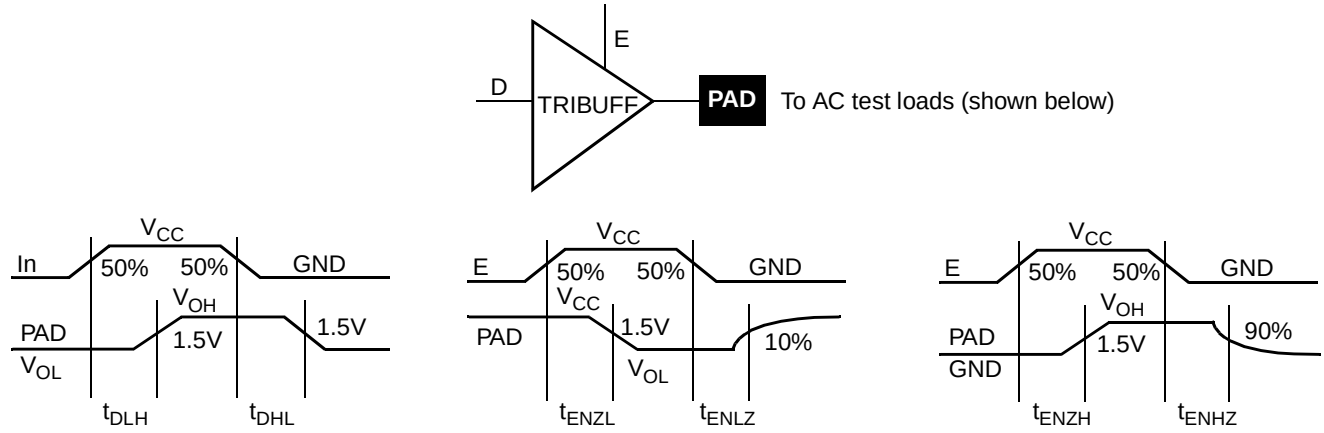
Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	295
Number of Logic Elements/Cells	-
Total RAM Bits	-
Number of I/O	57
Number of Gates	1200
Voltage - Supply	4.5V ~ 5.5V
Mounting Type	Through Hole
Operating Temperature	-55°C ~ 125°C (TC)
Package / Case	84-BCPGA
Supplier Device Package	84-CPGA (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/microsemi/a1010b-1pg84m

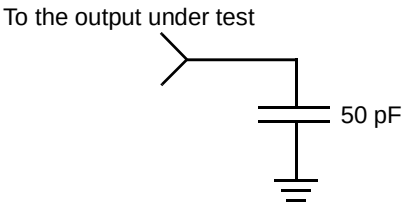
Parameter Measurement

Output Buffer Delays

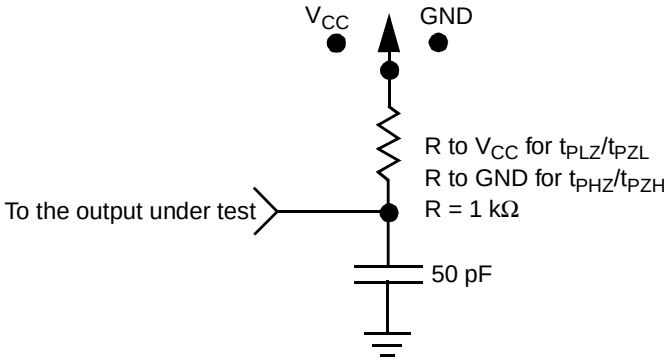


AC Test Load

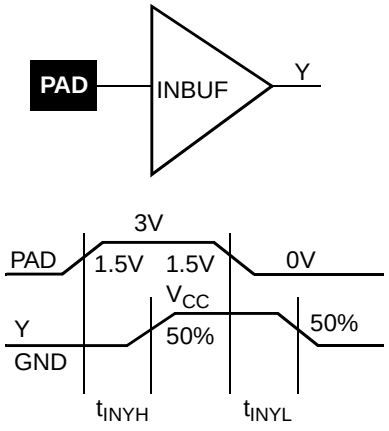
Load 1
(Used to measure propagation delay)



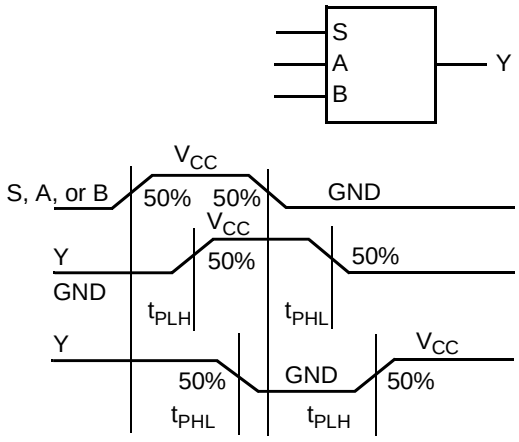
Load 2
(Used to measure rising/falling edges)



Input Buffer Delays

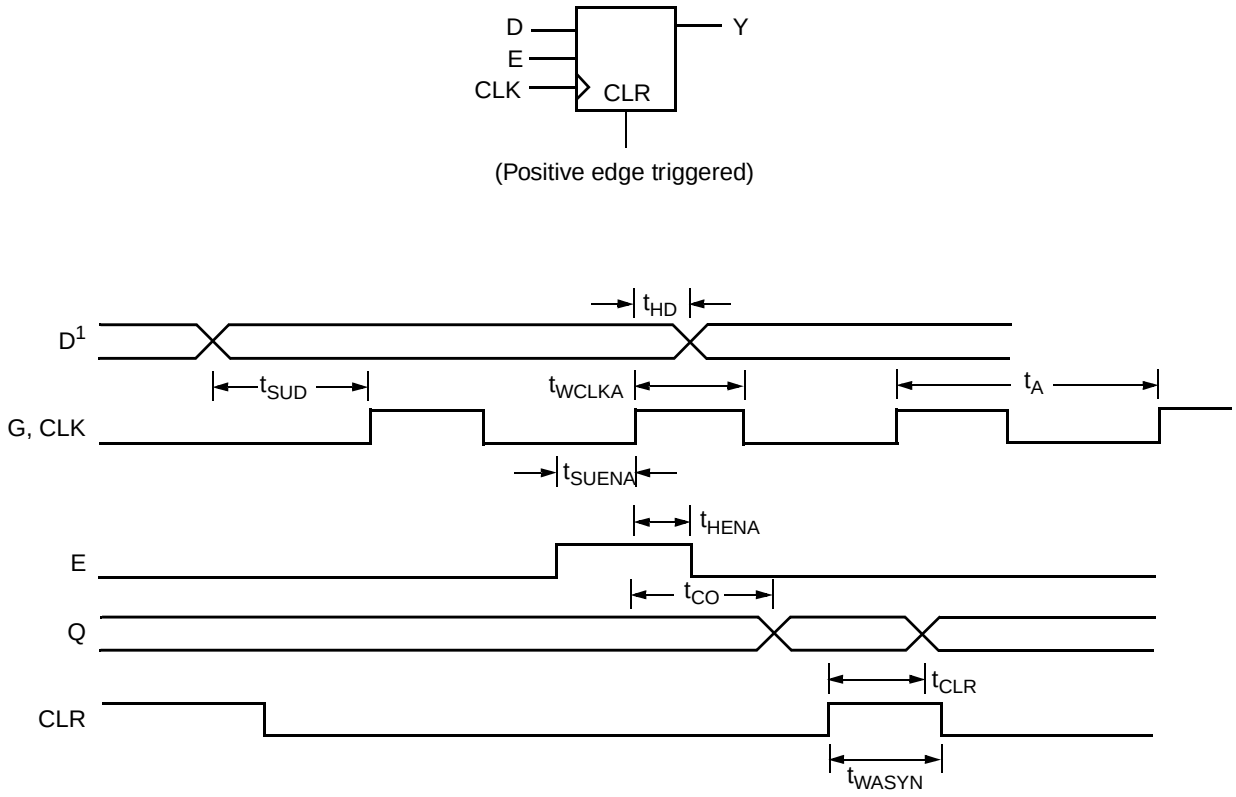


Combinatorial Macro Delays



Sequential Timing Characteristics

Flip-Flops and Latches (ACT 3)

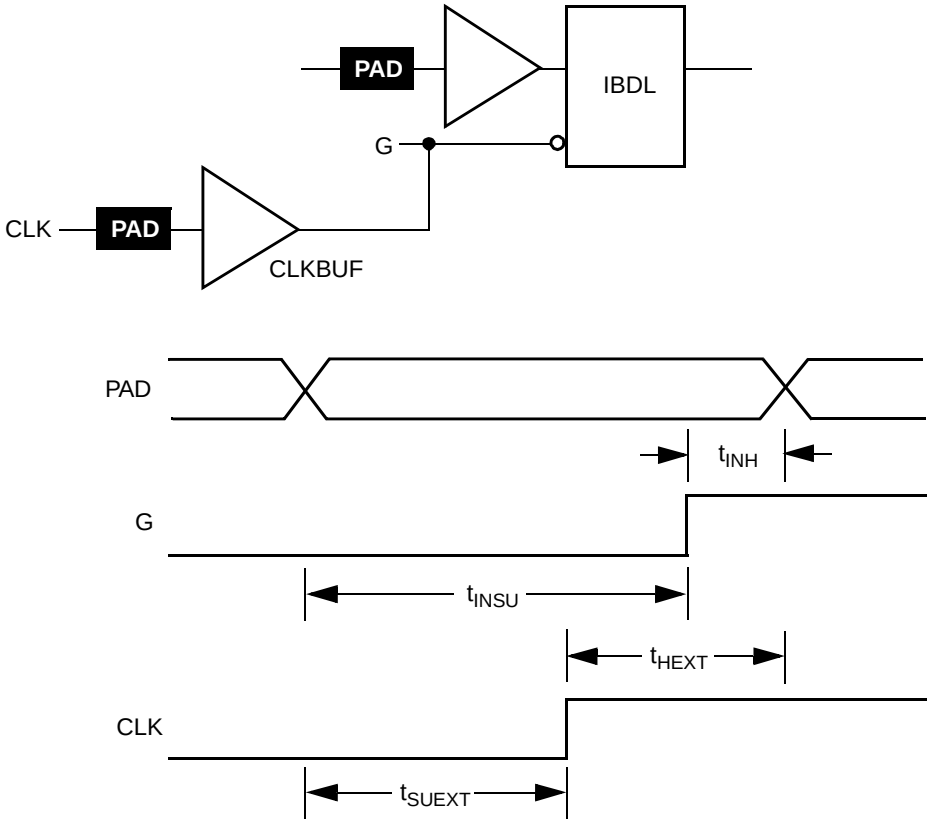


Note:

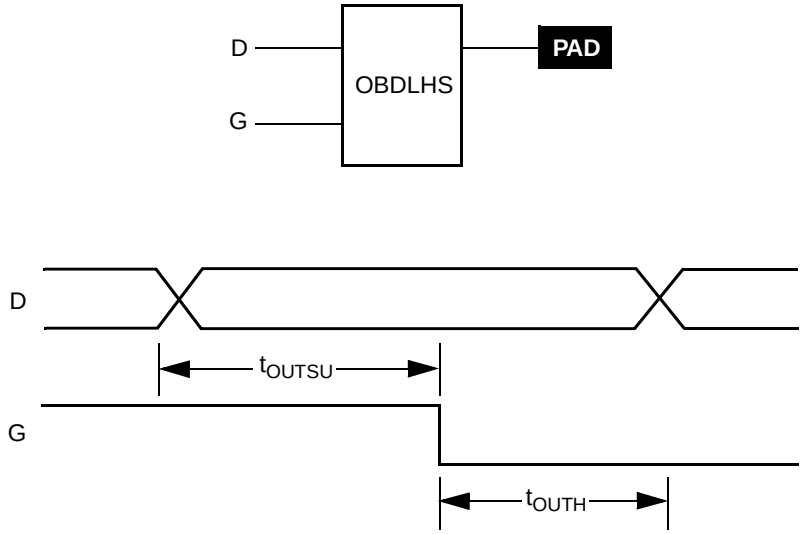
1. D represents all data functions involving A, B, and S for multiplexed flip-flops.

Sequential Timing Characteristics (continued)

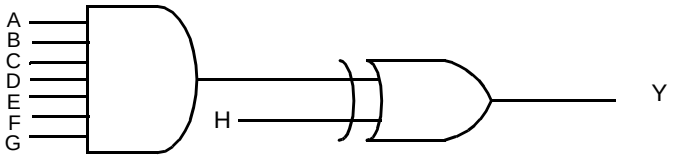
Input Buffer Latches (ACT 2 and 1200XL/3200DX)

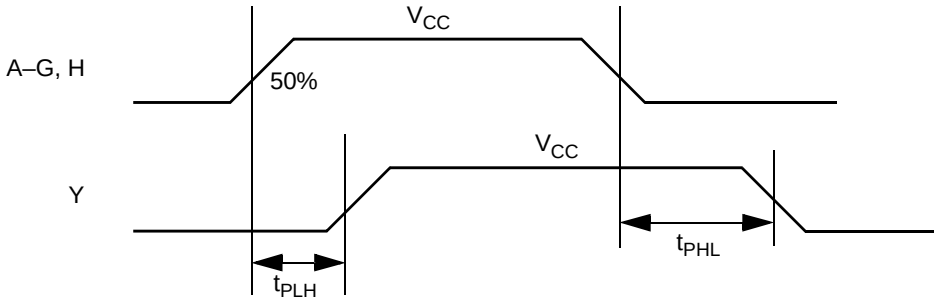


Output Buffer Latches (ACT 2 and 1200XL/3200DX)

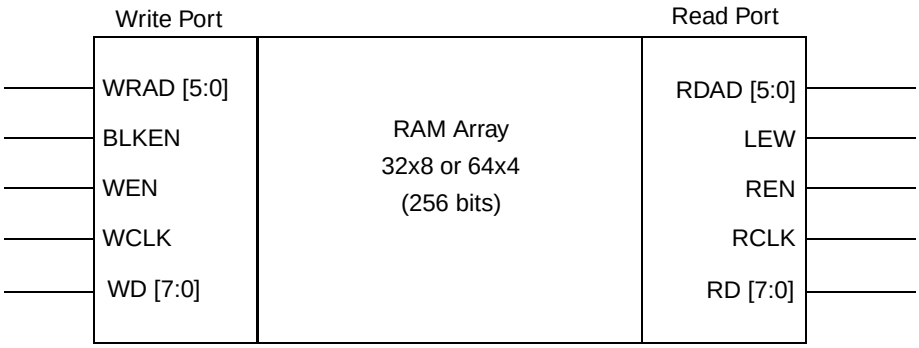


Decode Module Timing





SRAM Timing Characteristics



ACT 1 Timing Characteristics (continued)

(Worst-Case Military Conditions, V_{CC} = 4.5V, T_J = 125°C)

			'–1' Speed		'Std' Speed		
Parameter	**Description**		**Min.**	**Max.**	**Min.**	**Max.**	**Units**
Global Clock Network							
t_{CKH}	Input Low to High	FO = 16 FO = 128		7.8 8.9		9.2 10.5	ns
t_{CKL}	Input High to Low	FO = 16 FO = 128		10.3 11.2		12.1 13.2	ns
t_{PWH}	Minimum Pulse Width High	FO = 16 FO = 128	10.4 10.9		12.2 12.9		ns
t_{PWL}	Minimum Pulse Width Low	FO = 16 FO = 128	10.4 10.9		12.2 12.9		ns
t_{CKSW}	Maximum Skew	FO = 16 FO = 128		1.9 2.9		2.2 3.4	ns
t_P	Minimum Period	FO = 16 FO = 128	21.7 23.2		25.6 27.3		ns
f_{MAX}	Maximum Frequency	FO = 16 FO = 128		46 44		40 37	MHz
TTL Output Module Timing[1]							
t_{DLH}	Data to Pad High			12.1		14.2	ns
t_{DHL}	Data to Pad Low			13.8		16.3	ns
t_{ENZH}	Enable Pad Z to High			12.0		14.1	ns
t_{ENZL}	Enable Pad Z to Low			14.6		17.1	ns
t_{ENHZ}	Enable Pad High to Z			16.0		18.8	ns
t_{ENLZ}	Enable Pad Low to Z			14.5		17.0	ns
d_{TLH}	Delta Low to High			0.09		0.11	ns/pF
d_{THL}	Delta High to Low			0.12		0.15	ns/pF
CMOS Output Module Timing[1]							
t_{DLH}	Data to Pad High			15.1		17.7	ns
t_{DHL}	Data to Pad Low			11.5		13.6	ns
t_{ENZH}	Enable Pad Z to High			12.0		14.1	ns
t_{ENZL}	Enable Pad Z to Low			14.6		17.1	ns
t_{ENHZ}	Enable Pad High to Z			16.0		18.8	ns
t_{ENLZ}	Enable Pad Low to Z			14.5		17.0	ns
d_{TLH}	Delta Low to High			0.16		0.18	ns/pF
d_{THL}	Delta High to Low			0.09		0.11	ns/pF

Notes:

1. *Delays based on 50 pF loading.*
2. *SSO information can be found in the* Simultaneously Switching Output Limits for Actel FPGAs *application note at http://www.actel.com/appnotes.*

A1240A Timing Characteristics (continued)

(Worst-Case Military Conditions, V_{CC} = 4.5V, T_J = 125°C)

		'–1' Speed		'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
TTL Output Module Timing[1]						
t_{DLH}	Data to Pad High		11.0		13.0	ns
t_{DHL}	Data to Pad Low		13.9		16.4	ns
t_{ENZH}	Enable Pad Z to High		12.3		14.4	ns
t_{ENZL}	Enable Pad Z to Low		16.1		19.0	ns
t_{ENHZ}	Enable Pad High to Z		9.8		11.5	ns
t_{ENLZ}	Enable Pad Low to Z		11.5		13.6	ns
t_{GLH}	G to Pad High		12.4		14.6	ns
t_{GHL}	G to Pad Low		15.5		18.2	ns
d_{TLH}	Delta Low to High		0.09		0.11	ns/pF
d_{THL}	Delta High to Low		0.17		0.20	ns/pF
CMOS Output Module Timing[1]						
t_{DLH}	Data to Pad High		14.0		16.5	ns
t_{DHL}	Data to Pad Low		11.7		13.7	ns
t_{ENZH}	Enable Pad Z to High		12.3		14.4	ns
t_{ENZL}	Enable Pad Z to Low		16.1		19.0	ns
t_{ENHZ}	Enable Pad High to Z		9.8		11.5	ns
t_{ENLZ}	Enable Pad Low to Z		11.5		13.6	ns
t_{GLH}	G to Pad High		12.4		14.6	ns
t_{GHL}	G to Pad Low		15.5		18.2	ns
d_{TLH}	Delta Low to High		0.17		0.20	ns/pF
d_{THL}	Delta High to Low		0.12		0.15	ns/pF

Notes:

1. *Delays based on 50 pF loading.*
2. *SSO information can be found in the* Simultaneously Switching Output Limits for Actel FPGAs *application note at http://www.actel.com/appnotes.*

A1280A Timing Characteristics

(Worst-Case Military Conditions, V_{CC} = 4.5V, T_J = 125°C)

		'–1' Speed		'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
Logic Module Propagation Delays[1]						
t_{PD1}	Single Module		5.2		6.1	ns
t_{CO}	Sequential Clk to Q		5.2		6.1	ns
t_{GO}	Latch G to Q		5.2		6.1	ns
t_{RS}	Flip-Flop (Latch) Reset to Q		5.2		6.1	ns
Logic Module Predicted Routing Delays[2]						
t_{RD1}	FO=1 Routing Delay		2.4		2.8	ns
t_{RD2}	FO=2 Routing Delay		3.4		4.0	ns
t_{RD3}	FO=3 Routing Delay		4.2		4.9	ns
t_{RD4}	FO=4 Routing Delay		5.1		6.0	ns
t_{RD8}	FO=8 Routing Delay		9.2		10.8	ns
Logic Module Sequential Timing[3, 4]						
t_{SUD}	Flip-Flop (Latch) Data Input Setup	0.5		0.5		ns
t_{HD}	Flip-Flop (Latch) Data Input Hold	0.0		0.0		ns
t_{SUENA}	Flip-Flop (Latch) Enable Setup	1.3		1.3		ns
t_{HENA}	Flip-Flop (Latch) Enable Hold	0.0		0.0		ns
t_{WCLKA}	Flip-Flop (Latch) Clock Active Pulse Width	7.4		8.6		ns
t_{WASYN}	Flip-Flop (Latch) Asynchronous Pulse Width	7.4		8.6		ns
t_A	Flip-Flop Clock Input Period	16.4		22.1		ns
t_{INH}	Input Buffer Latch Hold	2.5		2.5		ns
t_{INSU}	Input Buffer Latch Setup	–3.5		–3.5		ns
t_{OUTH}	Output Buffer Latch Hold	0.0		0.0		ns
t_{OUTSU}	Output Buffer Latch Setup	0.5		0.5		ns
f_{MAX}	Flip-Flop (Latch) Clock Frequency		60		41	MHz

Notes:

1. *For dual-module macros, use $t_{PD1} + t_{RD1} + t_{PDn}$, $t_{CO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.*
2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*
3. *Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the DirectTime Analyzer utility.*
4. *Setup and hold timing parameters for the input buffer latch are defined with respect to the PAD and the D input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.*

A32100DX Timing Characteristics

(Worst-Case Military Conditions, V_{CC} = 4.5V, T_J = 125°C)

		'–1' Speed		'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
Logic Module Combinatorial Functions						
t_{PD}	Internal Array Module Delay		3.1		4.1	ns
t_{PDD}	Internal Decode Module Delay		3.3		4.3	ns
Logic Module Predicted Routing Delays[1]						
t_{RD1}	FO=1 Routing Delay		1.3		1.8	ns
t_{RD2}	FO=2 Routing Delay		1.9		2.6	ns
t_{RD3}	FO=3 Routing Delay		2.6		3.4	ns
t_{RD4}	FO=4 Routing Delay		3.3		4.3	ns
t_{RD5}	FO=8 Routing Delay		0.6		0.8	ns
t_{RDD}	Decode-to-Output Routing Delay		0.5		0.6	ns
Logic Module Sequential Timing						
t_{CO}	Flip-Flop Clock-to-Output		3.1		4.1	ns
t_{GO}	Latch Gate-to-Output		3.1		4.1	ns
t_{SU}	Flip-Flop (Latch) Setup Time	0.5		0.6		ns
t_{H}	Flip-Flop (Latch) Hold Time	0.0		0.0		ns
t_{RO}	Flip-Flop (Latch) Reset to Output		3.1		4.1	ns
t_{SUENA}	Flip-Flop (Latch) Enable Setup	0.9		1.2		ns
t_{HENA}	Flip-Flop (Latch) Enable Hold	0.0		0.0		ns
t_{WCLKA}	Flip-Flop (Latch) Clock Active Pulse Width	4.3		5.8		ns
t_{WASYN}	Flip-Flop (Latch) Asynchronous Pulse Width	5.6		7.5		ns

Note:

1. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.

A32100DX Timing Characteristics (continued)

(Worst-Case Military Conditions, V_{CC} = 4.5V, T_J = 125°C)

			'–1' Speed		'Std' Speed		
Parameter	**Description**		**Min.**	**Max.**	**Min.**	**Max.**	**Units**
Input Module Propagation Delays							
t_{INPY}	Input Data Pad to Y			1.9		2.6	ns
t_{INGO}	Input Latch Gate-to-Output			4.0		5.3	ns
t_{INH}	Input Latch Hold		0.0		0.0		ns
t_{INSU}	Input Latch Setup		0.7		0.9		ns
t_{ILA}	Latch Active Pulse Width		6.1		8.1		ns
Input Module Predicted Routing Delays[1]							
t_{IRD1}	FO=1 Routing Delay			2.2		2.9	ns
t_{IRD2}	FO=2 Routing Delay			2.8		3.8	ns
t_{IRD3}	FO=3 Routing Delay			3.5		4.7	ns
t_{IRD4}	FO=4 Routing Delay			3.5		4.7	ns
t_{IRD8}	FO=8 Routing Delay			5.6		7.5	ns
Global Clock Network							
t_{CKH}	Input Low to High	FO=32 FO=635		6.5 7.9		8.7 10.6	ns ns
t_{CKL}	Input High to Low	FO=32 FO=635		6.6 8.8		8.8 11.8	ns ns
t_{PWH}	Minimum Pulse Width High	FO=32 FO=635	4.1 4.6		5.5 6.1		ns ns
t_{PWL}	Minimum Pulse Width Low	FO=32 FO=635	4.1 4.6		5.5 6.1		ns ns
t_{CKSW}	Maximum Skew	FO=32 FO=635		1.8 1.8		2.4 2.4	ns ns
t_{SUEXT}	Input Latch External Setup	FO=32 FO=635	0.0 0.0		0.0 0.0		ns ns
t_{HEXT}	Input Latch External Hold	FO=32 FO=635	3.0 3.8		4.0 5.1		ns ns
t_P	Minimum Period (1/fmax)	FO=32 FO=635	7.1 7.9		9.5 10.5		ns ns
f_{HMAX}	Maximum Datapath Frequency	FO=32 FO=635		140 126		105 95	MHz MHz

Note:

1. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment. Optimization techniques may further reduce delays by 0 to 4 ns.

A32200DX Timing Characteristics (continued)

(Worst-Case Military Conditions, V_{CC} = 4.5V, T_J = 125°C)

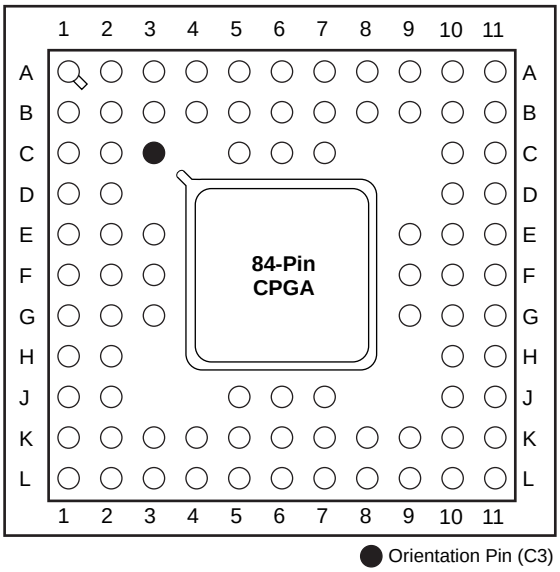
		'–1' Speed		'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
TTL Output Module Timing[1]						
t_{DLH}	Data to Pad High		5.1		6.8	ns
t_{DHL}	Data to Pad Low		6.3		8.3	ns
t_{ENZH}	Enable Pad Z to High		6.6		8.8	ns
t_{ENZL}	Enable Pad Z to Low		7.1		9.5	ns
t_{ENHZ}	Enable Pad High to Z		11.5		15.3	ns
t_{ENLZ}	Enable Pad Low to Z		11.5		15.3	ns
t_{GLH}	G to Pad High		11.5		15.3	ns
t_{GHL}	G to Pad Low		12.3		16.5	ns
t_{LSU}	I/O Latch Output Setup	0.4		0.5		ns
t_{LH}	I/O Latch Output Hold	0.0		0.0		ns
t_{LCO}	I/O Latch Clock-Out (Pad-to-Pad) 32 I/O		11.5		15.4	ns
t_{ACO}	Array Latch Clock-Out (Pad-to-Pad) 32 I/O		16.3		21.7	ns
d_{TLH}	Capacitive Loading, Low to High		0.04		0.06	ns/pF
d_{THL}	Capacitive Loading, High to Low		0.06		0.08	ns/pF
t_{WDO}	Hard-Wired Wide Decode Output		0.05		0.07	ns
CMOS Output Module Timing[1]						
t_{DLH}	Data to Pad High		5.1		6.8	ns
t_{DHL}	Data to Pad Low		6.3		8.3	ns
t_{ENZH}	Enable Pad Z to High		6.6		8.8	ns
t_{ENZL}	Enable Pad Z to Low		7.1		9.5	ns
t_{ENHZ}	Enable Pad High to Z		11.5		15.3	ns
t_{ENLZ}	Enable Pad Low to Z		11.5		15.3	ns
t_{GLH}	G to Pad High		11.5		15.3	ns
t_{GHL}	G to Pad Low		12.3		16.5	ns
t_{LSU}	I/O Latch Setup	0.4		0.5		ns
t_{LH}	I/O Latch Hold	0.0		0.0		ns
t_{LCO}	I/O Latch Clock-Out (Pad-to-Pad) 32 I/O		13.7		18.2	ns
t_{ACO}	Array Latch Clock-Out (Pad-to-Pad) 32 I/O		19.2		25.6	ns
d_{TLH}	Capacitive Loading, Low to High		0.06		0.08	ns/pF
d_{THL}	Capacitive Loading, High to Low		0.05		0.07	ns/pF
t_{WDO}	Hard-Wired Wide Decode Output		0.05		0.07	ns

Notes:

1. *Delays based on 35 pF loading.*
2. *SSO information can be found in the* Simultaneously Switching Output Limits for Actel FPGAs *application note at http://www.actel.com/appnotes.*

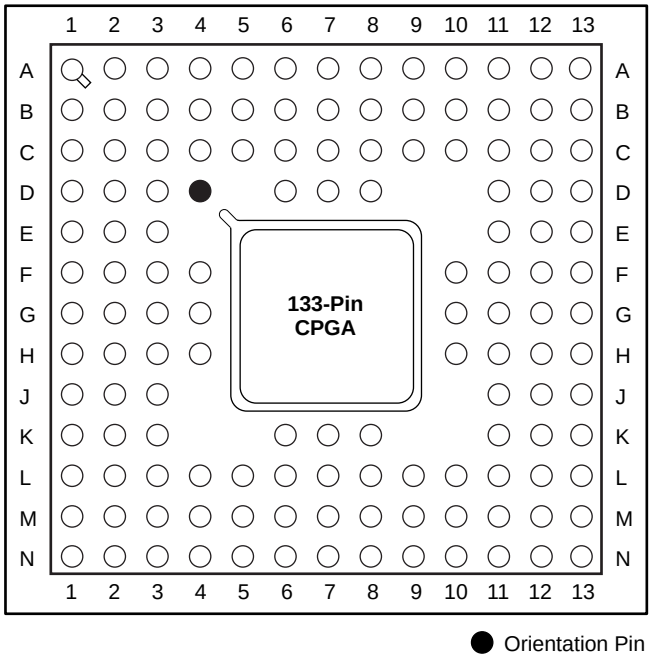
Package Pin Assignments

84-Pin CPGA (Top View)



Package Pin Assignments (continued)

133-Pin CPGA (Top View)



207-Pin CPGA

Pin Number	A1460A Function
A1	NC
A2	NC
A3	I/O
A4	I/O
A5	I/O
A6	I/O
A7	I/O
A8	I/O
A9	I/O
A10	I/O
A11	I/O
A12	I/O
A13	I/O
A14	I/O
A15	I/O
A16	NC
A17	NC
B1	NC
B2	V_{CC}
B3	I/O
B4	I/O
B5	I/O
B6	I/O
B7	I/O
B8	I/O
B9	V_{CC}
B10	I/O
B11	I/O
B12	I/O
B13	I/O
B14	I/O
B15	I/O
B16	V_{CC}
B17	NC
C1	NC
C2	NC
C3	SDI, I/O
C4	I/O
C5	I/O
C6	I/O
C7	I/O
C8	I/O
C9	I/O

Pin Number	A1460A Function
C10	I/O
C11	I/O
C12	I/O
C13	I/O
C14	I/O
C15	GND
C16	I/O
C17	I/O
D1	I/O
D2	I/O
D3	I/O
D4	GND
D5	GND
D6	I/O
D7	MODE
D8	I/O
D9	GND
D10	I/O
D11	V_{CC}
D12	I/O
D13	I/O
D14	GND
D15	I/O
D16	I/O
D17	I/O
E1	I/O
E2	I/O
E3	I/O
E4	DCLK, I/O
E14	I/O
E15	I/O
E16	I/O
E17	I/O
F1	I/O
F2	I/O
F3	I/O
F4	I/O
F14	I/O
F15	I/O
F16	I/O
F17	I/O
G1	I/O
G2	I/O

Pin Number	A1460A Function
G3	I/O
G4	I/O
G14	I/O
G15	I/O
G16	I/O
G17	I/O
H1	PRA, I/O
H2	I/O
H3	I/O
H4	I/O
H14	I/O
H15	I/O
H16	I/O
H17	I/O
J1	I/O
J2	V_{CC}
J3	CLKB, I/O
J4	GND
J14	GND
J15	HCLK, I/O
J16	V_{CC}
J17	I/O
K1	CLKA, I/O
K2	I/O
K3	I/O
K4	I/O
K14	I/O
K15	I/O
K16	PRB, I/O
K17	I/O
L1	I/O
L2	I/O
L3	I/O
L4	I/O
L14	I/O
L15	I/O
L16	I/O
L17	I/O
M1	I/O
M2	I/O
M3	I/O
M4	I/O
M14	I/O

207-Pin CPGA (Continued)

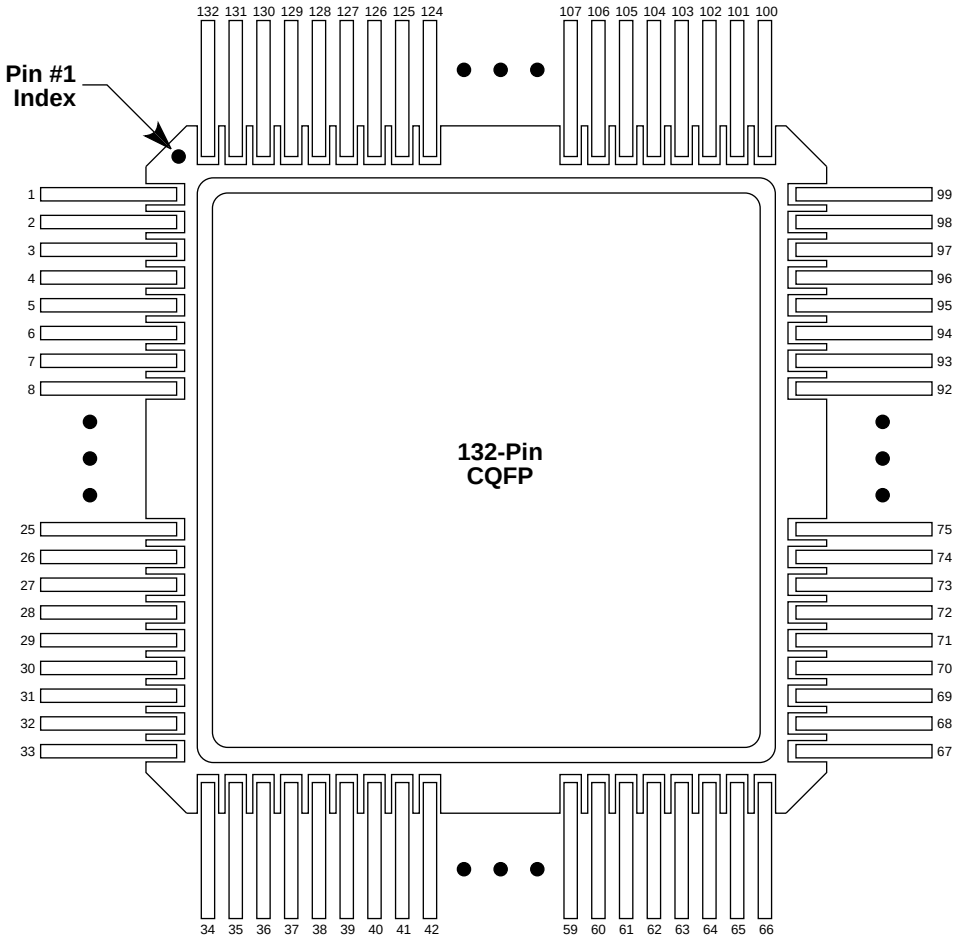
Pin Number	A1460A Function
M15	I/O
M16	I/O
M17	I/O
N1	I/O
N2	I/O
N3	I/O
N4	I/O
N14	IOPCL, I/O
N15	I/O
N16	I/O
N17	I/O
P1	I/O
P2	I/O
P3	GND
P4	GND
P5	IOCLK, I/O
P6	I/O
P7	GND
P8	I/O
P9	GND
P10	I/O
P11	I/O
P12	V_{CC}
P13	I/O
P14	GND
P15	I/O
P16	I/O

Pin Number	A1460A Function
P17	I/O
R1	I/O
R2	I/O
R3	I/O
R4	I/O
R5	I/O
R6	I/O
R7	I/O
R8	I/O
R9	I/O
R10	I/O
R11	I/O
R12	I/O
R13	I/O
R14	I/O
R15	GND
R16	I/O
R17	I/O
S1	NC
S2	V_{CC}
S3	NC
S4	I/O
S5	I/O
S6	I/O
S7	I/O
S8	I/O
S9	V_{CC}

Pin Number	A1460A Function
S10	I/O
S11	I/O
S12	I/O
S13	I/O
S14	I/O
S15	I/O
S16	V_{CC}
S17	NC
T1	NC
T2	NC
T3	I/O
T4	I/O
T5	V_{CC}
T6	I/O
T7	I/O
T8	I/O
T9	I/O
T10	I/O
T11	I/O
T12	I/O
T13	I/O
T14	I/O
T15	I/O
T16	NC
T17	NC

Package Pin Assignments (continued)

132-Pin CQFP (Top View)



172-Pin CQFP

Pin Number	A1280A Function	A1280XL Function
1	MODE	MODE
2	I/O	I/O
3	I/O	I/O
4	I/O	I/O
5	I/O	I/O
6	I/O	I/O
7	GND	GND
8	I/O	I/O
9	I/O	I/O
10	I/O	I/O
11	I/O	I/O
12	V_{CC}	V_{CC}
13	I/O	I/O
14	I/O	I/O
15	I/O	I/O
16	I/O	I/O
17	GND	GND
18	I/O	I/O
19	I/O	I/O
20	I/O	I/O
21	I/O	I/O
22	GND	GND
23	V_{CC}	V_{CC}
24	V_{CC}	V_{CC}
25	I/O	I/O
26	I/O	I/O
27	V_{CC}	V_{CC}
28	I/O	I/O
29	I/O	I/O
30	I/O	I/O
31	I/O	I/O
32	GND	GND
33	I/O	I/O
34	I/O	I/O
35	I/O	I/O
36	I/O	I/O
37	GND	GND
38	I/O	I/O
39	I/O	I/O
40	I/O	I/O
41	I/O	I/O
42	I/O	I/O
43	I/O	I/O
44	I/O	I/O

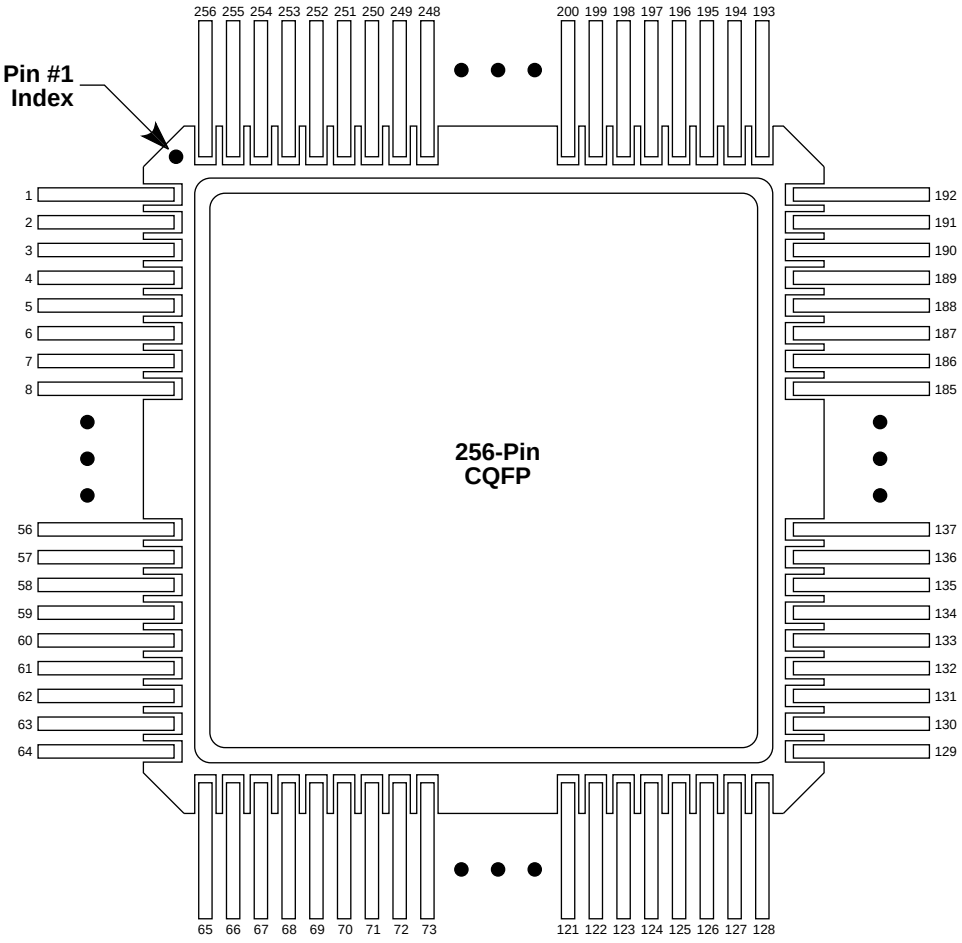
Pin Number	A1280A Function	A1280XL Function
45	I/O	I/O
46	I/O	I/O
47	I/O	I/O
48	I/O	I/O
49	I/O	I/O
50	V_{CC}	V_{CC}
51	I/O	I/O
52	I/O	I/O
53	I/O	I/O
54	I/O	I/O
55	GND	GND
56	I/O	I/O
57	I/O	I/O
58	I/O	I/O
59	I/O	I/O
60	I/O	I/O
61	I/O	I/O
62	I/O	I/O
63	I/O	I/O
64	I/O	I/O
65	GND	GND
66	V_{CC}	V_{CC}
67	I/O	I/O
68	I/O	I/O
69	I/O	I/O
70	I/O	I/O
71	I/O	I/O
72	I/O	I/O
73	I/O	I/O
74	I/O	I/O
75	GND	GND
76	I/O	I/O
77	I/O	I/O
78	I/O	I/O
79	I/O	I/O
80	V_{CC}	V_{CC}
81	I/O	I/O
82	I/O	I/O
83	I/O	I/O
84	I/O	I/O
85	I/O	I/O
86	I/O	I/O
87	I/O	I/O
88	I/O	I/O

196-Pin CQFP

Pin Number	A1460A Function
1	GND
2	SDI, I/O
3	I/O
4	I/O
5	I/O
6	I/O
7	I/O
8	I/O
9	I/O
10	I/O
11	MODE
12	V_{CC}
13	GND
14	I/O
15	I/O
16	I/O
17	I/O
18	I/O
19	I/O
20	I/O
21	I/O
22	I/O
23	I/O
24	I/O
25	I/O
26	I/O
27	I/O
28	I/O
29	I/O
30	I/O
31	I/O
32	I/O
33	I/O
34	I/O
35	I/O
36	I/O
37	GND
38	V_{CC}
39	V_{CC}
40	I/O
41	I/O
42	I/O
43	I/O
44	I/O
45	I/O
46	I/O
47	I/O
48	I/O
49	I/O
50	I/O
51	GND
52	GND
53	I/O
54	I/O
55	I/O
56	I/O
57	I/O
58	I/O
59	V_{CC}
60	I/O
61	I/O
62	I/O
63	I/O
64	GND
65	I/O
66	I/O
67	I/O
68	I/O
69	I/O
70	I/O
71	I/O
72	I/O
73	I/O
74	I/O
75	PRB, I/O
76	I/O
77	HCLK, I/O
78	I/O
79	I/O
80	I/O
81	I/O
82	I/O
83	I/O
84	I/O
85	I/O
86	GND
87	I/O
88	I/O
89	I/O
90	I/O
91	I/O
92	I/O
93	I/O
94	V_{CC}
95	I/O
96	I/O
97	I/O
98	GND
99	I/O
100	IOPCL, I/O
101	GND
102	I/O
103	I/O
104	I/O
105	I/O
106	I/O
107	I/O
108	I/O
109	I/O
110	V_{CC}
111	V_{CC}
112	GND
113	I/O
114	I/O
115	I/O
116	I/O
117	I/O
118	I/O
119	I/O
120	I/O
121	I/O
122	I/O
123	I/O
124	I/O
125	I/O
126	I/O
127	I/O
128	I/O
129	I/O

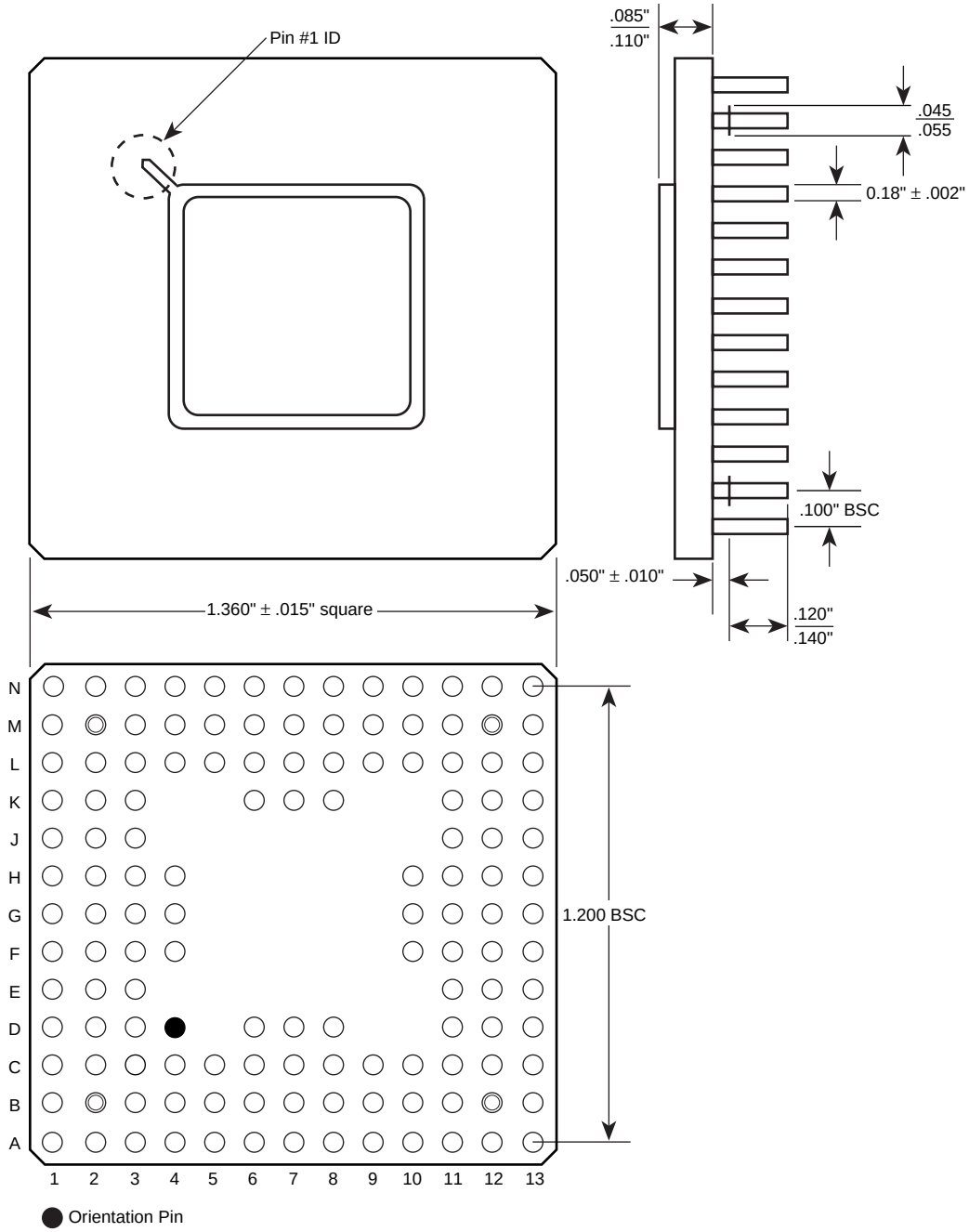
Package Pin Assignments (continued)

256-Pin CQFP (Top View)



Package Mechanical Drawings (continued)

132-Pin CPGA

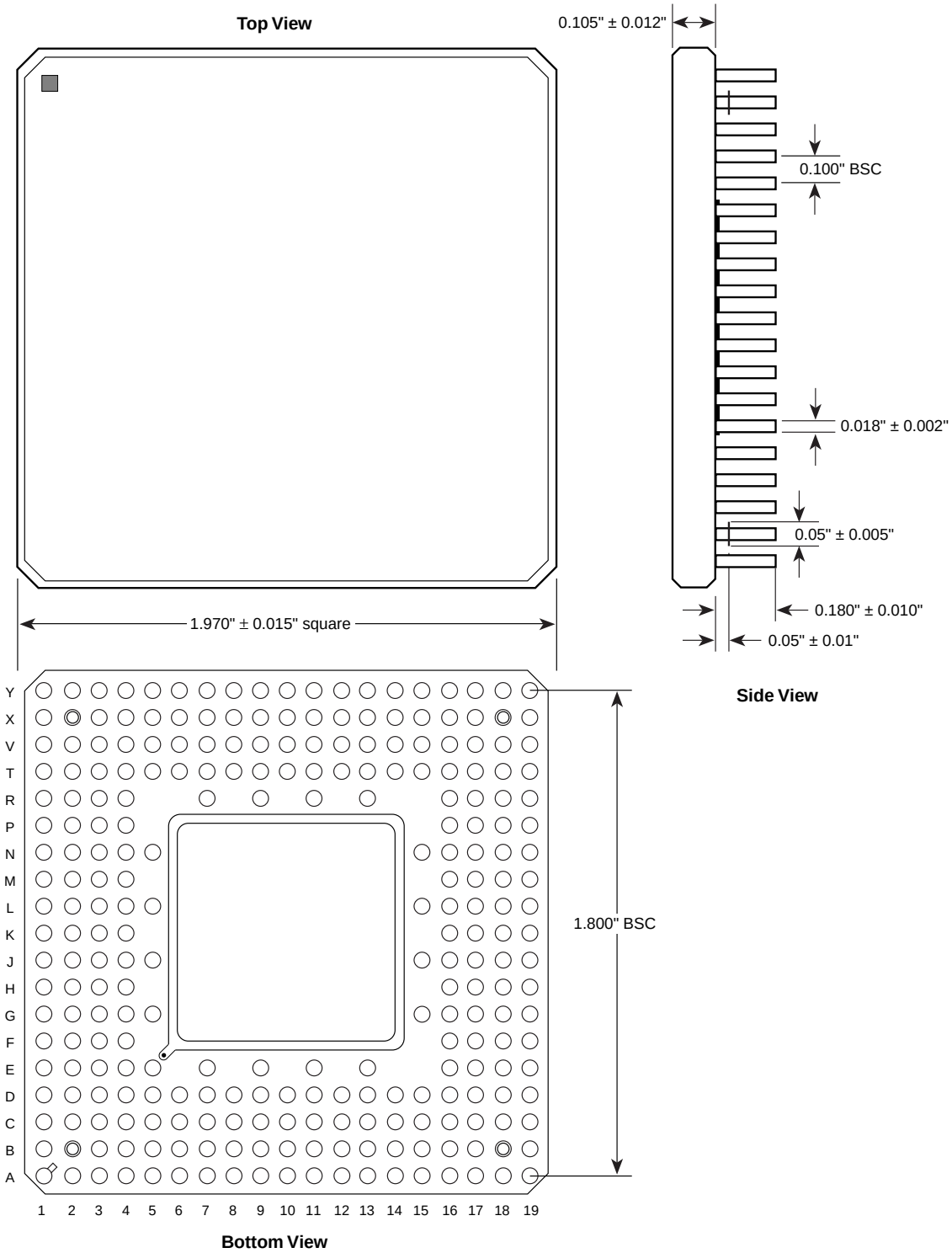


Notes:

1. *All dimensions are in inches unless otherwise stated.*
2. *BSC—Basic Spacing between Centers. This is a theoretical true position dimension and so has no tolerance.*

Package Mechanical Drawings (continued)

257-Pin CPGA



Notes:

1. *All dimensions are in inches unless otherwise stated.*
2. *BSC—Basic Spacing between Centers. This is a theoretical true position dimension and so has no tolerance.*