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Understanding Embedded - FPGAs (Field Programmable Gate Array)

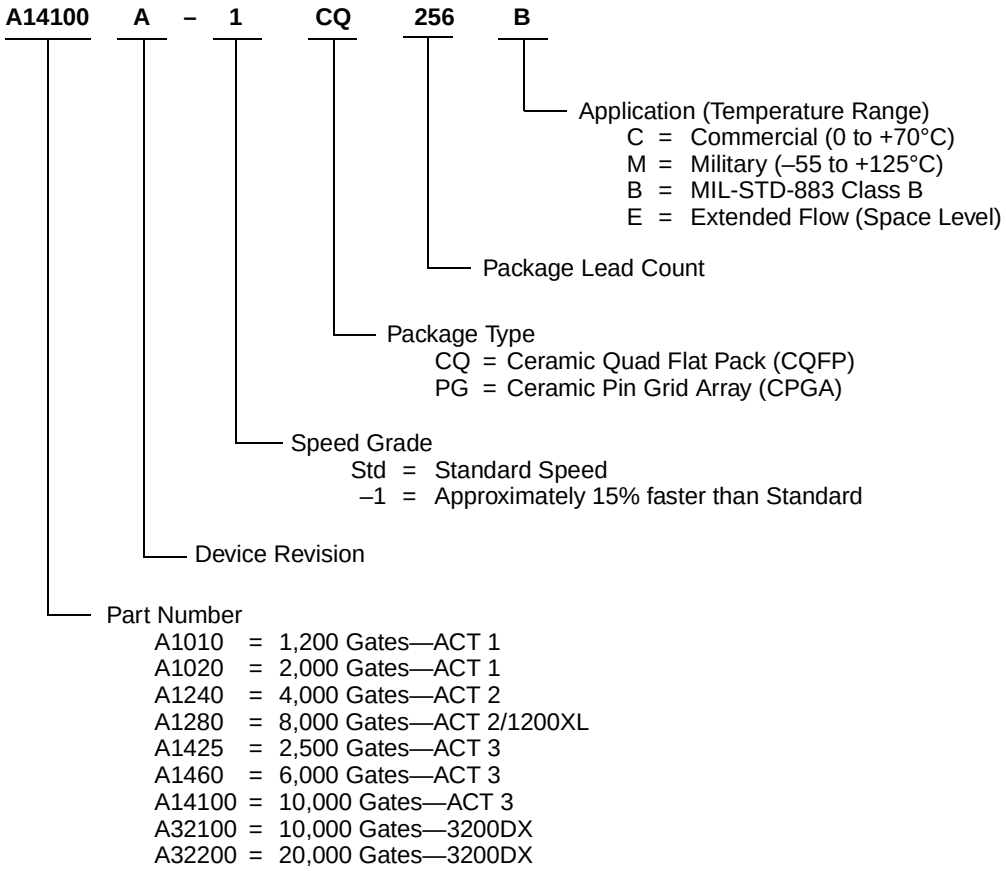
Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	295
Number of Logic Elements/Cells	-
Total RAM Bits	-
Number of I/O	57
Number of Gates	1200
Voltage - Supply	4.5V ~ 5.5V
Mounting Type	Through Hole
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	84-BCPGA
Supplier Device Package	84-CPGA (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/microsemi/a1010b-pg84c

Military Device Ordering Information



3200DX Device Resources

FPGA Device Type	Logic Modules	Gate Array Equivalent Gates	User I/Os		
			CQFP		
			84-pin	208-pin	256-pin
A32100DX	1,362	10,000	60	—	—
A32200DX	2,414	20,000	—	176	202

ACT 3 Device Resources

FPGA Device Type	Logic Modules	Gate Array Equivalent Gates	User I/Os					
			CQFP			CPGA		
			132-pin	196-pin	256-pin	133-pin	207-pin	257-pin
A1425A	310	2,500	100	—	—	100	—	—
A1460A	848	6,000	—	168	—	—	168	—
A14100A	1,377	10,000	—	—	228	—	—	228

1200XL Device Resources

FPGA Device Type	Logic Modules	Gate Array Equivalent Gates	User I/Os	
			CQFP	CPGA
			172-pin	176-pin
A1280XL	1,232	8,000	140	140

ACT 2 Device Resources

FPGA Device Type	Logic Modules	Gate Array Equivalent Gates	User I/Os		
			CQFP	CPGA	
			172-pin	132-pin	176-pin
A1240A	684	4,000	—	104	—
A1280A	1,232	8,000	140	—	140

ACT 1 Device Resources

FPGA Device Type	Logic Modules	Gate Array Equivalent Gates	User I/Os	
			CQFP	CPGA
			84-pin	84-pin
A1010B	295	1,200	—	57
A1020B	547	2,000	69	69

Fixed Capacitance Values for Actel FPGAs (pF)

Device Type	r_1 routed_Clk1	r_2 routed_Clk2
A1010B	41	n/a
A1020B	69	n/a
A1240A	134	134
A1280A	168	168
A1280XL	168	168
A1425A	75	75
A1460A	165	165
A14100A	195	195
A32100DX	178	178
A32200DX	230	230

Fixed Clock Loads (s_1/s_2—ACT 3 Only)

Device Type	s_1 Clock Loads on Dedicated Array Clock	s_2 Clock Loads on Dedicated I/O Clock
A1425A	160	100
A1460A	432	168
A14100A	697	228

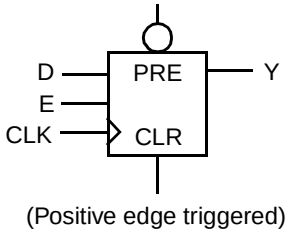
Determining Average Switching Frequency

To determine the switching frequency for a design, you must have a detailed understanding of the data values input to the circuit. The guidelines in the table below are meant to represent worst-case scenarios so that they can be generally used to predict the upper limits of power dissipation.

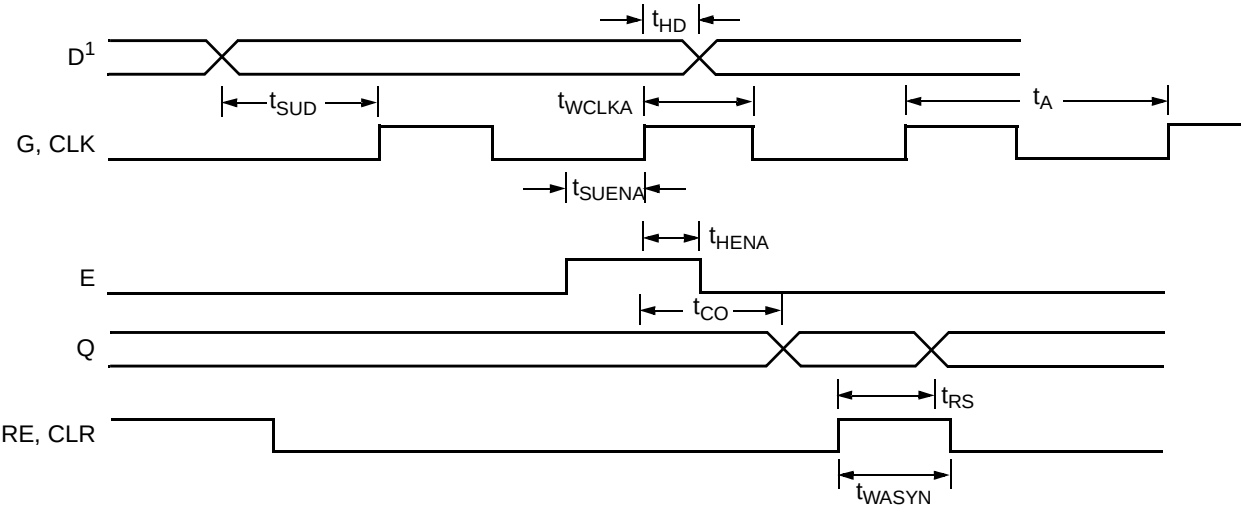
Type	ACT 3	3200DX/ACT 2/1200XL	ACT 1
Logic modules (m)	80% of modules	80% of modules	90% of modules
Input switching (n)	# inputs/4	# inputs/4	# inputs/4
Outputs switching (p)	#outputs/4	#outputs/4	#outputs/4
First routed array clock loads (q_1)	40% of sequential modules	40% of sequential modules	40% of modules
Second routed array clock loads (q_2)	40% of sequential modules	40% of sequential modules	n/a
Load capacitance (C_L)	35 pF	35 pF	35 pF
Average logic module switching rate (f_m)	F/10	F/10	F/10
Average input switching rate (f_n)	F/5	F/5	F/5
Average output switching rate (f_p)	F/10	F/10	F/10
Average first routed array clock rate (f_{q1})	F/2	F	F
Average second routed array clock rate (f_{q2})	F/2	F/2	n/a
Average dedicated array clock rate (f_{s1})	F	n/a	n/a
Average dedicated I/O clock rate (f_{s2})	F	n/a	n/a

Sequential Timing Characteristics (continued)

Flip-Flops and Latches (1200XL/3200DX, ACT 2, and ACT 1)



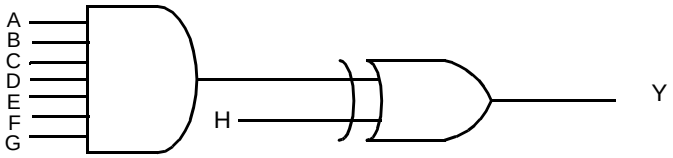
(Positive edge triggered)

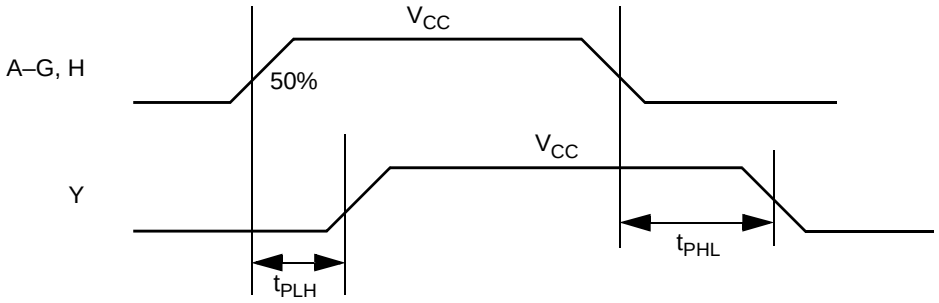


Note:

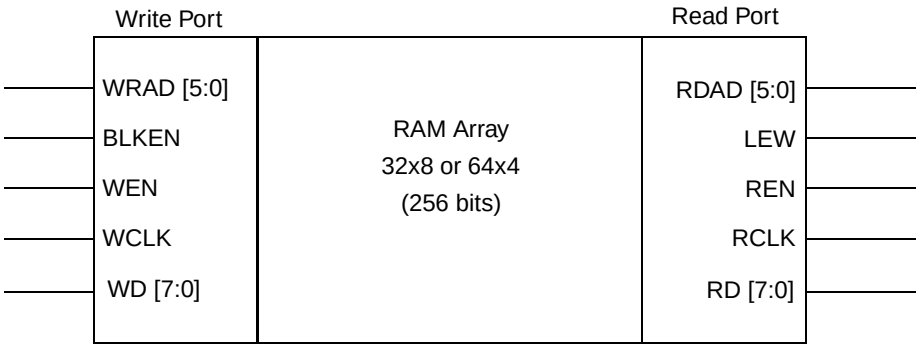
1. *D represents all data functions involving A, B, and S for multiplexed flip-flops.*

Decode Module Timing





SRAM Timing Characteristics



A1280XL Timing Characteristics (continued)

(Worst-Case Military Conditions, V_{CC} = 4.5V, T_J = 125°C)

			'–1' Speed		'Std' Speed		
Parameter	**Description**		**Min.**	**Max.**	**Min.**	**Max.**	**Units**
Input Module Propagation Delays							
t_{INYH}	Pad to Y High			1.5		1.7	ns
t_{INYL}	Pad to Y Low			1.7		2.1	ns
t_{INGH}	G to Y High			2.8		3.3	ns
t_{INGL}	G to Y Low			3.7		4.3	ns
Input Module Predicted Routing Delays[1]							
t_{RD1}	FO=1 Routing Delay			4.6		5.3	ns
t_{RD2}	FO=2 Routing Delay			5.2		6.1	ns
t_{RD3}	FO=3 Routing Delay			5.5		6.5	ns
t_{RD4}	FO=4 Routing Delay			6.4		7.5	ns
t_{RD8}	FO=8 Routing Delay			9.2		10.8	ns
Global Clock Network							
t_{CKH}	Input Low to High	FO = 32 FO = 384		7.1 8.0		8.4 9.5	ns
t_{CKL}	Input High to Low	FO = 32 FO = 384		7.0 8.0		8.3 9.5	ns
t_{PWH}	Minimum Pulse Width High	FO = 32 FO = 384	4.3 4.8		5.3 5.7		ns
t_{PWL}	Minimum Pulse Width Low	FO = 32 FO = 384	4.3 4.8		5.3 5.7		ns
t_{CKSW}	Maximum Skew	FO = 32 FO = 384		1.1 1.1		1.2 1.2	ns
t_{SUEXT}	Input Latch External Setup	FO = 32 FO = 384	0.0 0.0		0.0 0.0		ns
t_{HEXT}	Input Latch External Hold	FO = 32 FO = 384	3.6 4.6		4.2 5.3		ns
t_P	Minimum Period	FO = 32 FO = 384	9.1 9.8		10.7 11.8		ns
f_{MAX}	Maximum Frequency	FO = 32 FO = 384		110 100		90 85	MHz

Note:

1. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment. Optimization techniques may further reduce delays by 0 to 4 ns.

A1460A Timing Characteristics

(Worst-Case Military Conditions, V_{CC} = 4.5V, T_J = 125°C)

		'–1' Speed		'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
Logic Module Propagation Delays[1]						
t_{PD}	Internal Array Module		3.0		3.5	ns
t_{CO}	Sequential Clock to Q		3.0		3.5	ns
t_{CLR}	Asynchronous Clear to Q		3.0		3.5	ns
Logic Module Predicted Routing Delays[2]						
t_{RD1}	FO=1 Routing Delay		1.3		1.5	ns
t_{RD2}	FO=2 Routing Delay		1.9		2.1	ns
t_{RD3}	FO=3 Routing Delay		2.1		2.5	ns
t_{RD4}	FO=4 Routing Delay		2.6		2.9	ns
t_{RD8}	FO=8 Routing Delay		4.2		4.9	ns
Logic Module Sequential Timing						
t_{SUD}	Flip-Flop (Latch) Data Input Setup	0.9		1.0		ns
t_{HD}	Flip-Flop (Latch) Data Input Hold	0.0		0.0		ns
t_{SUENA}	Flip-Flop (Latch) Enable Setup	0.9		1.0		ns
t_{HENA}	Flip-Flop (Latch) Enable Hold	0.0		0.0		ns
t_{WASYN}	Asynchronous Pulse Width	4.8		5.6		ns
t_{WCLKA}	Flip-Flop Clock Pulse Width	4.8		5.6		ns
t_{A}	Flip-Flop Clock Input Period	9.9		11.6		ns
f_{MAX}	Flip-Flop Clock Frequency		100		85	MHz
Input Module Propagation Delays						
t_{INY}	Input Data Pad to Y		4.2		4.9	ns
t_{ICKY}	Input Reg IOCLK Pad to Y		7.0		8.2	ns
t_{OCKY}	Output Reg IOCLK Pad to Y		7.0		8.2	ns
t_{ICLRY}	Input Asynchronous Clear to Y		7.0		8.2	ns
t_{OCLRY}	Output Asynchronous Clear to Y		7.0		8.2	ns
Input Module Predicted Routing Delays[2, 3]						
t_{IRD1}	FO=1 Routing Delay		1.3		1.5	ns
t_{IRD2}	FO=2 Routing Delay		1.9		2.1	ns
t_{IRD3}	FO=3 Routing Delay		2.1		2.5	ns
t_{IRD4}	FO=4 Routing Delay		2.6		2.9	ns
t_{IRD8}	FO=8 Routing Delay		4.2		4.9	ns

Notes:

1. *For dual-module macros, use $t_{PD} + t_{RD1} + t_{PDn}$, $t_{CO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.*
2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*
3. *Optimization techniques may further reduce delays by 0 to 4 ns.*

A1460A Timing Characteristics (continued)

(Worst-Case Military Conditions, V_{CC} = 4.5V, T_J = 125°C)

		'–1' Speed		'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
I/O Module Sequential Timing						
t_{INH}	Input F-F Data Hold (w.r.t. IOCLK Pad)	0.0		0.0		ns
t_{INSU}	Input F-F Data Setup (w.r.t. IOCLK Pad)	2.1		2.4		ns
t_{IDEH}	Input Data Enable Hold (w.r.t. IOCLK Pad)	0.0		0.0		ns
t_{IDESU}	Input Data Enable Setup (w.r.t. IOCLK Pad)	8.7		10.0		ns
t_{OUTH}	Output F-F Data Hold (w.r.t. IOCLK Pad)	1.1		1.2		ns
t_{OUTSU}	Output F-F Data Setup (w.r.t. IOCLK Pad)	1.1		1.2		ns
t_{ODEH}	Output Data Enable Hold (w.r.t. IOCLK Pad)	0.5		0.6		ns
t_{ODESU}	Output Data Enable Setup (w.r.t. IOCLK Pad)	2.0		2.4		ns
TTL Output Module Timing[1]						
t_{DHS}	Data to Pad, High Slew		7.5		8.9	ns
t_{DLS}	Data to Pad, Low Slew		11.9		14.0	ns
t_{ENZHS}	Enable to Pad, Z to H/L, High Slew		6.0		7.0	ns
t_{ENZLS}	Enable to Pad, Z to H/L, Low Slew		10.9		12.8	ns
t_{ENHSZ}	Enable to Pad, H/L to Z, High Slew		11.5		13.5	ns
t_{ENLSZ}	Enable to Pad, H/L to Z, Low Slew		10.9		12.8	ns
t_{CKHS}	IOCLK Pad to Pad H/L, High Slew		11.6		13.4	ns
t_{CKLS}	IOCLK Pad to Pad H/L, Low Slew		17.8		19.8	ns
d_{TLHHS}	Delta Low to High, High Slew		0.04		0.04	ns/pF
d_{TLHLS}	Delta Low to High, Low Slew		0.07		0.08	ns/pF
d_{THLHS}	Delta High to Low, High Slew		0.05		0.06	ns/pF
d_{THLLS}	Delta High to Low, Low Slew		0.07		0.08	ns/pF

Note:

1. Delays based on 35 pF loading.

A14100A Timing Characteristics (continued)

(Worst-Case Military Conditions, V_{CC} = 4.5V, T_J = 125°C)

		'–1' Speed		'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
I/O Module Sequential Timing						
t_{INH}	Input F-F Data Hold (w.r.t. IOCLK Pad)	0.0		0.0		ns
t_{INSU}	Input F-F Data Setup (w.r.t. IOCLK Pad)	2.1		2.4		ns
t_{IDEH}	Input Data Enable Hold (w.r.t. IOCLK Pad)	0.0		0.0		ns
t_{IDESU}	Input Data Enable Setup (w.r.t. IOCLK Pad)	8.7		10.0		ns
t_{OUTH}	Output F-F Data Hold (w.r.t. IOCLK Pad)	1.2		1.2		ns
t_{OUTSU}	Output F-F Data Setup (w.r.t. IOCLK Pad)	1.2		1.2		ns
t_{ODEH}	Output Data Enable Hold (w.r.t. IOCLK Pad)	0.6		0.6		ns
t_{ODESU}	Output Data Enable Setup (w.r.t. IOCLK Pad)	2.4		2.4		ns
TTL Output Module Timing[1]						
t_{DHS}	Data to Pad, High Slew		7.5		8.9	ns
t_{DLS}	Data to Pad, Low Slew		11.9		14.0	ns
t_{ENZHS}	Enable to Pad, Z to H/L, High Slew		6.0		7.0	ns
t_{ENZLS}	Enable to Pad, Z to H/L, Low Slew		10.9		12.8	ns
t_{ENHSZ}	Enable to Pad, H/L to Z, High Slew		11.9		14.0	ns
t_{ENLSZ}	Enable to Pad, H/L to Z, Low Slew		10.9		12.8	ns
t_{CKHS}	IOCLK Pad to Pad H/L, High Slew		12.2		14.0	ns
t_{CKLS}	IOCLK Pad to Pad H/L, Low Slew		17.8		17.8	ns
d_{TLHHS}	Delta Low to High, High Slew		0.04		0.04	ns/pF
d_{TLHLS}	Delta Low to High, Low Slew		0.07		0.08	ns/pF
d_{THLHS}	Delta High to Low, High Slew		0.05		0.06	ns/pF
d_{THLLS}	Delta High to Low, Low Slew		0.07		0.08	ns/pF

Note:

1. Delays based on 35 pF loading.

Pin Description

CLK Clock (Input)

ACT 1 only. TTL Clock input for global clock distribution network. The Clock input is buffered prior to clocking the logic modules. This pin can also be used as an I/O.

CLKA Clock A (Input)

ACT 2, 1200XL, 3200DX, and ACT 3 only. TTL Clock input for global clock distribution networks. The Clock input is buffered prior to clocking the logic modules. This pin can also be used as an I/O.

CLKB Clock B (Input)

ACT 2, 1200XL, 3200DX, and ACT 3 only. TTL Clock input for global clock distribution networks. The Clock input is buffered prior to clocking the logic modules. This pin can also be used as an I/O.

DCLK Diagnostic Clock (Input)

TTL Clock input for diagnostic probe and device programming. DCLK is active when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

GND Ground

LOW supply voltage.

HCLK Dedicated (Hard-wired) Array Clock (Input)

ACT 3 only. TTL Clock input for sequential modules. This input is directly wired to each S-module and offers clock speeds independent of the number of S-modules being driven. This pin can also be used as an I/O.

I/O Input/Output (Input, Output)

I/O pin functions as an input, output, tristate, or bi-directional buffer. Input and output levels are compatible with standard TTL and CMOS specifications. In the ACT 3 and 3200DX families, unused I/Os are automatically tri-stated. With this configuration, the input buffer internal to the I/O module is disabled. In the ACT 1, ACT 2 and 1200XL families, unused I/Os are automatically configured as bi-directional buffers where each buffer is configured as a LOW driver.

IOCLK Dedicated (Hard-wired) I/O Clock (Input)

ACT 3 only. TTL Clock input for I/O modules. This input is directly wired to each I/O module and offers clock speeds independent of the number of I/O modules being driven. This pin can also be used as an I/O.

IOPCL Dedicated (Hard-wired) I/O Preset/Clear (Input)

ACT 3 only. TTL input for I/O preset or clear. This global input is directly wired to the preset and clear inputs of all I/O registers. This pin functions as an I/O when no I/O preset or clear macros are used.

MODE Mode (Input)

The MODE pin controls the use of diagnostic pins (DCLK, PRA, PRB, SDI). When the MODE pin is HIGH, the special functions are active. When the MODE pin is LOW, the pins function as I/Os. To provide debugging capability, the MODE pin should be terminated to GND through a 10 kΩ resistor so that the MODE pin can be pulled high when required.

NC No Connection

This pin is not connected to circuitry within the device.

PRA, I/O Probe A (Output)

The Probe A pin is used to output data from any user-defined design node within the device. This independent diagnostic pin can be used in conjunction with the Probe B pin to allow real-time diagnostic output of any signal path within the device. The Probe A pin can be used as a user-defined I/O when debugging has been completed. The pin's probe capabilities can be permanently disabled to protect programmed design confidentiality. PRA is accessible when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

PRB, I/O Probe B (Output)

The Probe B pin is used to output data from any user-defined design node within the device. This independent diagnostic pin can be used in conjunction with the Probe A pin to allow real-time diagnostic output of any signal path within the device. The Probe B pin can be used as a user-defined I/O when verification has been completed. The pin's probe capabilities can be permanently disabled to protect programmed design confidentiality. PRB is accessible when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

SDI Serial Data Input (Input)

Serial data input for diagnostic probe and device programming. SDI is active when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

V_{CC} 5.0V Supply Voltage

HIGH supply voltage.

QCLKA/B,C,D Quadrant Clock (Input/Output)

3200DX only. These four pins are the quadrant clock inputs. When not used as a register control signal, these pins can function as general purpose I/O.

TCK Test Clock

Clock signal to shift the JTAG data into the device. This pin functions as an I/O when the JTAG fuse is not programmed. JTAG pins are only available in the 3200DX device.

133-Pin CPGA

Pin Number	A1425A Function
A1	NC
A2	GND
A3	I/O
A4	I/O
A5	I/O
A6	PRA, I/O
A7	NC
A8	I/O
A9	I/O
A10	I/O
A11	I/O
A12	I/O
A13	NC
B1	I/O
B2	V_{CC}
B3	I/O
B4	I/O
B5	I/O
B6	CLKB, I/O
B7	V_{CC}
B8	I/O
B9	I/O
B10	I/O
B11	I/O
B12	V_{CC}
B13	I/O
C1	I/O
C2	SDI, I/O
C3	GND
C4	I/O
C5	I/O
C6	I/O
C7	GND
C8	I/O
C9	I/O
C10	IOCLK, I/O
C11	GND
C12	GND
C13	I/O
D1	I/O
D2	I/O
D3	I/O
D4	DCLK, I/O
D6	CLKA, I/O
D7	I/O
D8	I/O
D11	I/O
D12	I/O
D13	I/O
E1	I/O
E2	I/O
E3	MODE
E11	V_{CC}
E12	I/O
E13	I/O
F1	I/O
F2	I/O
F3	I/O
F4	I/O
F10	GND
F11	I/O
F12	I/O
F13	I/O
G1	NC
G2	V_{CC}
G3	GND
G4	I/O
G10	I/O
G11	GND
G12	V_{CC}
G13	NC
H1	I/O
H2	I/O
H3	I/O
H4	I/O
H10	I/O
H11	I/O
H12	I/O
H13	I/O
J1	I/O
J2	V_{CC}
J3	I/O
J11	I/O
J12	V_{CC}
J13	I/O
K1	I/O
K2	I/O
K3	I/O
K6	I/O
K7	HCLKA, I/O
K8	I/O
K11	I/O
K12	I/O
K13	I/O
L1	I/O
L2	I/O
L3	GND
L4	I/O
L5	I/O
L6	PRB, I/O
L7	GND
L8	I/O
L9	I/O
L10	IOPCL, I/O
L11	GND
L12	I/O
L13	I/O
M1	I/O
M2	V_{CC}
M3	GND
M4	I/O
M5	I/O
M6	I/O
M7	V_{CC}
M8	I/O
M9	I/O
M10	I/O
M11	I/O
M12	V_{CC}
M13	I/O
N1	NC
N2	I/O
N3	I/O
N4	I/O
N5	I/O
N6	I/O
N7	NC
N8	I/O
N9	I/O
N10	I/O
N11	I/O
N12	GND
N13	NC

207-Pin CPGA (Continued)

Pin Number	A1460A Function
M15	I/O
M16	I/O
M17	I/O
N1	I/O
N2	I/O
N3	I/O
N4	I/O
N14	IOPCL, I/O
N15	I/O
N16	I/O
N17	I/O
P1	I/O
P2	I/O
P3	GND
P4	GND
P5	IOCLK, I/O
P6	I/O
P7	GND
P8	I/O
P9	GND
P10	I/O
P11	I/O
P12	V_{CC}
P13	I/O
P14	GND
P15	I/O
P16	I/O

Pin Number	A1460A Function
P17	I/O
R1	I/O
R2	I/O
R3	I/O
R4	I/O
R5	I/O
R6	I/O
R7	I/O
R8	I/O
R9	I/O
R10	I/O
R11	I/O
R12	I/O
R13	I/O
R14	I/O
R15	GND
R16	I/O
R17	I/O
S1	NC
S2	V_{CC}
S3	NC
S4	I/O
S5	I/O
S6	I/O
S7	I/O
S8	I/O
S9	V_{CC}

Pin Number	A1460A Function
S10	I/O
S11	I/O
S12	I/O
S13	I/O
S14	I/O
S15	I/O
S16	V_{CC}
S17	NC
T1	NC
T2	NC
T3	I/O
T4	I/O
T5	V_{CC}
T6	I/O
T7	I/O
T8	I/O
T9	I/O
T10	I/O
T11	I/O
T12	I/O
T13	I/O
T14	I/O
T15	I/O
T16	NC
T17	NC

257-Pin CPGA (Continued)

Pin Number	A14100A Function
K19	I/O
L1	I/O
L2	I/O
L3	I/O
L4	CLKA, I/O
L5	CLKB, I/O
L15	GND
L16	I/O
L17	I/O
L18	I/O
L19	I/O
M1	I/O
M2	I/O
M3	I/O
M4	I/O
M16	I/O
M17	I/O
M18	I/O
M19	I/O
N1	I/O
N2	I/O
N3	I/O
N4	I/O
N5	I/O
N15	I/O
N16	I/O
N17	I/O
N18	I/O
N19	I/O
P1	I/O
P2	I/O
P3	I/O
P4	I/O
P16	I/O
P17	I/O
P18	I/O
P19	I/O
R1	I/O
R2	I/O
R3	I/O
R4	GND
R7	I/O

Pin Number	A14100A Function
R9	I/O
R11	I/O
R13	I/O
R16	IOPCL, I/O
R17	I/O
R18	I/O
R19	I/O
T1	I/O
T2	I/O
T3	I/O
T4	GND
T5	IOCLK, I/O
T6	I/O
T7	I/O
T8	I/O
T9	I/O
T10	GND
T11	I/O
T12	I/O
T13	I/O
T14	I/O
T15	I/O
T16	GND
T17	GND
T18	I/O
T19	I/O
V1	I/O
V2	I/O
V3	V_{CC}
V4	I/O
V5	I/O
V6	I/O
V7	V_{CC}
V8	I/O
V9	I/O
V10	V_{CC}
V11	I/O
V12	I/O
V13	I/O
V14	I/O
V15	I/O
V16	I/O

Pin Number	A14100A Function
V17	V_{CC}
V18	I/O
V19	I/O
X1	I/O
X2	I/O
X3	I/O
X4	I/O
X5	I/O
X6	I/O
X7	GND
X8	I/O
X9	I/O
X10	I/O
X11	I/O
X12	I/O
X13	I/O
X14	V_{CC}
X15	I/O
X16	I/O
X17	I/O
X18	I/O
X19	I/O
Y1	I/O
Y2	I/O
Y3	I/O
Y4	I/O
Y5	I/O
Y6	I/O
Y7	I/O
Y8	I/O
Y9	I/O
Y10	I/O
Y11	I/O
Y12	I/O
Y13	I/O
Y14	I/O
Y15	I/O
Y16	I/O
Y17	I/O
Y18	I/O
Y19	I/O

208-Pin CQFP (Continued)

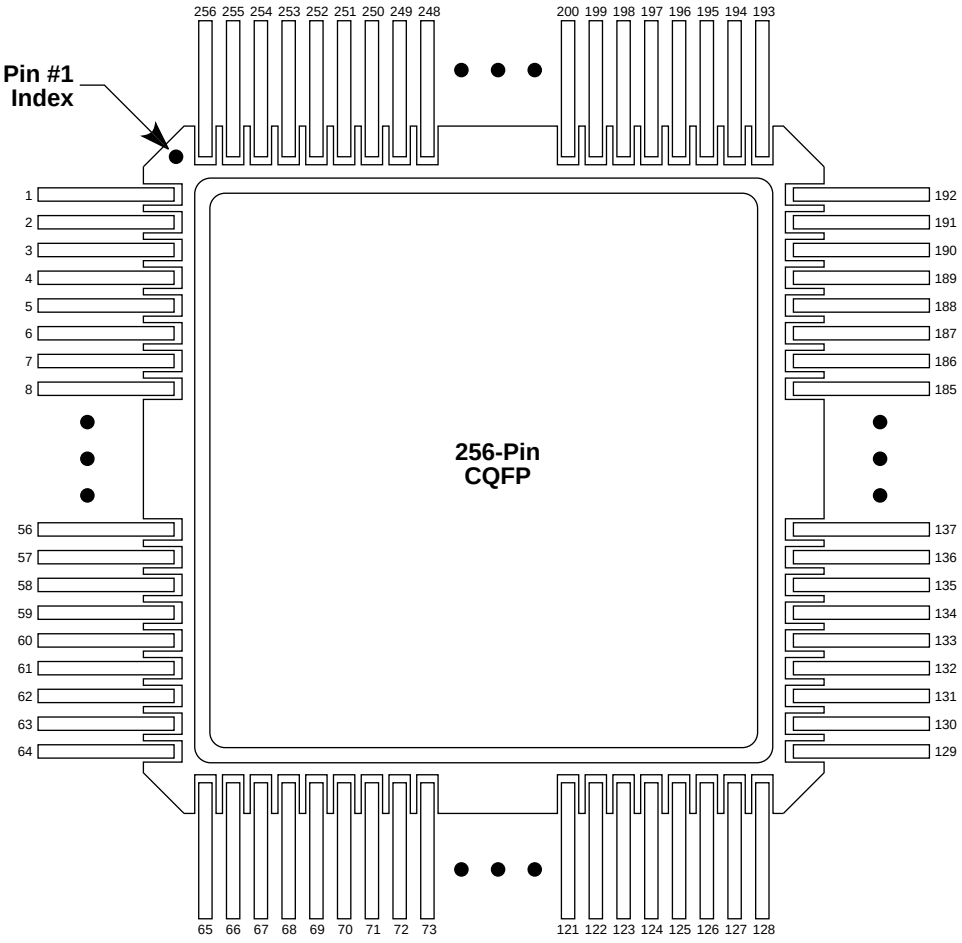
Pin Number	A32100DX Function
130	V_{CC}
131	GND
132	V_{CC}
133	V_{CC}
134	I/O
135	I/O
136	V_{CC}
137	I/O
138	I/O
139	I/O
140	I/O
141	I/O
142	I/O
143	I/O
144	I/O
145	I/O
146	I/O
147	I/O
148	I/O
149	I/O
150	GND
151	I/O
152	I/O
153	I/O
154	I/O
155	I/O
156	I/O

Pin Number	A32100DX Function
157	GND
158	I/O
159	SDI, I/O
160	I/O
161	I/O (WD)
162	I/O (WD)
163	I/O
164	V_{CC}
165	I/O
166	I/O
167	I/O
168	I/O (WD)
169	I/O (WD)
170	I/O
171	QCLKD, I/O
172	I/O
173	I/O
174	I/O
175	I/O
176	I/O (WD)
177	I/O (WD)
178	PRA, I/O
179	I/O
180	CLKA, I/O
181	I/O
182	V_{CC}
183	V_{CC}

Pin Number	A32100DX Function
184	GND
185	I/O
186	CLKB, I/O
187	I/O
188	PRB, I/O
189	I/O
190	I/O (WD)
191	I/O (WD)
192	I/O
193	I/O
194	I/O (WD)
195	I/O (WD)
196	QCLKC, I/O
197	I/O
198	I/O
199	I/O
200	I/O
201	I/O
202	V_{CC}
203	I/O (WD)
204	I/O (WD)
205	I/O
206	I/O
207	DCLK, I/O
208	I/O

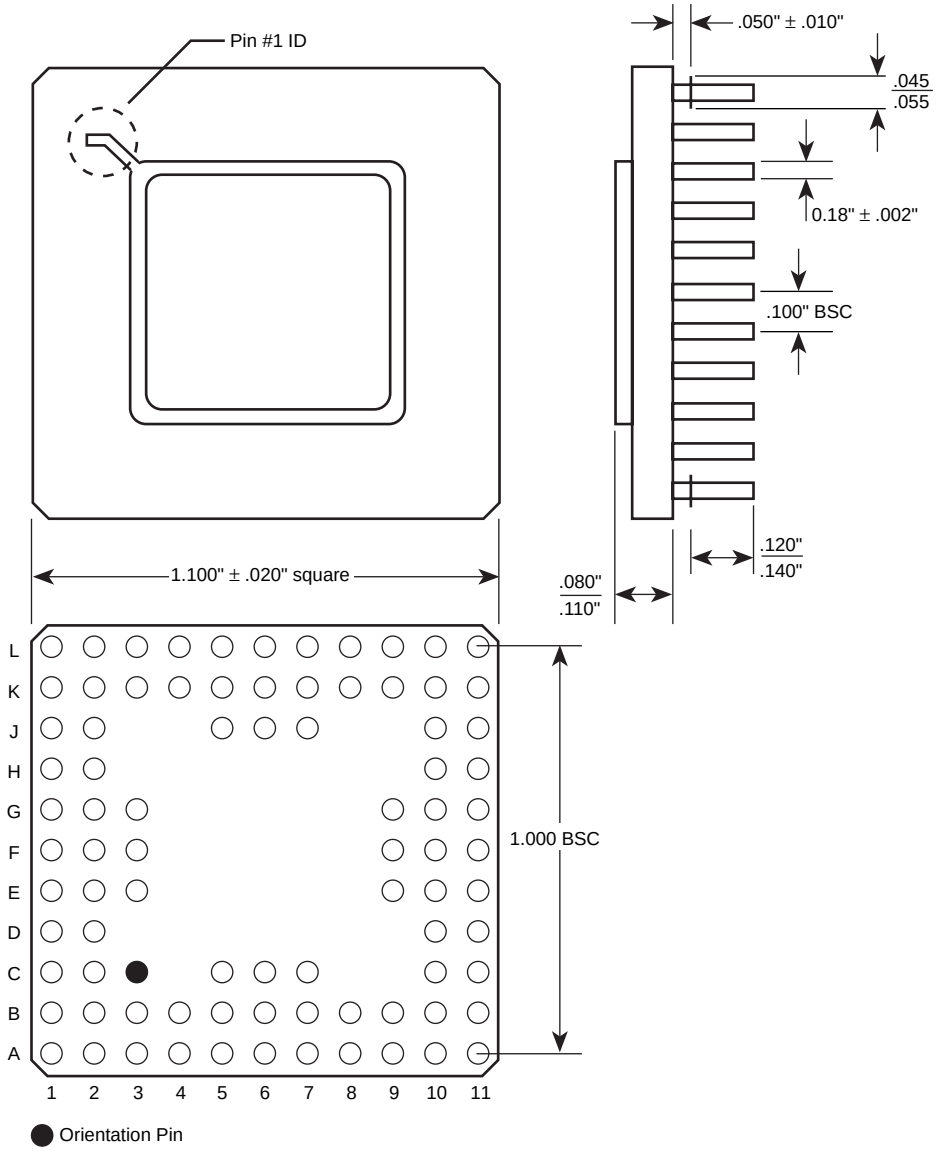
Package Pin Assignments (continued)

256-Pin CQFP (Top View)



Package Mechanical Drawings

84-Pin CPGA

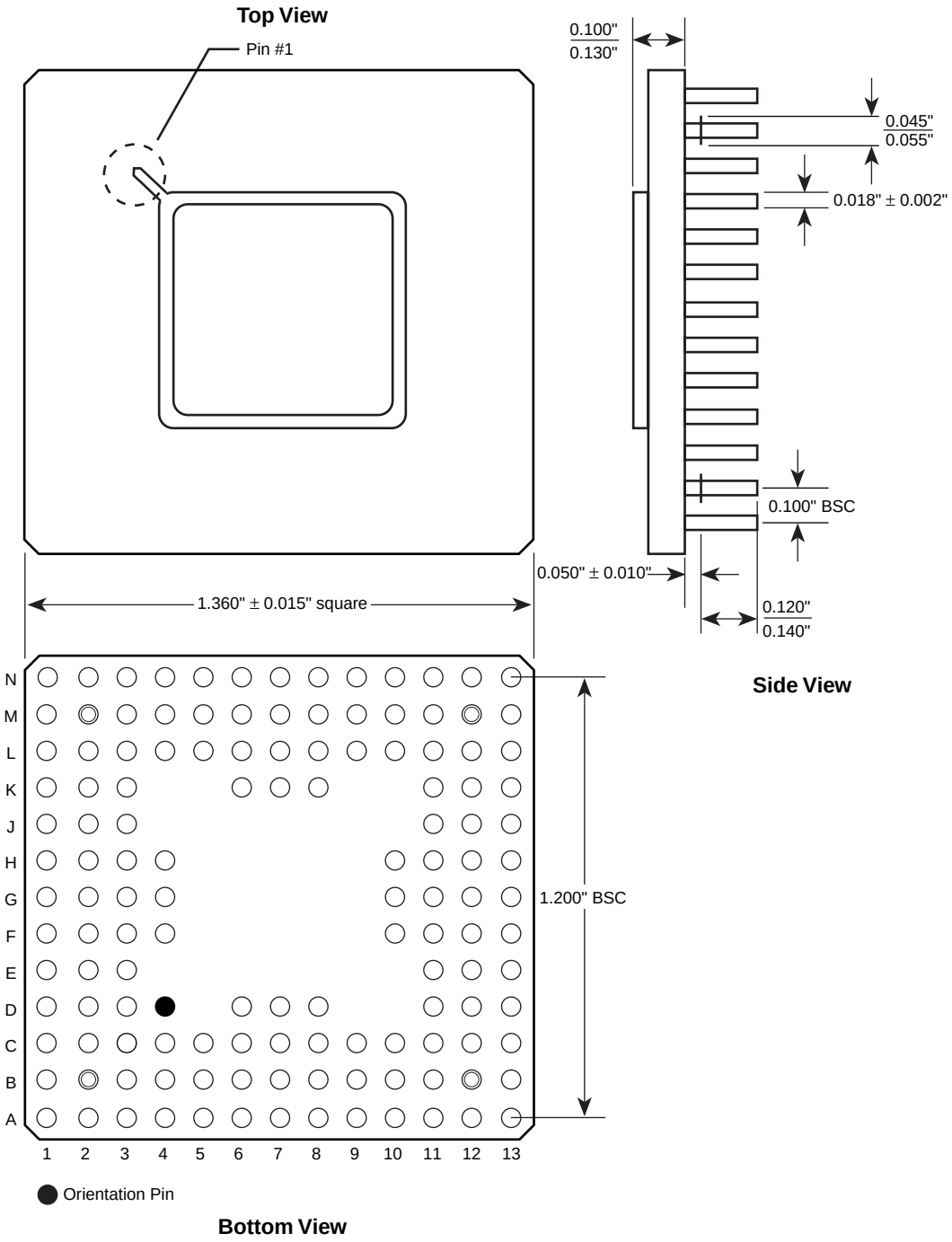


Notes:

1. *All dimensions are in inches unless otherwise stated.*
2. *BSC—Basic Spacing between Centers. This is a theoretical true position dimension and so has no tolerance.*

Package Mechanical Drawings (continued)

133-Pin CPGA

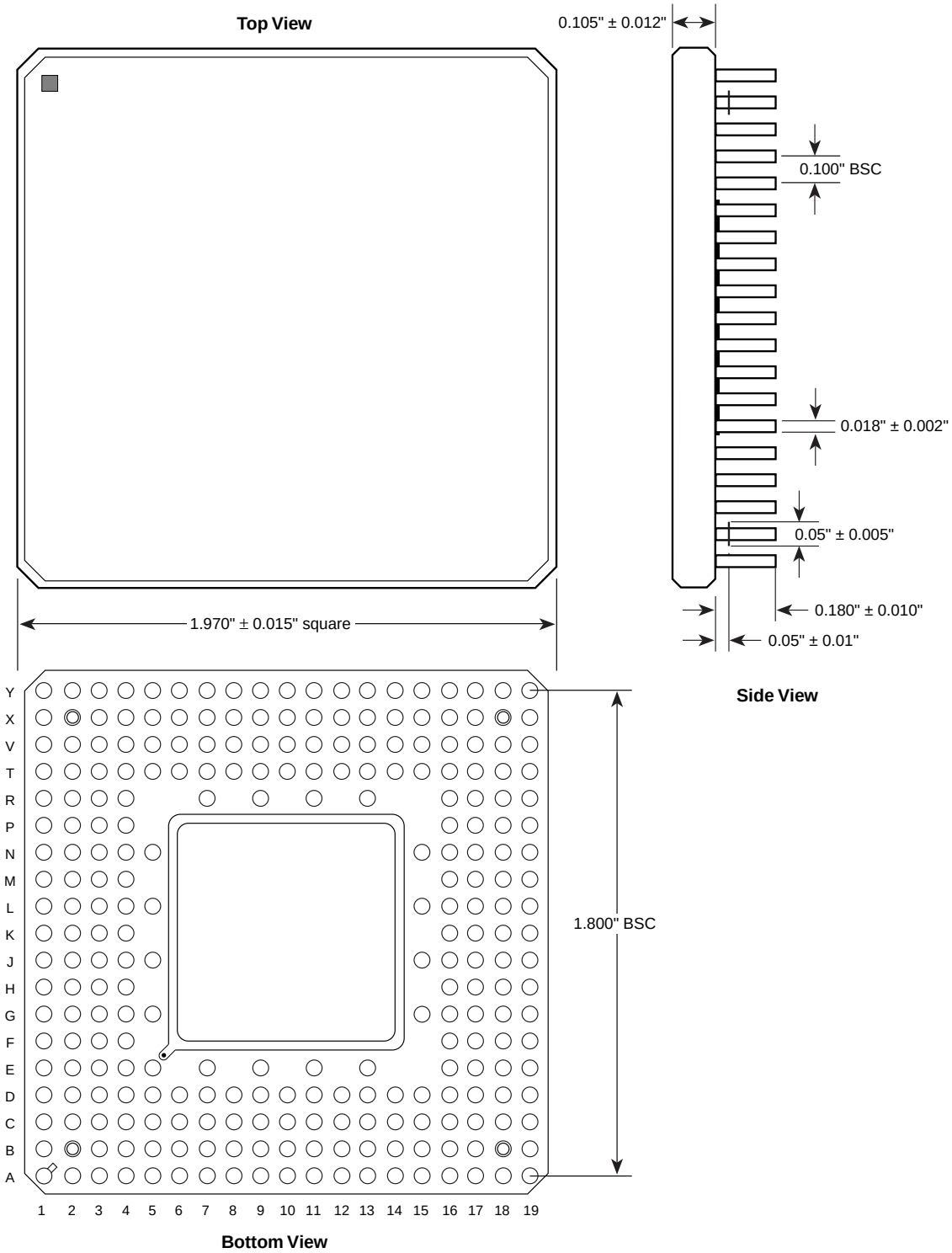


Notes:

1. *All dimensions are in inches unless otherwise stated.*
2. *BSC—Basic Spacing between Centers. This is a theoretical true position dimension and so has no tolerance.*

Package Mechanical Drawings (continued)

257-Pin CPGA

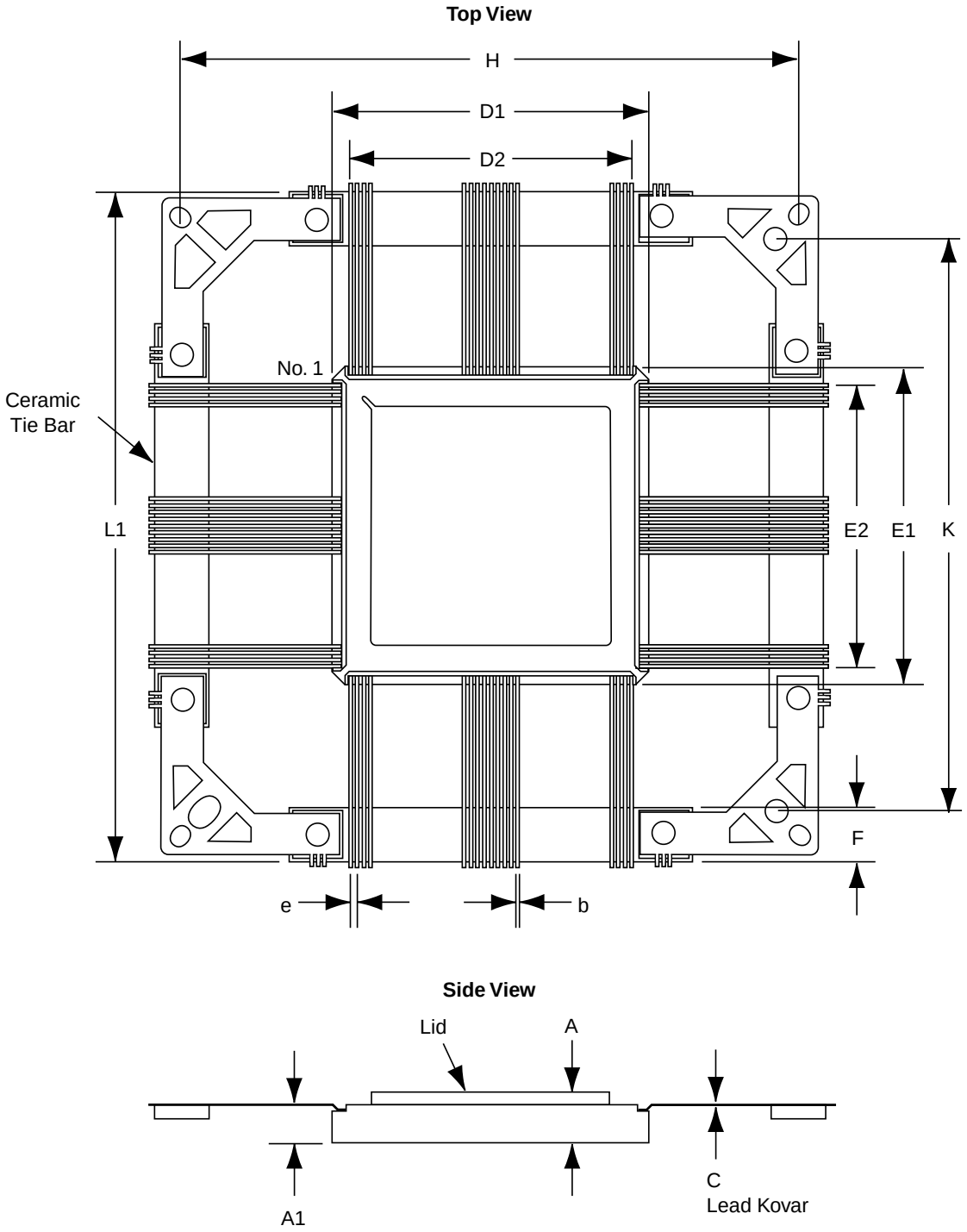


Notes:

1. *All dimensions are in inches unless otherwise stated.*
2. *BSC—Basic Spacing between Centers. This is a theoretical true position dimension and so has no tolerance.*

Package Mechanical Drawings (continued)

132-Pin, 172-Pin, 196-Pin, 208-Pin, and 256-Pin CQFP (Cavity Up)



Notes:

1. *Outside leadframe holes (from dimension H) are circular for the CQ208 and CQ256.*
2. *Seal ring and lid are connected to Ground.*
3. *Lead material is Kovar with minimum 50 microinches gold plate over nickel.*
4. *Packages are shipped unformed with the ceramic tie bar.*
5. *32200DX – CQ208 has a heat sink on the back.*

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