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Understanding Embedded - FPGAs (Field Programmable Gate Array)

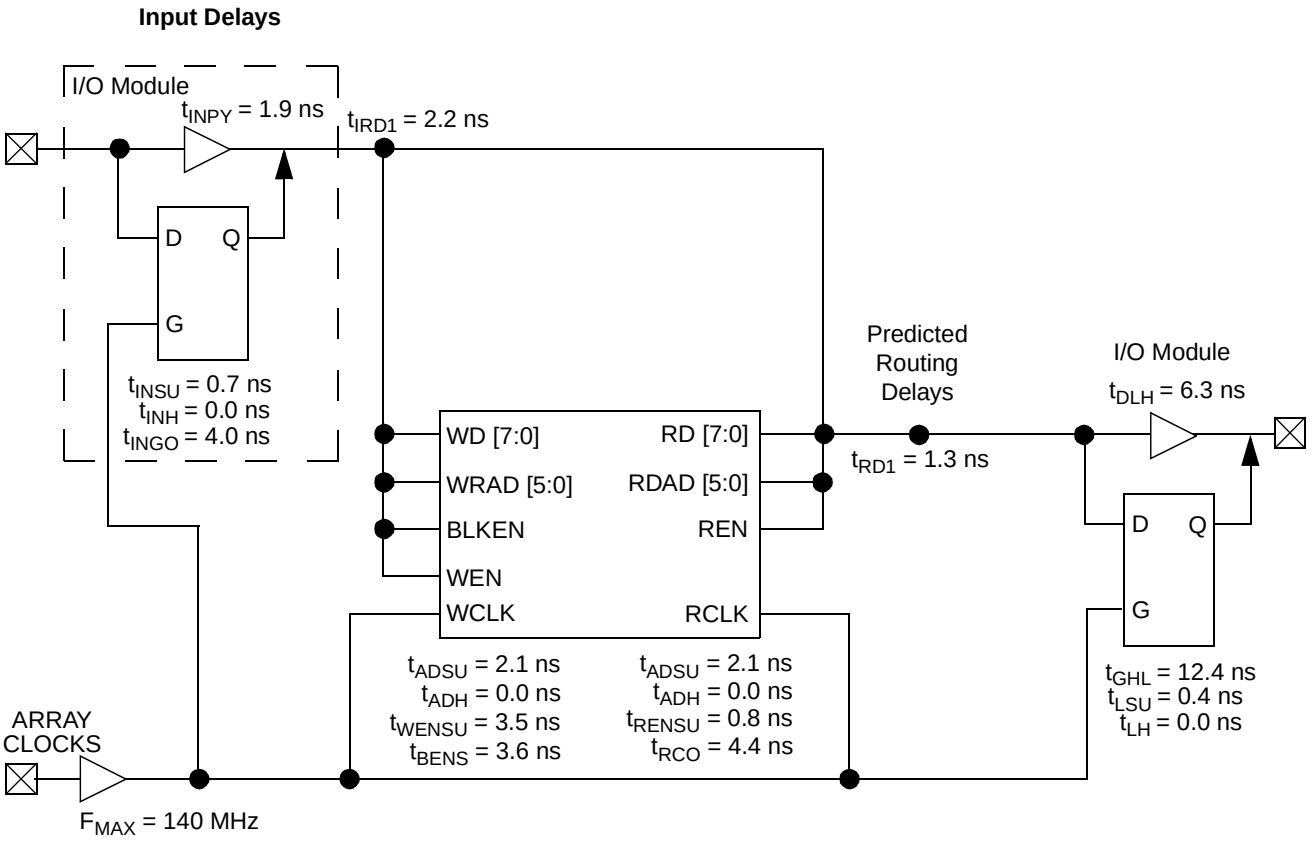
Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	295
Number of Logic Elements/Cells	-
Total RAM Bits	-
Number of I/O	57
Number of Gates	1200
Voltage - Supply	4.5V ~ 5.5V
Mounting Type	Through Hole
Operating Temperature	-55°C ~ 125°C (TC)
Package / Case	84-BCPGA
Supplier Device Package	84-CPGA (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/microsemi/a1010b-pg84m

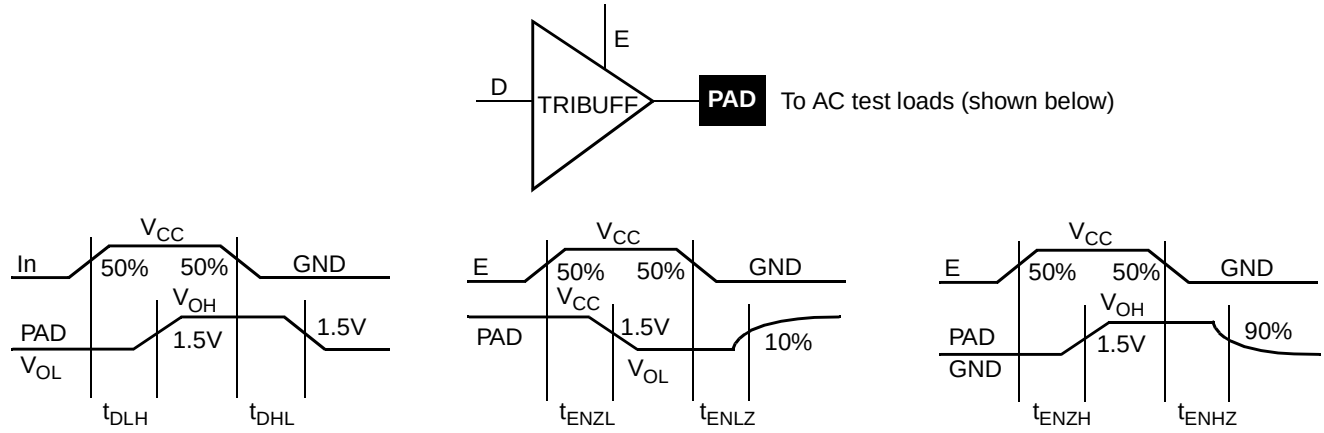
3200DX Timing Model (SRAM Functions)*



**Values shown for A32100DX–1 at worst-case military conditions.*

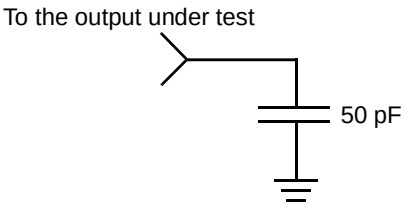
Parameter Measurement

Output Buffer Delays

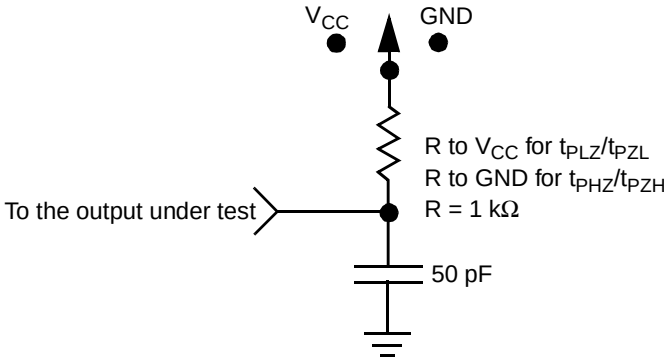


AC Test Load

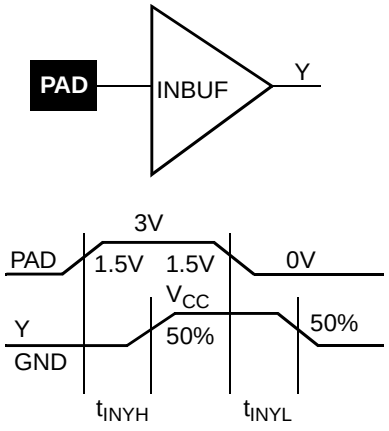
Load 1
(Used to measure propagation delay)



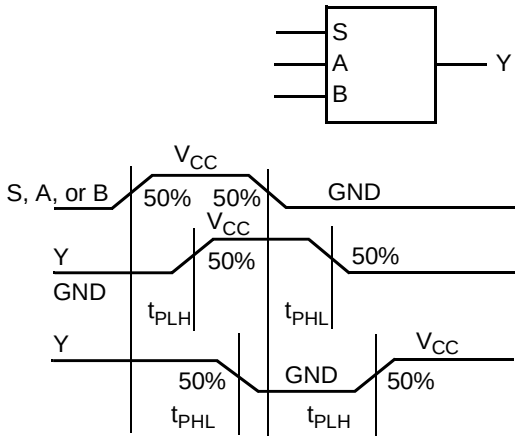
Load 2
(Used to measure rising/falling edges)



Input Buffer Delays

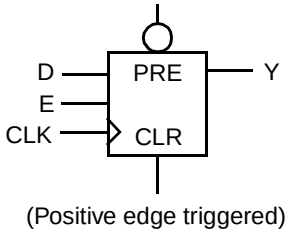


Combinatorial Macro Delays

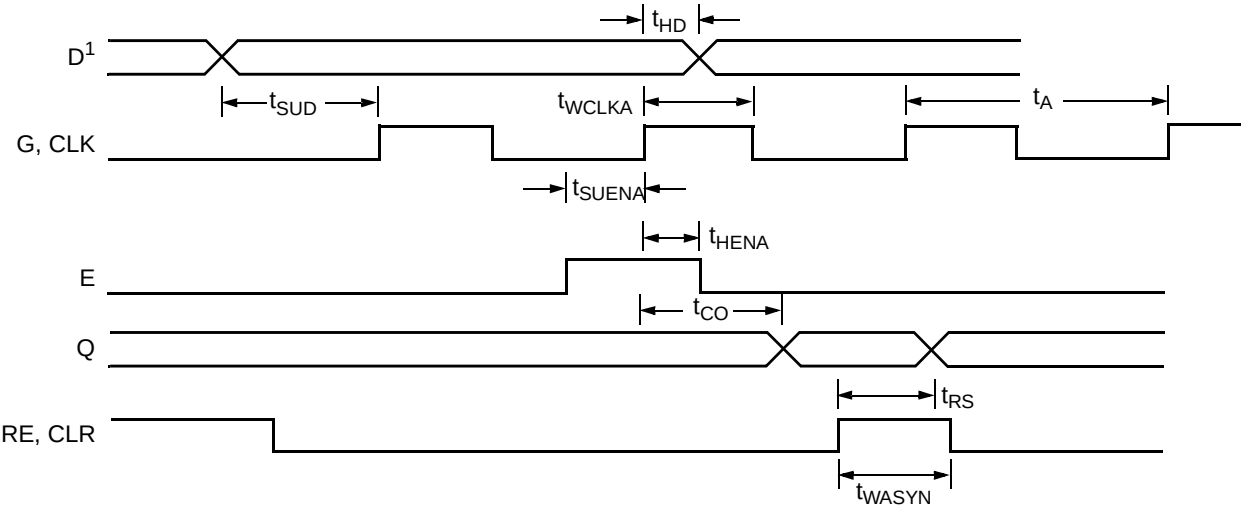


Sequential Timing Characteristics (continued)

Flip-Flops and Latches (1200XL/3200DX, ACT 2, and ACT 1)



(Positive edge triggered)



Note:

1. *D represents all data functions involving A, B, and S for multiplexed flip-flops.*

A1240A Timing Characteristics (continued)

(Worst-Case Military Conditions, V_{CC} = 4.5V, T_J = 125°C)

			'–1' Speed		'Std' Speed		
Parameter	**Description**		**Min.**	**Max.**	**Min.**	**Max.**	**Units**
Input Module Propagation Delays							
t_{INYH}	Pad to Y High			4.0		4.7	ns
t_{INYL}	Pad to Y Low			3.6		4.3	ns
t_{INGH}	G to Y High			6.9		8.1	ns
t_{INGL}	G to Y Low			6.6		7.7	ns
Input Module Predicted Routing Delays[1]							
t_{IRD1}	FO=1 Routing Delay			5.8		6.9	ns
t_{IRD2}	FO=2 Routing Delay			6.7		7.8	ns
t_{IRD3}	FO=3 Routing Delay			7.5		8.8	ns
t_{IRD4}	FO=4 Routing Delay			8.2		9.7	ns
t_{IRD8}	FO=8 Routing Delay			10.9		12.9	ns
Global Clock Network							
t_{CKH}	Input Low to High	FO = 32 FO = 256		13.3 16.3		15.7 19.2	ns
t_{CKL}	Input High to Low	FO = 32 FO = 256		13.3 16.5		15.7 19.5	ns
t_{PWH}	Minimum Pulse Width High	FO = 32 FO = 256	5.7 6.0		6.7 7.1		ns
t_{PWL}	Minimum Pulse Width Low	FO = 32 FO = 256	5.7 6.0		6.7 7.1		ns
t_{CKSW}	Maximum Skew	FO = 32 FO = 256		0.6 3.1		0.6 3.1	ns
t_{SUEXT}	Input Latch External Setup	FO = 32 FO = 256	0.0 0.0		0.0 0.0		ns
t_{HEXT}	Input Latch External Hold	FO = 32 FO = 256	8.6 13.8		8.6 13.8		ns
t_P	Minimum Period	FO = 32 FO = 256	11.5 12.2		13.5 14.3		ns
f_{MAX}	Maximum Frequency	FO = 32 FO = 256		87 82		74 70	MHz

Note:

1. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment. Optimization techniques may further reduce delays by 0 to 4 ns.

A1280XL Timing Characteristics

(Worst-Case Military Conditions, V_{CC} = 4.5V, T_J = 125°C)

		'–1' Speed		'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
Logic Module Propagation Delays[1]						
t_{PD1}	Single Module		3.7		4.3	ns
t_{CO}	Sequential Clk to Q		3.7		4.3	ns
t_{GO}	Latch G to Q		3.7		4.3	ns
t_{RS}	Flip-Flop (Latch) Reset to Q		3.7		4.3	ns
Logic Module Predicted Routing Delays[2]						
t_{RD1}	FO=1 Routing Delay		1.7		2.1	ns
t_{RD2}	FO=2 Routing Delay		2.5		3.0	ns
t_{RD3}	FO=3 Routing Delay		3.1		3.6	ns
t_{RD4}	FO=4 Routing Delay		3.7		4.3	ns
t_{RD8}	FO=8 Routing Delay		7.0		8.3	ns
Logic Module Sequential Timing[3, 4]						
t_{SUD}	Flip-Flop (Latch) Data Input Setup	0.4		0.5		ns
t_{HD}	Flip-Flop (Latch) Data Input Hold	0.0		0.0		ns
t_{SUENA}	Flip-Flop (Latch) Enable Setup	1.1		1.2		ns
t_{HENA}	Flip-Flop (Latch) Enable Hold	0.0		0.0		ns
t_{WCLKA}	Flip-Flop (Latch) Clock Active Pulse Width	5.3		6.1		ns
t_{WASYN}	Flip-Flop (Latch) Asynchronous Pulse Width	5.3		6.1		ns
t_A	Flip-Flop Clock Input Period	10.7		12.3		ns
t_{INH}	Input Buffer Latch Hold	0.0		0.0		ns
t_{INSU}	Input Buffer Latch Setup	0.4		0.4		ns
t_{OUTH}	Output Buffer Latch Hold	0.0		0.0		ns
t_{OUTSU}	Output Buffer Latch Setup	0.4		0.4		ns
f_{MAX}	Flip-Flop (Latch) Clock Frequency		90		75	MHz

Notes:

1. *For dual-module macros, use $t_{PD1} + t_{RD1} + t_{PDn}$, $t_{CO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.*
2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*
3. *Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the DirectTime Analyzer utility.*
4. *Setup and hold timing parameters for the input buffer latch are defined with respect to the PAD and the D input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.*

A1460A Timing Characteristics (continued)

(Worst-Case Military Conditions, V_{CC} = 4.5V, T_J = 125°C)

		'–1' Speed		'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
Routed Array Clock Networks						
t_{RCKH}	Input Low to High (FO=256)		9.0		10.5	ns
t_{RCKL}	Input High to Low (FO=256)		9.0		10.5	ns
t_{RPWH}	Min. Pulse Width High (FO=256)	6.3		7.1		ns
t_{RPWL}	Min. Pulse Width Low (FO=256)	6.3		7.1		ns
t_{RCKSW}	Maximum Skew (FO=128)		1.9		2.1	ns
t_{RP}	Minimum Period (FO=256)	12.9		14.5		ns
f_{RMAX}	Maximum Frequency (FO=256)		75		65	MHz
Clock-to-Clock Skews						
$t_{IOHCKSW}$	I/O Clock to H-Clock Skew	0.0	3.0	0.0	3.0	ns
$t_{IORCKSW}$	I/O Clock to R-Clock Skew	0.0	5.0	0.0	5.0	ns
t_{HRCKSW}	H-Clock to R-Clock Skew					
	(FO = 64)	0.0	1.0	0.0	1.0	ns
	(FO = 50% max.)	0.0	3.0	0.0	3.0	ns

A32100DX Timing Characteristics (continued)

(Worst-Case Military Conditions, V_{CC} = 4.5V, T_J = 125°C)

			'–1' Speed		'Std' Speed		
Parameter	**Description**		**Min.**	**Max.**	**Min.**	**Max.**	**Units**
Input Module Propagation Delays							
t_{INPY}	Input Data Pad to Y			1.9		2.6	ns
t_{INGO}	Input Latch Gate-to-Output			4.0		5.3	ns
t_{INH}	Input Latch Hold		0.0		0.0		ns
t_{INSU}	Input Latch Setup		0.7		0.9		ns
t_{ILA}	Latch Active Pulse Width		6.1		8.1		ns
Input Module Predicted Routing Delays[1]							
t_{IRD1}	FO=1 Routing Delay			2.2		2.9	ns
t_{IRD2}	FO=2 Routing Delay			2.8		3.8	ns
t_{IRD3}	FO=3 Routing Delay			3.5		4.7	ns
t_{IRD4}	FO=4 Routing Delay			3.5		4.7	ns
t_{IRD8}	FO=8 Routing Delay			5.6		7.5	ns
Global Clock Network							
t_{CKH}	Input Low to High	FO=32 FO=635		6.5 7.9		8.7 10.6	ns ns
t_{CKL}	Input High to Low	FO=32 FO=635		6.6 8.8		8.8 11.8	ns ns
t_{PWH}	Minimum Pulse Width High	FO=32 FO=635	4.1 4.6		5.5 6.1		ns ns
t_{PWL}	Minimum Pulse Width Low	FO=32 FO=635	4.1 4.6		5.5 6.1		ns ns
t_{CKSW}	Maximum Skew	FO=32 FO=635		1.8 1.8		2.4 2.4	ns ns
t_{SUEXT}	Input Latch External Setup	FO=32 FO=635	0.0 0.0		0.0 0.0		ns ns
t_{HEXT}	Input Latch External Hold	FO=32 FO=635	3.0 3.8		4.0 5.1		ns ns
t_P	Minimum Period (1/fmax)	FO=32 FO=635	7.1 7.9		9.5 10.5		ns ns
f_{HMAX}	Maximum Datapath Frequency	FO=32 FO=635		140 126		105 95	MHz MHz

Note:

1. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment. Optimization techniques may further reduce delays by 0 to 4 ns.

A32200DX Timing Characteristics (continued)

(Worst-Case Military Conditions, V_{CC} = 4.5V, T_J = 125°C)

		'–1' Speed		'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
Synchronous SRAM Operations						
t_{RC}	Read Cycle Time	8.8		11.8		ns
t_{WC}	Write Cycle Time	8.8		11.8		ns
t_{RCKHL}	Clock High/Low Time	4.4		5.9		ns
t_{RCO}	Data Valid After Clock High/Low		4.4		5.9	ns
t_{ADSU}	Address/Data Setup Time	2.1		2.8		ns
t_{ADH}	Address/Data Hold Time	0.0		0.0		ns
t_{RENSU}	Read Enable Setup	0.8		1.1		ns
t_{RENH}	Read Enable Hold	4.4		5.9		ns
t_{WENSU}	Write Enable Setup	3.5		4.7		ns
t_{WENH}	Write Enable Hold	0.0		0.0		ns
t_{BENS}	Block Enable Setup	3.6		4.8		ns
t_{BENH}	Block Enable Hold	0.0		0.0		ns
Asynchronous SRAM Operations						
t_{RPD}	Asynchronous Access Time		10.6		14.1	ns
t_{RDADV}	Read Address Valid	11.5		15.3		ns
t_{ADSU}	Address/Data Setup Time	2.1		2.8		ns
t_{ADH}	Address/Data Hold Time	0.0		0.0		ns
t_{RENSUA}	Read Enable Setup to Address Valid	0.8		1.1		ns
t_{RENHA}	Read Enable Hold	4.4		5.9		ns
t_{WENSU}	Write Enable Setup	3.5		4.7		ns
t_{WENH}	Write Enable Hold	0.0		0.0		ns
t_{DOH}	Data Out Hold Time		1.6		2.1	ns

A32200DX Timing Characteristics (continued)

(Worst-Case Military Conditions, V_{CC} = 4.5V, T_J = 125°C)

		'–1' Speed		'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
TTL Output Module Timing[1]						
t_{DLH}	Data to Pad High		5.1		6.8	ns
t_{DHL}	Data to Pad Low		6.3		8.3	ns
t_{ENZH}	Enable Pad Z to High		6.6		8.8	ns
t_{ENZL}	Enable Pad Z to Low		7.1		9.5	ns
t_{ENHZ}	Enable Pad High to Z		11.5		15.3	ns
t_{ENLZ}	Enable Pad Low to Z		11.5		15.3	ns
t_{GLH}	G to Pad High		11.5		15.3	ns
t_{GHL}	G to Pad Low		12.3		16.5	ns
t_{LSU}	I/O Latch Output Setup	0.4		0.5		ns
t_{LH}	I/O Latch Output Hold	0.0		0.0		ns
t_{LCO}	I/O Latch Clock-Out (Pad-to-Pad) 32 I/O		11.5		15.4	ns
t_{ACO}	Array Latch Clock-Out (Pad-to-Pad) 32 I/O		16.3		21.7	ns
d_{TLH}	Capacitive Loading, Low to High		0.04		0.06	ns/pF
d_{THL}	Capacitive Loading, High to Low		0.06		0.08	ns/pF
t_{WDO}	Hard-Wired Wide Decode Output		0.05		0.07	ns
CMOS Output Module Timing[1]						
t_{DLH}	Data to Pad High		5.1		6.8	ns
t_{DHL}	Data to Pad Low		6.3		8.3	ns
t_{ENZH}	Enable Pad Z to High		6.6		8.8	ns
t_{ENZL}	Enable Pad Z to Low		7.1		9.5	ns
t_{ENHZ}	Enable Pad High to Z		11.5		15.3	ns
t_{ENLZ}	Enable Pad Low to Z		11.5		15.3	ns
t_{GLH}	G to Pad High		11.5		15.3	ns
t_{GHL}	G to Pad Low		12.3		16.5	ns
t_{LSU}	I/O Latch Setup	0.4		0.5		ns
t_{LH}	I/O Latch Hold	0.0		0.0		ns
t_{LCO}	I/O Latch Clock-Out (Pad-to-Pad) 32 I/O		13.7		18.2	ns
t_{ACO}	Array Latch Clock-Out (Pad-to-Pad) 32 I/O		19.2		25.6	ns
d_{TLH}	Capacitive Loading, Low to High		0.06		0.08	ns/pF
d_{THL}	Capacitive Loading, High to Low		0.05		0.07	ns/pF
t_{WDO}	Hard-Wired Wide Decode Output		0.05		0.07	ns

Notes:

1. *Delays based on 35 pF loading.*
2. *SSO information can be found in the* Simultaneously Switching Output Limits for Actel FPGAs *application note at http://www.actel.com/appnotes.*

Pin Description

CLK Clock (Input)

ACT 1 only. TTL Clock input for global clock distribution network. The Clock input is buffered prior to clocking the logic modules. This pin can also be used as an I/O.

CLKA Clock A (Input)

ACT 2, 1200XL, 3200DX, and ACT 3 only. TTL Clock input for global clock distribution networks. The Clock input is buffered prior to clocking the logic modules. This pin can also be used as an I/O.

CLKB Clock B (Input)

ACT 2, 1200XL, 3200DX, and ACT 3 only. TTL Clock input for global clock distribution networks. The Clock input is buffered prior to clocking the logic modules. This pin can also be used as an I/O.

DCLK Diagnostic Clock (Input)

TTL Clock input for diagnostic probe and device programming. DCLK is active when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

GND Ground

LOW supply voltage.

HCLK Dedicated (Hard-wired) Array Clock (Input)

ACT 3 only. TTL Clock input for sequential modules. This input is directly wired to each S-module and offers clock speeds independent of the number of S-modules being driven. This pin can also be used as an I/O.

I/O Input/Output (Input, Output)

I/O pin functions as an input, output, tristate, or bi-directional buffer. Input and output levels are compatible with standard TTL and CMOS specifications. In the ACT 3 and 3200DX families, unused I/Os are automatically tri-stated. With this configuration, the input buffer internal to the I/O module is disabled. In the ACT 1, ACT 2 and 1200XL families, unused I/Os are automatically configured as bi-directional buffers where each buffer is configured as a LOW driver.

IOCLK Dedicated (Hard-wired) I/O Clock (Input)

ACT 3 only. TTL Clock input for I/O modules. This input is directly wired to each I/O module and offers clock speeds independent of the number of I/O modules being driven. This pin can also be used as an I/O.

IOPCL Dedicated (Hard-wired) I/O Preset/Clear (Input)

ACT 3 only. TTL input for I/O preset or clear. This global input is directly wired to the preset and clear inputs of all I/O registers. This pin functions as an I/O when no I/O preset or clear macros are used.

MODE Mode (Input)

The MODE pin controls the use of diagnostic pins (DCLK, PRA, PRB, SDI). When the MODE pin is HIGH, the special functions are active. When the MODE pin is LOW, the pins function as I/Os. To provide debugging capability, the MODE pin should be terminated to GND through a 10 kΩ resistor so that the MODE pin can be pulled high when required.

NC No Connection

This pin is not connected to circuitry within the device.

PRA, I/O Probe A (Output)

The Probe A pin is used to output data from any user-defined design node within the device. This independent diagnostic pin can be used in conjunction with the Probe B pin to allow real-time diagnostic output of any signal path within the device. The Probe A pin can be used as a user-defined I/O when debugging has been completed. The pin's probe capabilities can be permanently disabled to protect programmed design confidentiality. PRA is accessible when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

PRB, I/O Probe B (Output)

The Probe B pin is used to output data from any user-defined design node within the device. This independent diagnostic pin can be used in conjunction with the Probe A pin to allow real-time diagnostic output of any signal path within the device. The Probe B pin can be used as a user-defined I/O when verification has been completed. The pin's probe capabilities can be permanently disabled to protect programmed design confidentiality. PRB is accessible when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

SDI Serial Data Input (Input)

Serial data input for diagnostic probe and device programming. SDI is active when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

V_{CC} 5.0V Supply Voltage

HIGH supply voltage.

QCLKA/B,C,D Quadrant Clock (Input/Output)

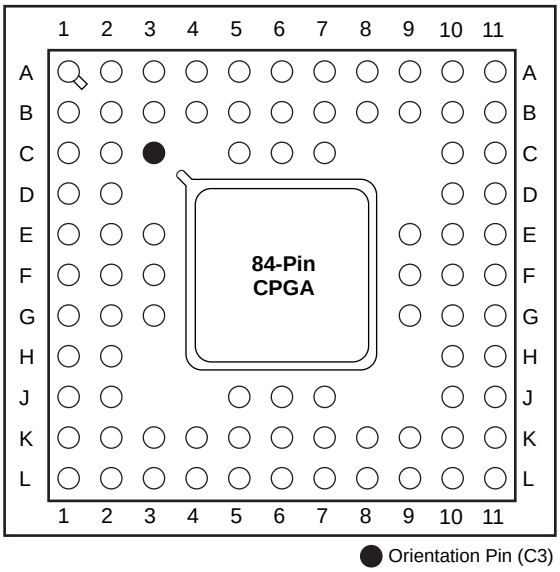
3200DX only. These four pins are the quadrant clock inputs. When not used as a register control signal, these pins can function as general purpose I/O.

TCK Test Clock

Clock signal to shift the JTAG data into the device. This pin functions as an I/O when the JTAG fuse is not programmed. JTAG pins are only available in the 3200DX device.

Package Pin Assignments

84-Pin CPGA (Top View)



176-Pin CPGA

Pin Number	A1280A Function	A1280XL Function
A1	I/O	I/O
A2	I/O	I/O
A3	I/O	I/O
A4	I/O	I/O
A5	I/O	I/O
A6	I/O	I/O
A7	I/O	I/O
A8	I/O	I/O
A9	CLKA, I/O	CLKA, I/O
A10	I/O	I/O
A11	I/O	I/O
A12	I/O	I/O
A13	I/O	I/O
A14	I/O	I/O
A15	I/O	I/O
B1	I/O	I/O
B2	I/O	I/O
B3	DCLK, I/O	DCLK, I/O
B4	I/O	I/O
B5	I/O	I/O
B6	I/O	I/O
B7	I/O	I/O
B8	CLKB, I/O	CLKB, I/O
B9	I/O	I/O
B10	I/O	I/O
B11	I/O	I/O
B12	I/O	I/O
B13	I/O	I/O
B14	SDI, I/O	SDI, I/O
B15	I/O	I/O
C1	I/O	I/O
C2	I/O	I/O
C3	MODE	MODE
C4	I/O	I/O
C5	I/O	I/O
C6	I/O	I/O
C7	I/O	I/O
C8	GND	GND
C9	PRA, I/O	PRA, I/O
C10	I/O	I/O
C11	I/O	I/O
C12	I/O	I/O
C13	I/O	I/O
C14	I/O	I/O
C15	I/O	I/O
D1	I/O	I/O
D2	I/O	I/O
D3	I/O	I/O
D4	GND	GND
D5	V_{CC}	V_{CC}
D6	GND	GND
D7	PRB, I/O	PRB, I/O
D8	V_{CC}	V_{CC}
D9	I/O	I/O
D10	GND	GND
D11	V_{CC}	V_{CC}
D12	GND	GND
D13	I/O	I/O
D14	I/O	I/O
D15	I/O	I/O
E1	I/O	I/O
E2	I/O	I/O
E3	I/O	I/O
E4	GND	GND
E12	GND	GND
E13	I/O	I/O
E14	I/O	I/O
E15	I/O	I/O
F1	I/O	I/O
F2	I/O	I/O
F3	I/O	I/O
F4	V_{CC}	V_{CC}
F12	GND	GND
F13	I/O	I/O
F14	I/O	I/O
F15	I/O	I/O
G1	I/O	I/O
G2	I/O	I/O
G3	I/O	I/O
G4	GND	GND
G12	V_{CC}	V_{CC}
G13	I/O	I/O
G14	I/O	I/O
G15	I/O	I/O
H1	I/O	I/O
H2	V_{CC}	V_{CC}
H3	V_{CC}	V_{CC}
H4	GND	GND

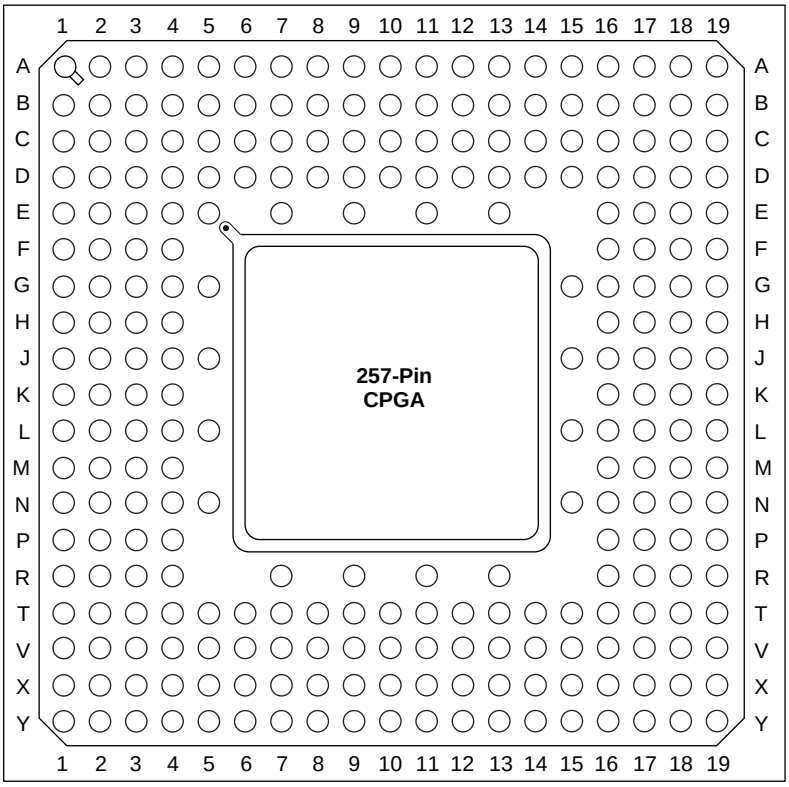
176-Pin CPGA (Continued)

Pin Number	A1280A Function	A1280XL Function
H12	GND	GND
H13	V_{CC}	V_{CC}
H14	V_{CC}	V_{CC}
H15	I/O	I/O
J1	I/O	I/O
J2	I/O	I/O
J3	I/O	I/O
J4	V_{CC}	V_{CC}
J12	GND	GND
J13	GND	GND
J14	V_{CC}	V_{CC}
J15	I/O	I/O
K1	I/O	I/O
K2	I/O	I/O
K3	I/O	I/O
K4	GND	GND
K12	GND	GND
K13	I/O	I/O
K14	I/O	I/O
K15	I/O	I/O
L1	I/O	I/O
L2	I/O	I/O
L3	I/O	I/O
L4	GND	GND
L12	I/O	I/O
L13	I/O	I/O
L14	I/O	I/O
L15	I/O	I/O
M1	I/O	I/O
M2	I/O	I/O
M3	I/O	I/O
M4	GND	GND
M5	V_{CC}	V_{CC}
M6	GND	GND
M7	I/O	I/O
M8	GND	GND
M9	I/O	I/O
M10	GND	GND
M11	V_{CC}	V_{CC}
M12	GND	GND
M13	I/O	I/O
M14	I/O	I/O
M15	I/O	I/O
N1	I/O	I/O

Pin Number	A1280A Function	A1280XL Function
N2	I/O	I/O
N3	I/O	I/O
N4	I/O	I/O
N5	I/O	I/O
N6	I/O	I/O
N7	I/O	I/O
N8	V_{CC}	V_{CC}
N9	I/O	I/O
N10	I/O	I/O
N11	I/O	I/O
N12	I/O	I/O
N13	I/O	I/O
N14	I/O	I/O
N15	I/O	I/O
P1	I/O	I/O
P2	I/O	I/O
P3	I/O	I/O
P4	I/O	I/O
P5	I/O	I/O
P6	I/O	I/O
P7	I/O	I/O
P8	I/O	I/O
P9	I/O	I/O
P10	I/O	I/O
P11	I/O	I/O
P12	I/O	I/O
P13	I/O	I/O
P14	I/O	I/O
P15	I/O	I/O
R1	I/O	I/O
R2	I/O	I/O
R3	I/O	I/O
R4	I/O	I/O
R5	I/O	I/O
R6	I/O	I/O
R7	I/O	I/O
R8	I/O	I/O
R9	I/O	I/O
R10	I/O	I/O
R11	I/O	I/O
R12	I/O	I/O
R13	I/O	I/O
R14	I/O	I/O
R15	I/O	I/O

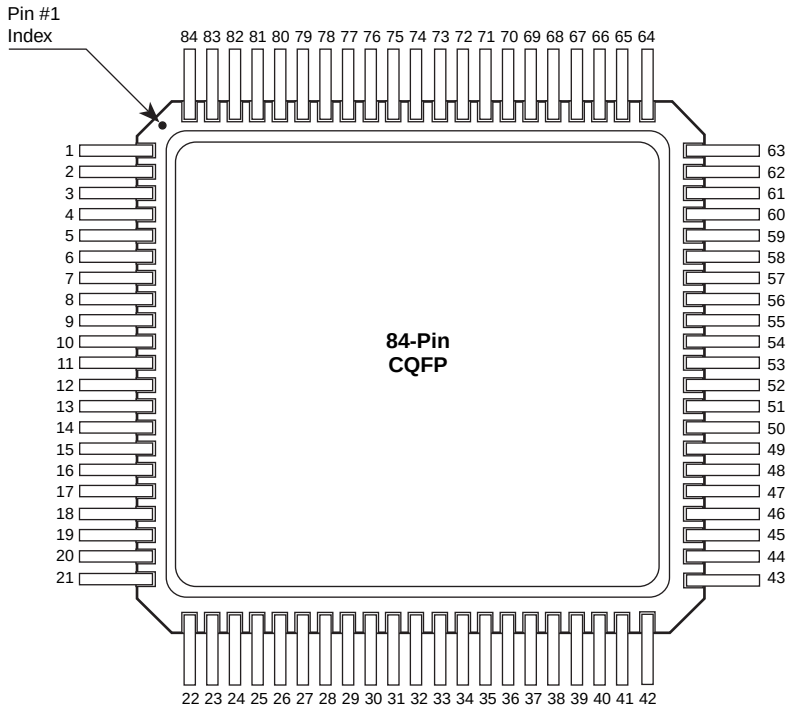
Package Pin Assignments (continued)

257-Pin CPGA (Top View)



Package Pin Assignments (continued)

84-Pin CQFP (Top View)



84-Pin CQFP

Pin Number	A1020B Function	A32100DX Function
1	NC	GND
2	I/O	MODE
3	I/O	I/O
4	I/O	I/O
5	I/O	I/O
6	I/O	I/O
7	GND	V_{CC}
8	GND	I/O
9	I/O	I/O
10	I/O	GND
11	I/O	V_{CC}
12	I/O	V_{CC}
13	I/O	I/O
14	V_{CC}	I/O
15	V_{CC}	I/O
16	I/O	I/O
17	I/O	GND
18	I/O	I/O
19	I/O	I/O
20	I/O	I/O
21	I/O	I/O
22	V_{CC}	GND
23	I/O	I/O
24	I/O	I/O
25	I/O	I/O (WD)
26	I/O	I/O (WD)
27	I/O	I/O
28	I/O	QCLKA, I/O
29	GND	GND
30	I/O	I/O (WD)
31	I/O	I/O
32	I/O	GND
33	I/O	V_{CC}
34	I/O	I/O (WD)
35	V_{CC}	I/O (WD)
36	I/O	QCLKB, I/O
37	I/O	I/O (WD)
38	I/O	GND
39	I/O	I/O (WD)
40	I/O	I/O (WD)
41	I/O	I/O (WD)
42	I/O	SDO, I/O

Pin Number	A1020B Function	A32100DX Function
43	I/O	GND
44	I/O	I/O
45	I/O	I/O
46	I/O	I/O
47	I/O	I/O
48	I/O	I/O
49	GND	I/O
50	GND	GND
51	I/O	TCK, I/O
52	I/O	GND
53	CLKA, I/O	V_{CC}
54	I/O	V_{CC}
55	MODE	V_{CC}
56	V_{CC}	V_{CC}
57	V_{CC}	I/O
58	I/O	I/O
59	I/O	GND
60	I/O	I/O
61	SDI, I/O	I/O
62	DCLK, I/O	I/O
63	PRA, I/O	GND
64	PRB, I/O	SDI, I/O
65	I/O	I/O (WD)
66	I/O	I/O (WD)
67	I/O	I/O (WD)
68	I/O	I/O (WD)
69	I/O	QCLKD, I/O
70	I/O	I/O (WD)
71	GND	I/O (WD)
72	I/O	PRA, I/O
73	I/O	CLKA, I/O
74	I/O	V_{CC}
75	I/O	GND
76	I/O	CLKB, I/O
77	V_{CC}	PRB, I/O
78	I/O	I/O (WD)
79	I/O	I/O (WD)
80	I/O	QCLKC, I/O
81	I/O	GND
82	I/O	I/O (WD)
83	I/O	I/O (WD)
84	I/O	DCLK, I/O

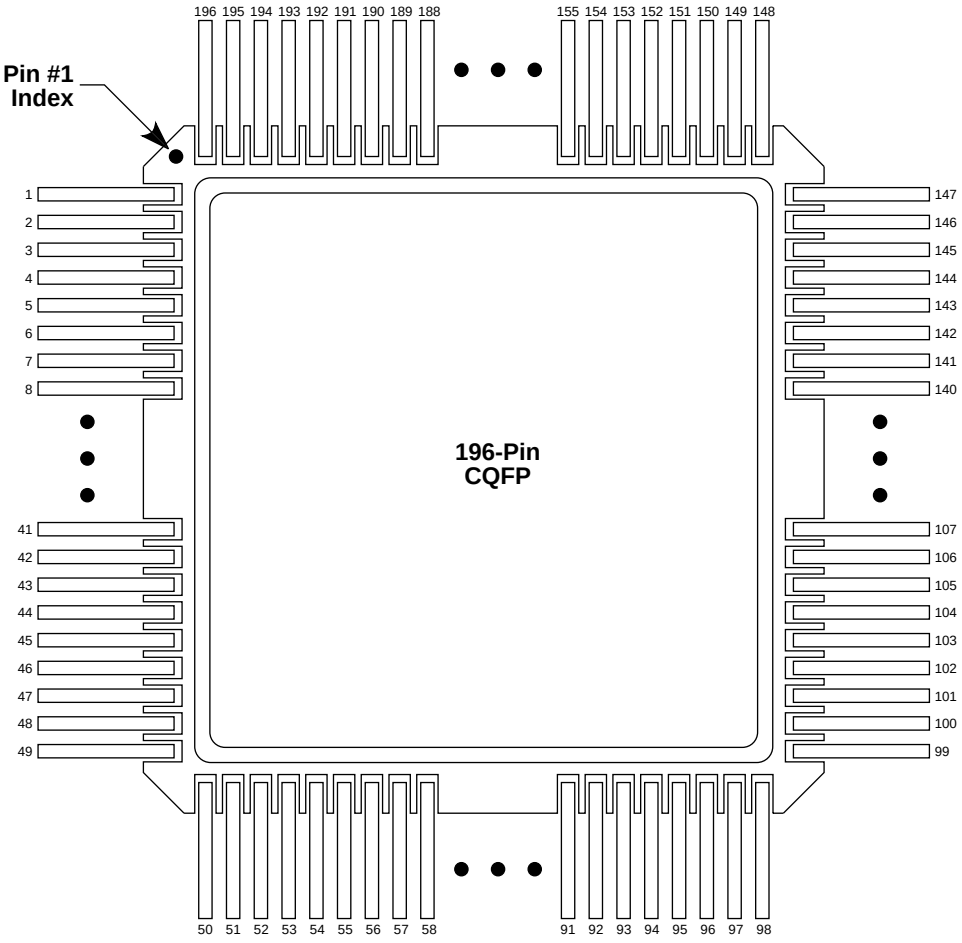
172-Pin CQFP (Continued)

Pin Number	A1280A Function	A1280XL Function
89	I/O	I/O
90	I/O	I/O
91	I/O	I/O
92	I/O	I/O
93	I/O	I/O
94	I/O	I/O
95	I/O	I/O
96	I/O	I/O
97	I/O	I/O
98	GND	GND
99	I/O	I/O
100	I/O	I/O
101	I/O	I/O
102	I/O	I/O
103	GND	GND
104	I/O	I/O
105	I/O	I/O
106	GND	GND
107	V_{CC}	V_{CC}
108	GND	GND
109	V_{CC}	V_{CC}
110	V_{CC}	V_{CC}
111	I/O	I/O
112	I/O	I/O
113	V_{CC}	V_{CC}
114	I/O	I/O
115	I/O	I/O
116	I/O	I/O
117	I/O	I/O
118	GND	GND
119	I/O	I/O
120	I/O	I/O
121	I/O	I/O
122	I/O	I/O
123	GND	GND
124	I/O	I/O
125	I/O	I/O
126	I/O	I/O
127	I/O	I/O
128	I/O	I/O
129	I/O	I/O
130	I/O	I/O

Pin Number	A1280A Function	A1280XL Function
131	SDI, I/O	SDI, I/O
132	I/O	I/O
133	I/O	I/O
134	I/O	I/O
135	I/O	I/O
136	V_{CC}	V_{CC}
137	I/O	I/O
138	I/O	I/O
139	I/O	I/O
140	I/O	I/O
141	GND	GND
142	I/O	I/O
143	I/O	I/O
144	I/O	I/O
145	I/O	I/O
146	I/O	I/O
147	I/O	I/O
148	PRA, I/O	PRA, I/O
149	I/O	I/O
150	CLKA, I/O	CLKA, I/O
151	V_{CC}	V_{CC}
152	GND	GND
153	I/O	I/O
154	CLKB, I/O	CLKB, I/O
155	I/O	I/O
156	PRB, I/O	PRB, I/O
157	I/O	I/O
158	I/O	I/O
159	I/O	I/O
160	I/O	I/O
161	GND	GND
162	I/O	I/O
163	I/O	I/O
164	I/O	I/O
165	I/O	I/O
166	V_{CC}	V_{CC}
167	I/O	I/O
168	I/O	I/O
169	I/O	I/O
170	I/O	I/O
171	DCLK, I/O	DCLK, I/O
172	I/O	I/O

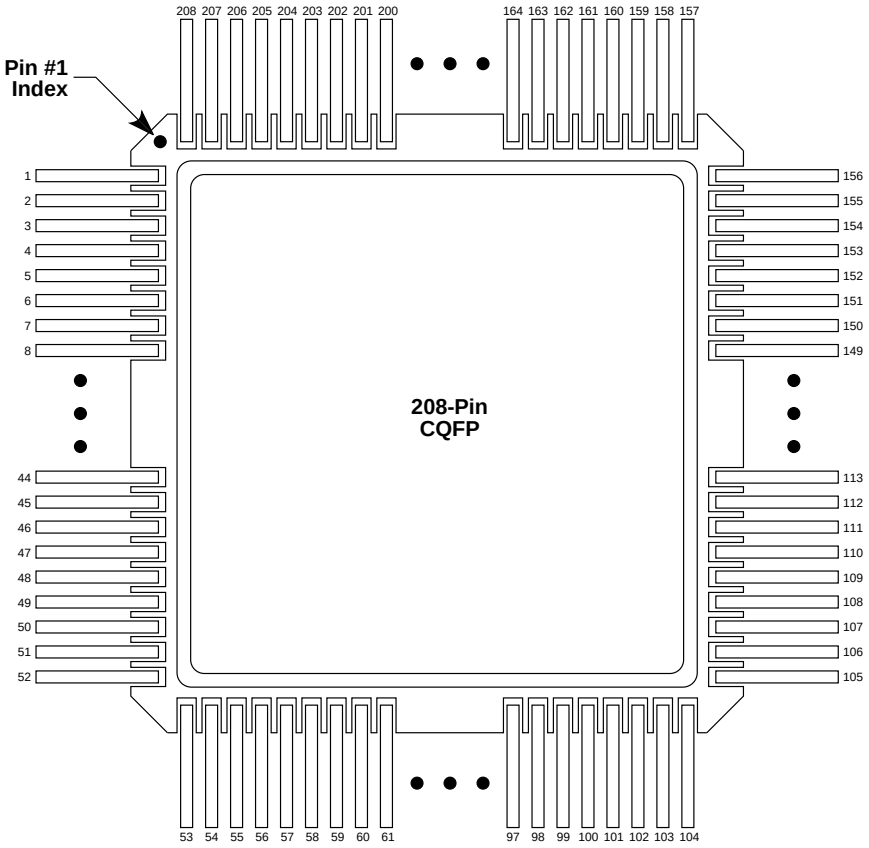
Package Pin Assignments (continued)

196-Pin CQFP (Top View)



Package Pin Assignments (continued)

208-Pin CQFP (Top View)



Package Pin Assignments (continued)

256-Pin CQFP (Top View)