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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	547
Number of Logic Elements/Cells	-
Total RAM Bits	-
Number of I/O	69
Number of Gates	2000
Voltage - Supply	4.5V ~ 5.5V
Mounting Type	Surface Mount
Operating Temperature	-55°C ~ 125°C (TC)
Package / Case	84-CQFP Exposed Pad and Tie Bar
Supplier Device Package	84-CQFP (42x42)
Purchase URL	https://www.e-xfl.com/product-detail/microsemi/a1020b-1cq84m

Product Family Profile

Family / Device	ACT 2 A1240A	ACT 2 A1280A	ACT 1 A1010B	ACT 1 A1020B
Capacity				
System Gates	6,000	12,000	1,800	3,000
Logic Gates	4,000	8,000	1,200	2,000
SRAM Bits	NA	NA	NA	NA
Logic Modules	684	1,232	295	547
S-Modules	348	624	—	—
C-Modules	336	608	295	547
Decode	NA	NA	NA	NA
Flip-Flops (maximum)	568	998	147	273
User I/Os (maximum)	104	140	57	69
Packages (by pin count)				
CPGA	132	176	84	84
CQFP	—	172	—	84
Performance				
System Speed (maximum)	40 MHz	40 MHz	20 MHz	20 MHz

High-Reliability, Low-Risk Solution

Actel builds the most reliable field programmable gate arrays (FPGAs) in the industry, with overall antifuse reliability ratings of less than 10 Failures-In-Time (FITs), corresponding to a useful life of more than 40 years. Actel FPGAs have been production proven, with more than five million devices shipped and more than one trillion antifuses manufactured. Actel devices are fully tested prior to shipment, with an outgoing defect level of less than 100 ppm. (Further reliability data is available in the *Actel Device Reliability Report*, at http://www.actel.com/hirel).

Benefits

Minimized Cost Risk

With Actel's line of development tools, designers can produce as many chips as they choose for just the cost of the device itself. There will be no NRE charges to cut into the development budget each time a new design is tried.

Minimized Time Risk

After the design is entered, placement and routing is automatic, and programming the device takes only about 5 to 15 minutes for an average design. Designers save time in the design entry process by using tools with which they are familiar.

Minimized Reliability Risk

The PLICE antifuse is a one-time programmable, nonvolatile connection. Since Actel devices are permanently programmed, no downloading from EPROM or SRAM storage is required. Inadvertent erasure is impossible, and there is no need to reload the program after power disruptions. Fabrication using a low-power CMOS process means cooler junction temperatures. Actel's non-PLD architecture delivers lower dynamic operating current. Our reliability tests show a very low failure rate of 6.6 FITs at 90°C junction temperature with no degradation in AC performance. Special stress testing at wafer test eliminates infant mortalities prior to packaging.

Minimized Security Risk

Reverse engineering of programmed Actel devices from optical or electrical data is extremely difficult. Programmed antifuses cannot be identified from a photograph or by using an SEM. The antifuse map cannot be deciphered either electrically or by microprobing. Each device has a silicon signature that identifies its origins, down to the wafer lot and fabrication facility.

Minimized Testing Risk

Unprogrammed Actel parts are extensively tested at the factory. Routing tracks, logic modules, and programming, debug and test circuits are 100 percent tested before shipment. AC performance is ensured by special speed path tests, and programming circuitry is verified on test antifuses. During the programming process, an algorithm is run to ensure that all antifuses are correctly programmed. In addition, Actel's Silicon Explorer diagnostic tool uses ActionProbe circuitry, allowing 100 percent observability of all internal nodes to check and debug the design.

Actel FPGA Description

The Actel families of FPGAs offer a variety of packages, speed/performance characteristics, and processing levels for use in all high reliability and military applications. Devices are implemented in a silicon gate, two-level metal CMOS process, utilizing Actel's PLICE antifuse technology. This

Fixed Capacitance Values for Actel FPGAs (pF)

Device Type	r_1 routed_Clk1	r_2 routed_Clk2
A1010B	41	n/a
A1020B	69	n/a
A1240A	134	134
A1280A	168	168
A1280XL	168	168
A1425A	75	75
A1460A	165	165
A14100A	195	195
A32100DX	178	178
A32200DX	230	230

Fixed Clock Loads (s_1/s_2—ACT 3 Only)

Device Type	s_1 Clock Loads on Dedicated Array Clock	s_2 Clock Loads on Dedicated I/O Clock
A1425A	160	100
A1460A	432	168
A14100A	697	228

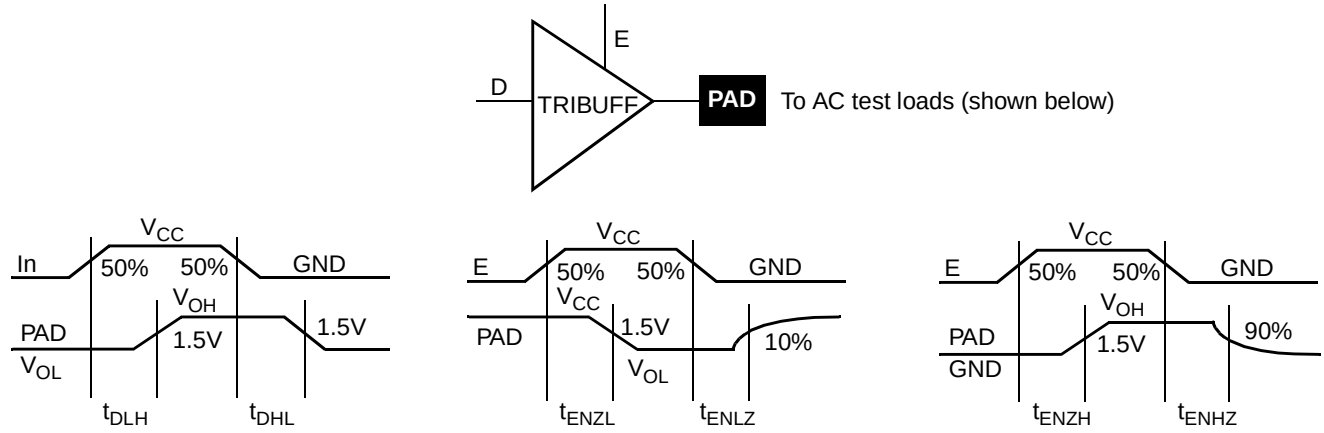
Determining Average Switching Frequency

To determine the switching frequency for a design, you must have a detailed understanding of the data values input to the circuit. The guidelines in the table below are meant to represent worst-case scenarios so that they can be generally used to predict the upper limits of power dissipation.

Type	ACT 3	3200DX/ACT 2/1200XL	ACT 1
Logic modules (m)	80% of modules	80% of modules	90% of modules
Input switching (n)	# inputs/4	# inputs/4	# inputs/4
Outputs switching (p)	#outputs/4	#outputs/4	#outputs/4
First routed array clock loads (q_1)	40% of sequential modules	40% of sequential modules	40% of modules
Second routed array clock loads (q_2)	40% of sequential modules	40% of sequential modules	n/a
Load capacitance (C_L)	35 pF	35 pF	35 pF
Average logic module switching rate (f_m)	F/10	F/10	F/10
Average input switching rate (f_n)	F/5	F/5	F/5
Average output switching rate (f_p)	F/10	F/10	F/10
Average first routed array clock rate (f_{q1})	F/2	F	F
Average second routed array clock rate (f_{q2})	F/2	F/2	n/a
Average dedicated array clock rate (f_{s1})	F	n/a	n/a
Average dedicated I/O clock rate (f_{s2})	F	n/a	n/a

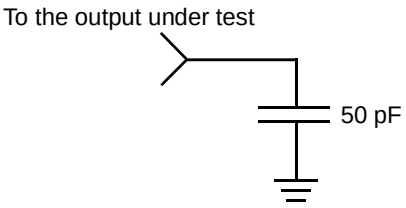
Parameter Measurement

Output Buffer Delays

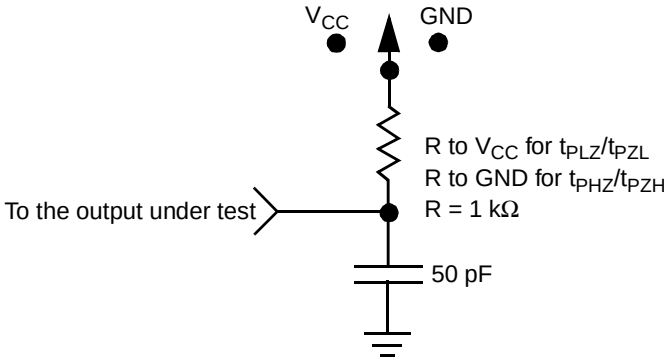


AC Test Load

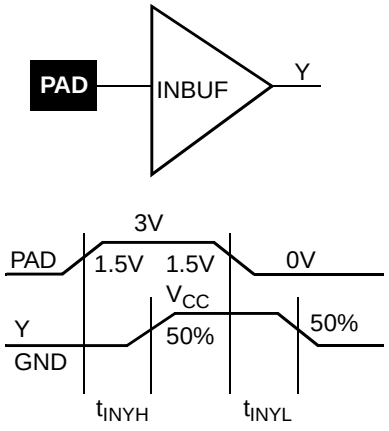
Load 1
(Used to measure propagation delay)



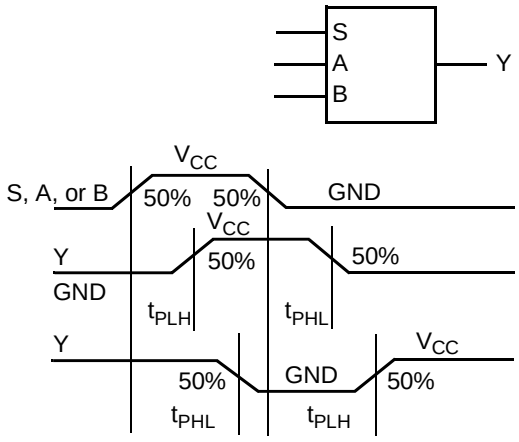
Load 2
(Used to measure rising/falling edges)



Input Buffer Delays



Combinatorial Macro Delays



ACT 1 Timing Characteristics (continued)

(Worst-Case Military Conditions, V_{CC} = 4.5V, T_J = 125°C)

			'–1' Speed		'Std' Speed		
Parameter	**Description**		**Min.**	**Max.**	**Min.**	**Max.**	**Units**
Global Clock Network							
t_{CKH}	Input Low to High	FO = 16 FO = 128		7.8 8.9		9.2 10.5	ns
t_{CKL}	Input High to Low	FO = 16 FO = 128		10.3 11.2		12.1 13.2	ns
t_{PWH}	Minimum Pulse Width High	FO = 16 FO = 128	10.4 10.9		12.2 12.9		ns
t_{PWL}	Minimum Pulse Width Low	FO = 16 FO = 128	10.4 10.9		12.2 12.9		ns
t_{CKSW}	Maximum Skew	FO = 16 FO = 128		1.9 2.9		2.2 3.4	ns
t_P	Minimum Period	FO = 16 FO = 128	21.7 23.2		25.6 27.3		ns
f_{MAX}	Maximum Frequency	FO = 16 FO = 128		46 44		40 37	MHz
TTL Output Module Timing[1]							
t_{DLH}	Data to Pad High			12.1		14.2	ns
t_{DHL}	Data to Pad Low			13.8		16.3	ns
t_{ENZH}	Enable Pad Z to High			12.0		14.1	ns
t_{ENZL}	Enable Pad Z to Low			14.6		17.1	ns
t_{ENHZ}	Enable Pad High to Z			16.0		18.8	ns
t_{ENLZ}	Enable Pad Low to Z			14.5		17.0	ns
d_{TLH}	Delta Low to High			0.09		0.11	ns/pF
d_{THL}	Delta High to Low			0.12		0.15	ns/pF
CMOS Output Module Timing[1]							
t_{DLH}	Data to Pad High			15.1		17.7	ns
t_{DHL}	Data to Pad Low			11.5		13.6	ns
t_{ENZH}	Enable Pad Z to High			12.0		14.1	ns
t_{ENZL}	Enable Pad Z to Low			14.6		17.1	ns
t_{ENHZ}	Enable Pad High to Z			16.0		18.8	ns
t_{ENLZ}	Enable Pad Low to Z			14.5		17.0	ns
d_{TLH}	Delta Low to High			0.16		0.18	ns/pF
d_{THL}	Delta High to Low			0.09		0.11	ns/pF

Notes:

1. *Delays based on 50 pF loading.*
2. *SSO information can be found in the* Simultaneously Switching Output Limits for Actel FPGAs *application note at http://www.actel.com/appnotes.*

A1240A Timing Characteristics (continued)

(Worst-Case Military Conditions, V_{CC} = 4.5V, T_J = 125°C)

		'–1' Speed		'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
TTL Output Module Timing[1]						
t_{DLH}	Data to Pad High		11.0		13.0	ns
t_{DHL}	Data to Pad Low		13.9		16.4	ns
t_{ENZH}	Enable Pad Z to High		12.3		14.4	ns
t_{ENZL}	Enable Pad Z to Low		16.1		19.0	ns
t_{ENHZ}	Enable Pad High to Z		9.8		11.5	ns
t_{ENLZ}	Enable Pad Low to Z		11.5		13.6	ns
t_{GLH}	G to Pad High		12.4		14.6	ns
t_{GHL}	G to Pad Low		15.5		18.2	ns
d_{TLH}	Delta Low to High		0.09		0.11	ns/pF
d_{THL}	Delta High to Low		0.17		0.20	ns/pF
CMOS Output Module Timing[1]						
t_{DLH}	Data to Pad High		14.0		16.5	ns
t_{DHL}	Data to Pad Low		11.7		13.7	ns
t_{ENZH}	Enable Pad Z to High		12.3		14.4	ns
t_{ENZL}	Enable Pad Z to Low		16.1		19.0	ns
t_{ENHZ}	Enable Pad High to Z		9.8		11.5	ns
t_{ENLZ}	Enable Pad Low to Z		11.5		13.6	ns
t_{GLH}	G to Pad High		12.4		14.6	ns
t_{GHL}	G to Pad Low		15.5		18.2	ns
d_{TLH}	Delta Low to High		0.17		0.20	ns/pF
d_{THL}	Delta High to Low		0.12		0.15	ns/pF

Notes:

1. *Delays based on 50 pF loading.*
2. *SSO information can be found in the* Simultaneously Switching Output Limits for Actel FPGAs *application note at http://www.actel.com/appnotes.*

A1425A Timing Characteristics (continued)

(Worst-Case Military Conditions, V_{CC} = 4.5V, T_J = 125°C)

		'–1' Speed		'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
I/O Module Sequential Timing						
t_{INH}	Input F-F Data Hold (w.r.t. IOCLK Pad)	0.0		0.0		ns
t_{INSU}	Input F-F Data Setup (w.r.t. IOCLK Pad)	2.1		2.4		ns
t_{IDEH}	Input Data Enable Hold (w.r.t. IOCLK Pad)	0.0		0.0		ns
t_{IDESU}	Input Data Enable Setup (w.r.t. IOCLK Pad)	8.7		10.0		ns
t_{OUTH}	Output F-F Data Hold (w.r.t. IOCLK Pad)	1.1		1.2		ns
t_{OUTSU}	Output F-F Data Setup (w.r.t. IOCLK Pad)	1.1		1.2		ns
t_{ODEH}	Output Data Enable Hold (w.r.t. IOCLK Pad)	0.5		0.6		ns
t_{ODESU}	Output Data Enable Setup (w.r.t. IOCLK Pad)	2.0		2.4		ns
TTL Output Module Timing[1]						
t_{DHS}	Data to Pad, High Slew		7.5		8.9	ns
t_{DLS}	Data to Pad, Low Slew		11.9		14.0	ns
t_{ENZHS}	Enable to Pad, Z to H/L, High Slew		6.0		7.0	ns
t_{ENZLS}	Enable to Pad, Z to H/L, Low Slew		10.9		12.8	ns
t_{ENHSZ}	Enable to Pad, H/L to Z, High Slew		9.9		11.6	ns
t_{ENLSZ}	Enable to Pad, H/L to Z, Low Slew		9.9		11.6	ns
t_{CKHS}	IOCLK Pad to Pad H/L, High Slew		10.5		11.6	ns
t_{CKLS}	IOCLK Pad to Pad H/L, Low Slew		15.7		17.4	ns
d_{TLHHS}	Delta Low to High, High Slew		0.04		0.04	ns/pF
d_{TLHLS}	Delta Low to High, Low Slew		0.07		0.08	ns/pF
d_{THLHS}	Delta High to Low, High Slew		0.05		0.06	ns/pF
d_{THLLS}	Delta High to Low, Low Slew		0.07		0.08	ns/pF

Note:

1. Delays based on 35 pF loading.

A1425A Timing Characteristics (continued)

(Worst-Case Military Conditions, V_{CC} = 4.5V, T_J = 125°C)

		'–1' Speed		'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
CMOS Output Module Timing[1]						
t_{DHS}	Data to Pad, High Slew		9.2		10.8	ns
t_{DLS}	Data to Pad, Low Slew		17.3		20.3	ns
t_{ENZHS}	Enable to Pad, Z to H/L, High Slew		7.7		9.1	ns
t_{ENZLS}	Enable to Pad, Z to H/L, Low Slew		13.1		15.5	ns
t_{ENHSZ}	Enable to Pad, H/L to Z, High Slew		9.9		11.6	ns
t_{ENLSZ}	Enable to Pad, H/L to Z, Low Slew		10.5		11.6	ns
t_{CKHS}	IOCLK Pad to Pad H/L, High Slew		12.5		13.7	ns
t_{CKLS}	IOCLK Pad to Pad H/L, Low Slew		18.1		20.1	ns
d_{TLHHS}	Delta Low to High, High Slew		0.06		0.07	ns/pF
d_{TLHLS}	Delta Low to High, Low Slew		0.11		0.13	ns/pF
d_{THLHS}	Delta High to Low, High Slew		0.04		0.05	ns/pF
d_{THLLS}	Delta High to Low, Low Slew		0.05		0.06	ns/pF
Dedicated (Hard-Wired) I/O Clock Network						
t_{IOCKH}	Input Low to High (Pad to I/O Module Input)		3.0		3.5	ns
t_{IOPWH}	Minimum Pulse Width High	3.9		4.4		ns
t_{IOPWL}	Minimum Pulse Width Low	3.9		4.4		ns
t_{IOSAPW}	Minimum Asynchronous Pulse Width	3.9		4.4		ns
t_{IOCKSW}	Maximum Skew		0.5		0.5	ns
t_{IOP}	Minimum Period	7.9		9.3		ns
f_{IOMAX}	Maximum Frequency		125		100	MHz
Dedicated (Hard-Wired) Array Clock Network						
t_{HCKH}	Input Low to High (Pad to S-Module Input)		4.6		5.3	ns
t_{HCKL}	Input High to Low (Pad to S-Module Input)		4.6		5.3	ns
t_{HPWH}	Minimum Pulse Width High	3.9		4.4		ns
t_{HPWL}	Minimum Pulse Width Low	3.9		4.4		ns
t_{HCKSW}	Maximum Skew		0.4		0.4	ns
t_{HP}	Minimum Period	7.9		9.3		ns
f_{HMAX}	Maximum Frequency		125		100	MHz

Notes:

1. *Delays based on 35 pF loading.*
2. *SSO information can be found in the* Simultaneously Switching Output Limits for Actel FPGAs *application note at http://www.actel.com/appnotes.*

A1460A Timing Characteristics (continued)

(Worst-Case Military Conditions, V_{CC} = 4.5V, T_J = 125°C)

		'–1' Speed		'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
I/O Module Sequential Timing						
t_{INH}	Input F-F Data Hold (w.r.t. IOCLK Pad)	0.0		0.0		ns
t_{INSU}	Input F-F Data Setup (w.r.t. IOCLK Pad)	2.1		2.4		ns
t_{IDEH}	Input Data Enable Hold (w.r.t. IOCLK Pad)	0.0		0.0		ns
t_{IDESU}	Input Data Enable Setup (w.r.t. IOCLK Pad)	8.7		10.0		ns
t_{OUTH}	Output F-F Data Hold (w.r.t. IOCLK Pad)	1.1		1.2		ns
t_{OUTSU}	Output F-F Data Setup (w.r.t. IOCLK Pad)	1.1		1.2		ns
t_{ODEH}	Output Data Enable Hold (w.r.t. IOCLK Pad)	0.5		0.6		ns
t_{ODESU}	Output Data Enable Setup (w.r.t. IOCLK Pad)	2.0		2.4		ns
TTL Output Module Timing[1]						
t_{DHS}	Data to Pad, High Slew		7.5		8.9	ns
t_{DLS}	Data to Pad, Low Slew		11.9		14.0	ns
t_{ENZHS}	Enable to Pad, Z to H/L, High Slew		6.0		7.0	ns
t_{ENZLS}	Enable to Pad, Z to H/L, Low Slew		10.9		12.8	ns
t_{ENHSZ}	Enable to Pad, H/L to Z, High Slew		11.5		13.5	ns
t_{ENLSZ}	Enable to Pad, H/L to Z, Low Slew		10.9		12.8	ns
t_{CKHS}	IOCLK Pad to Pad H/L, High Slew		11.6		13.4	ns
t_{CKLS}	IOCLK Pad to Pad H/L, Low Slew		17.8		19.8	ns
d_{TLHHS}	Delta Low to High, High Slew		0.04		0.04	ns/pF
d_{TLHLS}	Delta Low to High, Low Slew		0.07		0.08	ns/pF
d_{THLHS}	Delta High to Low, High Slew		0.05		0.06	ns/pF
d_{THLLS}	Delta High to Low, Low Slew		0.07		0.08	ns/pF

Note:

1. Delays based on 35 pF loading.

A1460A Timing Characteristics (continued)

(Worst-Case Military Conditions, V_{CC} = 4.5V, T_J = 125°C)

		'–1' Speed		'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
CMOS Output Module Timing[1]						
t_{DHS}	Data to Pad, High Slew		9.2		10.8	ns
t_{DLS}	Data to Pad, Low Slew		17.3		20.3	ns
t_{ENZHS}	Enable to Pad, Z to H/L, High Slew		7.7		9.1	ns
t_{ENZLS}	Enable to Pad, Z to H/L, Low Slew		13.1		15.5	ns
t_{ENHSZ}	Enable to Pad, H/L to Z, High Slew		10.9		12.8	ns
t_{ENLSZ}	Enable to Pad, H/L to Z, Low Slew		10.9		12.8	ns
t_{CKHS}	IOCLK Pad to Pad H/L, High Slew		14.1		16.0	ns
t_{CKLS}	IOCLK Pad to Pad H/L, Low Slew		20.2		22.4	ns
d_{TLHHS}	Delta Low to High, High Slew		0.06		0.07	ns/pF
d_{TLHLS}	Delta Low to High, Low Slew		0.11		0.13	ns/pF
d_{THLHS}	Delta High to Low, High Slew		0.04		0.05	ns/pF
d_{THLLS}	Delta High to Low, Low Slew		0.05		0.06	ns/pF
Dedicated (Hard-Wired) I/O Clock Network						
t_{IOCKH}	Input Low to High (Pad to I/O Module Input)		3.5		4.1	ns
t_{IOPWH}	Minimum Pulse Width High	4.8		5.7		ns
t_{IOPWL}	Minimum Pulse Width Low	4.8		5.7		ns
t_{IOSAPW}	Minimum Asynchronous Pulse Width	3.9		4.4		ns
t_{IOCKSW}	Maximum Skew		0.9		1.0	ns
t_{IOP}	Minimum Period	9.9		11.6		ns
f_{IOMAX}	Maximum Frequency		100		85	MHz
Dedicated (Hard-Wired) Array Clock Network						
t_{HCKH}	Input Low to High (Pad to S-Module Input)		5.5		6.4	ns
t_{HCKL}	Input High to Low (Pad to S-Module Input)		5.5		6.4	ns
t_{HPWH}	Minimum Pulse Width High	4.8		5.7		ns
t_{HPWL}	Minimum Pulse Width Low	4.8		5.7		ns
t_{HCKSW}	Maximum Skew		0.9		1.0	ns
t_{HP}	Minimum Period	9.9		11.6		ns
f_{HMAX}	Maximum Frequency		100		85	MHz

Notes:

1. *Delays based on 35 pF loading.*
2. *SSO information can be found in the* Simultaneously Switching Output Limits for Actel FPGAs *application note at http://www.actel.com/appnotes.*

A14100A Timing Characteristics (continued)

(Worst-Case Military Conditions, V_{CC} = 4.5V, T_J = 125°C)

		'–1' Speed		'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
Routed Array Clock Networks						
t_{RCKH}	Input Low to High (FO=256)		9.0		10.5	ns
t_{RCKL}	Input High to Low (FO=256)		9.0		10.5	ns
t_{RPWH}	Min. Pulse Width High (FO=256)	6.3		7.1		ns
t_{RPWL}	Min. Pulse Width Low (FO=256)	6.3		7.1		ns
t_{RCKSW}	Maximum Skew (FO=128)		1.9		2.1	ns
t_{RP}	Minimum Period (FO=256)	12.9		14.5		ns
f_{RMAX}	Maximum Frequency (FO=256)		75		65	MHz
Clock-to-Clock Skews						
$t_{IOHCKSW}$	I/O Clock to H-Clock Skew	0.0	3.5	0.0	3.5	ns
$t_{IORCKSW}$	I/O Clock to R-Clock Skew	0.0	5.0	0.0	5.0	ns
t_{HRCKSW}	H-Clock to R-Clock Skew (FO = 64) (FO = 50% max.)	 0.0 0.0	 1.0 3.0	 0.0 0.0	 1.0 3.0	ns

A32100DX Timing Characteristics (continued)

(Worst-Case Military Conditions, V_{CC} = 4.5V, T_J = 125°C)

		'–1' Speed		'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
Synchronous SRAM Operations						
t_{RC}	Read Cycle Time	8.8		11.8		ns
t_{WC}	Write Cycle Time	8.8		11.8		ns
t_{RCKHL}	Clock High/Low Time	4.4		5.9		ns
t_{RCO}	Data Valid After Clock High/Low		4.4		5.9	ns
t_{ADSU}	Address/Data Setup Time	2.1		2.8		ns
t_{ADH}	Address/Data Hold Time	0.0		0.0		ns
t_{RENSU}	Read Enable Setup	0.8		1.1		ns
t_{RENH}	Read Enable Hold	4.4		5.9		ns
t_{WENSU}	Write Enable Setup	3.5		4.7		ns
t_{WENH}	Write Enable Hold	0.0		0.0		ns
t_{BENS}	Block Enable Setup	3.6		4.8		ns
t_{BENH}	Block Enable Hold	0.0		0.0		ns
Asynchronous SRAM Operations						
t_{RPD}	Asynchronous Access Time		10.6		14.1	ns
t_{RDADV}	Read Address Valid	11.5		15.3		ns
t_{ADSU}	Address/Data Setup Time	2.1		2.8		ns
t_{ADH}	Address/Data Hold Time	0.0		0.0		ns
t_{RENSUA}	Read Enable Setup to Address Valid	0.8		1.1		ns
t_{RENHA}	Read Enable Hold	4.4		5.9		ns
t_{WENSU}	Write Enable Setup	3.5		4.7		ns
t_{WENH}	Write Enable Hold	0.0		0.0		ns
t_{DOH}	Data Out Hold Time		1.6		2.1	ns

A32100DX Timing Characteristics (continued)

(Worst-Case Military Conditions, V_{CC} = 4.5V, T_J = 125°C)

			'–1' Speed		'Std' Speed		
Parameter	**Description**		**Min.**	**Max.**	**Min.**	**Max.**	**Units**
Input Module Propagation Delays							
t_{INPY}	Input Data Pad to Y			1.9		2.6	ns
t_{INGO}	Input Latch Gate-to-Output			4.0		5.3	ns
t_{INH}	Input Latch Hold		0.0		0.0		ns
t_{INSU}	Input Latch Setup		0.7		0.9		ns
t_{ILA}	Latch Active Pulse Width		6.1		8.1		ns
Input Module Predicted Routing Delays[1]							
t_{IRD1}	FO=1 Routing Delay			2.2		2.9	ns
t_{IRD2}	FO=2 Routing Delay			2.8		3.8	ns
t_{IRD3}	FO=3 Routing Delay			3.5		4.7	ns
t_{IRD4}	FO=4 Routing Delay			3.5		4.7	ns
t_{IRD8}	FO=8 Routing Delay			5.6		7.5	ns
Global Clock Network							
t_{CKH}	Input Low to High	FO=32 FO=635		6.5 7.9		8.7 10.6	ns ns
t_{CKL}	Input High to Low	FO=32 FO=635		6.6 8.8		8.8 11.8	ns ns
t_{PWH}	Minimum Pulse Width High	FO=32 FO=635	4.1 4.6		5.5 6.1		ns ns
t_{PWL}	Minimum Pulse Width Low	FO=32 FO=635	4.1 4.6		5.5 6.1		ns ns
t_{CKSW}	Maximum Skew	FO=32 FO=635		1.8 1.8		2.4 2.4	ns ns
t_{SUEXT}	Input Latch External Setup	FO=32 FO=635	0.0 0.0		0.0 0.0		ns ns
t_{HEXT}	Input Latch External Hold	FO=32 FO=635	3.0 3.8		4.0 5.1		ns ns
t_P	Minimum Period (1/fmax)	FO=32 FO=635	7.1 7.9		9.5 10.5		ns ns
f_{HMAX}	Maximum Datapath Frequency	FO=32 FO=635		140 126		105 95	MHz MHz

Note:

1. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment. Optimization techniques may further reduce delays by 0 to 4 ns.

A32200DX Timing Characteristics (continued)

(Worst-Case Military Conditions, V_{CC} = 4.5V, T_J = 125°C)

			‘–1’ Speed		‘Std’ Speed		
Parameter	**Description**		**Min.**	**Max.**	**Min.**	**Max.**	**Units**
Input Module Propagation Delays							
t_{INPY}	Input Data Pad to Y			1.9		2.6	ns
t_{INGO}	Input Latch Gate-to-Output			4.6		6.0	ns
t_{INH}	Input Latch Hold		0.0		0.0		ns
t_{INSU}	Input Latch Setup		0.7		0.9		ns
t_{ILA}	Latch Active Pulse Width		6.1		8.1		ns
Input Module Predicted Routing Delays[1]							
t_{IRD1}	FO=1 Routing Delay			2.6		3.5	ns
t_{IRD2}	FO=2 Routing Delay			3.4		4.6	ns
t_{IRD3}	FO=3 Routing Delay			4.6		6.1	ns
t_{IRD4}	FO=4 Routing Delay			5.4		7.2	ns
t_{IRD5}	FO=8 Routing Delay			7.0		9.3	ns
Global Clock Network							
t_{CKH}	Input Low to High	FO=32		7.3		9.8	ns
		FO=635		8.5		11.3	ns
t_{CKL}	Input High to Low	FO=32		7.2		9.6	ns
		FO=635		9.3		12.5	ns
t_{PWH}	Minimum Pulse Width High	FO=32	3.2		4.3		ns
		FO=635	3.9		5.2		ns
t_{PWL}	Minimum Pulse Width Low	FO=32	3.2		4.3		ns
		FO=635	3.9		5.2		ns
t_{CKSW}	Maximum Skew	FO=32		1.8		2.4	ns
		FO=635		1.8		2.4	ns
t_{SUEXT}	Input Latch External Setup	FO=32	0.0		0.0		ns
		FO=635	0.0		0.0		ns
t_{HEXT}	Input Latch External Hold	FO=32	3.0		4.0		ns
		FO=635	3.8		5.1		ns
t_P	Minimum Period (1/fmax)	FO=32	5.8		7.7		ns
		FO=635	6.8		9.1		ns
f_{HMAX}	Maximum Datapath Frequency	FO=32		172		130	MHz
		FO=635		147		110	MHz

Note:

1. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment. Optimization techniques may further reduce delays by 0 to 4 ns.

Pin Description

CLK Clock (Input)

ACT 1 only. TTL Clock input for global clock distribution network. The Clock input is buffered prior to clocking the logic modules. This pin can also be used as an I/O.

CLKA Clock A (Input)

ACT 2, 1200XL, 3200DX, and ACT 3 only. TTL Clock input for global clock distribution networks. The Clock input is buffered prior to clocking the logic modules. This pin can also be used as an I/O.

CLKB Clock B (Input)

ACT 2, 1200XL, 3200DX, and ACT 3 only. TTL Clock input for global clock distribution networks. The Clock input is buffered prior to clocking the logic modules. This pin can also be used as an I/O.

DCLK Diagnostic Clock (Input)

TTL Clock input for diagnostic probe and device programming. DCLK is active when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

GND Ground

LOW supply voltage.

HCLK Dedicated (Hard-wired) Array Clock (Input)

ACT 3 only. TTL Clock input for sequential modules. This input is directly wired to each S-module and offers clock speeds independent of the number of S-modules being driven. This pin can also be used as an I/O.

I/O Input/Output (Input, Output)

I/O pin functions as an input, output, tristate, or bi-directional buffer. Input and output levels are compatible with standard TTL and CMOS specifications. In the ACT 3 and 3200DX families, unused I/Os are automatically tri-stated. With this configuration, the input buffer internal to the I/O module is disabled. In the ACT 1, ACT 2 and 1200XL families, unused I/Os are automatically configured as bi-directional buffers where each buffer is configured as a LOW driver.

IOCLK Dedicated (Hard-wired) I/O Clock (Input)

ACT 3 only. TTL Clock input for I/O modules. This input is directly wired to each I/O module and offers clock speeds independent of the number of I/O modules being driven. This pin can also be used as an I/O.

IOPCL Dedicated (Hard-wired) I/O Preset/Clear (Input)

ACT 3 only. TTL input for I/O preset or clear. This global input is directly wired to the preset and clear inputs of all I/O registers. This pin functions as an I/O when no I/O preset or clear macros are used.

MODE Mode (Input)

The MODE pin controls the use of diagnostic pins (DCLK, PRA, PRB, SDI). When the MODE pin is HIGH, the special functions are active. When the MODE pin is LOW, the pins function as I/Os. To provide debugging capability, the MODE pin should be terminated to GND through a 10 kΩ resistor so that the MODE pin can be pulled high when required.

NC No Connection

This pin is not connected to circuitry within the device.

PRA, I/O Probe A (Output)

The Probe A pin is used to output data from any user-defined design node within the device. This independent diagnostic pin can be used in conjunction with the Probe B pin to allow real-time diagnostic output of any signal path within the device. The Probe A pin can be used as a user-defined I/O when debugging has been completed. The pin's probe capabilities can be permanently disabled to protect programmed design confidentiality. PRA is accessible when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

PRB, I/O Probe B (Output)

The Probe B pin is used to output data from any user-defined design node within the device. This independent diagnostic pin can be used in conjunction with the Probe A pin to allow real-time diagnostic output of any signal path within the device. The Probe B pin can be used as a user-defined I/O when verification has been completed. The pin's probe capabilities can be permanently disabled to protect programmed design confidentiality. PRB is accessible when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

SDI Serial Data Input (Input)

Serial data input for diagnostic probe and device programming. SDI is active when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

V_{CC} 5.0V Supply Voltage

HIGH supply voltage.

QCLKA/B,C,D Quadrant Clock (Input/Output)

3200DX only. These four pins are the quadrant clock inputs. When not used as a register control signal, these pins can function as general purpose I/O.

TCK Test Clock

Clock signal to shift the JTAG data into the device. This pin functions as an I/O when the JTAG fuse is not programmed. JTAG pins are only available in the 3200DX device.

133-Pin CPGA

Pin Number	A1425A Function
A1	NC
A2	GND
A3	I/O
A4	I/O
A5	I/O
A6	PRA, I/O
A7	NC
A8	I/O
A9	I/O
A10	I/O
A11	I/O
A12	I/O
A13	NC
B1	I/O
B2	V_{CC}
B3	I/O
B4	I/O
B5	I/O
B6	CLKB, I/O
B7	V_{CC}
B8	I/O
B9	I/O
B10	I/O
B11	I/O
B12	V_{CC}
B13	I/O
C1	I/O
C2	SDI, I/O
C3	GND
C4	I/O
C5	I/O
C6	I/O
C7	GND
C8	I/O
C9	I/O
C10	IOCLK, I/O
C11	GND
C12	GND
C13	I/O
D1	I/O
D2	I/O
D3	I/O
D4	DCLK, I/O
D6	CLKA, I/O
D7	I/O
D8	I/O
D11	I/O
D12	I/O
D13	I/O
E1	I/O
E2	I/O
E3	MODE
E11	V_{CC}
E12	I/O
E13	I/O
F1	I/O
F2	I/O
F3	I/O
F4	I/O
F10	GND
F11	I/O
F12	I/O
F13	I/O
G1	NC
G2	V_{CC}
G3	GND
G4	I/O
G10	I/O
G11	GND
G12	V_{CC}
G13	NC
H1	I/O
H2	I/O
H3	I/O
H4	I/O
H10	I/O
H11	I/O
H12	I/O
H13	I/O
J1	I/O
J2	V_{CC}
J3	I/O
J11	I/O
J12	V_{CC}
J13	I/O
K1	I/O
K2	I/O
K3	I/O
K6	I/O
K7	HCLKA, I/O
K8	I/O
K11	I/O
K12	I/O
K13	I/O
L1	I/O
L2	I/O
L3	GND
L4	I/O
L5	I/O
L6	PRB, I/O
L7	GND
L8	I/O
L9	I/O
L10	IOPCL, I/O
L11	GND
L12	I/O
L13	I/O
M1	I/O
M2	V_{CC}
M3	GND
M4	I/O
M5	I/O
M6	I/O
M7	V_{CC}
M8	I/O
M9	I/O
M10	I/O
M11	I/O
M12	V_{CC}
M13	I/O
N1	NC
N2	I/O
N3	I/O
N4	I/O
N5	I/O
N6	I/O
N7	NC
N8	I/O
N9	I/O
N10	I/O
N11	I/O
N12	GND
N13	NC

176-Pin CPGA (Continued)

Pin Number	A1280A Function	A1280XL Function
H12	GND	GND
H13	V_{CC}	V_{CC}
H14	V_{CC}	V_{CC}
H15	I/O	I/O
J1	I/O	I/O
J2	I/O	I/O
J3	I/O	I/O
J4	V_{CC}	V_{CC}
J12	GND	GND
J13	GND	GND
J14	V_{CC}	V_{CC}
J15	I/O	I/O
K1	I/O	I/O
K2	I/O	I/O
K3	I/O	I/O
K4	GND	GND
K12	GND	GND
K13	I/O	I/O
K14	I/O	I/O
K15	I/O	I/O
L1	I/O	I/O
L2	I/O	I/O
L3	I/O	I/O
L4	GND	GND
L12	I/O	I/O
L13	I/O	I/O
L14	I/O	I/O
L15	I/O	I/O
M1	I/O	I/O
M2	I/O	I/O
M3	I/O	I/O
M4	GND	GND
M5	V_{CC}	V_{CC}
M6	GND	GND
M7	I/O	I/O
M8	GND	GND
M9	I/O	I/O
M10	GND	GND
M11	V_{CC}	V_{CC}
M12	GND	GND
M13	I/O	I/O
M14	I/O	I/O
M15	I/O	I/O
N1	I/O	I/O

Pin Number	A1280A Function	A1280XL Function
N2	I/O	I/O
N3	I/O	I/O
N4	I/O	I/O
N5	I/O	I/O
N6	I/O	I/O
N7	I/O	I/O
N8	V_{CC}	V_{CC}
N9	I/O	I/O
N10	I/O	I/O
N11	I/O	I/O
N12	I/O	I/O
N13	I/O	I/O
N14	I/O	I/O
N15	I/O	I/O
P1	I/O	I/O
P2	I/O	I/O
P3	I/O	I/O
P4	I/O	I/O
P5	I/O	I/O
P6	I/O	I/O
P7	I/O	I/O
P8	I/O	I/O
P9	I/O	I/O
P10	I/O	I/O
P11	I/O	I/O
P12	I/O	I/O
P13	I/O	I/O
P14	I/O	I/O
P15	I/O	I/O
R1	I/O	I/O
R2	I/O	I/O
R3	I/O	I/O
R4	I/O	I/O
R5	I/O	I/O
R6	I/O	I/O
R7	I/O	I/O
R8	I/O	I/O
R9	I/O	I/O
R10	I/O	I/O
R11	I/O	I/O
R12	I/O	I/O
R13	I/O	I/O
R14	I/O	I/O
R15	I/O	I/O

257-Pin CPGA

Pin Number	A14100A Function
A1	I/O
A2	I/O
A3	I/O
A4	I/O
A5	MODE
A6	I/O
A7	I/O
A8	I/O
A9	I/O
A10	I/O
A11	I/O
A12	I/O
A13	I/O
A14	I/O
A15	I/O
A16	I/O
A17	I/O
A18	I/O
A19	I/O
B1	I/O
B2	I/O
B3	I/O
B4	SDI, I/O
B5	I/O
B6	I/O
B7	I/O
B8	I/O
B9	I/O
B10	I/O
B11	I/O
B12	I/O
B13	I/O
B14	I/O
B15	I/O
B16	GND
B17	I/O
B18	I/O
B19	I/O
C1	I/O
C2	I/O
C3	V_{CC}
C4	GND
C5	I/O
C6	I/O

Pin Number	A14100A Function
C7	I/O
C8	I/O
C9	I/O
C10	V_{CC}
C11	I/O
C12	I/O
C13	V_{CC}
C14	I/O
C15	I/O
C16	I/O
C17	V_{CC}
C18	I/O
C19	I/O
D1	I/O
D2	I/O
D3	I/O
D4	GND
D5	I/O
D6	I/O
D7	I/O
D8	I/O
D9	I/O
D10	GND
D11	I/O
D12	I/O
D13	I/O
D14	I/O
D15	I/O
D16	GND
D17	I/O
D18	I/O
D19	I/O
E1	I/O
E2	I/O
E3	I/O
E4	DCLK, I/O
E5	NC
E7	I/O
E9	I/O
E11	GND
E13	I/O
E16	I/O
E17	I/O
E18	I/O

Pin Number	A14100A Function
E19	I/O
F1	I/O
F2	I/O
F3	I/O
F4	I/O
F16	I/O
F17	I/O
F18	I/O
F19	I/O
G1	I/O
G2	I/O
G3	I/O
G4	I/O
G5	I/O
G15	I/O
G16	I/O
G17	I/O
G18	I/O
G19	I/O
H1	I/O
H2	I/O
H3	I/O
H4	I/O
H16	I/O
H17	I/O
H18	I/O
H19	I/O
J1	PRA, I/O
J2	I/O
J3	I/O
J4	I/O
J5	GND
J15	I/O
J16	HCLK, I/O
J17	PRB, I/O
J18	I/O
J19	I/O
K1	I/O
K2	I/O
K3	V_{CC}
K4	GND
K16	GND
K17	V_{CC}
K18	I/O

208-Pin CQFP

Pin Number	A32100DX Function
1	GND
2	V_{CC}
3	MODE
4	I/O
5	I/O
6	I/O
7	I/O
8	I/O
9	I/O
10	I/O
11	I/O
12	I/O
13	I/O
14	I/O
15	I/O
16	I/O
17	V_{CC}
18	I/O
19	I/O
20	I/O
21	I/O
22	GND
23	I/O
24	I/O
25	I/O
26	I/O
27	GND
28	V_{CC}
29	V_{CC}
30	I/O
31	I/O
32	V_{CC}
33	I/O
34	I/O
35	I/O
36	I/O
37	I/O
38	I/O
39	I/O
40	I/O
41	I/O
42	I/O
43	I/O

Pin Number	A32100DX Function
44	I/O
45	I/O
46	I/O
47	I/O
48	I/O
49	I/O
50	I/O
51	I/O
52	GND
53	GND
54	TMS, I/O
55	TDI, I/O
56	I/O
57	I/O (WD)
58	I/O (WD)
59	I/O
60	V_{CC}
61	I/O
62	I/O
63	I/O
64	I/O
65	QCLKA, I/O
66	I/O (WD)
67	I/O (WD)
68	I/O
69	I/O
70	I/O (WD)
71	I/O (WD)
72	I/O
73	I/O
74	I/O
75	I/O
76	I/O
77	I/O
78	GND
79	V_{CC}
80	V_{CC}
81	I/O
82	I/O
83	I/O
84	I/O
85	I/O (WD)
86	I/O (WD)

Pin Number	A32100DX Function
87	I/O
88	I/O
89	I/O
90	I/O
91	QCLKB, I/O
92	I/O
93	I/O (WD)
94	I/O (WD)
95	I/O
96	I/O
97	I/O
98	V_{CC}
99	I/O
100	I/O (WD)
101	I/O (WD)
102	I/O
103	SDO, I/O
104	I/O
105	GND
106	V_{CC}
107	I/O
108	I/O
109	I/O
110	I/O
111	I/O
112	I/O
113	I/O
114	I/O
115	I/O
116	I/O
117	I/O
118	I/O
119	I/O
120	I/O
121	I/O
122	I/O
123	I/O
124	I/O
125	I/O
126	GND
127	I/O
128	TCK, I/O
129	GND

208-Pin CQFP (Continued)

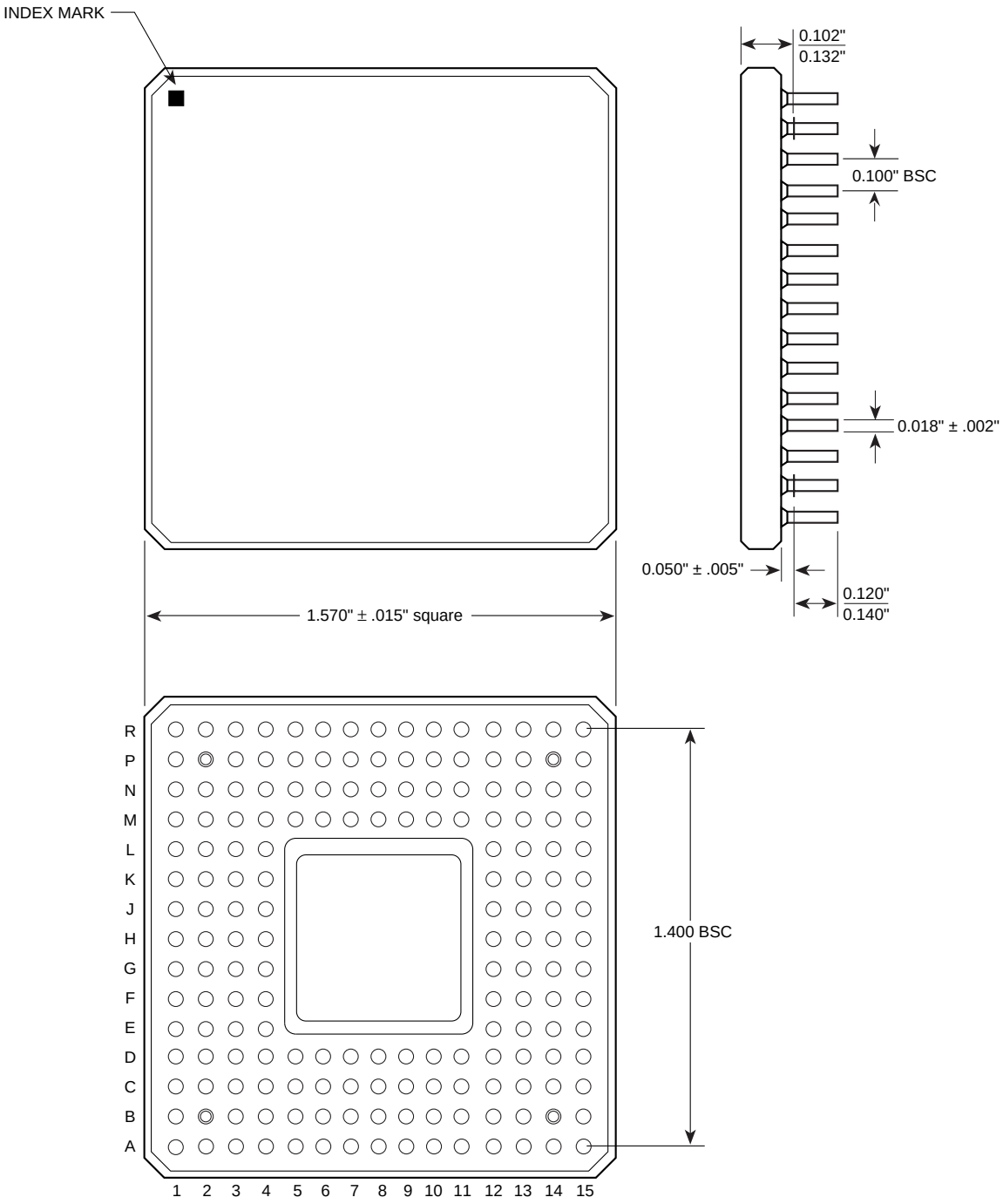
Pin Number	A32100DX Function
130	V_{CC}
131	GND
132	V_{CC}
133	V_{CC}
134	I/O
135	I/O
136	V_{CC}
137	I/O
138	I/O
139	I/O
140	I/O
141	I/O
142	I/O
143	I/O
144	I/O
145	I/O
146	I/O
147	I/O
148	I/O
149	I/O
150	GND
151	I/O
152	I/O
153	I/O
154	I/O
155	I/O
156	I/O

Pin Number	A32100DX Function
157	GND
158	I/O
159	SDI, I/O
160	I/O
161	I/O (WD)
162	I/O (WD)
163	I/O
164	V_{CC}
165	I/O
166	I/O
167	I/O
168	I/O (WD)
169	I/O (WD)
170	I/O
171	QCLKD, I/O
172	I/O
173	I/O
174	I/O
175	I/O
176	I/O (WD)
177	I/O (WD)
178	PRA, I/O
179	I/O
180	CLKA, I/O
181	I/O
182	V_{CC}
183	V_{CC}

Pin Number	A32100DX Function
184	GND
185	I/O
186	CLKB, I/O
187	I/O
188	PRB, I/O
189	I/O
190	I/O (WD)
191	I/O (WD)
192	I/O
193	I/O
194	I/O (WD)
195	I/O (WD)
196	QCLKC, I/O
197	I/O
198	I/O
199	I/O
200	I/O
201	I/O
202	V_{CC}
203	I/O (WD)
204	I/O (WD)
205	I/O
206	I/O
207	DCLK, I/O
208	I/O

Package Mechanical Drawings (continued)

176-Pin CPGA



Notes:

1. *All dimensions are in inches unless otherwise stated.*
2. *BSC—Basic Spacing between Centers. This is a theoretical true position dimension and so has no tolerance.*