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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	547
Number of Logic Elements/Cells	-
Total RAM Bits	-
Number of I/O	69
Number of Gates	2000
Voltage - Supply	4.5V ~ 5.5V
Mounting Type	Through Hole
Operating Temperature	-55°C ~ 125°C (TJ)
Package / Case	84-BCPGA
Supplier Device Package	84-CPGA (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/microsemi/a1020b-1pg84b

unique architecture offers gate array flexibility, high performance, and quick turnaround through user programming. Device utilization is typically 95 percent of available logic modules. All Actel devices include on-chip clock drivers and a hard-wired distribution network.

User-definable I/Os are capable of driving at both TTL and CMOS drive levels. Available packages for the military are the Ceramic Quad Flat Pack (CQFP) and the Ceramic Pin Grid Array (CPGA). See the "Product Plan" section on page 6 for details.

QML Certification

Actel has achieved full QML certification, demonstrating that quality management, procedures, processes, and controls are in place and comply with MIL-PRF-38535, the performance specification used by the Department of Defense for monolithic integrated circuits. QML certification is a good example of Actel's commitment to supplying the highest quality products for all types of high-reliability, military and space applications.

Many suppliers of microelectronics components have implemented QML as their primary worldwide business system. Appropriate use of this system not only helps in the implementation of advanced technologies, but also allows for a quality, reliable and cost-effective logistics support throughout QML products' life cycles.

Development Tool Support

The HiRel devices are fully supported by Actel's line of FPGA development tools, including the Actel DeskTOP series and Designer Advantage tools. The Actel DeskTOP Series is an integrated design environment for PCs that includes design entry, simulation, synthesis, and place and route tools. Designer Advantage is Actel's suite of FPGA development point tools for PCs and Workstations that includes the ACTgen Macro Builder, Designer with DirectTime timing driven place and route and analysis tools, and device programming software.

In addition, the HiRel devices contain ActionProbe circuitry that provides built-in access to every node in a design, enabling 100 percent real-time observation and analysis of a device's internal logic nodes without design iteration. The probe circuitry is accessed by Silicon Explorer, an easy to use integrated verification and logic analysis tool that can sample data at 100 MHz (asynchronous) or 66 MHz (synchronous). Silicon Explorer attaches to a PC's standard COM port, turning the PC into a fully functional 18 channel logic analyzer. Silicon Explorer allows designers to complete the design verification process at their desks and reduces verification time from several hours per cycle to a few seconds.

ACT 3 Description

The ACT 3 family is the third-generation Actel FPGA family. This family offers the highest-performance and highest-capacity devices, ranging from 2,500 to 10,000 gates, with system performance up to 60 MHz over the military temperature range. The devices have four clock distribution networks, including dedicated array and I/O clocks. In addition, the ACT 3 family offers the highest I/O-to-gate ratio available. ACT 3 devices are manufactured using 0.8µ CMOS technology.

1200XL/3200DX Description

3200DX and 1200XL FPGAs were designed to integrate system logic which is typically implemented in multiple CPLDs, PALs, and FPGAs. These devices provide the features and performance required for today's complex, high-speed digital logic systems. The 3200DX family offers the industry's fastest dual-port SRAM for implementing fast FIFOs, LIFOs, and temporary data storage.

ACT 2 Description

The ACT 2 family is the second-generation Actel FPGA family. This family offers the best-value, high-capacity devices, ranging from 4,000 to 8,000 gates, with system performance up to 40 MHz over the military temperature range. The devices have two routed array clock distribution networks. ACT 2 devices are manufactured using 1.0µ CMOS technology.

ACT 1 Description

The ACT 1 family is the first Actel FPGA family and the first antifuse-based FPGA. This family offers the lowest-cost logic integration, with devices ranging from 1,200 to 2,000 gates, with system performance up to 20 MHz over the military temperature range. The devices have one routed array clock distribution network. ACT 1 devices are manufactured using 1.0µ CMOS technology.

DESC SMD/Actel Part Number Cross Reference

Actel Part Number (Gold Leads)	DSCC SMD (Gold Leads)	DSCC SMD (Solder Dipped)
A1010B-PG84B	5962-9096403MXC	5962-9096403MXA
A1010B-1PG84B	5962-9096404MXC	5962-9096404MXA
A1020B-PG84B	5962-9096503MUC	5962-9096503MUA
A1020B-1PG84B	5962-9096504MUC	5962-9096504MUA
A1020B-CQ84B	5962-9096503MTC	5962-9096503MTA
A1020B-1CQ84B	5962-9096504MTC	5962-9096504MTA
A1240A-PG132B	5962-9322101MXC	5962-9322101MXA
A1240A-1PG132B	5962-9322102MXC	5962-9322102MXA
A1280A-PG176B	5962-9215601MXC	5962-9215601MXA
A1280A-1PG176B	5962-9215602MXC	5962-9215602MXA
A1280A-CQ172B	5962-9215601MYC	5962-9215601MYA
A1280A-1CQ172B	5962-9215602MYC	5962-9215602MYA
A1425A-PG133B	5962-9552001MXC	N/A
A1425A-1PG133B	5962-9552002MXC	N/A
A1425A-CQ132B	5962-9552001MYC	N/A
A1425A-1CQ132B	5962-9552002MYC	N/A
A1460A-PG207B	5962-9550801MXC	N/A
A1460A-1PG207B	5962-9550802MXC	N/A
A1460A-CQ196B	5962-9550801MYC	N/A
A1460A-1CQ196B	5962-9550802MYC	N/A
A14100A-PG257B	5962-9552101MXC	N/A
A14100A-1PG257B	5962-9552102MXC	N/A
A14100A-CQ256B	5962-9552101MYC	N/A
A14100A-1CQ256B	5962-9552102MYC	N/A
A32100DX-CQ84B	5962-9875901QXC	N/A
A32100DX-1CQ84B	5962-9857902QXC	N/A
A32200DX-CQ256B	5962-9952701QXC	N/A
A32200DX-1CQ256B	5962-9952702QXC	N/A
A32200DX-CQ208B	5962-9952701QYC	N/A
A32200DX-1CQ208B	5962-9952702QYC	N/A

Package Thermal Characteristics

The device junction to case thermal characteristic is θ_{jc}, and the junction to ambient air characteristic is θ_{ja}. The thermal characteristics for θ_{ja} are shown with two different air flow rates.

Maximum junction temperature is 150°C.

A sample calculation of the absolute maximum power dissipation allowed for a CPGA 176-pin package at military temperature is as follows:

$$\frac{\text{Max. junction temp. (°C)} - \text{Max. military temp.}}{\theta_{ja}\ (°C/W)} = \frac{150°C - 125°C}{23°C/W} = 1.1\ W$$

Package Type	Pin Count	θ_{jc}	θ_{ja} Still Air	θ_{ja} 300 ft/min	Units
Ceramic Pin Grid Array	84	6.0	33	20	°C/W
	132	4.8	25	16	°C/W
	133	4.8	25	15	°C/W
	176	4.6	23	12	°C/W
	207	3.5	21	10	°C/W
	257	2.8	15	8	°C/W
Ceramic Quad Flat Pack	84	7.8	40	30	°C/W
	132	7.2	35	25	°C/W
	172	6.8	25	20	°C/W
	196	6.4	23	15	°C/W
	256	6.2	20	10	°C/W

Power Dissipation

General Power Equation

$$P = [I_{CC}standby + I_{CC}active] * V_{CC} + I_{OL} * V_{OL} * N + I_{OH} * (V_{CC} - V_{OH}) * M$$

where:

$I_{CC}standby$ is the current flowing when no inputs or outputs are changing.

$I_{CC}active$ is the current flowing due to CMOS switching.

I_{OL}, I_{OH} are TTL sink/source currents.

V_{OL}, V_{OH} are TTL level output voltages.

N equals the number of outputs driving TTL loads to V_{OL}.

M equals the number of outputs driving TTL loads to V_{OH}.

Accurate values for N and M are difficult to determine because they depend on the family type, on the design, and on the system I/O. The power can be divided into two components—static and active.

Static Power Component

Actel FPGAs have small static power components that result in power dissipation lower than that of PALs or PLDs. By integrating multiple PALs or PLDs into one FPGA, an even greater reduction in board-level power dissipation can be achieved.

The power due to standby current is typically a small component of the overall power. Standby power is calculated below for commercial, worst-case conditions.

Family	I_{CC}	V_{CC}	Power
ACT 3	2 mA	5.25V	10.5 mW
1200XL/3200DX	2 mA	5.25V	10.5 mW
ACT 2	2 mA	5.25V	10.5 mW
ACT 1	3 mA	5.25V	15.8 mW

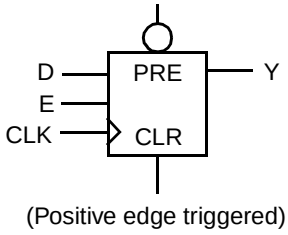
The static power dissipated by TTL loads depends on the number of outputs driving high or low and the DC load current. Again, this value is typically small. For instance, a 32-bit bus sinking 4 mA at 0.33V will generate 42 mW with all outputs driving low, and 140 mW with all outputs driving high.

Active Power Component

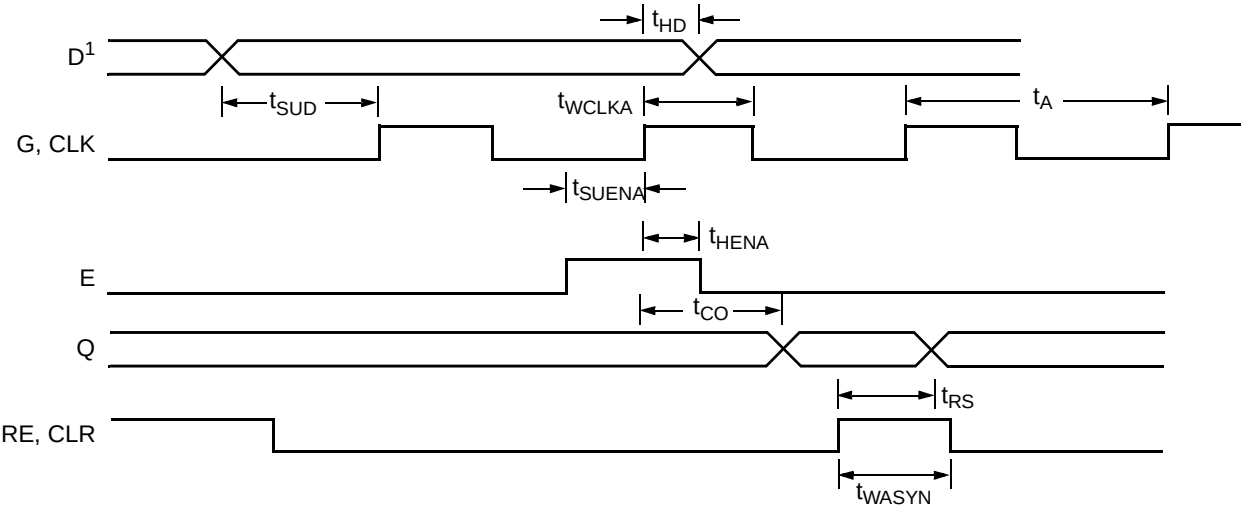
Power dissipation in CMOS devices is usually dominated by the active (dynamic) power dissipation. This component is frequency dependent, a function of the logic and the external I/O. Active power dissipation results from charging internal chip capacitances of the interconnect, unprogrammed antifuses, module inputs, and module outputs, plus external capacitance due to PC board traces and load device inputs. An additional component of the active power dissipation is the totempole current in CMOS transistor pairs. The net effect can be associated with an equivalent capacitance that

Sequential Timing Characteristics (continued)

Flip-Flops and Latches (1200XL/3200DX, ACT 2, and ACT 1)



(Positive edge triggered)

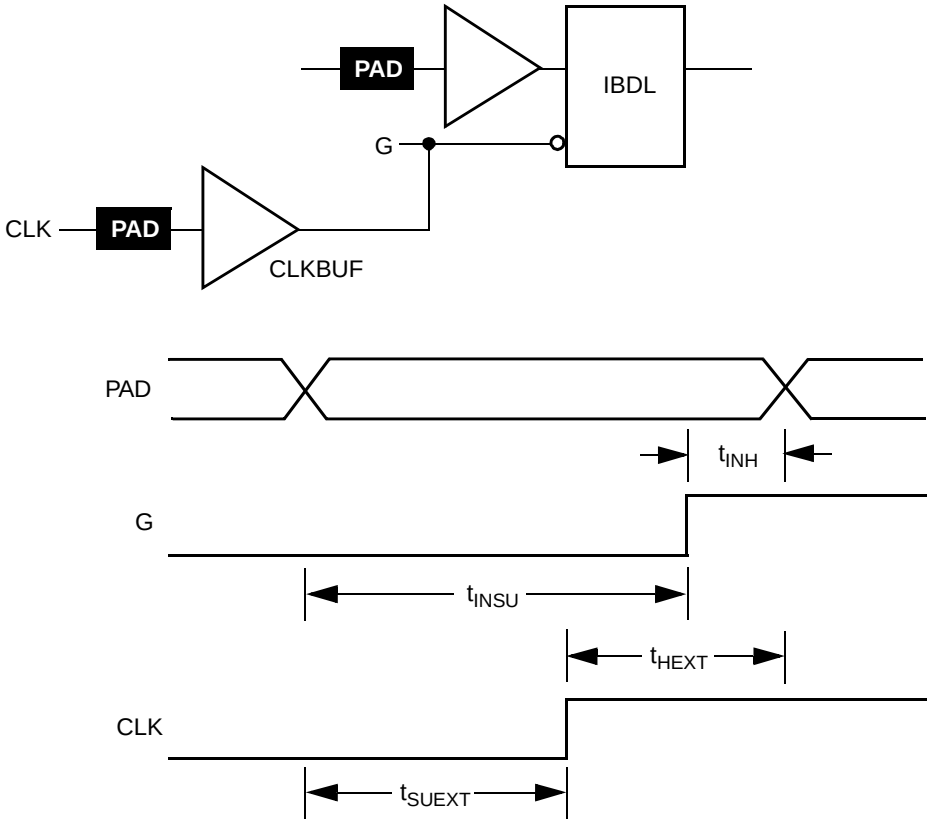


Note:

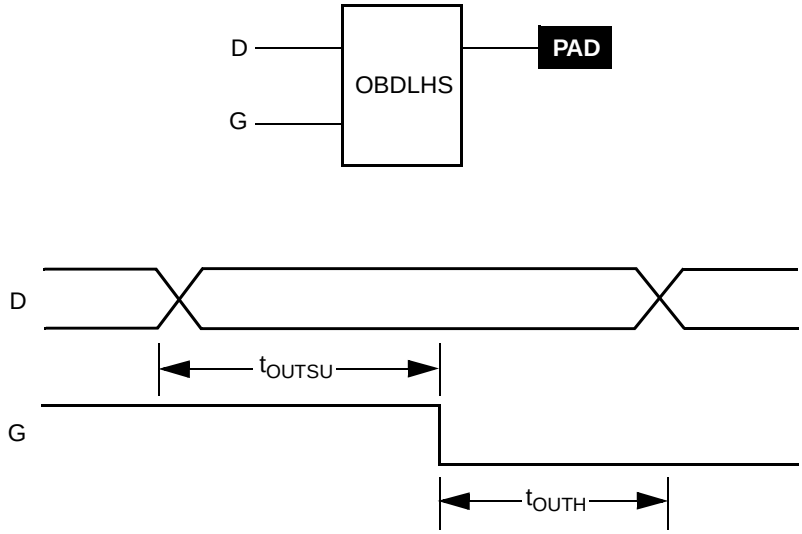
1. *D represents all data functions involving A, B, and S for multiplexed flip-flops.*

Sequential Timing Characteristics (continued)

Input Buffer Latches (ACT 2 and 1200XL/3200DX)

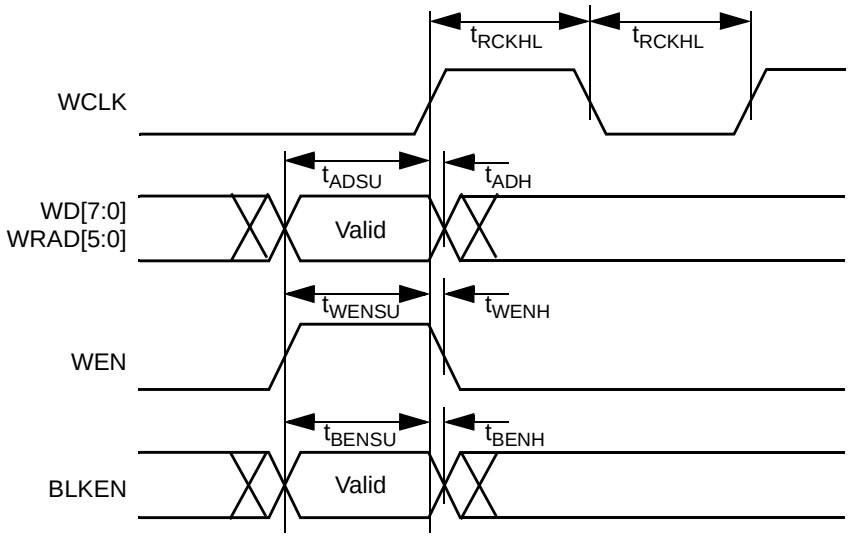


Output Buffer Latches (ACT 2 and 1200XL/3200DX)



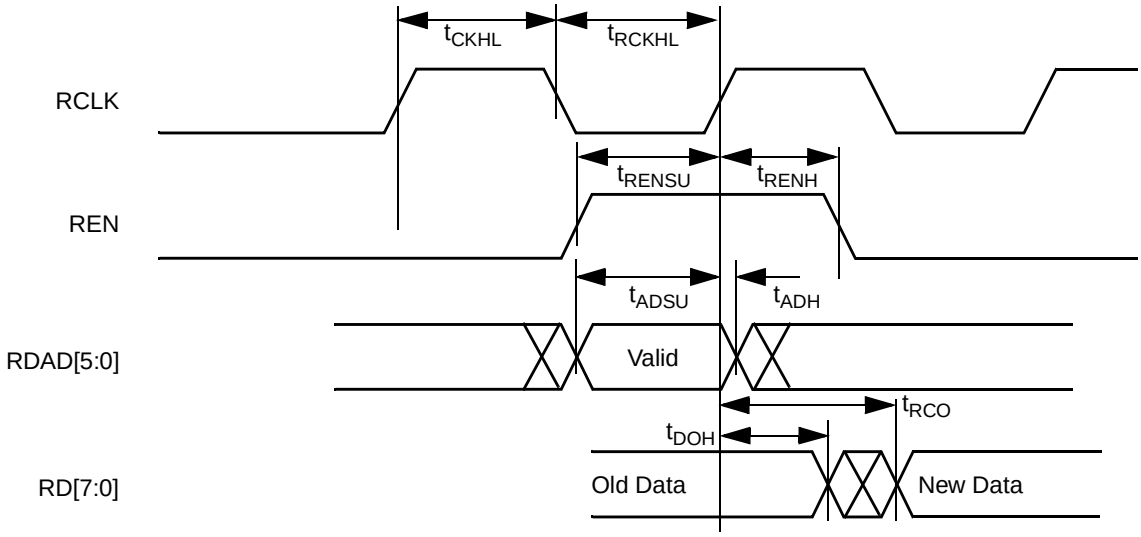
Dual-Port SRAM Timing Waveforms

3200DX SRAM Write Operation



Note: *Identical timing for falling-edge clock.*

3200DX SRAM Synchronous Read Operation



Note: *Identical timing for falling-edge clock.*

ACT 1 Timing Characteristics

(Worst-Case Military Conditions, V_{CC} = 4.5V, T_J = 125°C)

		'–1' Speed		'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
Logic Module Propagation Delays						
t_{PD1}	Single Module		4.7		5.5	ns
t_{PD2}	Dual Module Macros		10.8		12.7	ns
t_{CO}	Sequential Clk to Q		4.7		5.5	ns
t_{GO}	Latch G to Q		4.7		5.5	ns
t_{RS}	Flip-Flop (Latch) Reset to Q		4.7		5.5	ns
Logic Module Predicted Routing Delays[1]						
t_{RD1}	FO=1 Routing Delay		1.5		1.7	ns
t_{RD2}	FO=2 Routing Delay		2.3		2.7	ns
t_{RD3}	FO=3 Routing Delay		3.4		4.0	ns
t_{RD4}	FO=4 Routing Delay		5.0		5.9	ns
t_{RD8}	FO=8 Routing Delay		10.6		12.5	ns
Logic Module Sequential Timing [2]						
t_{SUD}	Flip-Flop (Latch) Data Input Setup	8.8		10.4		ns
t_{HD}	Flip-Flop (Latch) Data Input Hold	0.0		0.0		ns
t_{SUENA}	Flip-Flop (Latch) Enable Setup	8.8		10.4		ns
t_{HENA}	Flip-Flop (Latch) Enable Hold	0.0		0.0		ns
t_{WCLKA}	Flip-Flop (Latch) Clock Active Pulse Width	10.9		12.9		ns
t_{WASYN}	Flip-Flop (Latch) Asynchronous Pulse Width	10.9		12.9		ns
t_A	Flip-Flop Clock Input Period	23.2		27.3		ns
f_{MAX}	Flip-Flop (Latch) Clock Frequency		44		37	MHz
Input Module Propagation Delays						
t_{INYH}	Pad to Y High		4.9		5.8	ns
t_{INYL}	Pad to Y Low		4.9		5.8	ns
Input Module Predicted Routing Delays[1, 3]						
t_{IRD1}	FO=1 Routing Delay		1.5		1.7	ns
t_{IRD2}	FO=2 Routing Delay		2.3		2.7	ns
t_{IRD3}	FO=3 Routing Delay		3.4		4.0	ns
t_{IRD4}	FO=4 Routing Delay		5.0		5.9	ns
t_{IRD8}	FO=8 Routing Delay		10.6		12.5	ns

Notes:

1. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*
2. *Setup times assume fanout of 3. Further derating information can be obtained from the DirectTime Analyzer utility.*
3. *Optimization techniques may further reduce delays by 0 to 4 ns.*

A1240A Timing Characteristics

(Worst-Case Military Conditions, V_{CC} = 4.5V, T_J = 125°C)

		'–1' Speed		'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
Logic Module Propagation Delays[1]						
t_{PD1}	Single Module		5.2		6.1	ns
t_{CO}	Sequential Clk to Q		5.2		6.1	ns
t_{GO}	Latch G to Q		5.2		6.1	ns
t_{RS}	Flip-Flop (Latch) Reset to Q		5.2		6.1	ns
Logic Module Predicted Routing Delays[2]						
t_{RD1}	FO=1 Routing Delay		1.9		2.2	ns
t_{RD2}	FO=2 Routing Delay		2.4		2.8	ns
t_{RD3}	FO=3 Routing Delay		3.1		3.7	ns
t_{RD4}	FO=4 Routing Delay		4.3		5.0	ns
t_{RD8}	FO=8 Routing Delay		6.6		7.7	ns
Logic Module Sequential Timing[3, 4]						
t_{SUD}	Flip-Flop (Latch) Data Input Setup	0.5		0.5		ns
t_{HD}	Flip-Flop (Latch) Data Input Hold	0.0		0.0		ns
t_{SUENA}	Flip-Flop (Latch) Enable Setup	1.3		1.3		ns
t_{HENA}	Flip-Flop (Latch) Enable Hold	0.0		0.0		ns
t_{WCLKA}	Flip-Flop (Latch) Clock Active Pulse Width	7.4		8.1		ns
t_{WASYN}	Flip-Flop (Latch) Asynchronous Pulse Width	7.4		8.1		ns
t_A	Flip-Flop Clock Input Period	14.8		18.6		ns
t_{INH}	Input Buffer Latch Hold	2.5		2.5		ns
t_{INSU}	Input Buffer Latch Setup	–3.5		–3.5		ns
t_{OUTH}	Output Buffer Latch Hold	0.0		0.0		ns
t_{OUTSU}	Output Buffer Latch Setup	0.5		0.5		ns
f_{MAX}	Flip-Flop (Latch) Clock Frequency		63		54	MHz

Notes:

1. *For dual-module macros, use $t_{PD1} + t_{RD1} + t_{PDn}$, $t_{CO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.*
2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*
3. *Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the DirectTime Analyzer utility.*
4. *Setup and hold timing parameters for the Input Buffer Latch are defined with respect to the PAD and the D input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.*

A32100DX Timing Characteristics

(Worst-Case Military Conditions, V_{CC} = 4.5V, T_J = 125°C)

		'–1' Speed		'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
Logic Module Combinatorial Functions						
t_{PD}	Internal Array Module Delay		3.1		4.1	ns
t_{PDD}	Internal Decode Module Delay		3.3		4.3	ns
Logic Module Predicted Routing Delays[1]						
t_{RD1}	FO=1 Routing Delay		1.3		1.8	ns
t_{RD2}	FO=2 Routing Delay		1.9		2.6	ns
t_{RD3}	FO=3 Routing Delay		2.6		3.4	ns
t_{RD4}	FO=4 Routing Delay		3.3		4.3	ns
t_{RD5}	FO=8 Routing Delay		0.6		0.8	ns
t_{RDD}	Decode-to-Output Routing Delay		0.5		0.6	ns
Logic Module Sequential Timing						
t_{CO}	Flip-Flop Clock-to-Output		3.1		4.1	ns
t_{GO}	Latch Gate-to-Output		3.1		4.1	ns
t_{SU}	Flip-Flop (Latch) Setup Time	0.5		0.6		ns
t_{H}	Flip-Flop (Latch) Hold Time	0.0		0.0		ns
t_{RO}	Flip-Flop (Latch) Reset to Output		3.1		4.1	ns
t_{SUENA}	Flip-Flop (Latch) Enable Setup	0.9		1.2		ns
t_{HENA}	Flip-Flop (Latch) Enable Hold	0.0		0.0		ns
t_{WCLKA}	Flip-Flop (Latch) Clock Active Pulse Width	4.3		5.8		ns
t_{WASYN}	Flip-Flop (Latch) Asynchronous Pulse Width	5.6		7.5		ns

Note:

1. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.

A32100DX Timing Characteristics (continued)

(Worst-Case Military Conditions, V_{CC} = 4.5V, T_J = 125°C)

		'–1' Speed		'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
Synchronous SRAM Operations						
t_{RC}	Read Cycle Time	8.8		11.8		ns
t_{WC}	Write Cycle Time	8.8		11.8		ns
t_{RCKHL}	Clock High/Low Time	4.4		5.9		ns
t_{RCO}	Data Valid After Clock High/Low		4.4		5.9	ns
t_{ADSU}	Address/Data Setup Time	2.1		2.8		ns
t_{ADH}	Address/Data Hold Time	0.0		0.0		ns
t_{RENSU}	Read Enable Setup	0.8		1.1		ns
t_{RENH}	Read Enable Hold	4.4		5.9		ns
t_{WENSU}	Write Enable Setup	3.5		4.7		ns
t_{WENH}	Write Enable Hold	0.0		0.0		ns
t_{BENS}	Block Enable Setup	3.6		4.8		ns
t_{BENH}	Block Enable Hold	0.0		0.0		ns
Asynchronous SRAM Operations						
t_{RPD}	Asynchronous Access Time		10.6		14.1	ns
t_{RDADV}	Read Address Valid	11.5		15.3		ns
t_{ADSU}	Address/Data Setup Time	2.1		2.8		ns
t_{ADH}	Address/Data Hold Time	0.0		0.0		ns
t_{RENSUA}	Read Enable Setup to Address Valid	0.8		1.1		ns
t_{RENHA}	Read Enable Hold	4.4		5.9		ns
t_{WENSU}	Write Enable Setup	3.5		4.7		ns
t_{WENH}	Write Enable Hold	0.0		0.0		ns
t_{DOH}	Data Out Hold Time		1.6		2.1	ns

A32200DX Timing Characteristics (continued)

(Worst-Case Military Conditions, V_{CC} = 4.5V, T_J = 125°C)

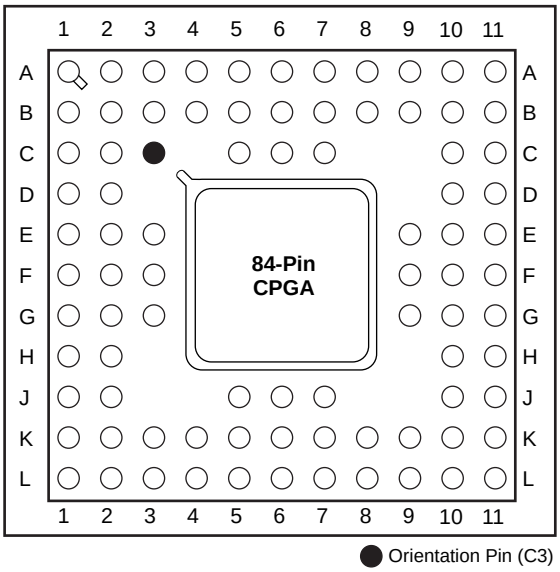
			‘–1’ Speed		‘Std’ Speed		
Parameter	**Description**		**Min.**	**Max.**	**Min.**	**Max.**	**Units**
Input Module Propagation Delays							
t_{INPY}	Input Data Pad to Y			1.9		2.6	ns
t_{INGO}	Input Latch Gate-to-Output			4.6		6.0	ns
t_{INH}	Input Latch Hold		0.0		0.0		ns
t_{INSU}	Input Latch Setup		0.7		0.9		ns
t_{ILA}	Latch Active Pulse Width		6.1		8.1		ns
Input Module Predicted Routing Delays[1]							
t_{IRD1}	FO=1 Routing Delay			2.6		3.5	ns
t_{IRD2}	FO=2 Routing Delay			3.4		4.6	ns
t_{IRD3}	FO=3 Routing Delay			4.6		6.1	ns
t_{IRD4}	FO=4 Routing Delay			5.4		7.2	ns
t_{IRD5}	FO=8 Routing Delay			7.0		9.3	ns
Global Clock Network							
t_{CKH}	Input Low to High	FO=32		7.3		9.8	ns
		FO=635		8.5		11.3	ns
t_{CKL}	Input High to Low	FO=32		7.2		9.6	ns
		FO=635		9.3		12.5	ns
t_{PWH}	Minimum Pulse Width High	FO=32	3.2		4.3		ns
		FO=635	3.9		5.2		ns
t_{PWL}	Minimum Pulse Width Low	FO=32	3.2		4.3		ns
		FO=635	3.9		5.2		ns
t_{CKSW}	Maximum Skew	FO=32		1.8		2.4	ns
		FO=635		1.8		2.4	ns
t_{SUEXT}	Input Latch External Setup	FO=32	0.0		0.0		ns
		FO=635	0.0		0.0		ns
t_{HEXT}	Input Latch External Hold	FO=32	3.0		4.0		ns
		FO=635	3.8		5.1		ns
t_P	Minimum Period (1/fmax)	FO=32	5.8		7.7		ns
		FO=635	6.8		9.1		ns
f_{HMAX}	Maximum Datapath Frequency	FO=32		172		130	MHz
		FO=635		147		110	MHz

Note:

1. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment. Optimization techniques may further reduce delays by 0 to 4 ns.

Package Pin Assignments

84-Pin CPGA (Top View)



133-Pin CPGA

Pin Number	A1425A Function
A1	NC
A2	GND
A3	I/O
A4	I/O
A5	I/O
A6	PRA, I/O
A7	NC
A8	I/O
A9	I/O
A10	I/O
A11	I/O
A12	I/O
A13	NC
B1	I/O
B2	V_{CC}
B3	I/O
B4	I/O
B5	I/O
B6	CLKB, I/O
B7	V_{CC}
B8	I/O
B9	I/O
B10	I/O
B11	I/O
B12	V_{CC}
B13	I/O
C1	I/O
C2	SDI, I/O
C3	GND
C4	I/O
C5	I/O
C6	I/O
C7	GND
C8	I/O
C9	I/O
C10	IOCLK, I/O
C11	GND
C12	GND
C13	I/O
D1	I/O
D2	I/O
D3	I/O
D4	DCLK, I/O
D6	CLKA, I/O
D7	I/O
D8	I/O
D11	I/O
D12	I/O
D13	I/O
E1	I/O
E2	I/O
E3	MODE
E11	V_{CC}
E12	I/O
E13	I/O
F1	I/O
F2	I/O
F3	I/O
F4	I/O
F10	GND
F11	I/O
F12	I/O
F13	I/O
G1	NC
G2	V_{CC}
G3	GND
G4	I/O
G10	I/O
G11	GND
G12	V_{CC}
G13	NC
H1	I/O
H2	I/O
H3	I/O
H4	I/O
H10	I/O
H11	I/O
H12	I/O
H13	I/O
J1	I/O
J2	V_{CC}
J3	I/O
J11	I/O
J12	V_{CC}
J13	I/O
K1	I/O
K2	I/O
K3	I/O
K6	I/O
K7	HCLKA, I/O
K8	I/O
K11	I/O
K12	I/O
K13	I/O
L1	I/O
L2	I/O
L3	GND
L4	I/O
L5	I/O
L6	PRB, I/O
L7	GND
L8	I/O
L9	I/O
L10	IOPCL, I/O
L11	GND
L12	I/O
L13	I/O
M1	I/O
M2	V_{CC}
M3	GND
M4	I/O
M5	I/O
M6	I/O
M7	V_{CC}
M8	I/O
M9	I/O
M10	I/O
M11	I/O
M12	V_{CC}
M13	I/O
N1	NC
N2	I/O
N3	I/O
N4	I/O
N5	I/O
N6	I/O
N7	NC
N8	I/O
N9	I/O
N10	I/O
N11	I/O
N12	GND
N13	NC

257-Pin CPGA (Continued)

Pin Number	A14100A Function
K19	I/O
L1	I/O
L2	I/O
L3	I/O
L4	CLKA, I/O
L5	CLKB, I/O
L15	GND
L16	I/O
L17	I/O
L18	I/O
L19	I/O
M1	I/O
M2	I/O
M3	I/O
M4	I/O
M16	I/O
M17	I/O
M18	I/O
M19	I/O
N1	I/O
N2	I/O
N3	I/O
N4	I/O
N5	I/O
N15	I/O
N16	I/O
N17	I/O
N18	I/O
N19	I/O
P1	I/O
P2	I/O
P3	I/O
P4	I/O
P16	I/O
P17	I/O
P18	I/O
P19	I/O
R1	I/O
R2	I/O
R3	I/O
R4	GND
R7	I/O

Pin Number	A14100A Function
R9	I/O
R11	I/O
R13	I/O
R16	IOPCL, I/O
R17	I/O
R18	I/O
R19	I/O
T1	I/O
T2	I/O
T3	I/O
T4	GND
T5	IOCLK, I/O
T6	I/O
T7	I/O
T8	I/O
T9	I/O
T10	GND
T11	I/O
T12	I/O
T13	I/O
T14	I/O
T15	I/O
T16	GND
T17	GND
T18	I/O
T19	I/O
V1	I/O
V2	I/O
V3	V_{CC}
V4	I/O
V5	I/O
V6	I/O
V7	V_{CC}
V8	I/O
V9	I/O
V10	V_{CC}
V11	I/O
V12	I/O
V13	I/O
V14	I/O
V15	I/O
V16	I/O

Pin Number	A14100A Function
V17	V_{CC}
V18	I/O
V19	I/O
X1	I/O
X2	I/O
X3	I/O
X4	I/O
X5	I/O
X6	I/O
X7	GND
X8	I/O
X9	I/O
X10	I/O
X11	I/O
X12	I/O
X13	I/O
X14	V_{CC}
X15	I/O
X16	I/O
X17	I/O
X18	I/O
X19	I/O
Y1	I/O
Y2	I/O
Y3	I/O
Y4	I/O
Y5	I/O
Y6	I/O
Y7	I/O
Y8	I/O
Y9	I/O
Y10	I/O
Y11	I/O
Y12	I/O
Y13	I/O
Y14	I/O
Y15	I/O
Y16	I/O
Y17	I/O
Y18	I/O
Y19	I/O

132-Pin CQFP

Pin Number	A1425A Function
1	NC
2	GND
3	SDI, I/O
4	I/O
5	I/O
6	I/O
7	I/O
8	I/O
9	MODE
10	GND
11	V_{CC}
12	I/O
13	I/O
14	I/O
15	I/O
16	I/O
17	I/O
18	I/O
19	I/O
20	I/O
21	I/O
22	V_{CC}
23	I/O
24	I/O
25	I/O
26	GND
27	V_{CC}
28	I/O
29	I/O
30	I/O
31	I/O
32	I/O
33	I/O
34	NC
35	I/O
36	GND
37	I/O
38	I/O
39	I/O
40	I/O
41	I/O
42	GND
43	V_{CC}
44	I/O

Pin Number	A1425A Function
45	I/O
46	I/O
47	I/O
48	PRB, I/O
49	I/O
50	HCLK, I/O
51	I/O
52	I/O
53	I/O
54	I/O
55	I/O
56	I/O
57	I/O
58	GND
59	V_{CC}
60	I/O
61	I/O
62	I/O
63	I/O
64	IOPCL, I/O
65	GND
66	NC
67	NC
68	I/O
69	I/O
70	I/O
71	I/O
72	I/O
73	I/O
74	GND
75	V_{CC}
76	I/O
77	I/O
78	V_{CC}
79	I/O
80	I/O
81	I/O
82	I/O
83	I/O
84	I/O
85	I/O
86	I/O
87	I/O
88	I/O

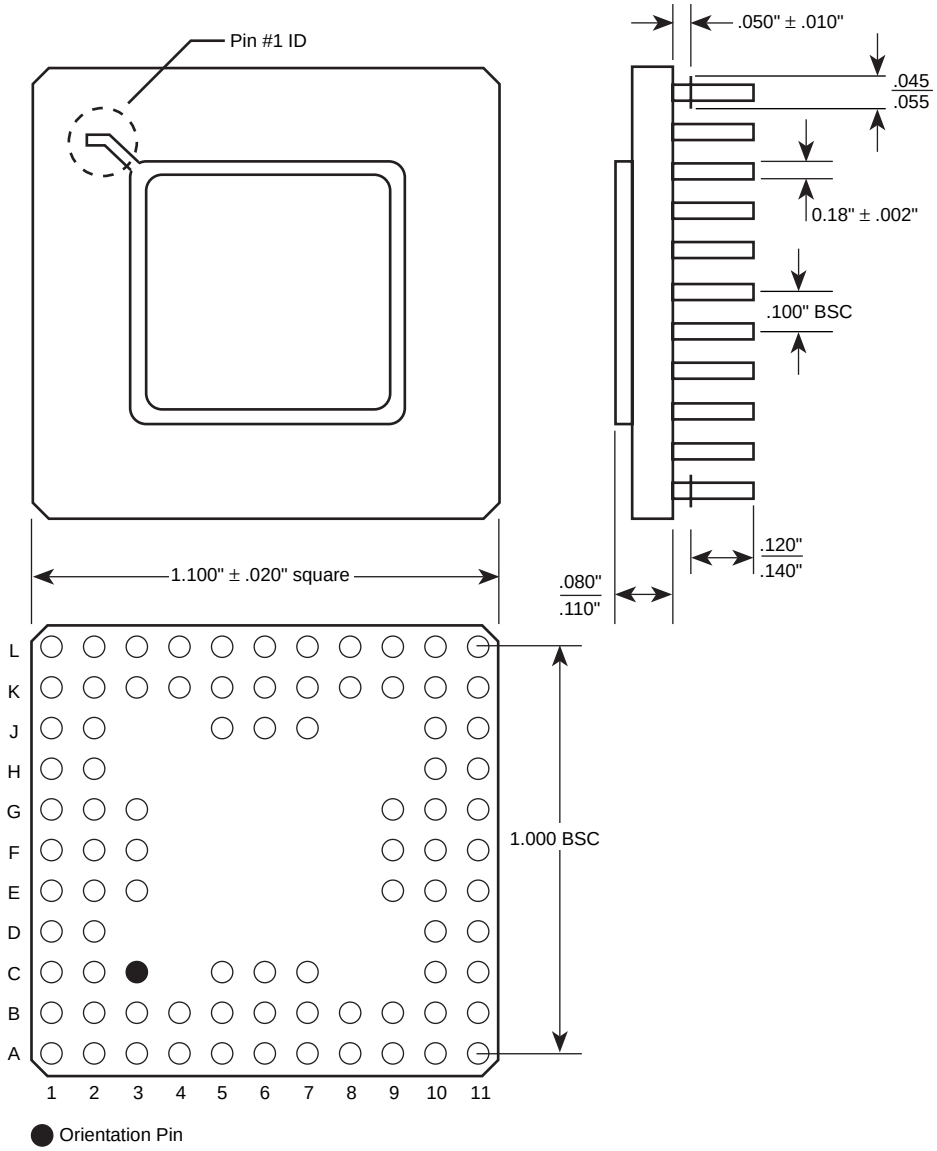
Pin Number	A1425A Function
89	V_{CC}
90	GND
91	V_{CC}
92	GND
93	I/O
94	I/O
95	I/O
96	I/O
97	I/O
98	IOCLK, I/O
99	NC
100	NC
101	GND
102	I/O
103	I/O
104	I/O
105	I/O
106	GND
107	V_{CC}
108	I/O
109	I/O
110	I/O
111	I/O
112	I/O
113	I/O
114	I/O
115	I/O
116	CLKA, I/O
117	CLKB, I/O
118	PRA, I/O
119	I/O
120	I/O
121	I/O
122	GND
123	V_{CC}
124	I/O
125	I/O
126	I/O
127	I/O
128	I/O
129	I/O
130	I/O
131	DCLK, I/O
132	NC

256-Pin CQFP (Continued)

Pin Number	A14100A Function	A32200DX Function
133	I/O	I/O
134	I/O	I/O
135	I/O	I/O
136	I/O	I/O
137	I/O	I/O
138	I/O	I/O
139	I/O	GND
140	I/O	I/O
141	V_{CC}	I/O
142	I/O	I/O
143	I/O	I/O
144	I/O	I/O
145	I/O	I/O
146	I/O	I/O
147	I/O	I/O
148	I/O	I/O
149	I/O	I/O
150	I/O	I/O
151	I/O	I/O
152	I/O	I/O
153	I/O	I/O
154	I/O	I/O
155	I/O	V_{CC}
156	I/O	I/O
157	I/O	I/O
158	GND	V_{CC}
159	V_{CC}	V_{CC}
160	GND	GND
161	V_{CC}	I/O
162	I/O	I/O
163	I/O	I/O
164	I/O	I/O
165	I/O	GND
166	I/O	I/O
167	I/O	I/O
168	I/O	I/O
169	I/O	I/O
170	I/O	V_{CC}
171	I/O	I/O
172	I/O	I/O
173	I/O	I/O
174	V_{CC}	I/O
175	GND	I/O
176	GND	I/O
177	I/O	I/O
178	I/O	I/O
179	I/O	I/O
180	I/O	GND
181	I/O	I/O
182	I/O	I/O
183	I/O	I/O
184	I/O	I/O
185	I/O	I/O
186	I/O	I/O
187	I/O	I/O
188	IOCLK, I/O	MODE
189	GND	V_{CC}
190	I/O	GND
191	I/O	NC
192	I/O	NC
193	I/O	NC
194	I/O	I/O
195	I/O	DCLK, I/O
196	I/O	I/O
197	I/O	I/O
198	I/O	I/O
199	I/O	I/O (WD)
200	I/O	I/O (WD)
201	I/O	V_{CC}
202	I/O	I/O
203	I/O	I/O
204	I/O	I/O
205	I/O	I/O
206	I/O	GND
207	I/O	I/O
208	I/O	I/O
209	I/O	QCLKC, I/O
210	I/O	I/O
211	I/O	I/O (WD)
212	I/O	I/O (WD)
213	I/O	I/O
214	I/O	I/O
215	I/O	I/O (WD)
216	I/O	I/O (WD)
217	I/O	I/O
218	I/O	PRB, I/O
219	CLKA, I/O	I/O
220	CLKB, I/O	CLKB, I/O
221	V_{CC}	I/O
222	GND	GND
223	V_{CC}	GND
224	GND	V_{CC}
225	PRA, I/O	V_{CC}
226	I/O	I/O
227	I/O	CLKA, I/O
228	I/O	I/O
229	I/O	PRA, I/O
230	I/O	I/O
231	I/O	I/O
232	I/O	I/O (WD)
233	I/O	I/O (WD)
234	I/O	I/O
235	I/O	I/O
236	I/O	I/O
237	I/O	I/O
238	I/O	I/O
239	I/O	I/O
240	GND	QCLKD, I/O
241	I/O	I/O
242	I/O	I/O (WD)
243	I/O	GND
244	I/O	I/O (WD)
245	I/O	I/O
246	I/O	I/O
247	I/O	I/O
248	I/O	V_{CC}
249	I/O	I/O
250	I/O	I/O (WD)
251	I/O	I/O (WD)
252	I/O	I/O
253	I/O	SDI, I/O
254	I/O	I/O
255	I/O	GND
256	DCLK, I/O	NC

Package Mechanical Drawings

84-Pin CPGA

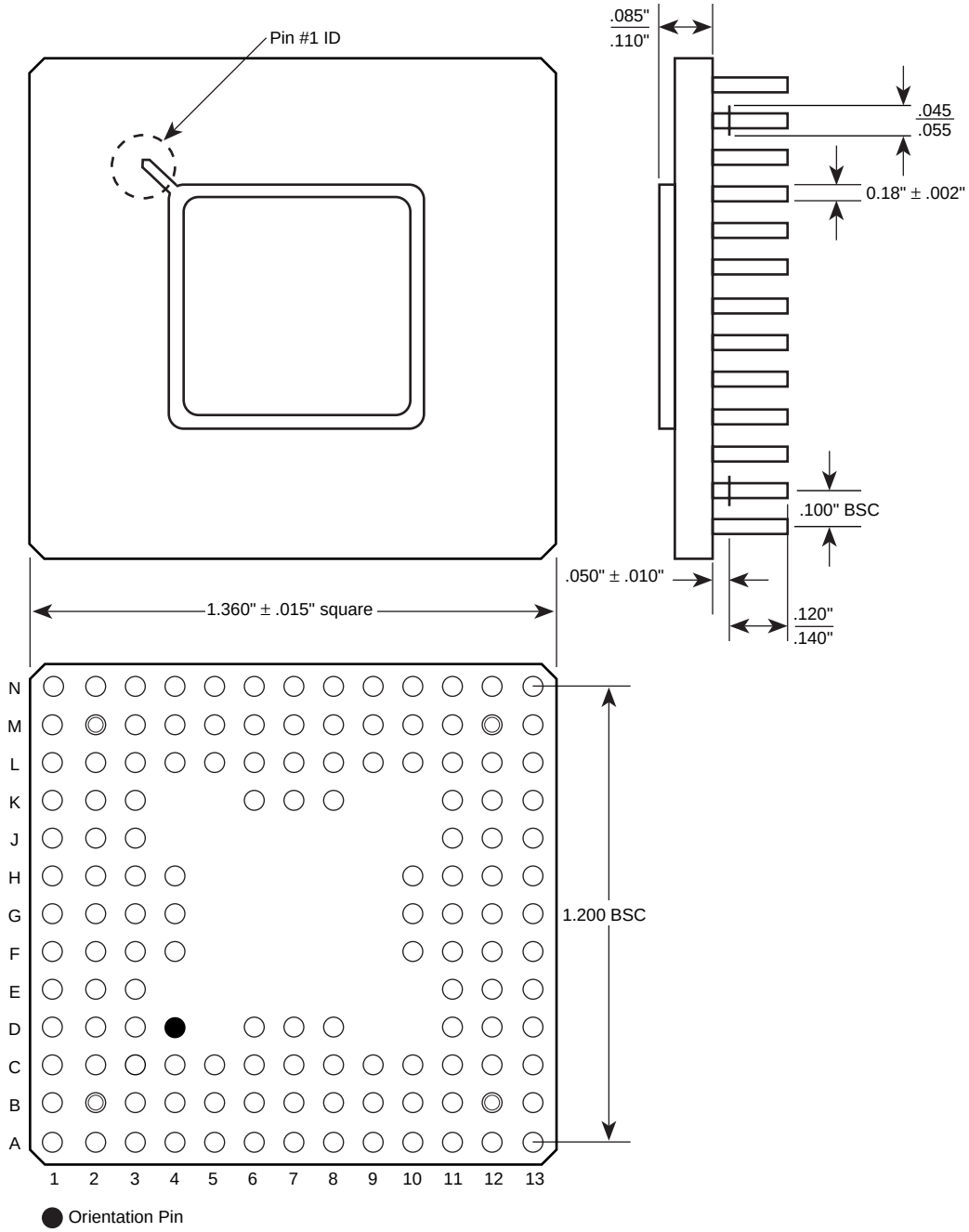


Notes:

1. *All dimensions are in inches unless otherwise stated.*
2. *BSC—Basic Spacing between Centers. This is a theoretical true position dimension and so has no tolerance.*

Package Mechanical Drawings (continued)

132-Pin CPGA

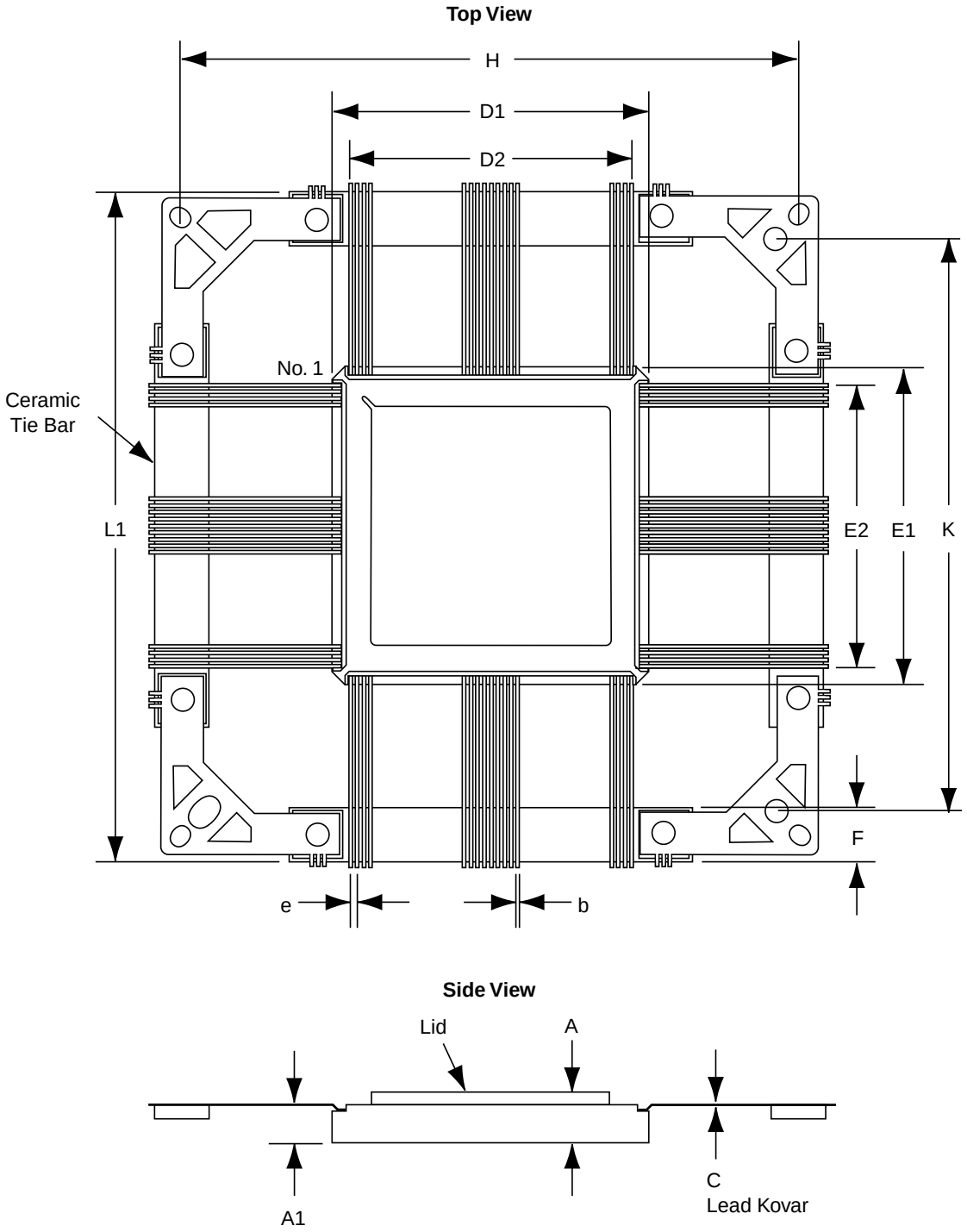


Notes:

1. *All dimensions are in inches unless otherwise stated.*
2. *BSC—Basic Spacing between Centers. This is a theoretical true position dimension and so has no tolerance.*

Package Mechanical Drawings (continued)

132-Pin, 172-Pin, 196-Pin, 208-Pin, and 256-Pin CQFP (Cavity Up)



Notes:

1. *Outside leadframe holes (from dimension H) are circular for the CQ208 and CQ256.*
2. *Seal ring and lid are connected to Ground.*
3. *Lead material is Kovar with minimum 50 microinches gold plate over nickel.*
4. *Packages are shipped unformed with the ceramic tie bar.*
5. *32200DX – CQ208 has a heat sink on the back.*

CQFP (Ceramic Quad Flat Pack)

	CQFP 84			CQFP 132			CQFP 172			CQFP 196		
Symbol	**Min.**	**Nom.**	**Max.**	**Min.**	**Nom.**	**Max.**	**Min.**	**Nom.**	**Max.**	**Min.**	**Nom.**	**Max.**
A	0.070	0.090	0.100	0.094	0.105	0.116	0.094	0.105	0.116	0.094	0.105	0.116
A1	0.060	0.075	0.080	0.080	0.090	0.100	0.080	0.090	0.100	0.080	0.090	0.100
b	0.008	0.010	0.012	0.007	0.008	0.010	0.007	0.008	0.010	0.007	0.008	0.010
c	0.004	0.006	0.008	0.004	0.006	0.008	0.004	0.006	0.008	0.004	0.006	0.008
D1/E1	0.640	0.650	0.660	0.940	0.950	0.960	1.168	1.180	1.192	1.336	1.350	1.364
D2/E2	0.500 BSC			0.800 BSC			1.050 BSC			1.200 BSC		
e	0.025 BSC			0.025 BSC			0.025 BSC			0.025 BSC		
F	0.130	0.140	0.150	0.325	0.350	0.375	0.175	0.200	0.225	0.175	0.200	0.225
H	1.460 BSC			2.320 BSC			2.320 BSC			2.320 BSC		
K	—			2.140 BSC			2.140 BSC			2.140 BSC		
L1	1.595	1.600	1.615	2.485	2.500	2.505	2.485	2.495	2.505	2.485	2.495	2.505

Note:

1. All dimensions are in inches except CQ208 and CQ256, which are in millimeters.

2. BSC equals Basic Spacing between Centers. This is a theoretical true position dimension and so has no tolerance.

CQFP (Ceramic Quad Flat Pack)

	CQFP 208			CQFP 256		
Symbol	**Min.**	**Nom.**	**Max.**	**Min.**	**Nom.**	**Max.**
A	2.78	3.17	3.56	2.28	2.67	3.06
A1	2.43	2.79	3.15	1.93	2.29	2.65
b	0.18	0.20	0.22	0.18	0.20	0.22
c	0.11	0.15	0.17	0.11	0.15	0.18
D1/E1	28.96	29.21	29.46	35.64	36.00	36.36
D2/E2	25.5 BSC			31.5 BSC		
e	0.50 BSC			0.50 BSC		
F	7.05	7.75	8.45	7.05	7.75	8.45
H	70.00 BSC			70.00 BSC		
K	65.90 BSC			65.90 BSC		
L1	74.60	75.00	75.40	74.60	75.00	75.40

Note:

1. All dimensions are in inches except CQ208 and CQ256, which are in millimeters.

2. BSC equals Basic Spacing between Centers. This is a theoretical true position dimension and so has no tolerance.