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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Obsolete
Number of LABs/CLBs	547
Number of Logic Elements/Cells	-
Total RAM Bits	-
Number of I/O	69
Number of Gates	2000
Voltage - Supply	4.5V ~ 5.5V
Mounting Type	Through Hole
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	84-BCPGA
Supplier Device Package	84-CPGA (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/microsemi/a1020b-1pg84c

Product Plan

3200DX Family	Speed Grade Std	Speed Grade –1*	Application C	Application M	Application B	Application E
A32100DX Device						
84-pin Ceramic Quad Flat Pack (CQFP)	✔	✔	✔	✔	✔	—
A32200DX Device						
208-pin Ceramic Quad Flat Pack (CQFP)	✔	✔	✔	✔	✔	—
256-pin Ceramic Quad Flat Pack (CQFP)	✔	✔	✔	✔	✔	—
ACT 3 Family						
A1425A Device						
132-pin Ceramic Quad Flat Pack (CQFP)	✔	✔	✔	✔	✔	✔
133-pin Ceramic Pin Grid Array (CPGA)	✔	✔	✔	✔	✔	✔
A1460A Device						
196-pin Ceramic Quad Flat Pack (CQFP)	✔	✔	✔	✔	✔	✔
207-pin Ceramic Pin Grid Array (CPGA)	✔	✔	✔	✔	✔	✔
A14100A Device						
256-pin Ceramic Quad Flat Pack (CQFP)	✔	✔	✔	✔	✔	✔
257-pin Ceramic Pin Grid Array (CPGA)	✔	✔	✔	✔	✔	✔
1200XL Family						
A1280XL Device						
172-pin Ceramic Quad Flat Pack (CQFP)	✔	✔	✔	✔	✔	—
176-pin Ceramic Pin Grid Array (CPGA)	✔	✔	✔	✔	✔	—
ACT 2 Family						
A1240A Device						
132-pin Ceramic Pin Grid Array (CPGA)	✔	✔	✔	✔	✔	—
A1280A Device						
172-pin Ceramic Quad Flat Pack (CQFP)	✔	✔	✔	✔	✔	✔
176-pin Ceramic Pin Grid Array (CPGA)	✔	✔	✔	✔	✔	✔
ACT 1 Family						
A1010B Device						
84-pin Ceramic Pin Grid Array (CPGA)	✔	✔	✔	✔	✔	—
A1020B Device						
84-pin Ceramic Quad Flat Pack (CQFP)	✔	✔	✔	✔	✔	✔
84-pin Ceramic Pin Grid Array (CPGA)	✔	✔	✔	✔	✔	✔

Applications: C = *Commercial*
M = *Military*
B = *MIL-STD-883*
E = *Extended Flow*

Availability: ✔ = *Available*
— = *Not Planned*

**Speed Grade:* –1 = *Approx. 15% faster than Standard* can be combined with frequency and voltage to represent active power dissipation.

Equivalent Capacitance

The power dissipated by a CMOS circuit can be expressed by Equation 1:

$$\text{Power (uW)} = C_{EQ} * V_{CC}^{2} * F \qquad (1)$$

where:

C_{EQ} = Equivalent capacitance in pF

V_{CC} = Power supply in volts (V)

F = Switching frequency in MHz

Equivalent capacitance is calculated by measuring I_{CC}active at a specified frequency and voltage for each circuit component of interest. Measurements are made over a range of frequencies at a fixed value of V_{CC}. Equivalent capacitance is frequency independent so that the results can be used over a wide range of operating conditions. Equivalent capacitance values are shown below.

CEQ Values for Actel FPGAs

	ACT 3	1200XL 3200DX	ACT 2	ACT 1
Modules (C_{EQM})	6.7	5.2	5.8	3.7
Input Buffers (C_{EQI})	7.2	11.6	12.9	22.1
Output Buffers (C_{EQO})	10.4	23.8	23.8	31.2
Routed Array Clock Buffer Loads (C_{EQCR})	1.6	3.5	3.9	4.6
Dedicated Clock Buffer Loads (C_{EQCD})	0.7	N/A	N/A	N/A
I/O Clock Buffer Loads (C_{EQCI})	0.9	N/A	N/A	N/A

To calculate the active power dissipated from the complete design, the switching frequency of each part of the logic must be known. Equation 2 shows a piecewise linear summation over all components that applies to all ACT 1, 1200XL, 3200DX, ACT 2, and ACT 3 devices. Since the ACT 1 family has only one routed array clock, the terms labeled routed_Clk2, dedicated_Clk, and IO_Clk do not apply. Similarly, the ACT 2 family has two routed array clocks, and the dedicated_Clk and IO_Clk terms do not apply. For ACT 3 devices, all terms will apply.

$$\text{Power} = V_{CC}^{2} * [(m * C_{EQM} * f_m)_{modules} + (n * C_{EQI} * f_n)_{inputs} + (p * (C_{EQO} + C_L) * f_p)_{outputs} + 0.5 * (q_1 * C_{EQCR} * f_{q1})_{routed\_Clk1} + (r_1 * f_{q1})_{routed\_Clk1} + 0.5 * (q_2 * C_{EQCR} * f_{q2})_{routed\_Clk2} + (r_2 * f_{q2})_{routed\_Clk2} + 0.5 * (s_1 * C_{EQCD} * f_{s1})_{dedicated\_Clk} + (s_2 * C_{EQCI} * f_{s2})_{IO\_Clk}] \qquad (2)$$

where:

m = Number of logic modules switching at f_m

n = Number of input buffers switching at f_n

p = Number of output buffers switching at f_p

q_1 = Number of clock loads on the first routed array clock (all families)

q_2 = Number of clock loads on the second routed array clock (ACT 2, 1200XL, 3200DX, ACT 3 only)

r_1 = Fixed capacitance due to first routed array clock (all families)

r_2 = Fixed capacitance due to second routed array clock (ACT 2, 1200XL, 3200DX, ACT 3 only)

s_1 = Fixed number of clock loads on the dedicated array clock (ACT 3 only)

s_2 = Fixed number of clock loads on the dedicated I/O clock (ACT 3 only)

C_{EQM} = Equivalent capacitance of logic modules in pF

C_{EQI} = Equivalent capacitance of input buffers in pF

C_{EQO} = Equivalent capacitance of output buffers in pF

C_{EQCR} = Equivalent capacitance of routed array clock in pF

C_{EQCD} = Equivalent capacitance of dedicated array clock in pF

C_{EQCI} = Equivalent capacitance of dedicated I/O clock in pF

C_L = Output lead capacitance in pF

f_m = Average logic module switching rate in MHz

f_n = Average input buffer switching rate in MHz

f_p = Average output buffer switching rate in MHz

f_{q1} = Average first routed array clock rate in MHz (all families)

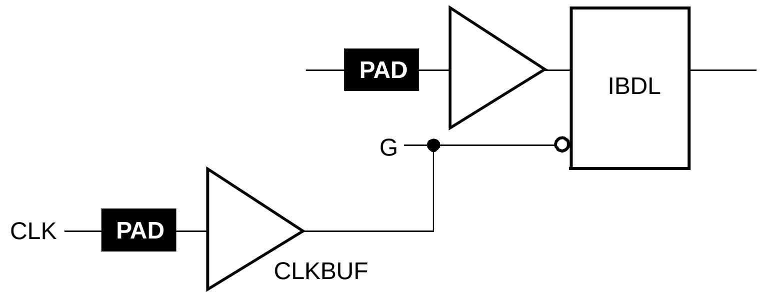
f_{q2} = Average second routed array clock rate in MHz (ACT 2, 1200XL, 3200DX, ACT 3 only)

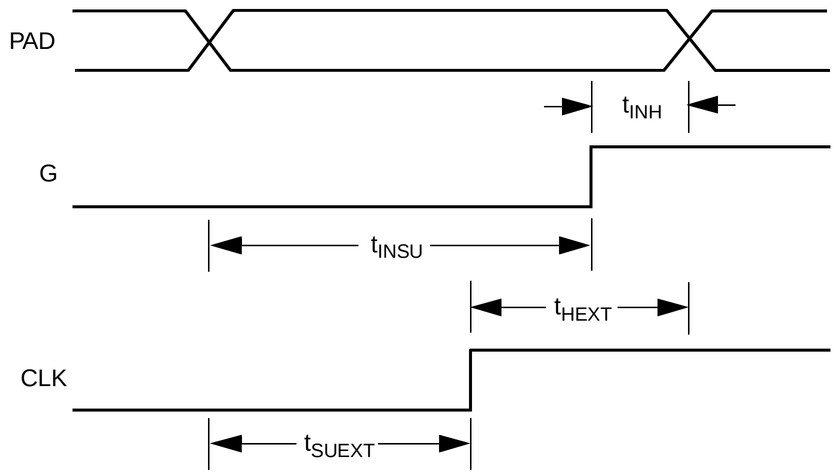
f_{s1} = Average dedicated array clock rate in MHz (ACT 3 only)

f_{s2} = Average dedicated I/O clock rate in MHz (ACT 3 only)

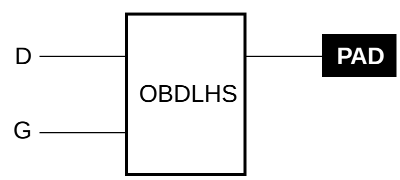
Sequential Timing Characteristics (continued)

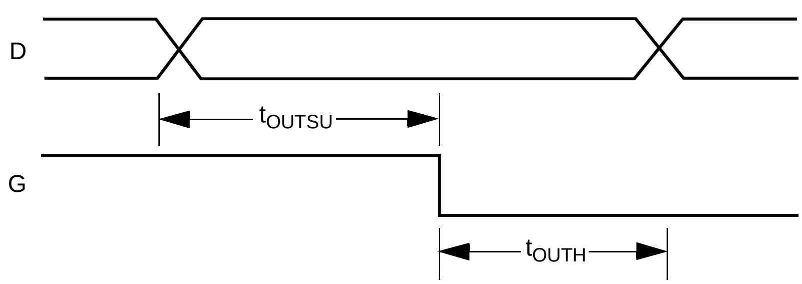
Input Buffer Latches (ACT 2 and 1200XL/3200DX)





Output Buffer Latches (ACT 2 and 1200XL/3200DX)





A1460A Timing Characteristics (continued)

(Worst-Case Military Conditions, V_{CC} = 4.5V, T_J = 125°C)

		'–1' Speed		'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
CMOS Output Module Timing[1]						
t_{DHS}	Data to Pad, High Slew		9.2		10.8	ns
t_{DLS}	Data to Pad, Low Slew		17.3		20.3	ns
t_{ENZHS}	Enable to Pad, Z to H/L, High Slew		7.7		9.1	ns
t_{ENZLS}	Enable to Pad, Z to H/L, Low Slew		13.1		15.5	ns
t_{ENHSZ}	Enable to Pad, H/L to Z, High Slew		10.9		12.8	ns
t_{ENLSZ}	Enable to Pad, H/L to Z, Low Slew		10.9		12.8	ns
t_{CKHS}	IOCLK Pad to Pad H/L, High Slew		14.1		16.0	ns
t_{CKLS}	IOCLK Pad to Pad H/L, Low Slew		20.2		22.4	ns
d_{TLHHS}	Delta Low to High, High Slew		0.06		0.07	ns/pF
d_{TLHLS}	Delta Low to High, Low Slew		0.11		0.13	ns/pF
d_{THLHS}	Delta High to Low, High Slew		0.04		0.05	ns/pF
d_{THLLS}	Delta High to Low, Low Slew		0.05		0.06	ns/pF
Dedicated (Hard-Wired) I/O Clock Network						
t_{IOCKH}	Input Low to High (Pad to I/O Module Input)		3.5		4.1	ns
t_{IOPWH}	Minimum Pulse Width High	4.8		5.7		ns
t_{IOPWL}	Minimum Pulse Width Low	4.8		5.7		ns
t_{IOSAPW}	Minimum Asynchronous Pulse Width	3.9		4.4		ns
t_{IOCKSW}	Maximum Skew		0.9		1.0	ns
t_{IOP}	Minimum Period	9.9		11.6		ns
f_{IOMAX}	Maximum Frequency		100		85	MHz
Dedicated (Hard-Wired) Array Clock Network						
t_{HCKH}	Input Low to High (Pad to S-Module Input)		5.5		6.4	ns
t_{HCKL}	Input High to Low (Pad to S-Module Input)		5.5		6.4	ns
t_{HPWH}	Minimum Pulse Width High	4.8		5.7		ns
t_{HPWL}	Minimum Pulse Width Low	4.8		5.7		ns
t_{HCKSW}	Maximum Skew		0.9		1.0	ns
t_{HP}	Minimum Period	9.9		11.6		ns
f_{HMAX}	Maximum Frequency		100		85	MHz

Notes:

1. *Delays based on 35 pF loading.*
2. *SSO information can be found in the* Simultaneously Switching Output Limits for Actel FPGAs *application note at http://www.actel.com/appnotes.*

A14100A Timing Characteristics

(Worst-Case Military Conditions, V_{CC} = 4.5V, T_J = 125°C)

		'–1' Speed		'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
Logic Module Propagation Delays[1]						
t_{PD}	Internal Array Module		3.0		3.5	ns
t_{CO}	Sequential Clock to Q		3.0		3.5	ns
t_{CLR}	Asynchronous Clear to Q		3.0		3.5	ns
Logic Module Predicted Routing Delays[2]						
t_{RD1}	FO=1 Routing Delay		1.3		1.5	ns
t_{RD2}	FO=2 Routing Delay		1.9		2.1	ns
t_{RD3}	FO=3 Routing Delay		2.1		2.5	ns
t_{RD4}	FO=4 Routing Delay		2.6		2.9	ns
t_{RD8}	FO=8 Routing Delay		4.2		4.9	ns
Logic Module Sequential Timing						
t_{SUD}	Flip-Flop (Latch) Data Input Setup	1.0		1.0		ns
t_{HD}	Flip-Flop (Latch) Data Input Hold	0.6		0.6		ns
t_{SUENA}	Flip-Flop (Latch) Enable Setup	1.0		1.0		ns
t_{HENA}	Flip-Flop (Latch) Enable Hold	0.6		0.6		ns
t_{WASYN}	Asynchronous Pulse Width	4.8		5.6		ns
t_{WCLKA}	Flip-Flop Clock Pulse Width	4.8		5.6		ns
t_A	Flip-Flop Clock Input Period	9.9		11.6		ns
f_{MAX}	Flip-Flop Clock Frequency		100		85	MHz
Input Module Propagation Delays						
t_{INY}	Input Data Pad to Y		4.2		4.9	ns
t_{ICKY}	Input Reg IOCLK Pad to Y		7.0		8.2	ns
t_{OCKY}	Output Reg IOCLK Pad to Y		7.0		8.2	ns
t_{ICLRY}	Input Asynchronous Clear to Y		7.0		8.2	ns
t_{OCLRY}	Output Asynchronous Clear to Y		7.0		8.2	ns
Input Module Predicted Routing Delays[2, 3]						
t_{IRD1}	FO=1 Routing Delay		1.3		1.5	ns
t_{IRD2}	FO=2 Routing Delay		1.9		2.1	ns
t_{IRD3}	FO=3 Routing Delay		2.1		2.5	ns
t_{IRD4}	FO=4 Routing Delay		2.6		2.9	ns
t_{IRD8}	FO=8 Routing Delay		4.2		4.9	ns

Notes:

1. *For dual-module macros, use $t_{PD} + t_{RD1} + t_{PDn}$, $t_{CO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.*
2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*
3. *Optimization techniques may further reduce delays by 0 to 4 ns.*

A32100DX Timing Characteristics (continued)

(Worst-Case Military Conditions, V_{CC} = 4.5V, T_J = 125°C)

		'–1' Speed		'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
TTL Output Module Timing[1]						
t_{DLH}	Data to Pad High		5.1		6.8	ns
t_{DHL}	Data to Pad Low		6.3		8.3	ns
t_{ENZH}	Enable Pad Z to High		6.6		8.8	ns
t_{ENZL}	Enable Pad Z to Low		7.1		9.4	ns
t_{ENHZ}	Enable Pad High to Z		11.5		15.3	ns
t_{ENLZ}	Enable Pad Low to Z		11.5		15.3	ns
t_{GLH}	G to Pad High		11.5		15.3	ns
t_{GHL}	G to Pad Low		12.4		16.6	ns
t_{LSU}	I/O Latch Output Setup	0.4		0.5		ns
t_{LH}	I/O Latch Output Hold	0.0		0.0		ns
t_{LCO}	I/O Latch Clock-Out (Pad-to-Pad) 32 I/O		11.5		15.4	ns
t_{ACO}	Array Latch Clock-Out (Pad-to-Pad) 32 I/O		16.3		21.7	ns
d_{TLH}	Capacitive Loading, Low to High		0.04		0.06	ns/pF
d_{THL}	Capacitive Loading, High to Low		0.06		0.08	ns/pF
t_{WDO}	Hard-Wired Wide Decode Output		0.05		0.07	ns
CMOS Output Module Timing[1]						
t_{DLH}	Data to Pad High		6.3		8.3	ns
t_{DHL}	Data to Pad Low		5.1		6.8	ns
t_{ENZH}	Enable Pad Z to High		6.6		8.8	ns
t_{ENZL}	Enable Pad Z to Low		7.1		9.4	ns
t_{ENHZ}	Enable Pad High to Z		11.5		15.3	ns
t_{ENLZ}	Enable Pad Low to Z		11.5		15.3	ns
t_{GLH}	G to Pad High		11.5		15.3	ns
t_{GHL}	G to Pad Low		12.4		16.6	ns
t_{LSU}	I/O Latch Setup	0.4		0.5		ns
t_{LH}	I/O Latch Hold	0.0		0.0		ns
t_{LCO}	I/O Latch Clock-Out (Pad-to-Pad) 32 I/O		13.7		18.2	ns
t_{ACO}	Array Latch Clock-Out (Pad-to-Pad) 32 I/O		19.2		25.6	ns
d_{TLH}	Capacitive Loading, Low to High		0.06		0.08	ns/pF
d_{THL}	Capacitive Loading, High to Low		0.05		0.07	ns/pF
t_{WDO}	Hard-Wired Wide Decode Output		0.05		0.07	ns

Notes:

1. *Delays based on 35 pF loading.*
2. *SSO information can be found in the* Simultaneously Switching Output Limits for Actel FPGAs *application note at http://www.actel.com/appnotes.*

A32200DX Timing Characteristics

(Worst-Case Military Conditions, V_{CC} = 4.5V, T_J = 125°C)

		'–1' Speed		'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
Logic Module Combinatorial Functions						
t_{PD}	Internal Array Module Delay		2.8		3.8	ns
t_{PDD}	Internal Decode Module Delay		3.4		4.6	ns
Logic Module Predicted Routing Delays[1]						
t_{RD1}	FO=1 Routing Delay		1.6		2.1	ns
t_{RD2}	FO=2 Routing Delay		2.3		3.1	ns
t_{RD3}	FO=3 Routing Delay		2.9		3.9	ns
t_{RD4}	FO=4 Routing Delay		3.5		4.7	ns
t_{RD5}	FO=8 Routing Delay		6.2		8.2	ns
t_{RDD}	Decode-to-Output Routing Delay		0.8		1.1	ns
Logic Module Sequential Timing Characteristics						
t_{CO}	Flip-Flop Clock-to-Output		3.2		4.2	ns
t_{GO}	Latch Gate-to-Output		2.8		3.8	ns
t_{SU}	Flip-Flop (Latch) Setup Time	0.5		0.6		ns
t_H	Flip-Flop (Latch) Hold Time	0.0		0.0		ns
t_{RO}	Flip-Flop (Latch) Reset to Output		3.2		4.2	ns
t_{SUENA}	Flip-Flop (Latch) Enable Setup	0.9		1.2		ns
t_{HENA}	Flip-Flop (Latch) Enable Hold	0.0		0.0		ns
t_{WCLKA}	Flip-Flop (Latch) Clock Active Pulse Width	4.3		5.8		ns
t_{WASYN}	Flip-Flop (Latch) Asynchronous Pulse Width	5.7		7.6		ns

Note:

1. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*

A32200DX Timing Characteristics (continued)

(Worst-Case Military Conditions, V_{CC} = 4.5V, T_J = 125°C)

			'–1' Speed		'Std' Speed		
Parameter	**Description**		**Min.**	**Max.**	**Min.**	**Max.**	**Units**
Input Module Propagation Delays							
t_{INPY}	Input Data Pad to Y			1.9		2.6	ns
t_{INGO}	Input Latch Gate-to-Output			4.6		6.0	ns
t_{INH}	Input Latch Hold		0.0		0.0		ns
t_{INSU}	Input Latch Setup		0.7		0.9		ns
t_{ILA}	Latch Active Pulse Width		6.1		8.1		ns
Input Module Predicted Routing Delays[1]							
t_{IRD1}	FO=1 Routing Delay			2.6		3.5	ns
t_{IRD2}	FO=2 Routing Delay			3.4		4.6	ns
t_{IRD3}	FO=3 Routing Delay			4.6		6.1	ns
t_{IRD4}	FO=4 Routing Delay			5.4		7.2	ns
t_{IRD5}	FO=8 Routing Delay			7.0		9.3	ns
Global Clock Network							
t_{CKH}	Input Low to High	FO=32 FO=635		7.3 8.5		9.8 11.3	ns ns
t_{CKL}	Input High to Low	FO=32 FO=635		7.2 9.3		9.6 12.5	ns ns
t_{PWH}	Minimum Pulse Width High	FO=32 FO=635	3.2 3.9		4.3 5.2		ns ns
t_{PWL}	Minimum Pulse Width Low	FO=32 FO=635	3.2 3.9		4.3 5.2		ns ns
t_{CKSW}	Maximum Skew	FO=32 FO=635		1.8 1.8		2.4 2.4	ns ns
t_{SUEXT}	Input Latch External Setup	FO=32 FO=635	0.0 0.0		0.0 0.0		ns ns
t_{HEXT}	Input Latch External Hold	FO=32 FO=635	3.0 3.8		4.0 5.1		ns ns
t_P	Minimum Period (1/fmax)	FO=32 FO=635	5.8 6.8		7.7 9.1		ns ns
f_{HMAX}	Maximum Datapath Frequency	FO=32 FO=635		172 147		130 110	MHz MHz

Note:

1. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment. Optimization techniques may further reduce delays by 0 to 4 ns.*

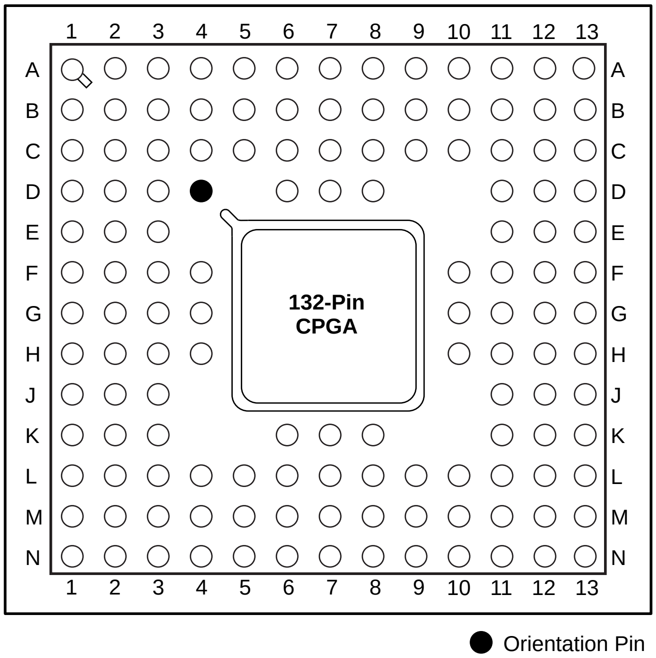
84-Pin CPGA

Pin Number	A1010B Function	A1020B Function
A1	I/O	I/O
A2	I/O	I/O
A3	I/O	I/O
A4	I/O	I/O
A5	I/O	I/O
A6	I/O	I/O
A7	I/O	I/O
A8	I/O	I/O
A9	I/O	I/O
A10	I/O	I/O
A11	PRA, I/O	PRA, I/O
B1	NC	I/O
B2	NC	NC
B3	I/O	I/O
B4	I/O	I/O
B5	V_{CC}	V_{CC}
B6	I/O	I/O
B7	GND	GND
B8	I/O	I/O
B9	I/O	I/O
B10	PRB, I/O	PRB, I/O
B11	SDI, I/O	SDI, I/O
C1	NC	I/O
C2	NC	I/O
C5	I/O	I/O
C6	I/O	I/O
C7	I/O	I/O
C10	DCLK, I/O	DCLK, I/O
C11	NC	I/O
D1	I/O	I/O
D2	I/O	I/O
D10	NC	I/O
D11	NC	I/O
E1	I/O	I/O
E2	GND	GND
E3	GND	GND
E9	V_{CC}	V_{CC}
E10	V_{CC}	V_{CC}
E11	MODE	MODE
F1	V_{CC}	V_{CC}
F2	I/O	I/O
F3	I/O	I/O

Pin Number	A1010B Function	A1020B Function
F9	CLK, I/O	CLK, I/O
F10	GND	GND
F11	I/O	I/O
G1	I/O	I/O
G2	V_{CC}	V_{CC}
G3	I/O	I/O
G9	I/O	I/O
G10	GND	GND
G11	I/O	I/O
H1	I/O	I/O
H2	I/O	I/O
H10	I/O	I/O
H11	I/O	I/O
J1	I/O	I/O
J2	NC	I/O
J5	I/O	I/O
J6	I/O	I/O
J7	I/O	I/O
J10	NC	I/O
J11	I/O	I/O
K1	NC	I/O
K2	V_{CC}	V_{CC}
K3	I/O	I/O
K4	I/O	I/O
K5	GND	GND
K6	I/O	I/O
K7	V_{CC}	V_{CC}
K8	I/O	I/O
K9	I/O	I/O
K10	NC	I/O
K11	NC	I/O
L1	NC	I/O
L2	I/O	I/O
L3	I/O	I/O
L4	I/O	I/O
L5	I/O	I/O
L6	I/O	I/O
L7	I/O	I/O
L8	I/O	I/O
L9	I/O	I/O
L10	I/O	I/O
L11	I/O	I/O

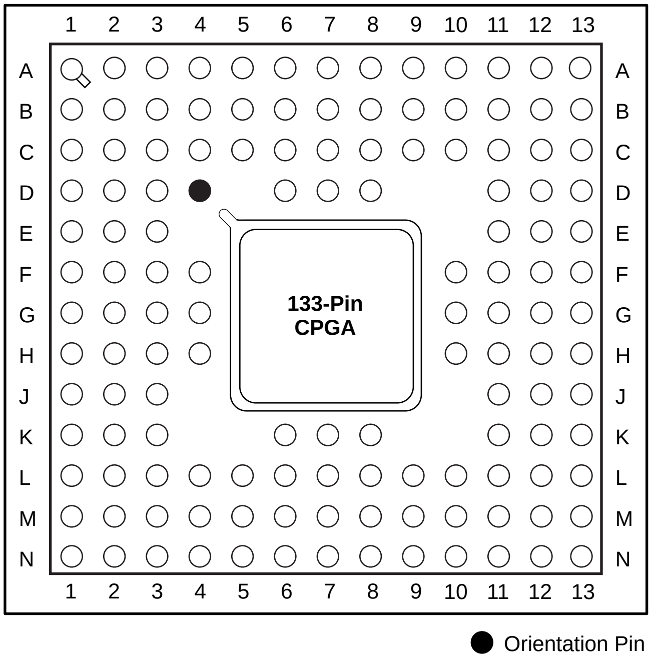
Package Pin Assignments (continued)

132-Pin CPGA (Top View)



Package Pin Assignments (continued)

133-Pin CPGA (Top View)

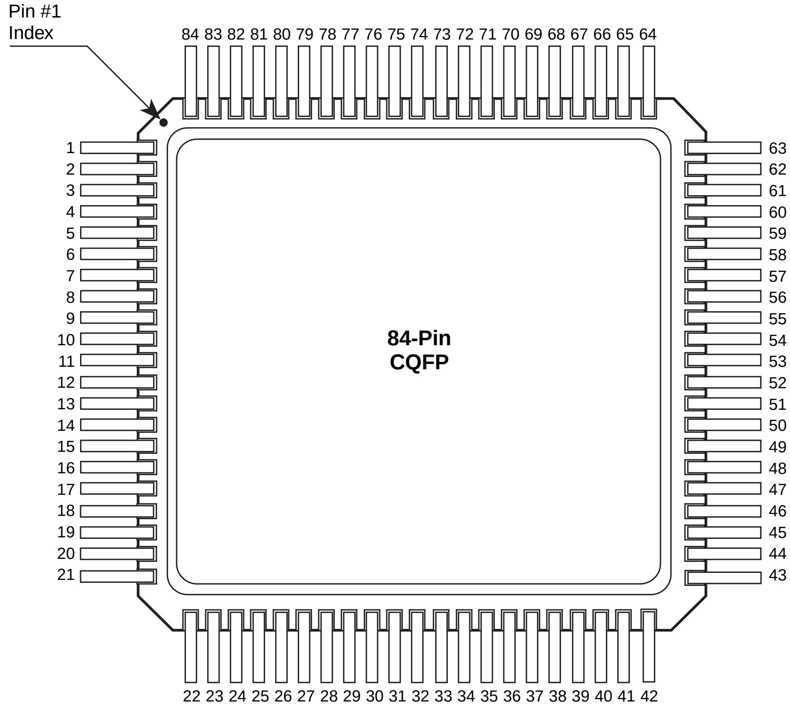


133-Pin CPGA

Pin Number	A1425A Function
A1	NC
A2	GND
A3	I/O
A4	I/O
A5	I/O
A6	PRA, I/O
A7	NC
A8	I/O
A9	I/O
A10	I/O
A11	I/O
A12	I/O
A13	NC
B1	I/O
B2	V_{CC}
B3	I/O
B4	I/O
B5	I/O
B6	CLKB, I/O
B7	V_{CC}
B8	I/O
B9	I/O
B10	I/O
B11	I/O
B12	V_{CC}
B13	I/O
C1	I/O
C2	SDI, I/O
C3	GND
C4	I/O
C5	I/O
C6	I/O
C7	GND
C8	I/O
C9	I/O
C10	IOCLK, I/O
C11	GND
C12	GND
C13	I/O
D1	I/O
D2	I/O
D3	I/O
D4	DCLK, I/O
D6	CLKA, I/O
D7	I/O
D8	I/O
D11	I/O
D12	I/O
D13	I/O
E1	I/O
E2	I/O
E3	MODE
E11	V_{CC}
E12	I/O
E13	I/O
F1	I/O
F2	I/O
F3	I/O
F4	I/O
F10	GND
F11	I/O
F12	I/O
F13	I/O
G1	NC
G2	V_{CC}
G3	GND
G4	I/O
G10	I/O
G11	GND
G12	V_{CC}
G13	NC
H1	I/O
H2	I/O
H3	I/O
H4	I/O
H10	I/O
H11	I/O
H12	I/O
H13	I/O
J1	I/O
J2	V_{CC}
J3	I/O
J11	I/O
J12	V_{CC}
J13	I/O
K1	I/O
K2	I/O
K3	I/O
K6	I/O
K7	HCLKA, I/O
K8	I/O
K11	I/O
K12	I/O
K13	I/O
L1	I/O
L2	I/O
L3	GND
L4	I/O
L5	I/O
L6	PRB, I/O
L7	GND
L8	I/O
L9	I/O
L10	IOPCL, I/O
L11	GND
L12	I/O
L13	I/O
M1	I/O
M2	V_{CC}
M3	GND
M4	I/O
M5	I/O
M6	I/O
M7	V_{CC}
M8	I/O
M9	I/O
M10	I/O
M11	I/O
M12	V_{CC}
M13	I/O
N1	NC
N2	I/O
N3	I/O
N4	I/O
N5	I/O
N6	I/O
N7	NC
N8	I/O
N9	I/O
N10	I/O
N11	I/O
N12	GND
N13	NC

Package Pin Assignments (continued)

84-Pin CQFP (Top View)



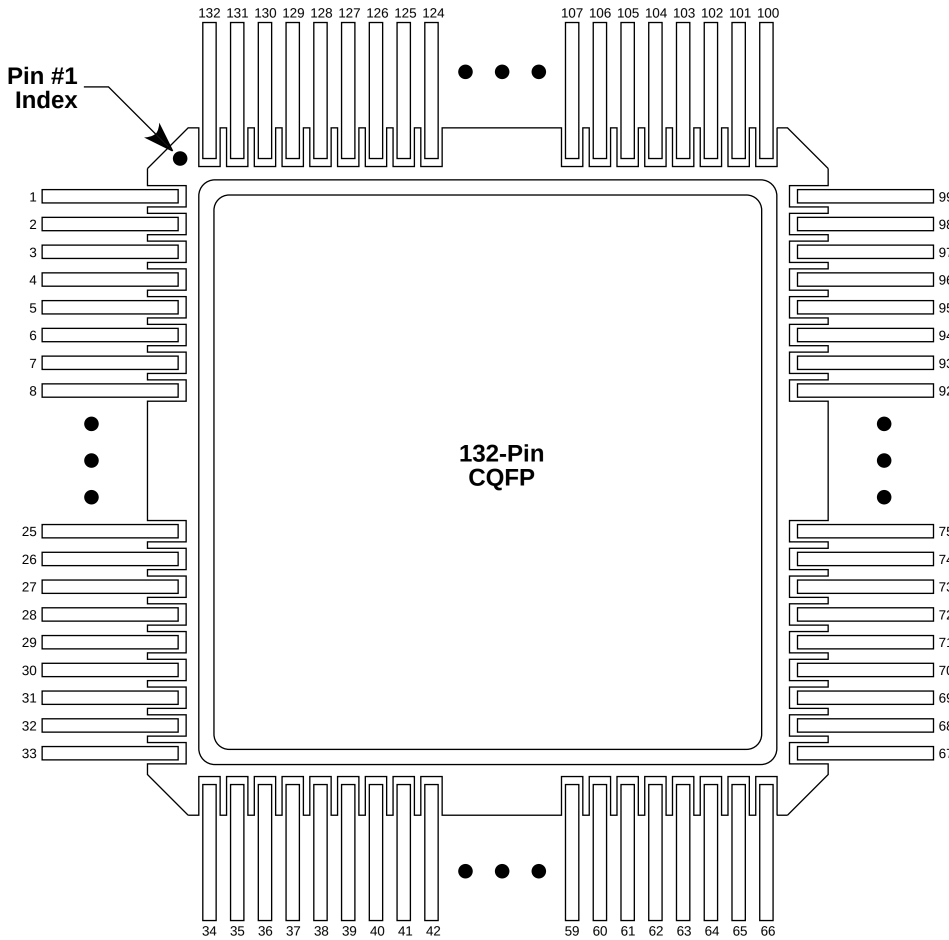
84-Pin CQFP

Pin Number	A1020B Function	A32100DX Function
1	NC	GND
2	I/O	MODE
3	I/O	I/O
4	I/O	I/O
5	I/O	I/O
6	I/O	I/O
7	GND	V_{CC}
8	GND	I/O
9	I/O	I/O
10	I/O	GND
11	I/O	V_{CC}
12	I/O	V_{CC}
13	I/O	I/O
14	V_{CC}	I/O
15	V_{CC}	I/O
16	I/O	I/O
17	I/O	GND
18	I/O	I/O
19	I/O	I/O
20	I/O	I/O
21	I/O	I/O
22	V_{CC}	GND
23	I/O	I/O
24	I/O	I/O
25	I/O	I/O (WD)
26	I/O	I/O (WD)
27	I/O	I/O
28	I/O	QCLKA, I/O
29	GND	GND
30	I/O	I/O (WD)
31	I/O	I/O
32	I/O	GND
33	I/O	V_{CC}
34	I/O	I/O (WD)
35	V_{CC}	I/O (WD)
36	I/O	QCLKB, I/O
37	I/O	I/O (WD)
38	I/O	GND
39	I/O	I/O (WD)
40	I/O	I/O (WD)
41	I/O	I/O (WD)
42	I/O	SDO, I/O

Pin Number	A1020B Function	A32100DX Function
43	I/O	GND
44	I/O	I/O
45	I/O	I/O
46	I/O	I/O
47	I/O	I/O
48	I/O	I/O
49	GND	I/O
50	GND	GND
51	I/O	TCK, I/O
52	I/O	GND
53	CLKA, I/O	V_{CC}
54	I/O	V_{CC}
55	MODE	V_{CC}
56	V_{CC}	V_{CC}
57	V_{CC}	I/O
58	I/O	I/O
59	I/O	GND
60	I/O	I/O
61	SDI, I/O	I/O
62	DCLK, I/O	I/O
63	PRA, I/O	GND
64	PRB, I/O	SDI, I/O
65	I/O	I/O (WD)
66	I/O	I/O (WD)
67	I/O	I/O (WD)
68	I/O	I/O (WD)
69	I/O	QCLKD, I/O
70	I/O	I/O (WD)
71	GND	I/O (WD)
72	I/O	PRA, I/O
73	I/O	CLKA, I/O
74	I/O	V_{CC}
75	I/O	GND
76	I/O	CLKB, I/O
77	V_{CC}	PRB, I/O
78	I/O	I/O (WD)
79	I/O	I/O (WD)
80	I/O	QCLKC, I/O
81	I/O	GND
82	I/O	I/O (WD)
83	I/O	I/O (WD)
84	I/O	DCLK, I/O

Package Pin Assignments (continued)

132-Pin CQFP (Top View)



132-Pin CQFP

Pin Number	A1425A Function
1	NC
2	GND
3	SDI, I/O
4	I/O
5	I/O
6	I/O
7	I/O
8	I/O
9	MODE
10	GND
11	V_{CC}
12	I/O
13	I/O
14	I/O
15	I/O
16	I/O
17	I/O
18	I/O
19	I/O
20	I/O
21	I/O
22	V_{CC}
23	I/O
24	I/O
25	I/O
26	GND
27	V_{CC}
28	I/O
29	I/O
30	I/O
31	I/O
32	I/O
33	I/O
34	NC
35	I/O
36	GND
37	I/O
38	I/O
39	I/O
40	I/O
41	I/O
42	GND
43	V_{CC}
44	I/O

Pin Number	A1425A Function
45	I/O
46	I/O
47	I/O
48	PRB, I/O
49	I/O
50	HCLK, I/O
51	I/O
52	I/O
53	I/O
54	I/O
55	I/O
56	I/O
57	I/O
58	GND
59	V_{CC}
60	I/O
61	I/O
62	I/O
63	I/O
64	IOPCL, I/O
65	GND
66	NC
67	NC
68	I/O
69	I/O
70	I/O
71	I/O
72	I/O
73	I/O
74	GND
75	V_{CC}
76	I/O
77	I/O
78	V_{CC}
79	I/O
80	I/O
81	I/O
82	I/O
83	I/O
84	I/O
85	I/O
86	I/O
87	I/O
88	I/O

Pin Number	A1425A Function
89	V_{CC}
90	GND
91	V_{CC}
92	GND
93	I/O
94	I/O
95	I/O
96	I/O
97	I/O
98	IOCLK, I/O
99	NC
100	NC
101	GND
102	I/O
103	I/O
104	I/O
105	I/O
106	GND
107	V_{CC}
108	I/O
109	I/O
110	I/O
111	I/O
112	I/O
113	I/O
114	I/O
115	I/O
116	CLKA, I/O
117	CLKB, I/O
118	PRA, I/O
119	I/O
120	I/O
121	I/O
122	GND
123	V_{CC}
124	I/O
125	I/O
126	I/O
127	I/O
128	I/O
129	I/O
130	I/O
131	DCLK, I/O
132	NC

256-Pin CQFP (Continued)

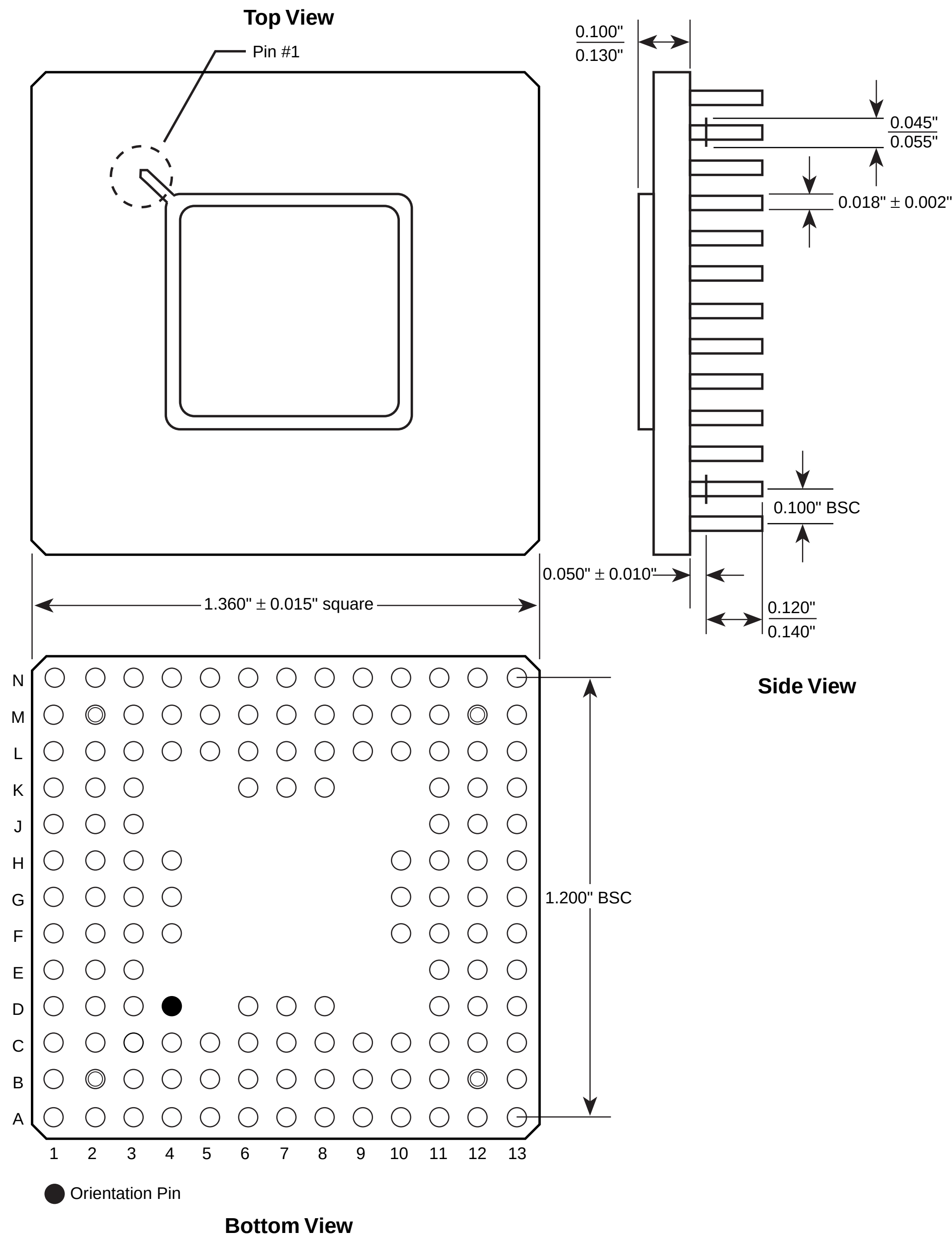
Pin Number	A14100A Function	A32200DX Function
133	I/O	I/O
134	I/O	I/O
135	I/O	I/O
136	I/O	I/O
137	I/O	I/O
138	I/O	I/O
139	I/O	GND
140	I/O	I/O
141	V_{CC}	I/O
142	I/O	I/O
143	I/O	I/O
144	I/O	I/O
145	I/O	I/O
146	I/O	I/O
147	I/O	I/O
148	I/O	I/O
149	I/O	I/O
150	I/O	I/O
151	I/O	I/O
152	I/O	I/O
153	I/O	I/O
154	I/O	I/O
155	I/O	V_{CC}
156	I/O	I/O
157	I/O	I/O
158	GND	V_{CC}
159	V_{CC}	V_{CC}
160	GND	GND
161	V_{CC}	I/O
162	I/O	I/O
163	I/O	I/O
164	I/O	I/O
165	I/O	GND
166	I/O	I/O
167	I/O	I/O
168	I/O	I/O
169	I/O	I/O
170	I/O	V_{CC}
171	I/O	I/O
172	I/O	I/O
173	I/O	I/O
174	V_{CC}	I/O

Pin Number	A14100A Function	A32200DX Function
175	GND	I/O
176	GND	I/O
177	I/O	I/O
178	I/O	I/O
179	I/O	I/O
180	I/O	GND
181	I/O	I/O
182	I/O	I/O
183	I/O	I/O
184	I/O	I/O
185	I/O	I/O
186	I/O	I/O
187	I/O	I/O
188	IOCLK, I/O	MODE
189	GND	V_{CC}
190	I/O	GND
191	I/O	NC
192	I/O	NC
193	I/O	NC
194	I/O	I/O
195	I/O	DCLK, I/O
196	I/O	I/O
197	I/O	I/O
198	I/O	I/O
199	I/O	I/O (WD)
200	I/O	I/O (WD)
201	I/O	V_{CC}
202	I/O	I/O
203	I/O	I/O
204	I/O	I/O
205	I/O	I/O
206	I/O	GND
207	I/O	I/O
208	I/O	I/O
209	I/O	QCLKC, I/O
210	I/O	I/O
211	I/O	I/O (WD)
212	I/O	I/O (WD)
213	I/O	I/O
214	I/O	I/O
215	I/O	I/O (WD)
216	I/O	I/O (WD)

Pin Number	A14100A Function	A32200DX Function
217	I/O	I/O
218	I/O	PRB, I/O
219	CLKA, I/O	I/O
220	CLKB, I/O	CLKB, I/O
221	V_{CC}	I/O
222	GND	GND
223	V_{CC}	GND
224	GND	V_{CC}
225	PRA, I/O	V_{CC}
226	I/O	I/O
227	I/O	CLKA, I/O
228	I/O	I/O
229	I/O	PRA, I/O
230	I/O	I/O
231	I/O	I/O
232	I/O	I/O (WD)
233	I/O	I/O (WD)
234	I/O	I/O
235	I/O	I/O
236	I/O	I/O
237	I/O	I/O
238	I/O	I/O
239	I/O	I/O
240	GND	QCLKD, I/O
241	I/O	I/O
242	I/O	I/O (WD)
243	I/O	GND
244	I/O	I/O (WD)
245	I/O	I/O
246	I/O	I/O
247	I/O	I/O
248	I/O	V_{CC}
249	I/O	I/O
250	I/O	I/O (WD)
251	I/O	I/O (WD)
252	I/O	I/O
253	I/O	SDI, I/O
254	I/O	I/O
255	I/O	GND
256	DCLK, I/O	NC

Package Mechanical Drawings (continued)

133-Pin CPGA



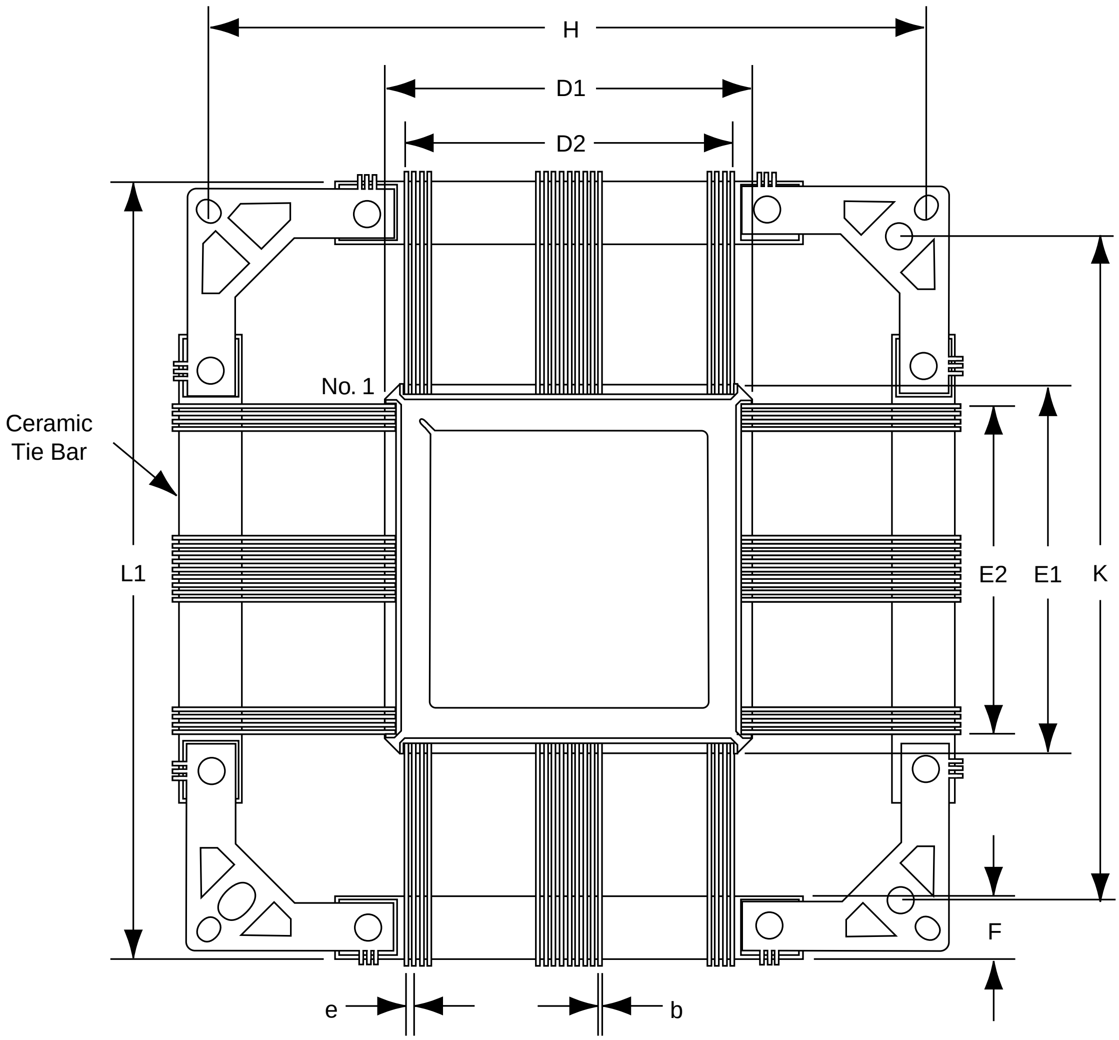
Notes:

1. *All dimensions are in inches unless otherwise stated.*
2. *BSC—Basic Spacing between Centers. This is a theoretical true position dimension and so has no tolerance.*

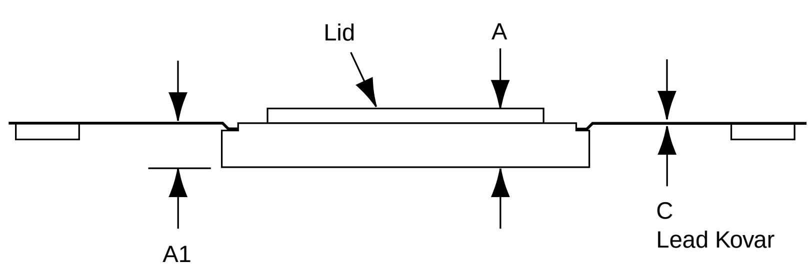
Package Mechanical Drawings (continued)

132-Pin, 172-Pin, 196-Pin, 208-Pin, and 256-Pin CQFP (Cavity Up)

Top View



Side View



Notes:

1. *Outside leadframe holes (from dimension H) are circular for the CQ208 and CQ256.*
2. *Seal ring and lid are connected to Ground.*
3. *Lead material is Kovar with minimum 50 microinches gold plate over nickel.*
4. *Packages are shipped unformed with the ceramic tie bar.*
5. *32200DX – CQ208 has a heat sink on the back.*

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