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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	547
Number of Logic Elements/Cells	-
Total RAM Bits	-
Number of I/O	69
Number of Gates	2000
Voltage - Supply	4.5V ~ 5.5V
Mounting Type	Surface Mount
Operating Temperature	-55°C ~ 125°C (TJ)
Package / Case	84-CQFP Exposed Pad and Tie Bar
Supplier Device Package	84-CQFP (42x42)
Purchase URL	https://www.e-xfl.com/product-detail/microsemi/a1020b-cq84b

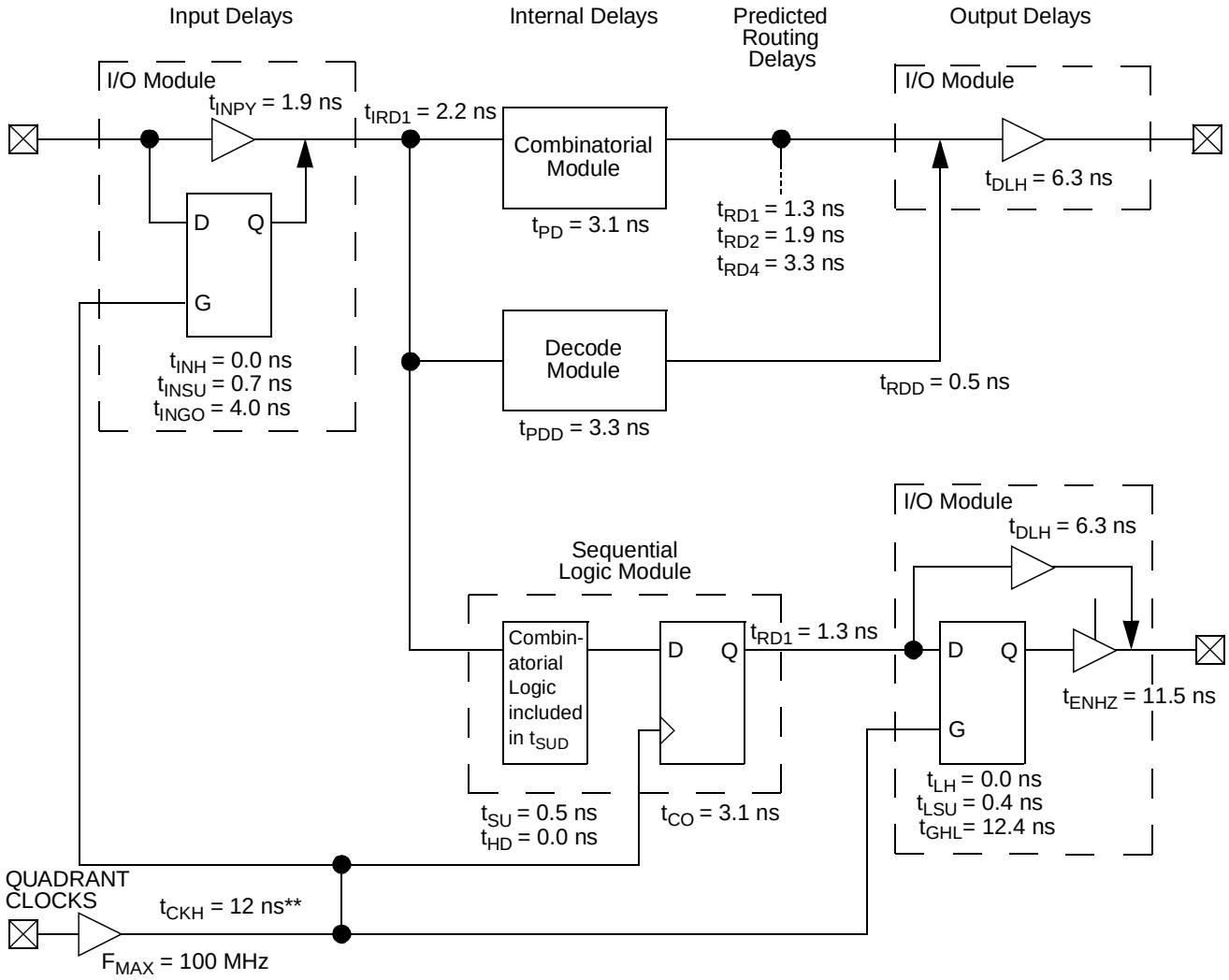
Actel Extended Flow[1]

Step	Screen	Method	Require-ment
1.	Wafer Lot Acceptance[2]	5007 with Step Coverage Waiver	All Lots
2.	Destructive In-Line Bond Pull[3]	2011, Condition D	Sample
3.	Internal Visual	2010, Condition A	100%
4.	Serialization		100%
5.	Temperature Cycling	1010, Condition C	100%
6.	Constant Acceleration	2001, Condition D or E, Y_1 Orientation Only	100%
7.	Particle Impact Noise Detection	2020, Condition A	100%
8.	Radiographic	2012 (one view only)	100%
9.	Pre-Burn-In Test	In accordance with applicable Actel device specification	100%
10.	Burn-in Test	1015, Condition D, 240 hours @ 125°C minimum	100%
11.	Interim (Post-Burn-In) Electrical Parameters	In accordance with applicable Actel device specification	100%
12.	Reverse Bias Burn-In	1015, Condition C, 72 hours @ 150°C minimum	100%
13.	Interim (Post-Burn-In) Electrical Parameters	In accordance with applicable Actel device specification	100%
14.	Percent Defective Allowable (PDA) Calculation	5%, 3% Functional Parameters @ 25°C	All Lots
15.	Final Electrical Test	In accordance with Actel applicable device specification which includes a, b, and c:	100%
	a. Static Tests		100%
	(1) 25°C (Subgroup 1, Table1)	5005	
	(2) –55°C and +125°C (Subgroups 2, 3, Table 1)	5005	
	b. Functional Tests		100%
	(1) 25°C (Subgroup 7, Table 15)	5005	
	(2) –55°C and +125°C (Subgroups 8A and B, Table 1)	5005	
	c. Switching Tests at 25°C (Subgroup 9, Table 1)	5005	100%
16.	Seal	1014	100%
	a. Fine		
	b. Gross		
17.	External Visual	2009	100%

Notes:

1. Actel offers the extended flow for customers who require additional screening beyond the requirements of the MIL-STD-883 Cla compliant to the requirements of MIL-STD-883, Paragraph 1.2.1, and MIL-I-38535, Appendix A. Actel is offering this incorporating the majority of the screening procedures as outlined in Method 5004 of MIL-STD-883, Class S. The exceptions to Me are shown in notes 2 and 3 below.
2. Wafer lot acceptance is performed to Method 5007; however, the step coverage requirement as specified in Method 2018 must be
3. MIL-STD-883, Method 5004 requires 100 percent Radiation latch-up testing (Method 1020). Actel will not be performing this testing, and this requirement must be waived in its entirety.

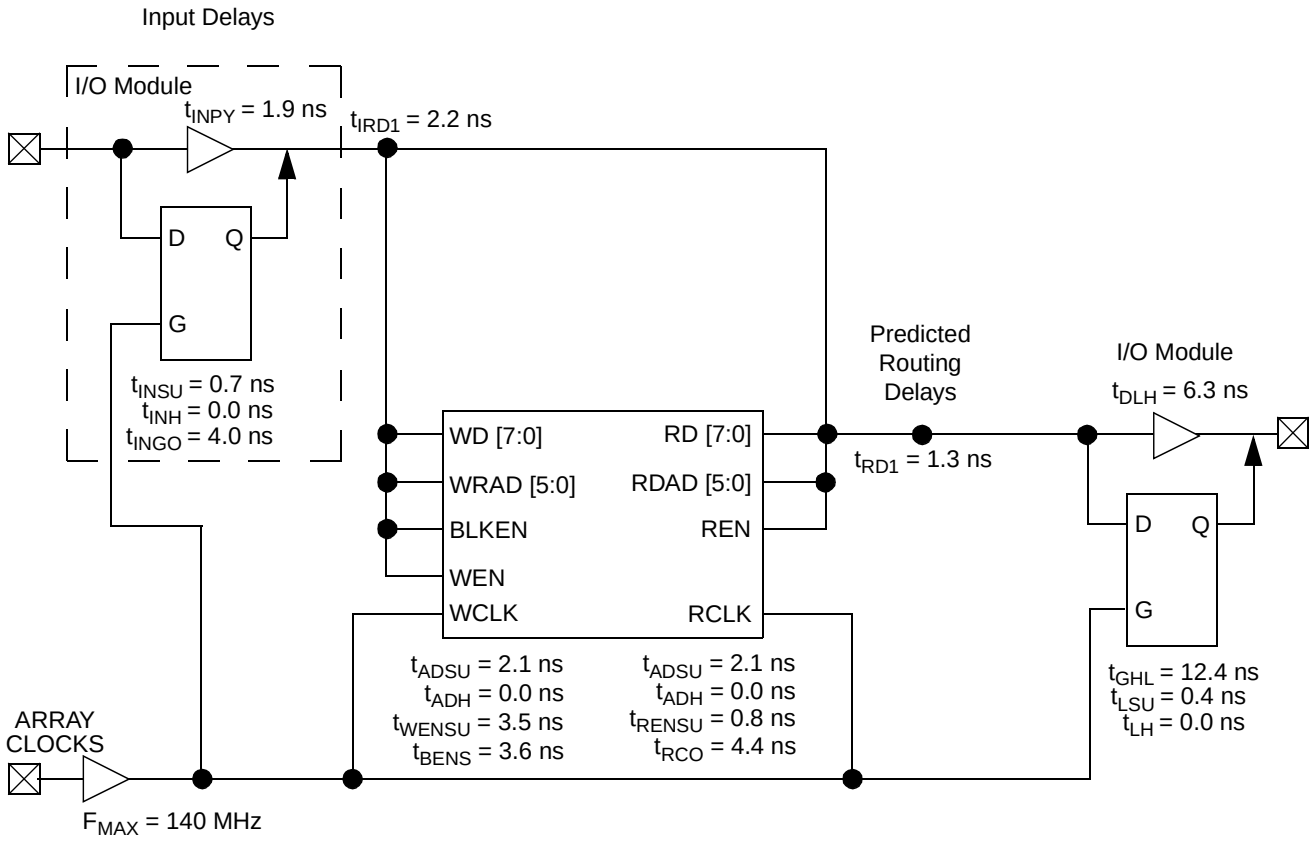
3200DX Timing Model (Logic Functions using Quadrant Clocks)*



* Values shown for A32100DX–1 at worst-case military conditions.

** Load dependent.

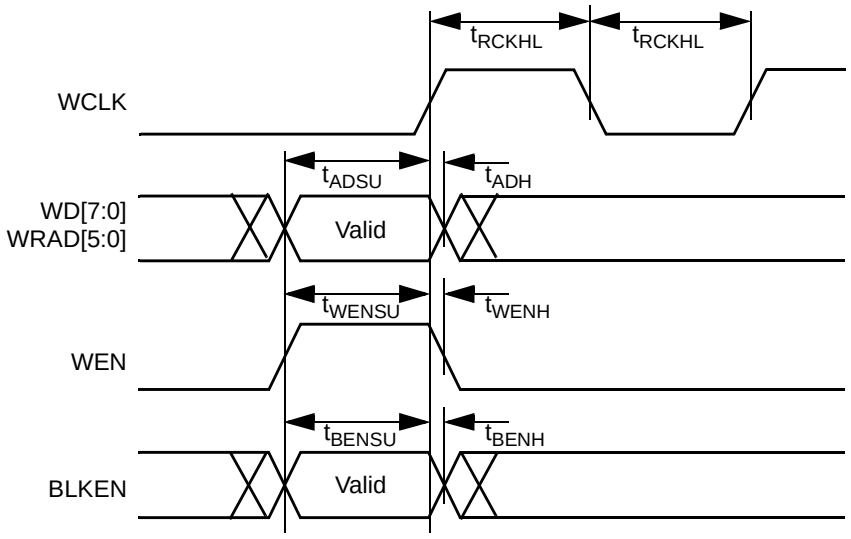
3200DX Timing Model (SRAM Functions)*



*Values shown for A32100DX–1 at worst-case military conditions.

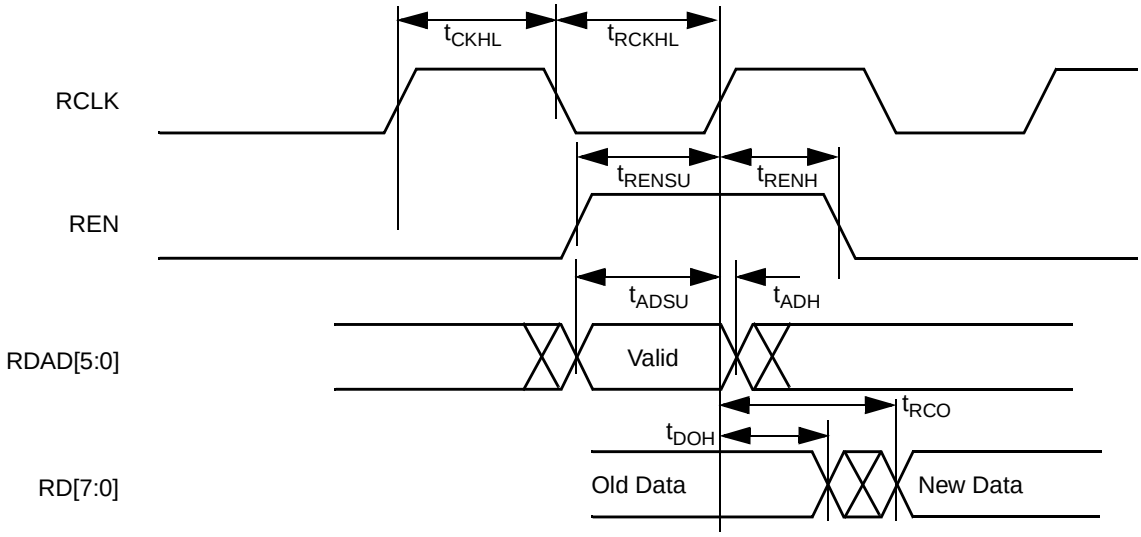
Dual-Port SRAM Timing Waveforms

3200DX SRAM Write Operation



Note: Identical timing for falling-edge clock.

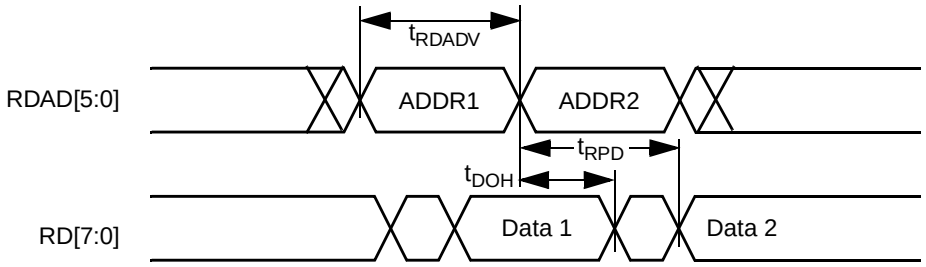
3200DX SRAM Synchronous Read Operation



Note: Identical timing for falling-edge clock.

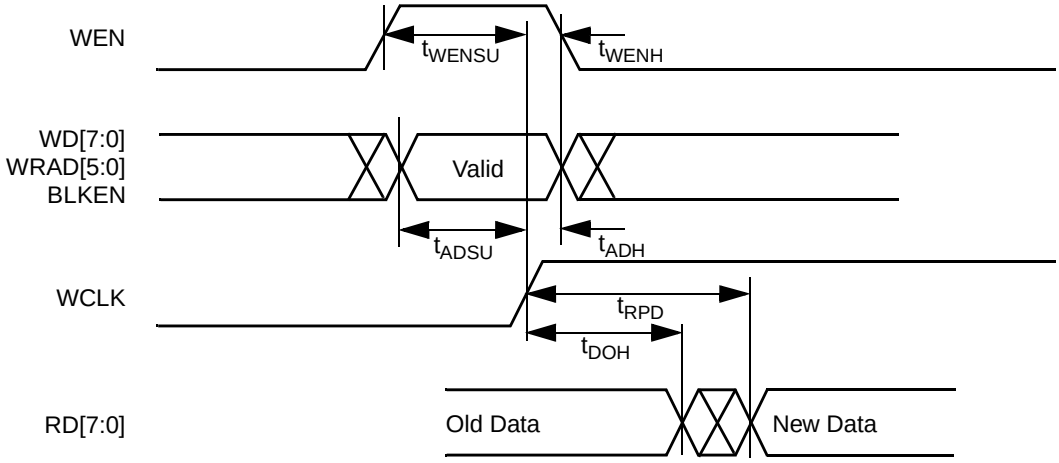
3200DX SRAM Asynchronous Read Operation Type 1

(Read Address Controlled)



3200DX SRAM Asynchronous Read Operation Type 2

(Write Address Controlled)



ACT 1 Timing Characteristics (continued)

(Worst-Case Military Conditions, V_{CC} = 4.5V, T_J = 125°C)

			'–1' Speed		'Std' Speed		
Parameter	Description		Min.	Max.	Min.	Max.	Units
Global Clock Network							
t_{CKH}	Input Low to High	FO = 16 FO = 128		7.8 8.9		9.2 10.5	ns
t_{CKL}	Input High to Low	FO = 16 FO = 128		10.3 11.2		12.1 13.2	ns
t_{PWH}	Minimum Pulse Width High	FO = 16 FO = 128	10.4 10.9		12.2 12.9		ns
t_{PWL}	Minimum Pulse Width Low	FO = 16 FO = 128	10.4 10.9		12.2 12.9		ns
t_{CKSW}	Maximum Skew	FO = 16 FO = 128		1.9 2.9		2.2 3.4	ns
t_P	Minimum Period	FO = 16 FO = 128	21.7 23.2		25.6 27.3		ns
f_{MAX}	Maximum Frequency	FO = 16 FO = 128		46 44		40 37	MHz
TTL Output Module Timing [1]							
t_{DLH}	Data to Pad High			12.1		14.2	ns
t_{DHL}	Data to Pad Low			13.8		16.3	ns
t_{ENZH}	Enable Pad Z to High			12.0		14.1	ns
t_{ENZL}	Enable Pad Z to Low			14.6		17.1	ns
t_{ENHZ}	Enable Pad High to Z			16.0		18.8	ns
t_{ENLZ}	Enable Pad Low to Z			14.5		17.0	ns
d_{TLH}	Delta Low to High			0.09		0.11	ns/pF
d_{THL}	Delta High to Low			0.12		0.15	ns/pF
CMOS Output Module Timing [1]							
t_{DLH}	Data to Pad High			15.1		17.7	ns
t_{DHL}	Data to Pad Low			11.5		13.6	ns
t_{ENZH}	Enable Pad Z to High			12.0		14.1	ns
t_{ENZL}	Enable Pad Z to Low			14.6		17.1	ns
t_{ENHZ}	Enable Pad High to Z			16.0		18.8	ns
t_{ENLZ}	Enable Pad Low to Z			14.5		17.0	ns
d_{TLH}	Delta Low to High			0.16		0.18	ns/pF
d_{THL}	Delta High to Low			0.09		0.11	ns/pF

Notes:

1. Delays based on 50 pF loading.
2. SSO information can be found in the Simultaneously Switching Output Limits for Actel FPGAs application note at http://www.actel.com/appnotes

A1240A Timing Characteristics (continued)

(Worst-Case Military Conditions, V_{CC} = 4.5V, T_J = 125°C)

			'–1' Speed		'Std' Speed		
Parameter	Description		Min.	Max.	Min.	Max.	Units
Input Module Propagation Delays							
t_{INYH}	Pad to Y High			4.0		4.7	ns
t_{INYL}	Pad to Y Low			3.6		4.3	ns
t_{INGH}	G to Y High			6.9		8.1	ns
t_{INGL}	G to Y Low			6.6		7.7	ns
Input Module Predicted Routing Delays [1]							
t_{IRD1}	FO=1 Routing Delay			5.8		6.9	ns
t_{IRD2}	FO=2 Routing Delay			6.7		7.8	ns
t_{IRD3}	FO=3 Routing Delay			7.5		8.8	ns
t_{IRD4}	FO=4 Routing Delay			8.2		9.7	ns
t_{IRD8}	FO=8 Routing Delay			10.9		12.9	ns
Global Clock Network							
t_{CKH}	Input Low to High	FO = 32 FO = 256		13.3 16.3		15.7 19.2	ns
t_{CKL}	Input High to Low	FO = 32 FO = 256		13.3 16.5		15.7 19.5	ns
t_{PWH}	Minimum Pulse Width High	FO = 32 FO = 256	5.7 6.0		6.7 7.1		ns
t_{PWL}	Minimum Pulse Width Low	FO = 32 FO = 256	5.7 6.0		6.7 7.1		ns
t_{CKSW}	Maximum Skew	FO = 32 FO = 256		0.6 3.1		0.6 3.1	ns
t_{SUEXT}	Input Latch External Setup	FO = 32 FO = 256	0.0 0.0		0.0 0.0		ns
t_{HEXT}	Input Latch External Hold	FO = 32 FO = 256	8.6 13.8		8.6 13.8		ns
t_P	Minimum Period	FO = 32 FO = 256	11.5 12.2		13.5 14.3		ns
f_{MAX}	Maximum Frequency	FO = 32 FO = 256		87 82		74 70	MHz

Note:

1. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used before estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment. Optimization techniques may further reduce delays by 0 to 4 ns.

A14100A Timing Characteristics (continued)

(Worst-Case Military Conditions, V_{CC} = 4.5V, T_J = 125°C)

		'–1' Speed		'Std' Speed		
Parameter	Description	Min.	Max.	Min.	Max.	Units
I/O Module Sequential Timing						
t_{INH}	Input F-F Data Hold (w.r.t. IOCLK Pad)	0.0		0.0		ns
t_{INSU}	Input F-F Data Setup (w.r.t. IOCLK Pad)	2.1		2.4		ns
t_{IDEH}	Input Data Enable Hold (w.r.t. IOCLK Pad)	0.0		0.0		ns
t_{IDESU}	Input Data Enable Setup (w.r.t. IOCLK Pad)	8.7		10.0		ns
t_{OUTH}	Output F-F Data Hold (w.r.t. IOCLK Pad)	1.2		1.2		ns
t_{OUTSU}	Output F-F Data Setup (w.r.t. IOCLK Pad)	1.2		1.2		ns
t_{ODEH}	Output Data Enable Hold (w.r.t. IOCLK Pad)	0.6		0.6		ns
t_{ODESU}	Output Data Enable Setup (w.r.t. IOCLK Pad)	2.4		2.4		ns
TTL Output Module Timing [1]						
t_{DHS}	Data to Pad, High Slew		7.5		8.9	ns
t_{DLS}	Data to Pad, Low Slew		11.9		14.0	ns
t_{ENZHS}	Enable to Pad, Z to H/L, High Slew		6.0		7.0	ns
t_{ENZLS}	Enable to Pad, Z to H/L, Low Slew		10.9		12.8	ns
t_{ENHSZ}	Enable to Pad, H/L to Z, High Slew		11.9		14.0	ns
t_{ENLSZ}	Enable to Pad, H/L to Z, Low Slew		10.9		12.8	ns
t_{CKHS}	IOCLK Pad to Pad H/L, High Slew		12.2		14.0	ns
t_{CKLS}	IOCLK Pad to Pad H/L, Low Slew		17.8		17.8	ns
d_{TLHHS}	Delta Low to High, High Slew		0.04		0.04	ns/pF
d_{TLHLS}	Delta Low to High, Low Slew		0.07		0.08	ns/pF
d_{THLHS}	Delta High to Low, High Slew		0.05		0.06	ns/pF
d_{THLLS}	Delta High to Low, Low Slew		0.07		0.08	ns/pF

Note:

1. Delays based on 35 pF loading.

A32100DX Timing Characteristics

(Worst-Case Military Conditions, V_{CC} = 4.5V, T_J = 125°C)

		'–1' Speed		'Std' Speed		
Parameter	Description	Min.	Max.	Min.	Max.	Units
Logic Module Combinatorial Functions						
t_{PD}	Internal Array Module Delay		3.1		4.1	ns
t_{PDD}	Internal Decode Module Delay		3.3		4.3	ns
Logic Module Predicted Routing Delays [1]						
t_{RD1}	FO=1 Routing Delay		1.3		1.8	ns
t_{RD2}	FO=2 Routing Delay		1.9		2.6	ns
t_{RD3}	FO=3 Routing Delay		2.6		3.4	ns
t_{RD4}	FO=4 Routing Delay		3.3		4.3	ns
t_{RD5}	FO=8 Routing Delay		0.6		0.8	ns
t_{RDD}	Decode-to-Output Routing Delay		0.5		0.6	ns
Logic Module Sequential Timing						
t_{CO}	Flip-Flop Clock-to-Output		3.1		4.1	ns
t_{GO}	Latch Gate-to-Output		3.1		4.1	ns
t_{SU}	Flip-Flop (Latch) Setup Time	0.5		0.6		ns
t_H	Flip-Flop (Latch) Hold Time	0.0		0.0		ns
t_{RO}	Flip-Flop (Latch) Reset to Output		3.1		4.1	ns
t_{SUENA}	Flip-Flop (Latch) Enable Setup	0.9		1.2		ns
t_{HENA}	Flip-Flop (Latch) Enable Hold	0.0		0.0		ns
t_{WCLKA}	Flip-Flop (Latch) Clock Active Pulse Width	4.3		5.8		ns
t_{WASYN}	Flip-Flop (Latch) Asynchronous Pulse Width	5.6		7.5		ns

Note:

1. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.

A32100DX Timing Characteristics (continued)

(Worst-Case Military Conditions, V_{CC} = 4.5V, T_J = 125°C)

		'–1' Speed		'Std' Speed		
Parameter	Description	Min.	Max.	Min.	Max.	Units
TTL Output Module Timing [1]						
t_{DLH}	Data to Pad High		5.1		6.8	ns
t_{DHL}	Data to Pad Low		6.3		8.3	ns
t_{ENZH}	Enable Pad Z to High		6.6		8.8	ns
t_{ENZL}	Enable Pad Z to Low		7.1		9.4	ns
t_{ENHZ}	Enable Pad High to Z		11.5		15.3	ns
t_{ENLZ}	Enable Pad Low to Z		11.5		15.3	ns
t_{GLH}	G to Pad High		11.5		15.3	ns
t_{GHL}	G to Pad Low		12.4		16.6	ns
t_{LSU}	I/O Latch Output Setup	0.4		0.5		ns
t_{LH}	I/O Latch Output Hold	0.0		0.0		ns
t_{LCO}	I/O Latch Clock-Out (Pad-to-Pad) 32 I/O		11.5		15.4	ns
t_{ACO}	Array Latch Clock-Out (Pad-to-Pad) 32 I/O		16.3		21.7	ns
d_{TLH}	Capacitive Loading, Low to High		0.04		0.06	ns/pF
d_{THL}	Capacitive Loading, High to Low		0.06		0.08	ns/pF
t_{WDO}	Hard-Wired Wide Decode Output		0.05		0.07	ns
CMOS Output Module Timing [1]						
t_{DLH}	Data to Pad High		6.3		8.3	ns
t_{DHL}	Data to Pad Low		5.1		6.8	ns
t_{ENZH}	Enable Pad Z to High		6.6		8.8	ns
t_{ENZL}	Enable Pad Z to Low		7.1		9.4	ns
t_{ENHZ}	Enable Pad High to Z		11.5		15.3	ns
t_{ENLZ}	Enable Pad Low to Z		11.5		15.3	ns
t_{GLH}	G to Pad High		11.5		15.3	ns
t_{GHL}	G to Pad Low		12.4		16.6	ns
t_{LSU}	I/O Latch Setup	0.4		0.5		ns
t_{LH}	I/O Latch Hold	0.0		0.0		ns
t_{LCO}	I/O Latch Clock-Out (Pad-to-Pad) 32 I/O		13.7		18.2	ns
t_{ACO}	Array Latch Clock-Out (Pad-to-Pad) 32 I/O		19.2		25.6	ns
d_{TLH}	Capacitive Loading, Low to High		0.06		0.08	ns/pF
d_{THL}	Capacitive Loading, High to Low		0.05		0.07	ns/pF
t_{WDO}	Hard-Wired Wide Decode Output		0.05		0.07	ns

Notes:

1. Delays based on 35 pF loading.
2. SSO information can be found in the Simultaneously Switching Output Limits for Actel FPGAs application note at http://www.actel.com/appnotes

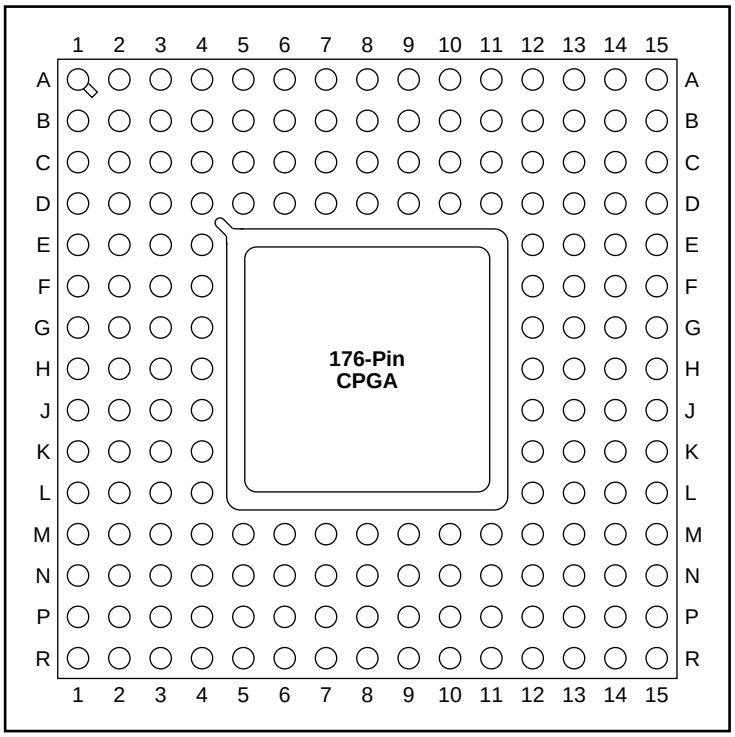
84-Pin CPGA

Pin Number	A1010B Function	A1020B Function
A1	I/O	I/O
A2	I/O	I/O
A3	I/O	I/O
A4	I/O	I/O
A5	I/O	I/O
A6	I/O	I/O
A7	I/O	I/O
A8	I/O	I/O
A9	I/O	I/O
A10	I/O	I/O
A11	PRA, I/O	PRA, I/O
B1	NC	I/O
B2	NC	NC
B3	I/O	I/O
B4	I/O	I/O
B5	V_{CC}	V_{CC}
B6	I/O	I/O
B7	GND	GND
B8	I/O	I/O
B9	I/O	I/O
B10	PRB, I/O	PRB, I/O
B11	SDI, I/O	SDI, I/O
C1	NC	I/O
C2	NC	I/O
C5	I/O	I/O
C6	I/O	I/O
C7	I/O	I/O
C10	DCLK, I/O	DCLK, I/O
C11	NC	I/O
D1	I/O	I/O
D2	I/O	I/O
D10	NC	I/O
D11	NC	I/O
E1	I/O	I/O
E2	GND	GND
E3	GND	GND
E9	V_{CC}	V_{CC}
E10	V_{CC}	V_{CC}
E11	MODE	MODE
F1	V_{CC}	V_{CC}
F2	I/O	I/O
F3	I/O	I/O

Pin Number	A1010B Function	A1020B Function
F9	CLK, I/O	CLK, I/O
F10	GND	GND
F11	I/O	I/O
G1	I/O	I/O
G2	V_{CC}	V_{CC}
G3	I/O	I/O
G9	I/O	I/O
G10	GND	GND
G11	I/O	I/O
H1	I/O	I/O
H2	I/O	I/O
H10	I/O	I/O
H11	I/O	I/O
J1	I/O	I/O
J2	NC	I/O
J5	I/O	I/O
J6	I/O	I/O
J7	I/O	I/O
J10	NC	I/O
J11	I/O	I/O
K1	NC	I/O
K2	V_{CC}	V_{CC}
K3	I/O	I/O
K4	I/O	I/O
K5	GND	GND
K6	I/O	I/O
K7	V_{CC}	V_{CC}
K8	I/O	I/O
K9	I/O	I/O
K10	NC	I/O
K11	NC	I/O
L1	NC	I/O
L2	I/O	I/O
L3	I/O	I/O
L4	I/O	I/O
L5	I/O	I/O
L6	I/O	I/O
L7	I/O	I/O
L8	I/O	I/O
L9	I/O	I/O
L10	I/O	I/O
L11	I/O	I/O

Package Pin Assignments (continued)

176-Pin CPGA (Top View)



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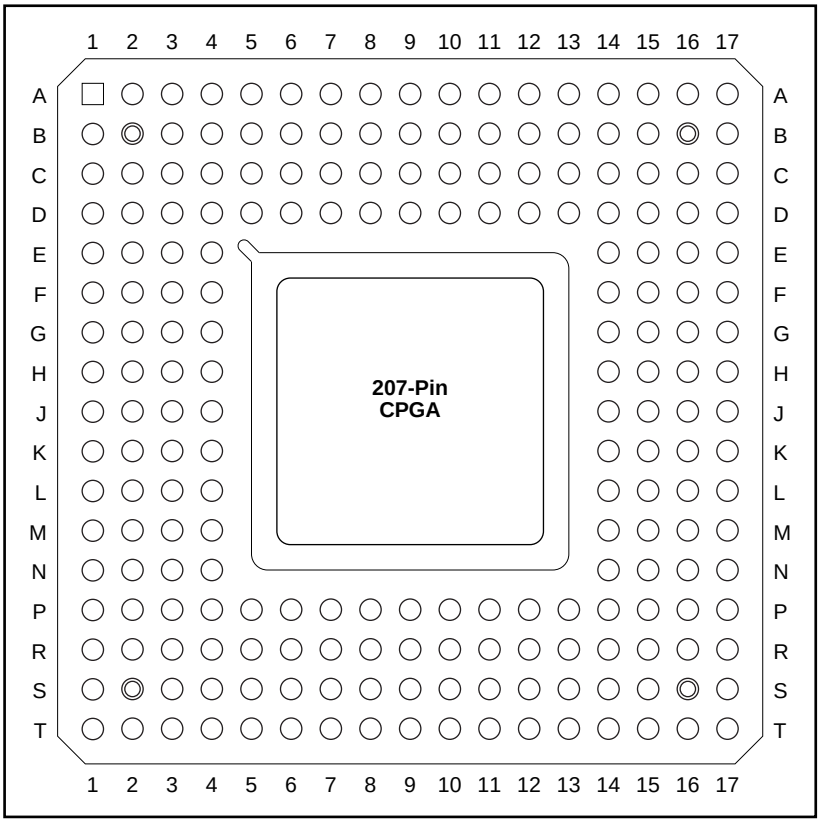
Package Pin Assignments (continued)

207-Pin CPGA (Top View)



257-Pin CPGA

Pin Number	A14100A Function
A1	I/O
A2	I/O
A3	I/O
A4	I/O
A5	MODE
A6	I/O
A7	I/O
A8	I/O
A9	I/O
A10	I/O
A11	I/O
A12	I/O
A13	I/O
A14	I/O
A15	I/O
A16	I/O
A17	I/O
A18	I/O
A19	I/O
B1	I/O
B2	I/O
B3	I/O
B4	SDI, I/O
B5	I/O
B6	I/O
B7	I/O
B8	I/O
B9	I/O
B10	I/O
B11	I/O
B12	I/O
B13	I/O
B14	I/O
B15	I/O
B16	GND
B17	I/O
B18	I/O
B19	I/O
C1	I/O
C2	I/O
C3	V_{CC}
C4	GND
C5	I/O
C6	I/O

Pin Number	A14100A Function
C7	I/O
C8	I/O
C9	I/O
C10	V_{CC}
C11	I/O
C12	I/O
C13	V_{CC}
C14	I/O
C15	I/O
C16	I/O
C17	V_{CC}
C18	I/O
C19	I/O
D1	I/O
D2	I/O
D3	I/O
D4	GND
D5	I/O
D6	I/O
D7	I/O
D8	I/O
D9	I/O
D10	GND
D11	I/O
D12	I/O
D13	I/O
D14	I/O
D15	I/O
D16	GND
D17	I/O
D18	I/O
D19	I/O
E1	I/O
E2	I/O
E3	I/O
E4	DCLK, I/O
E5	NC
E7	I/O
E9	I/O
E11	GND
E13	I/O
E16	I/O
E17	I/O
E18	I/O

Pin Number	A14100A Function
E19	I/O
F1	I/O
F2	I/O
F3	I/O
F4	I/O
F16	I/O
F17	I/O
F18	I/O
F19	I/O
G1	I/O
G2	I/O
G3	I/O
G4	I/O
G5	I/O
G15	I/O
G16	I/O
G17	I/O
G18	I/O
G19	I/O
H1	I/O
H2	I/O
H3	I/O
H4	I/O
H16	I/O
H17	I/O
H18	I/O
H19	I/O
J1	PRA, I/O
J2	I/O
J3	I/O
J4	I/O
J5	GND
J15	I/O
J16	HCLK, I/O
J17	PRB, I/O
J18	I/O
J19	I/O
K1	I/O
K2	I/O
K3	V_{CC}
K4	GND
K16	GND
K17	V_{CC}
K18	I/O

257-Pin CPGA (Continued)

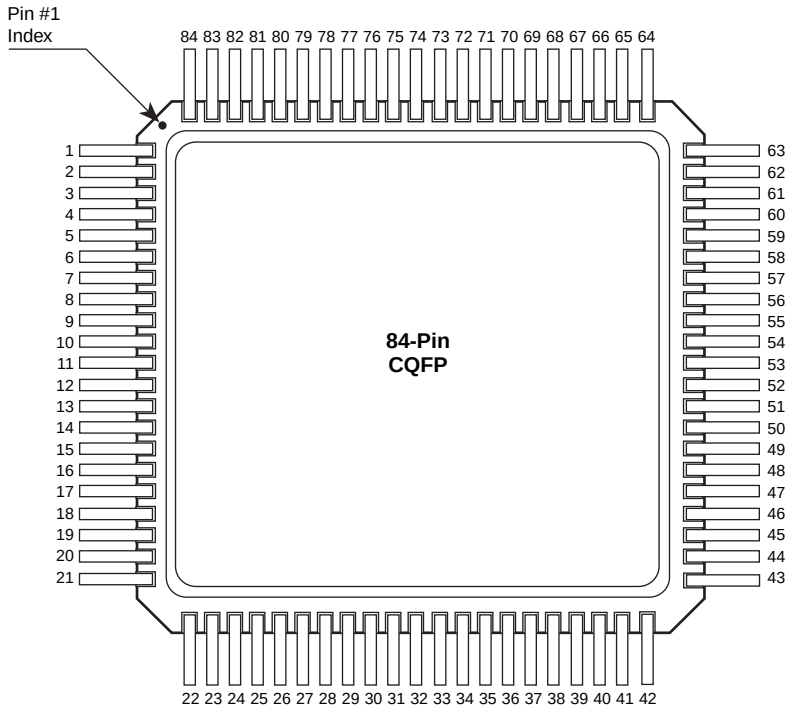
Pin Number	A14100A Function
K19	I/O
L1	I/O
L2	I/O
L3	I/O
L4	CLKA, I/O
L5	CLKB, I/O
L15	GND
L16	I/O
L17	I/O
L18	I/O
L19	I/O
M1	I/O
M2	I/O
M3	I/O
M4	I/O
M16	I/O
M17	I/O
M18	I/O
M19	I/O
N1	I/O
N2	I/O
N3	I/O
N4	I/O
N5	I/O
N15	I/O
N16	I/O
N17	I/O
N18	I/O
N19	I/O
P1	I/O
P2	I/O
P3	I/O
P4	I/O
P16	I/O
P17	I/O
P18	I/O
P19	I/O
R1	I/O
R2	I/O
R3	I/O
R4	GND
R7	I/O

Pin Number	A14100A Function
R9	I/O
R11	I/O
R13	I/O
R16	IOPCL, I/O
R17	I/O
R18	I/O
R19	I/O
T1	I/O
T2	I/O
T3	I/O
T4	GND
T5	IOCLK, I/O
T6	I/O
T7	I/O
T8	I/O
T9	I/O
T10	GND
T11	I/O
T12	I/O
T13	I/O
T14	I/O
T15	I/O
T16	GND
T17	GND
T18	I/O
T19	I/O
V1	I/O
V2	I/O
V3	V_{CC}
V4	I/O
V5	I/O
V6	I/O
V7	V_{CC}
V8	I/O
V9	I/O
V10	V_{CC}
V11	I/O
V12	I/O
V13	I/O
V14	I/O
V15	I/O
V16	I/O

Pin Number	A14100A Function
V17	V_{CC}
V18	I/O
V19	I/O
X1	I/O
X2	I/O
X3	I/O
X4	I/O
X5	I/O
X6	I/O
X7	GND
X8	I/O
X9	I/O
X10	I/O
X11	I/O
X12	I/O
X13	I/O
X14	V_{CC}
X15	I/O
X16	I/O
X17	I/O
X18	I/O
X19	I/O
Y1	I/O
Y2	I/O
Y3	I/O
Y4	I/O
Y5	I/O
Y6	I/O
Y7	I/O
Y8	I/O
Y9	I/O
Y10	I/O
Y11	I/O
Y12	I/O
Y13	I/O
Y14	I/O
Y15	I/O
Y16	I/O
Y17	I/O
Y18	I/O
Y19	I/O

Package Pin Assignments (continued)

84-Pin CQFP (Top View)



172-Pin CQFP

Pin Number	A1280A Function	A1280XL Function
1	MODE	MODE
2	I/O	I/O
3	I/O	I/O
4	I/O	I/O
5	I/O	I/O
6	I/O	I/O
7	GND	GND
8	I/O	I/O
9	I/O	I/O
10	I/O	I/O
11	I/O	I/O
12	V_{CC}	V_{CC}
13	I/O	I/O
14	I/O	I/O
15	I/O	I/O
16	I/O	I/O
17	GND	GND
18	I/O	I/O
19	I/O	I/O
20	I/O	I/O
21	I/O	I/O
22	GND	GND
23	V_{CC}	V_{CC}
24	V_{CC}	V_{CC}
25	I/O	I/O
26	I/O	I/O
27	V_{CC}	V_{CC}
28	I/O	I/O
29	I/O	I/O
30	I/O	I/O
31	I/O	I/O
32	GND	GND
33	I/O	I/O
34	I/O	I/O
35	I/O	I/O
36	I/O	I/O
37	GND	GND
38	I/O	I/O
39	I/O	I/O
40	I/O	I/O
41	I/O	I/O
42	I/O	I/O
43	I/O	I/O
44	I/O	I/O

Pin Number	A1280A Function	A1280XL Function
45	I/O	I/O
46	I/O	I/O
47	I/O	I/O
48	I/O	I/O
49	I/O	I/O
50	V_{CC}	V_{CC}
51	I/O	I/O
52	I/O	I/O
53	I/O	I/O
54	I/O	I/O
55	GND	GND
56	I/O	I/O
57	I/O	I/O
58	I/O	I/O
59	I/O	I/O
60	I/O	I/O
61	I/O	I/O
62	I/O	I/O
63	I/O	I/O
64	I/O	I/O
65	GND	GND
66	V_{CC}	V_{CC}
67	I/O	I/O
68	I/O	I/O
69	I/O	I/O
70	I/O	I/O
71	I/O	I/O
72	I/O	I/O
73	I/O	I/O
74	I/O	I/O
75	GND	GND
76	I/O	I/O
77	I/O	I/O
78	I/O	I/O
79	I/O	I/O
80	V_{CC}	V_{CC}
81	I/O	I/O
82	I/O	I/O
83	I/O	I/O
84	I/O	I/O
85	I/O	I/O
86	I/O	I/O
87	I/O	I/O
88	I/O	I/O

172-Pin CQFP (Continued)

Pin Number	A1280A Function	A1280XL Function
89	I/O	I/O
90	I/O	I/O
91	I/O	I/O
92	I/O	I/O
93	I/O	I/O
94	I/O	I/O
95	I/O	I/O
96	I/O	I/O
97	I/O	I/O
98	GND	GND
99	I/O	I/O
100	I/O	I/O
101	I/O	I/O
102	I/O	I/O
103	GND	GND
104	I/O	I/O
105	I/O	I/O
106	GND	GND
107	V_{CC}	V_{CC}
108	GND	GND
109	V_{CC}	V_{CC}
110	V_{CC}	V_{CC}
111	I/O	I/O
112	I/O	I/O
113	V_{CC}	V_{CC}
114	I/O	I/O
115	I/O	I/O
116	I/O	I/O
117	I/O	I/O
118	GND	GND
119	I/O	I/O
120	I/O	I/O
121	I/O	I/O
122	I/O	I/O
123	GND	GND
124	I/O	I/O
125	I/O	I/O
126	I/O	I/O
127	I/O	I/O
128	I/O	I/O
129	I/O	I/O
130	I/O	I/O

Pin Number	A1280A Function	A1280XL Function
131	SDI, I/O	SDI, I/O
132	I/O	I/O
133	I/O	I/O
134	I/O	I/O
135	I/O	I/O
136	V_{CC}	V_{CC}
137	I/O	I/O
138	I/O	I/O
139	I/O	I/O
140	I/O	I/O
141	GND	GND
142	I/O	I/O
143	I/O	I/O
144	I/O	I/O
145	I/O	I/O
146	I/O	I/O
147	I/O	I/O
148	PRA, I/O	PRA, I/O
149	I/O	I/O
150	CLKA, I/O	CLKA, I/O
151	V_{CC}	V_{CC}
152	GND	GND
153	I/O	I/O
154	CLKB, I/O	CLKB, I/O
155	I/O	I/O
156	PRB, I/O	PRB, I/O
157	I/O	I/O
158	I/O	I/O
159	I/O	I/O
160	I/O	I/O
161	GND	GND
162	I/O	I/O
163	I/O	I/O
164	I/O	I/O
165	I/O	I/O
166	V_{CC}	V_{CC}
167	I/O	I/O
168	I/O	I/O
169	I/O	I/O
170	I/O	I/O
171	DCLK, I/O	DCLK, I/O
172	I/O	I/O

196-Pin CQFP (Continued)

Pin Number	A1460A Function
130	I/O
131	I/O
132	I/O
133	I/O
134	I/O
135	I/O
136	I/O
137	V_{CC}
138	GND
139	GND
140	V_{CC}
141	I/O
142	I/O
143	I/O
144	I/O
145	I/O
146	I/O
147	I/O
148	IOCLK, I/O
149	GND
150	I/O
151	I/O
152	I/O

Pin Number	A1460A Function
153	I/O
154	I/O
155	V_{CC}
156	I/O
157	I/O
158	I/O
159	I/O
160	I/O
161	I/O
162	GND
163	I/O
164	I/O
165	I/O
166	I/O
167	I/O
168	I/O
169	I/O
170	I/O
171	I/O
172	CLKA, I/O
173	CLKB, I/O
174	PRA, I/O
175	I/O

Pin Number	A1460A Function
176	I/O
177	I/O
178	I/O
179	I/O
180	I/O
181	I/O
182	I/O
183	GND
184	I/O
185	I/O
186	I/O
187	I/O
188	I/O
189	V_{CC}
190	I/O
191	I/O
192	I/O
193	GND
194	I/O
195	I/O
196	DCLK, I/O