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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	547
Number of Logic Elements/Cells	-
Total RAM Bits	-
Number of I/O	69
Number of Gates	2000
Voltage - Supply	4.5V ~ 5.5V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	84-CQFP Exposed Pad and Tie Bar
Supplier Device Package	84-CQFP (42x42)
Purchase URL	https://www.e-xfl.com/product-detail/microsemi/a1020b-cq84c

Product Plan

	Speed Grade		Application			
3200DX Family	**Std**	**–1***	**C**	**M**	**B**	**E**
A32100DX Device						
84-pin Ceramic Quad Flat Pack (CQFP)	✔	✔	✔	✔	✔	—
A32200DX Device						
208-pin Ceramic Quad Flat Pack (CQFP)	✔	✔	✔	✔	✔	—
256-pin Ceramic Quad Flat Pack (CQFP)	✔	✔	✔	✔	✔	—
ACT 3 Family						
A1425A Device						
132-pin Ceramic Quad Flat Pack (CQFP)	✔	✔	✔	✔	✔	✔
133-pin Ceramic Pin Grid Array (CPGA)	✔	✔	✔	✔	✔	✔
A1460A Device						
196-pin Ceramic Quad Flat Pack (CQFP)	✔	✔	✔	✔	✔	✔
207-pin Ceramic Pin Grid Array (CPGA)	✔	✔	✔	✔	✔	✔
A14100A Device						
256-pin Ceramic Quad Flat Pack (CQFP)	✔	✔	✔	✔	✔	✔
257-pin Ceramic Pin Grid Array (CPGA)	✔	✔	✔	✔	✔	✔
1200XL Family						
A1280XL Device						
172-pin Ceramic Quad Flat Pack (CQFP)	✔	✔	✔	✔	✔	—
176-pin Ceramic Pin Grid Array (CPGA)	✔	✔	✔	✔	✔	—
ACT 2 Family						
A1240A Device						
132-pin Ceramic Pin Grid Array (CPGA)	✔	✔	✔	✔	✔	—
A1280A Device						
172-pin Ceramic Quad Flat Pack (CQFP)	✔	✔	✔	✔	✔	✔
176-pin Ceramic Pin Grid Array (CPGA)	✔	✔	✔	✔	✔	✔
ACT 1 Family						
A1010B Device						
84-pin Ceramic Pin Grid Array (CPGA)	✔	✔	✔	✔	✔	—
A1020B Device						
84-pin Ceramic Quad Flat Pack (CQFP)	✔	✔	✔	✔	✔	✔
84-pin Ceramic Pin Grid Array (CPGA)	✔	✔	✔	✔	✔	✔

Applications: *C = Commercial* *M = Military* *B = MIL-STD-883* *E = Extended Flow*

Availability: ✔ = *Available* — = *Not Planned*

**Speed Grade:* *–1 = Approx. 15% faster than Standard*

Fixed Capacitance Values for Actel FPGAs (pF)

Device Type	r_1 routed_Clk1	r_2 routed_Clk2
A1010B	41	n/a
A1020B	69	n/a
A1240A	134	134
A1280A	168	168
A1280XL	168	168
A1425A	75	75
A1460A	165	165
A14100A	195	195
A32100DX	178	178
A32200DX	230	230

Fixed Clock Loads (s_1/s_2—ACT 3 Only)

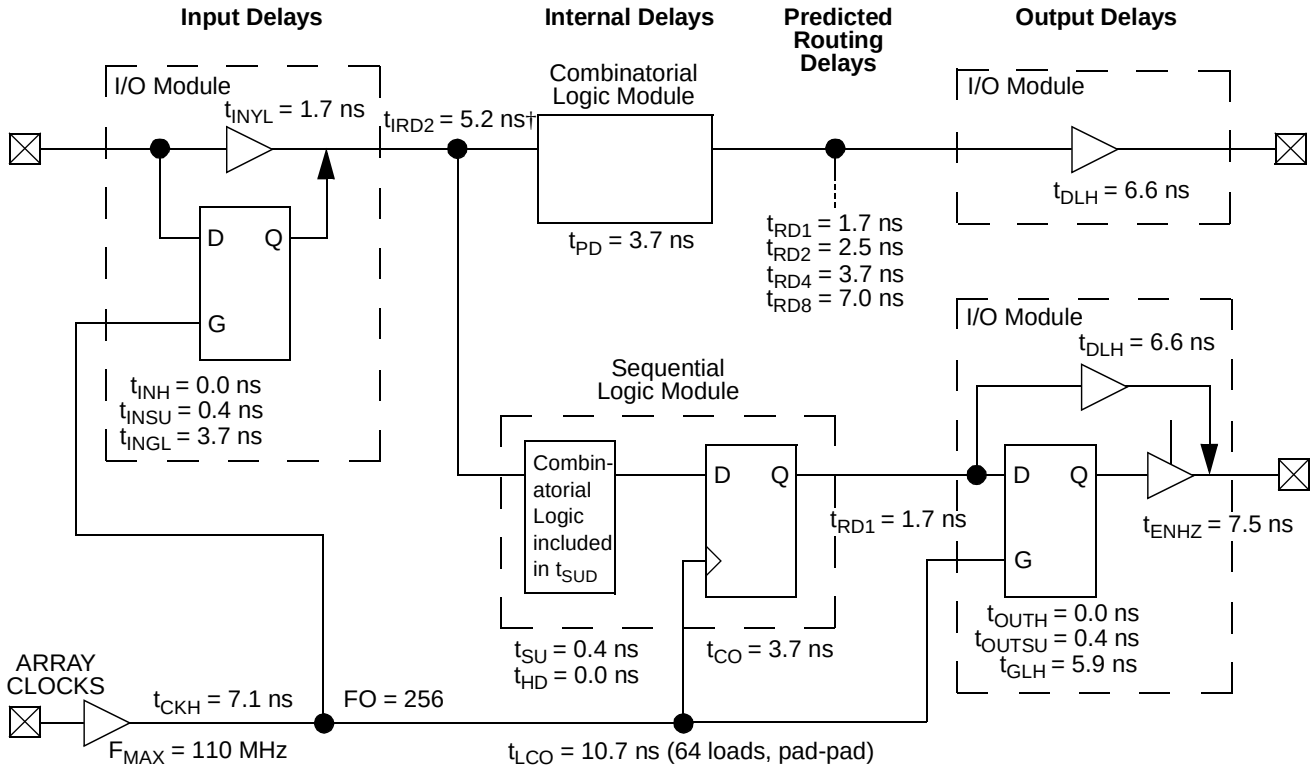
Device Type	s_1 Clock Loads on Dedicated Array Clock	s_2 Clock Loads on Dedicated I/O Clock
A1425A	160	100
A1460A	432	168
A14100A	697	228

Determining Average Switching Frequency

To determine the switching frequency for a design, you must have a detailed understanding of the data values input to the circuit. The guidelines in the table below are meant to represent worst-case scenarios so that they can be generally used to predict the upper limits of power dissipation.

Type	ACT 3	3200DX/ACT 2/1200XL	ACT 1
Logic modules (m)	80% of modules	80% of modules	90% of modules
Input switching (n)	# inputs/4	# inputs/4	# inputs/4
Outputs switching (p)	#outputs/4	#outputs/4	#outputs/4
First routed array clock loads (q_1)	40% of sequential modules	40% of sequential modules	40% of modules
Second routed array clock loads (q_2)	40% of sequential modules	40% of sequential modules	n/a
Load capacitance (C_L)	35 pF	35 pF	35 pF
Average logic module switching rate (f_m)	F/10	F/10	F/10
Average input switching rate (f_n)	F/5	F/5	F/5
Average output switching rate (f_p)	F/10	F/10	F/10
Average first routed array clock rate (f_{q1})	F/2	F	F
Average second routed array clock rate (f_{q2})	F/2	F/2	n/a
Average dedicated array clock rate (f_{s1})	F	n/a	n/a
Average dedicated I/O clock rate (f_{s2})	F	n/a	n/a

1200XL Timing Model*

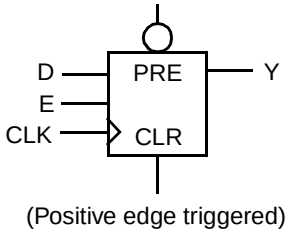


**Values shown for A1280XL–1 at worst-case military conditions.*

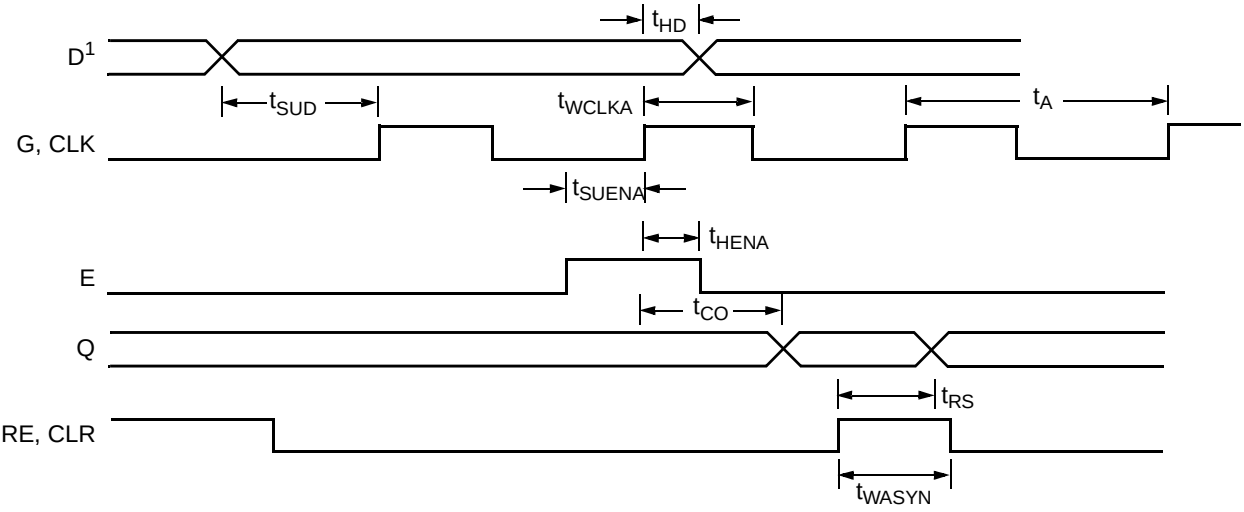
† Input module predicted routing delay.

Sequential Timing Characteristics (continued)

Flip-Flops and Latches (1200XL/3200DX, ACT 2, and ACT 1)



(Positive edge triggered)

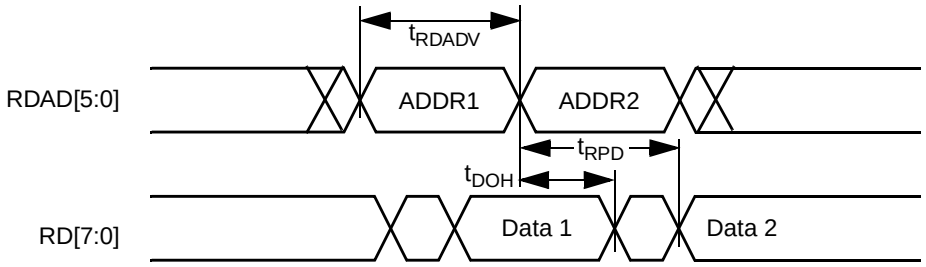


Note:

1. *D represents all data functions involving A, B, and S for multiplexed flip-flops.*

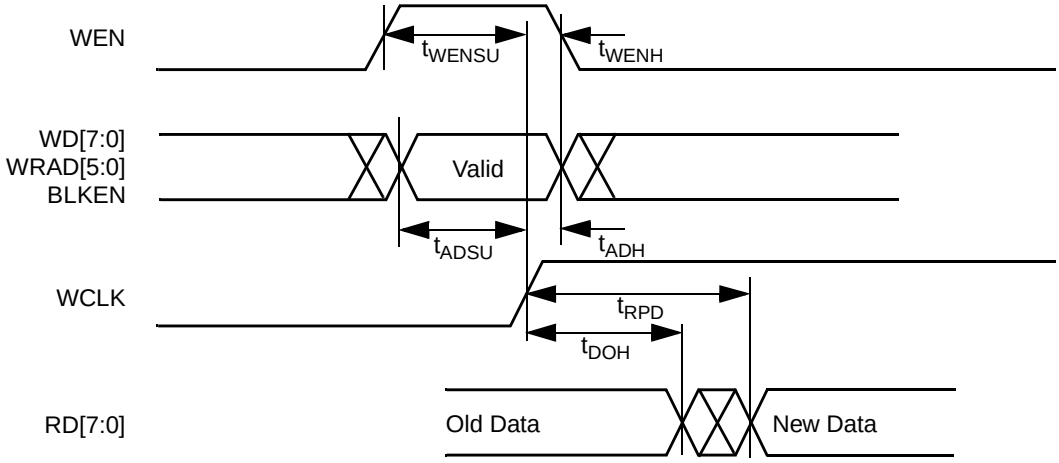
3200DX SRAM Asynchronous Read Operation—Type 1

(Read Address Controlled)



3200DX SRAM Asynchronous Read Operation—Type 2

(Write Address Controlled)



A1240A Timing Characteristics

(Worst-Case Military Conditions, V_{CC} = 4.5V, T_J = 125°C)

		'–1' Speed		'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
Logic Module Propagation Delays[1]						
t_{PD1}	Single Module		5.2		6.1	ns
t_{CO}	Sequential Clk to Q		5.2		6.1	ns
t_{GO}	Latch G to Q		5.2		6.1	ns
t_{RS}	Flip-Flop (Latch) Reset to Q		5.2		6.1	ns
Logic Module Predicted Routing Delays[2]						
t_{RD1}	FO=1 Routing Delay		1.9		2.2	ns
t_{RD2}	FO=2 Routing Delay		2.4		2.8	ns
t_{RD3}	FO=3 Routing Delay		3.1		3.7	ns
t_{RD4}	FO=4 Routing Delay		4.3		5.0	ns
t_{RD8}	FO=8 Routing Delay		6.6		7.7	ns
Logic Module Sequential Timing[3, 4]						
t_{SUD}	Flip-Flop (Latch) Data Input Setup	0.5		0.5		ns
t_{HD}	Flip-Flop (Latch) Data Input Hold	0.0		0.0		ns
t_{SUENA}	Flip-Flop (Latch) Enable Setup	1.3		1.3		ns
t_{HENA}	Flip-Flop (Latch) Enable Hold	0.0		0.0		ns
t_{WCLKA}	Flip-Flop (Latch) Clock Active Pulse Width	7.4		8.1		ns
t_{WASYN}	Flip-Flop (Latch) Asynchronous Pulse Width	7.4		8.1		ns
t_A	Flip-Flop Clock Input Period	14.8		18.6		ns
t_{INH}	Input Buffer Latch Hold	2.5		2.5		ns
t_{INSU}	Input Buffer Latch Setup	–3.5		–3.5		ns
t_{OUTH}	Output Buffer Latch Hold	0.0		0.0		ns
t_{OUTSU}	Output Buffer Latch Setup	0.5		0.5		ns
f_{MAX}	Flip-Flop (Latch) Clock Frequency		63		54	MHz

Notes:

1. *For dual-module macros, use $t_{PD1} + t_{RD1} + t_{PDn}$, $t_{CO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.*
2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*
3. *Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the DirectTime Analyzer utility.*
4. *Setup and hold timing parameters for the Input Buffer Latch are defined with respect to the PAD and the D input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.*

A1280XL Timing Characteristics

(Worst-Case Military Conditions, V_{CC} = 4.5V, T_J = 125°C)

		'–1' Speed		'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
Logic Module Propagation Delays[1]						
t_{PD1}	Single Module		3.7		4.3	ns
t_{CO}	Sequential Clk to Q		3.7		4.3	ns
t_{GO}	Latch G to Q		3.7		4.3	ns
t_{RS}	Flip-Flop (Latch) Reset to Q		3.7		4.3	ns
Logic Module Predicted Routing Delays[2]						
t_{RD1}	FO=1 Routing Delay		1.7		2.1	ns
t_{RD2}	FO=2 Routing Delay		2.5		3.0	ns
t_{RD3}	FO=3 Routing Delay		3.1		3.6	ns
t_{RD4}	FO=4 Routing Delay		3.7		4.3	ns
t_{RD8}	FO=8 Routing Delay		7.0		8.3	ns
Logic Module Sequential Timing[3, 4]						
t_{SUD}	Flip-Flop (Latch) Data Input Setup	0.4		0.5		ns
t_{HD}	Flip-Flop (Latch) Data Input Hold	0.0		0.0		ns
t_{SUENA}	Flip-Flop (Latch) Enable Setup	1.1		1.2		ns
t_{HENA}	Flip-Flop (Latch) Enable Hold	0.0		0.0		ns
t_{WCLKA}	Flip-Flop (Latch) Clock Active Pulse Width	5.3		6.1		ns
t_{WASYN}	Flip-Flop (Latch) Asynchronous Pulse Width	5.3		6.1		ns
t_A	Flip-Flop Clock Input Period	10.7		12.3		ns
t_{INH}	Input Buffer Latch Hold	0.0		0.0		ns
t_{INSU}	Input Buffer Latch Setup	0.4		0.4		ns
t_{OUTH}	Output Buffer Latch Hold	0.0		0.0		ns
t_{OUTSU}	Output Buffer Latch Setup	0.4		0.4		ns
f_{MAX}	Flip-Flop (Latch) Clock Frequency		90		75	MHz

Notes:

1. *For dual-module macros, use $t_{PD1} + t_{RD1} + t_{PDn}$, $t_{CO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.*
2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*
3. *Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the DirectTime Analyzer utility.*
4. *Setup and hold timing parameters for the input buffer latch are defined with respect to the PAD and the D input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.*

A14100A Timing Characteristics (continued)

(Worst-Case Military Conditions, V_{CC} = 4.5V, T_J = 125°C)

		'–1' Speed		'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
I/O Module Sequential Timing						
t_{INH}	Input F-F Data Hold (w.r.t. IOCLK Pad)	0.0		0.0		ns
t_{INSU}	Input F-F Data Setup (w.r.t. IOCLK Pad)	2.1		2.4		ns
t_{IDEH}	Input Data Enable Hold (w.r.t. IOCLK Pad)	0.0		0.0		ns
t_{IDESU}	Input Data Enable Setup (w.r.t. IOCLK Pad)	8.7		10.0		ns
t_{OUTH}	Output F-F Data Hold (w.r.t. IOCLK Pad)	1.2		1.2		ns
t_{OUTSU}	Output F-F Data Setup (w.r.t. IOCLK Pad)	1.2		1.2		ns
t_{ODEH}	Output Data Enable Hold (w.r.t. IOCLK Pad)	0.6		0.6		ns
t_{ODESU}	Output Data Enable Setup (w.r.t. IOCLK Pad)	2.4		2.4		ns
TTL Output Module Timing[1]						
t_{DHS}	Data to Pad, High Slew		7.5		8.9	ns
t_{DLS}	Data to Pad, Low Slew		11.9		14.0	ns
t_{ENZHS}	Enable to Pad, Z to H/L, High Slew		6.0		7.0	ns
t_{ENZLS}	Enable to Pad, Z to H/L, Low Slew		10.9		12.8	ns
t_{ENHSZ}	Enable to Pad, H/L to Z, High Slew		11.9		14.0	ns
t_{ENLSZ}	Enable to Pad, H/L to Z, Low Slew		10.9		12.8	ns
t_{CKHS}	IOCLK Pad to Pad H/L, High Slew		12.2		14.0	ns
t_{CKLS}	IOCLK Pad to Pad H/L, Low Slew		17.8		17.8	ns
d_{TLHHS}	Delta Low to High, High Slew		0.04		0.04	ns/pF
d_{TLHLS}	Delta Low to High, Low Slew		0.07		0.08	ns/pF
d_{THLHS}	Delta High to Low, High Slew		0.05		0.06	ns/pF
d_{THLLS}	Delta High to Low, Low Slew		0.07		0.08	ns/pF

Note:

1. Delays based on 35 pF loading.

A32100DX Timing Characteristics (continued)

(Worst-Case Military Conditions, V_{CC} = 4.5V, T_J = 125°C)

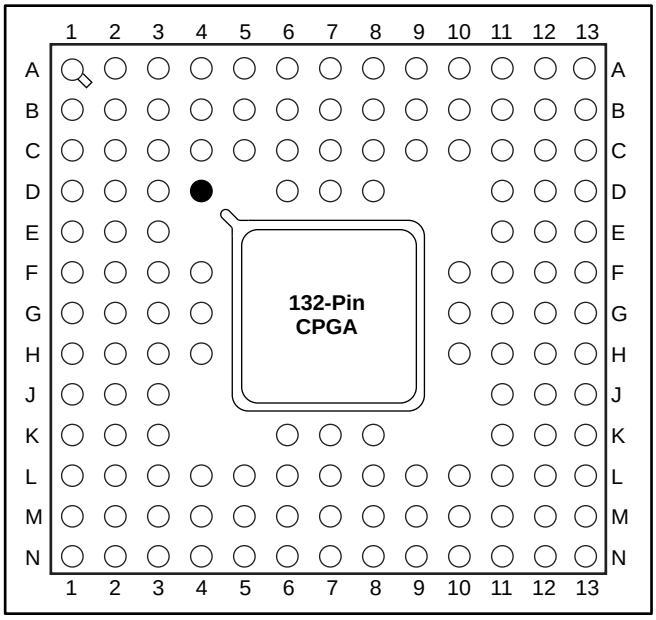
			'–1' Speed		'Std' Speed		
Parameter	**Description**		**Min.**	**Max.**	**Min.**	**Max.**	**Units**
Input Module Propagation Delays							
t_{INPY}	Input Data Pad to Y			1.9		2.6	ns
t_{INGO}	Input Latch Gate-to-Output			4.0		5.3	ns
t_{INH}	Input Latch Hold		0.0		0.0		ns
t_{INSU}	Input Latch Setup		0.7		0.9		ns
t_{ILA}	Latch Active Pulse Width		6.1		8.1		ns
Input Module Predicted Routing Delays[1]							
t_{IRD1}	FO=1 Routing Delay			2.2		2.9	ns
t_{IRD2}	FO=2 Routing Delay			2.8		3.8	ns
t_{IRD3}	FO=3 Routing Delay			3.5		4.7	ns
t_{IRD4}	FO=4 Routing Delay			3.5		4.7	ns
t_{IRD8}	FO=8 Routing Delay			5.6		7.5	ns
Global Clock Network							
t_{CKH}	Input Low to High	FO=32 FO=635		6.5 7.9		8.7 10.6	ns ns
t_{CKL}	Input High to Low	FO=32 FO=635		6.6 8.8		8.8 11.8	ns ns
t_{PWH}	Minimum Pulse Width High	FO=32 FO=635	4.1 4.6		5.5 6.1		ns ns
t_{PWL}	Minimum Pulse Width Low	FO=32 FO=635	4.1 4.6		5.5 6.1		ns ns
t_{CKSW}	Maximum Skew	FO=32 FO=635		1.8 1.8		2.4 2.4	ns ns
t_{SUEXT}	Input Latch External Setup	FO=32 FO=635	0.0 0.0		0.0 0.0		ns ns
t_{HEXT}	Input Latch External Hold	FO=32 FO=635	3.0 3.8		4.0 5.1		ns ns
t_P	Minimum Period (1/fmax)	FO=32 FO=635	7.1 7.9		9.5 10.5		ns ns
f_{HMAX}	Maximum Datapath Frequency	FO=32 FO=635		140 126		105 95	MHz MHz

Note:

1. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment. Optimization techniques may further reduce delays by 0 to 4 ns.

Package Pin Assignments (continued)

132-Pin CPGA (Top View)



133-Pin CPGA

Pin Number	A1425A Function
A1	NC
A2	GND
A3	I/O
A4	I/O
A5	I/O
A6	PRA, I/O
A7	NC
A8	I/O
A9	I/O
A10	I/O
A11	I/O
A12	I/O
A13	NC
B1	I/O
B2	V_{CC}
B3	I/O
B4	I/O
B5	I/O
B6	CLKB, I/O
B7	V_{CC}
B8	I/O
B9	I/O
B10	I/O
B11	I/O
B12	V_{CC}
B13	I/O
C1	I/O
C2	SDI, I/O
C3	GND
C4	I/O
C5	I/O
C6	I/O
C7	GND
C8	I/O
C9	I/O
C10	IOCLK, I/O
C11	GND
C12	GND
C13	I/O
D1	I/O
D2	I/O
D3	I/O
D4	DCLK, I/O
D6	CLKA, I/O
D7	I/O
D8	I/O
D11	I/O
D12	I/O
D13	I/O
E1	I/O
E2	I/O
E3	MODE
E11	V_{CC}
E12	I/O
E13	I/O
F1	I/O
F2	I/O
F3	I/O
F4	I/O
F10	GND
F11	I/O
F12	I/O
F13	I/O
G1	NC
G2	V_{CC}
G3	GND
G4	I/O
G10	I/O
G11	GND
G12	V_{CC}
G13	NC
H1	I/O
H2	I/O
H3	I/O
H4	I/O
H10	I/O
H11	I/O
H12	I/O
H13	I/O
J1	I/O
J2	V_{CC}
J3	I/O
J11	I/O
J12	V_{CC}
J13	I/O
K1	I/O
K2	I/O
K3	I/O
K6	I/O
K7	HCLKA, I/O
K8	I/O
K11	I/O
K12	I/O
K13	I/O
L1	I/O
L2	I/O
L3	GND
L4	I/O
L5	I/O
L6	PRB, I/O
L7	GND
L8	I/O
L9	I/O
L10	IOPCL, I/O
L11	GND
L12	I/O
L13	I/O
M1	I/O
M2	V_{CC}
M3	GND
M4	I/O
M5	I/O
M6	I/O
M7	V_{CC}
M8	I/O
M9	I/O
M10	I/O
M11	I/O
M12	V_{CC}
M13	I/O
N1	NC
N2	I/O
N3	I/O
N4	I/O
N5	I/O
N6	I/O
N7	NC
N8	I/O
N9	I/O
N10	I/O
N11	I/O
N12	GND
N13	NC

207-Pin CPGA

Pin Number	A1460A Function
A1	NC
A2	NC
A3	I/O
A4	I/O
A5	I/O
A6	I/O
A7	I/O
A8	I/O
A9	I/O
A10	I/O
A11	I/O
A12	I/O
A13	I/O
A14	I/O
A15	I/O
A16	NC
A17	NC
B1	NC
B2	V_{CC}
B3	I/O
B4	I/O
B5	I/O
B6	I/O
B7	I/O
B8	I/O
B9	V_{CC}
B10	I/O
B11	I/O
B12	I/O
B13	I/O
B14	I/O
B15	I/O
B16	V_{CC}
B17	NC
C1	NC
C2	NC
C3	SDI, I/O
C4	I/O
C5	I/O
C6	I/O
C7	I/O
C8	I/O
C9	I/O

Pin Number	A1460A Function
C10	I/O
C11	I/O
C12	I/O
C13	I/O
C14	I/O
C15	GND
C16	I/O
C17	I/O
D1	I/O
D2	I/O
D3	I/O
D4	GND
D5	GND
D6	I/O
D7	MODE
D8	I/O
D9	GND
D10	I/O
D11	V_{CC}
D12	I/O
D13	I/O
D14	GND
D15	I/O
D16	I/O
D17	I/O
E1	I/O
E2	I/O
E3	I/O
E4	DCLK, I/O
E14	I/O
E15	I/O
E16	I/O
E17	I/O
F1	I/O
F2	I/O
F3	I/O
F4	I/O
F14	I/O
F15	I/O
F16	I/O
F17	I/O
G1	I/O
G2	I/O

Pin Number	A1460A Function
G3	I/O
G4	I/O
G14	I/O
G15	I/O
G16	I/O
G17	I/O
H1	PRA, I/O
H2	I/O
H3	I/O
H4	I/O
H14	I/O
H15	I/O
H16	I/O
H17	I/O
J1	I/O
J2	V_{CC}
J3	CLKB, I/O
J4	GND
J14	GND
J15	HCLK, I/O
J16	V_{CC}
J17	I/O
K1	CLKA, I/O
K2	I/O
K3	I/O
K4	I/O
K14	I/O
K15	I/O
K16	PRB, I/O
K17	I/O
L1	I/O
L2	I/O
L3	I/O
L4	I/O
L14	I/O
L15	I/O
L16	I/O
L17	I/O
M1	I/O
M2	I/O
M3	I/O
M4	I/O
M14	I/O

132-Pin CQFP

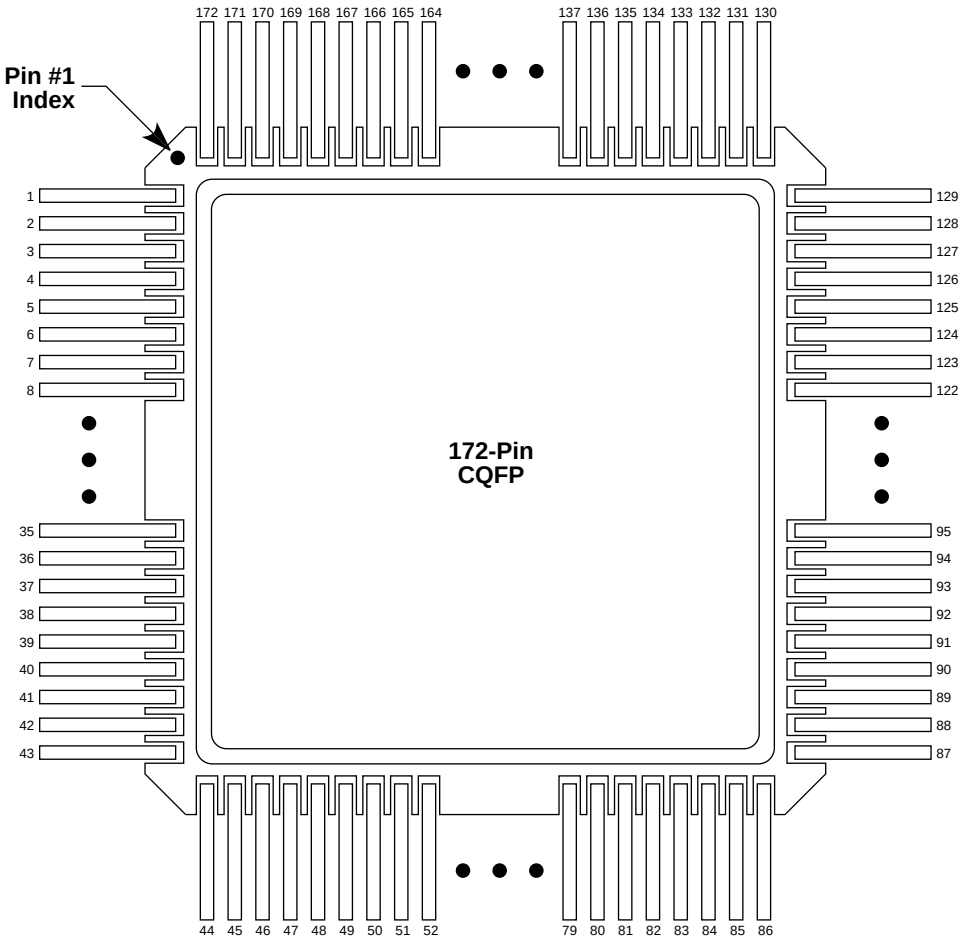
Pin Number	A1425A Function
1	NC
2	GND
3	SDI, I/O
4	I/O
5	I/O
6	I/O
7	I/O
8	I/O
9	MODE
10	GND
11	V_{CC}
12	I/O
13	I/O
14	I/O
15	I/O
16	I/O
17	I/O
18	I/O
19	I/O
20	I/O
21	I/O
22	V_{CC}
23	I/O
24	I/O
25	I/O
26	GND
27	V_{CC}
28	I/O
29	I/O
30	I/O
31	I/O
32	I/O
33	I/O
34	NC
35	I/O
36	GND
37	I/O
38	I/O
39	I/O
40	I/O
41	I/O
42	GND
43	V_{CC}
44	I/O

Pin Number	A1425A Function
45	I/O
46	I/O
47	I/O
48	PRB, I/O
49	I/O
50	HCLK, I/O
51	I/O
52	I/O
53	I/O
54	I/O
55	I/O
56	I/O
57	I/O
58	GND
59	V_{CC}
60	I/O
61	I/O
62	I/O
63	I/O
64	IOPCL, I/O
65	GND
66	NC
67	NC
68	I/O
69	I/O
70	I/O
71	I/O
72	I/O
73	I/O
74	GND
75	V_{CC}
76	I/O
77	I/O
78	V_{CC}
79	I/O
80	I/O
81	I/O
82	I/O
83	I/O
84	I/O
85	I/O
86	I/O
87	I/O
88	I/O

Pin Number	A1425A Function
89	V_{CC}
90	GND
91	V_{CC}
92	GND
93	I/O
94	I/O
95	I/O
96	I/O
97	I/O
98	IOCLK, I/O
99	NC
100	NC
101	GND
102	I/O
103	I/O
104	I/O
105	I/O
106	GND
107	V_{CC}
108	I/O
109	I/O
110	I/O
111	I/O
112	I/O
113	I/O
114	I/O
115	I/O
116	CLKA, I/O
117	CLKB, I/O
118	PRA, I/O
119	I/O
120	I/O
121	I/O
122	GND
123	V_{CC}
124	I/O
125	I/O
126	I/O
127	I/O
128	I/O
129	I/O
130	I/O
131	DCLK, I/O
132	NC

Package Pin Assignments (continued)

172-Pin CQFP (Top View)



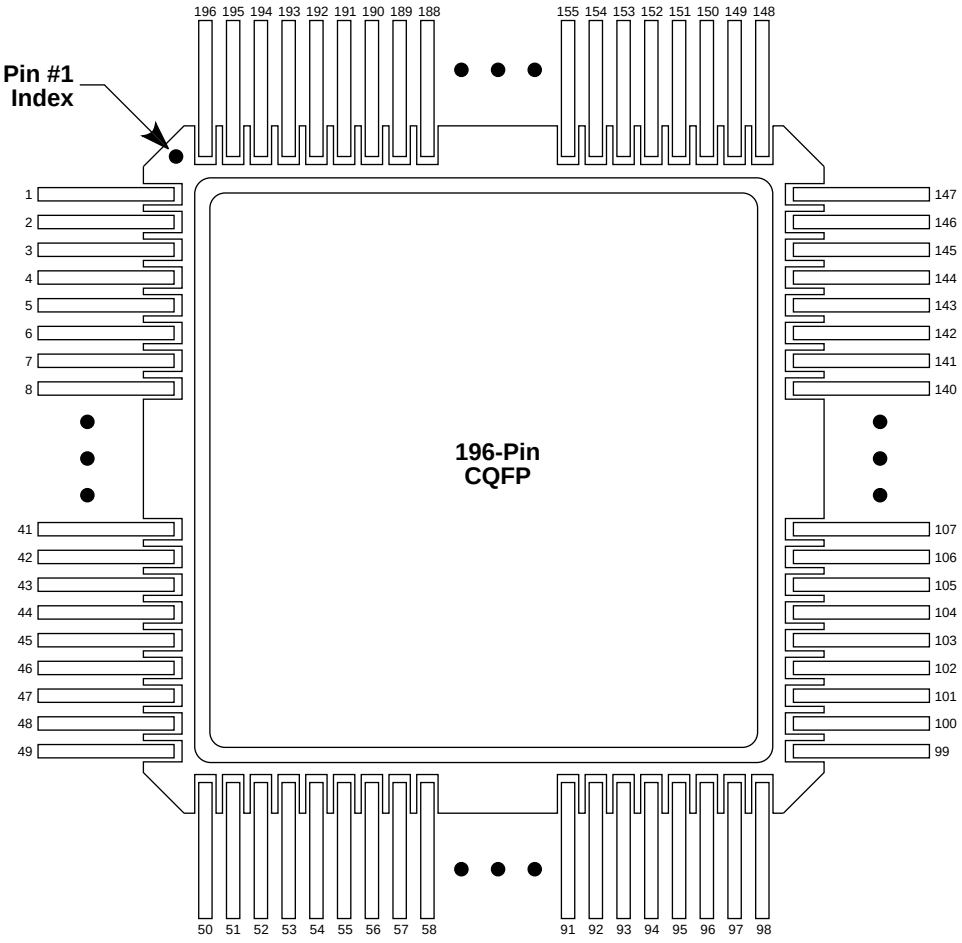
172-Pin CQFP

Pin Number	A1280A Function	A1280XL Function
1	MODE	MODE
2	I/O	I/O
3	I/O	I/O
4	I/O	I/O
5	I/O	I/O
6	I/O	I/O
7	GND	GND
8	I/O	I/O
9	I/O	I/O
10	I/O	I/O
11	I/O	I/O
12	V_{CC}	V_{CC}
13	I/O	I/O
14	I/O	I/O
15	I/O	I/O
16	I/O	I/O
17	GND	GND
18	I/O	I/O
19	I/O	I/O
20	I/O	I/O
21	I/O	I/O
22	GND	GND
23	V_{CC}	V_{CC}
24	V_{CC}	V_{CC}
25	I/O	I/O
26	I/O	I/O
27	V_{CC}	V_{CC}
28	I/O	I/O
29	I/O	I/O
30	I/O	I/O
31	I/O	I/O
32	GND	GND
33	I/O	I/O
34	I/O	I/O
35	I/O	I/O
36	I/O	I/O
37	GND	GND
38	I/O	I/O
39	I/O	I/O
40	I/O	I/O
41	I/O	I/O
42	I/O	I/O
43	I/O	I/O
44	I/O	I/O

Pin Number	A1280A Function	A1280XL Function
45	I/O	I/O
46	I/O	I/O
47	I/O	I/O
48	I/O	I/O
49	I/O	I/O
50	V_{CC}	V_{CC}
51	I/O	I/O
52	I/O	I/O
53	I/O	I/O
54	I/O	I/O
55	GND	GND
56	I/O	I/O
57	I/O	I/O
58	I/O	I/O
59	I/O	I/O
60	I/O	I/O
61	I/O	I/O
62	I/O	I/O
63	I/O	I/O
64	I/O	I/O
65	GND	GND
66	V_{CC}	V_{CC}
67	I/O	I/O
68	I/O	I/O
69	I/O	I/O
70	I/O	I/O
71	I/O	I/O
72	I/O	I/O
73	I/O	I/O
74	I/O	I/O
75	GND	GND
76	I/O	I/O
77	I/O	I/O
78	I/O	I/O
79	I/O	I/O
80	V_{CC}	V_{CC}
81	I/O	I/O
82	I/O	I/O
83	I/O	I/O
84	I/O	I/O
85	I/O	I/O
86	I/O	I/O
87	I/O	I/O
88	I/O	I/O

Package Pin Assignments (continued)

196-Pin CQFP (Top View)



196-Pin CQFP

Pin Number	A1460A Function
1	GND
2	SDI, I/O
3	I/O
4	I/O
5	I/O
6	I/O
7	I/O
8	I/O
9	I/O
10	I/O
11	MODE
12	V_{CC}
13	GND
14	I/O
15	I/O
16	I/O
17	I/O
18	I/O
19	I/O
20	I/O
21	I/O
22	I/O
23	I/O
24	I/O
25	I/O
26	I/O
27	I/O
28	I/O
29	I/O
30	I/O
31	I/O
32	I/O
33	I/O
34	I/O
35	I/O
36	I/O
37	GND
38	V_{CC}
39	V_{CC}
40	I/O
41	I/O
42	I/O
43	I/O
44	I/O
45	I/O
46	I/O
47	I/O
48	I/O
49	I/O
50	I/O
51	GND
52	GND
53	I/O
54	I/O
55	I/O
56	I/O
57	I/O
58	I/O
59	V_{CC}
60	I/O
61	I/O
62	I/O
63	I/O
64	GND
65	I/O
66	I/O
67	I/O
68	I/O
69	I/O
70	I/O
71	I/O
72	I/O
73	I/O
74	I/O
75	PRB, I/O
76	I/O
77	HCLK, I/O
78	I/O
79	I/O
80	I/O
81	I/O
82	I/O
83	I/O
84	I/O
85	I/O
86	GND
87	I/O
88	I/O
89	I/O
90	I/O
91	I/O
92	I/O
93	I/O
94	V_{CC}
95	I/O
96	I/O
97	I/O
98	GND
99	I/O
100	IOPCL, I/O
101	GND
102	I/O
103	I/O
104	I/O
105	I/O
106	I/O
107	I/O
108	I/O
109	I/O
110	V_{CC}
111	V_{CC}
112	GND
113	I/O
114	I/O
115	I/O
116	I/O
117	I/O
118	I/O
119	I/O
120	I/O
121	I/O
122	I/O
123	I/O
124	I/O
125	I/O
126	I/O
127	I/O
128	I/O
129	I/O

196-Pin CQFP (Continued)

Pin Number	A1460A Function
130	I/O
131	I/O
132	I/O
133	I/O
134	I/O
135	I/O
136	I/O
137	V_{CC}
138	GND
139	GND
140	V_{CC}
141	I/O
142	I/O
143	I/O
144	I/O
145	I/O
146	I/O
147	I/O
148	IOCLK, I/O
149	GND
150	I/O
151	I/O
152	I/O

Pin Number	A1460A Function
153	I/O
154	I/O
155	V_{CC}
156	I/O
157	I/O
158	I/O
159	I/O
160	I/O
161	I/O
162	GND
163	I/O
164	I/O
165	I/O
166	I/O
167	I/O
168	I/O
169	I/O
170	I/O
171	I/O
172	CLKA, I/O
173	CLKB, I/O
174	PRA, I/O
175	I/O

Pin Number	A1460A Function
176	I/O
177	I/O
178	I/O
179	I/O
180	I/O
181	I/O
182	I/O
183	GND
184	I/O
185	I/O
186	I/O
187	I/O
188	I/O
189	V_{CC}
190	I/O
191	I/O
192	I/O
193	GND
194	I/O
195	I/O
196	DCLK, I/O

208-Pin CQFP

Pin Number	A32100DX Function
1	GND
2	V_{CC}
3	MODE
4	I/O
5	I/O
6	I/O
7	I/O
8	I/O
9	I/O
10	I/O
11	I/O
12	I/O
13	I/O
14	I/O
15	I/O
16	I/O
17	V_{CC}
18	I/O
19	I/O
20	I/O
21	I/O
22	GND
23	I/O
24	I/O
25	I/O
26	I/O
27	GND
28	V_{CC}
29	V_{CC}
30	I/O
31	I/O
32	V_{CC}
33	I/O
34	I/O
35	I/O
36	I/O
37	I/O
38	I/O
39	I/O
40	I/O
41	I/O
42	I/O
43	I/O

Pin Number	A32100DX Function
44	I/O
45	I/O
46	I/O
47	I/O
48	I/O
49	I/O
50	I/O
51	I/O
52	GND
53	GND
54	TMS, I/O
55	TDI, I/O
56	I/O
57	I/O (WD)
58	I/O (WD)
59	I/O
60	V_{CC}
61	I/O
62	I/O
63	I/O
64	I/O
65	QCLKA, I/O
66	I/O (WD)
67	I/O (WD)
68	I/O
69	I/O
70	I/O (WD)
71	I/O (WD)
72	I/O
73	I/O
74	I/O
75	I/O
76	I/O
77	I/O
78	GND
79	V_{CC}
80	V_{CC}
81	I/O
82	I/O
83	I/O
84	I/O
85	I/O (WD)
86	I/O (WD)

Pin Number	A32100DX Function
87	I/O
88	I/O
89	I/O
90	I/O
91	QCLKB, I/O
92	I/O
93	I/O (WD)
94	I/O (WD)
95	I/O
96	I/O
97	I/O
98	V_{CC}
99	I/O
100	I/O (WD)
101	I/O (WD)
102	I/O
103	SDO, I/O
104	I/O
105	GND
106	V_{CC}
107	I/O
108	I/O
109	I/O
110	I/O
111	I/O
112	I/O
113	I/O
114	I/O
115	I/O
116	I/O
117	I/O
118	I/O
119	I/O
120	I/O
121	I/O
122	I/O
123	I/O
124	I/O
125	I/O
126	GND
127	I/O
128	TCK, I/O
129	GND

256-Pin CQFP

Pin Number	A14100A Function	A32200DX Function
1	GND	NC
2	SDI, I/O	GND
3	I/O	I/O
4	I/O	I/O
5	I/O	I/O
6	I/O	I/O
7	I/O	I/O
8	I/O	I/O
9	I/O	I/O
10	I/O	GND
11	MODE	I/O
12	I/O	I/O
13	I/O	I/O
14	I/O	I/O
15	I/O	I/O
16	I/O	I/O
17	I/O	I/O
18	I/O	I/O
19	I/O	I/O
20	I/O	I/O
21	I/O	I/O
22	I/O	I/O
23	I/O	I/O
24	I/O	I/O
25	I/O	I/O
26	I/O	V_{CC}
27	I/O	I/O
28	V_{CC}	I/O
29	GND	V_{CC}
30	V_{CC}	V_{CC}
31	GND	GND
32	I/O	V_{CC}
33	I/O	GND
34	I/O	TCK, I/O
35	I/O	I/O
36	I/O	GND
37	I/O	I/O
38	I/O	I/O
39	I/O	I/O
40	I/O	I/O
41	I/O	I/O
42	I/O	I/O
43	I/O	I/O
44	I/O	I/O
45	I/O	I/O
46	V_{CC}	I/O
47	I/O	I/O
48	I/O	GND
49	I/O	I/O
50	I/O	I/O
51	I/O	I/O
52	I/O	I/O
53	I/O	I/O
54	I/O	I/O
55	I/O	I/O
56	I/O	I/O
57	I/O	I/O
58	I/O	I/O
59	GND	I/O
60	I/O	V_{CC}
61	I/O	GND
62	I/O	GND
63	I/O	NC
64	I/O	NC
65	I/O	NC
66	I/O	I/O
67	I/O	SDO, I/O
68	I/O	I/O
69	I/O	I/O (WD)
70	I/O	I/O (WD)
71	I/O	I/O
72	I/O	V_{CC}
73	I/O	I/O
74	I/O	I/O
75	I/O	I/O
76	I/O	I/O (WD)
77	I/O	GND
78	I/O	I/O (WD)
79	I/O	I/O
80	I/O	QCLKB, I/O
81	I/O	I/O
82	I/O	I/O
83	I/O	I/O
84	I/O	I/O
85	I/O	I/O
86	I/O	I/O
87	I/O	I/O (WD)
88	I/O	I/O (WD)
89	I/O	I/O
90	PRB, I/O	I/O
91	GND	I/O
92	V_{CC}	I/O
93	GND	I/O
94	V_{CC}	I/O
95	I/O	V_{CC}
96	HCLK, I/O	V_{CC}
97	I/O	GND
98	I/O	GND
99	I/O	I/O
100	I/O	I/O
101	I/O	I/O
102	I/O	I/O
103	I/O	I/O
104	I/O	I/O
105	I/O	I/O (WD)
106	I/O	I/O (WD)
107	I/O	I/O
108	I/O	I/O
109	I/O	I/O (WD)
110	GND	I/O (WD)
111	I/O	I/O
112	I/O	QCLKA, I/O
113	I/O	I/O
114	I/O	GND
115	I/O	I/O
116	I/O	I/O
117	I/O	I/O
118	I/O	I/O
119	I/O	V_{CC}
120	I/O	I/O
121	I/O	I/O (WD)
122	I/O	I/O (WD)
123	I/O	I/O
124	I/O	I/O
125	I/O	TDI, I/O
126	I/O	TMS, I/O
127	IOPCL, I/O	GND
128	GND	NC
129	I/O	NC
130	I/O	NC
131	I/O	GND
132	I/O	I/O