Welcome to E-XFL.COM

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	547
Number of Logic Elements/Cells	-
Total RAM Bits	-
Number of I/O	69
Number of Gates	2000
Voltage - Supply	4.5V ~ 5.5V
Mounting Type	Surface Mount
Operating Temperature	-55°C ~ 125°C (TC)
Package / Case	84-CQFP Exposed Pad and Tie Bar
Supplier Device Package	84-CQFP (42x42)
Purchase URL	https://www.e-xfl.com/product-detail/microsemi/a1020b-cq84m

unique architecture offers gate array flexibility, high performance, and quick turnaround through user programming. Device utilization is typically 95 percent of available logic modules. All Actel devices include on-chip clock drivers and a hard-wired distribution network.

User-definable I/Os are capable of driving at both TTL and CMOS drive levels. Available packages for the military are the Ceramic Quad Flat Pack (CQFP) and the Ceramic Pin Grid Array (CPGA). See the "Product Plan" section on page 6 for details.

QML Certification

Actel has achieved full QML certification, demonstrating that quality management, procedures, processes, and controls are in place and comply with MIL-PRF-38535, the performance specification used by the Department of Defense for monolithic integrated circuits. QML certification is a good example of Actel's commitment to supplying the highest quality products for all types of high-reliability, military and space applications.

Many suppliers of microelectronics components have implemented QML as their primary worldwide business system. Appropriate use of this system not only helps in the implementation of advanced technologies, but also allows for a quality, reliable and cost-effective logistics support throughout QML products' life cycles.

Development Tool Support

The HiRel devices are fully supported by Actel's line of FPGA development tools, including the Actel DeskTOP series and Designer Advantage tools. The Actel DeskTOP Series is an integrated design environment for PCs that includes design entry, simulation, synthesis, and place and route tools. Designer Advantage is Actel's suite of FPGA development point tools for PCs and Workstations that includes the ACTgen Macro Builder, Designer with DirectTime timing driven place and route and analysis tools, and device programming software.

In addition, the HiRel devices contain ActionProbe circuitry that provides built-in access to every node in a design, enabling 100 percent real-time observation and analysis of a device's internal logic nodes without design iteration. The probe circuitry is accessed by Silicon Explorer, an easy to use integrated verification and logic analysis tool that can sample data at 100 MHz (asynchronous) or 66 MHz (synchronous). Silicon Explorer attaches to a PC's standard COM port, turning the PC into a fully functional 18 channel logic analyzer. Silicon Explorer allows designers to complete the design verification process at their desks and reduces verification time from several hours per cycle to a few seconds.

ACT 3 Description

The ACT 3 family is the third-generation Actel FPGA family. This family offers the highest-performance and highest-capacity devices, ranging from 2,500 to 10,000 gates, with system performance up to 60 MHz over the military temperature range. The devices have four clock distribution networks, including dedicated array and I/O clocks. In addition, the ACT 3 family offers the highest I/O-to-gate ratio available. ACT 3 devices are manufactured using 0.8µ CMOS technology.

1200XL/3200DX Description

3200DX and 1200XL FPGAs were designed to integrate system logic which is typically implemented in multiple CPLDs, PALs, and FPGAs. These devices provide the features and performance required for today's complex, high-speed digital logic systems. The 3200DX family offers the industry's fastest dual-port SRAM for implementing fast FIFOs, LIFOs, and temporary data storage.

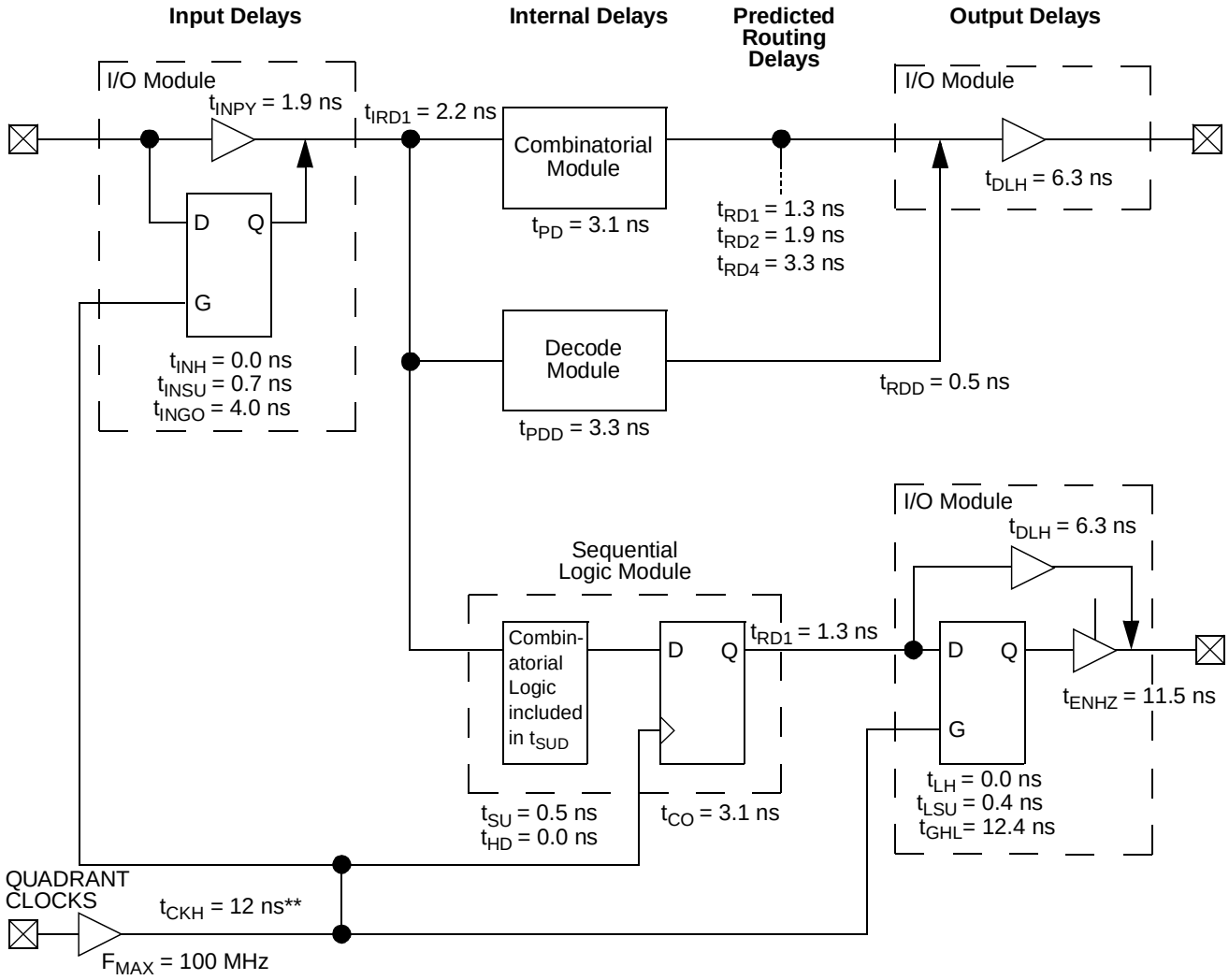
ACT 2 Description

The ACT 2 family is the second-generation Actel FPGA family. This family offers the best-value, high-capacity devices, ranging from 4,000 to 8,000 gates, with system performance up to 40 MHz over the military temperature range. The devices have two routed array clock distribution networks. ACT 2 devices are manufactured using 1.0µ CMOS technology.

ACT 1 Description

The ACT 1 family is the first Actel FPGA family and the first antifuse-based FPGA. This family offers the lowest-cost logic integration, with devices ranging from 1,200 to 2,000 gates, with system performance up to 20 MHz over the military temperature range. The devices have one routed array clock distribution network. ACT 1 devices are manufactured using 1.0µ CMOS technology.

3200DX Timing Model (Logic Functions using Quadrant Clocks)*

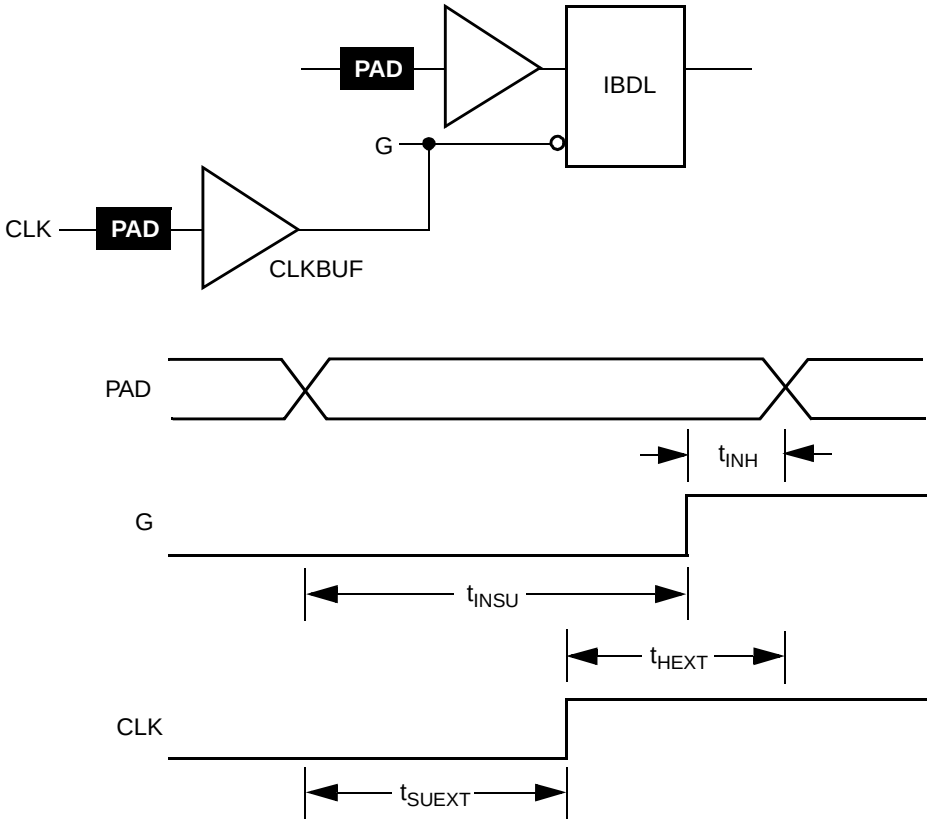


** Values shown for A32100DX–1 at worst-case military conditions.*

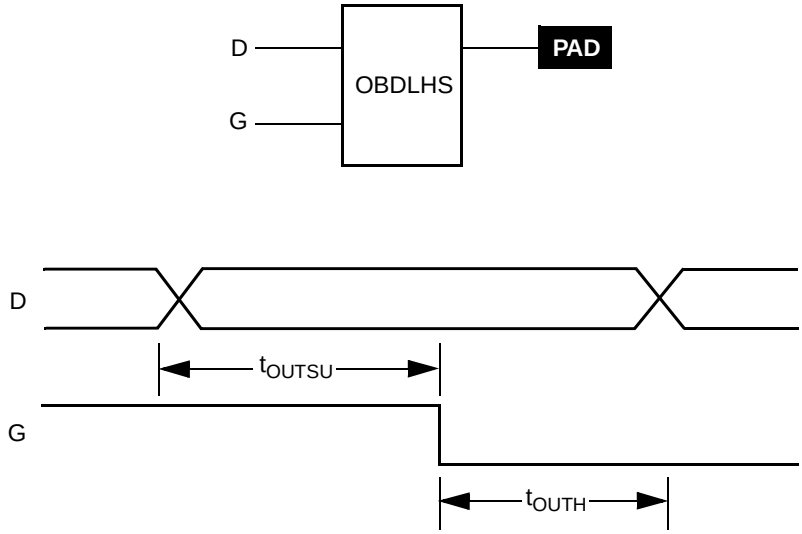
*** Load dependent.*

Sequential Timing Characteristics (continued)

Input Buffer Latches (ACT 2 and 1200XL/3200DX)



Output Buffer Latches (ACT 2 and 1200XL/3200DX)



A1280A Timing Characteristics

(Worst-Case Military Conditions, V_{CC} = 4.5V, T_J = 125°C)

		'–1' Speed		'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
Logic Module Propagation Delays[1]						
t_{PD1}	Single Module		5.2		6.1	ns
t_{CO}	Sequential Clk to Q		5.2		6.1	ns
t_{GO}	Latch G to Q		5.2		6.1	ns
t_{RS}	Flip-Flop (Latch) Reset to Q		5.2		6.1	ns
Logic Module Predicted Routing Delays[2]						
t_{RD1}	FO=1 Routing Delay		2.4		2.8	ns
t_{RD2}	FO=2 Routing Delay		3.4		4.0	ns
t_{RD3}	FO=3 Routing Delay		4.2		4.9	ns
t_{RD4}	FO=4 Routing Delay		5.1		6.0	ns
t_{RD8}	FO=8 Routing Delay		9.2		10.8	ns
Logic Module Sequential Timing[3, 4]						
t_{SUD}	Flip-Flop (Latch) Data Input Setup	0.5		0.5		ns
t_{HD}	Flip-Flop (Latch) Data Input Hold	0.0		0.0		ns
t_{SUENA}	Flip-Flop (Latch) Enable Setup	1.3		1.3		ns
t_{HENA}	Flip-Flop (Latch) Enable Hold	0.0		0.0		ns
t_{WCLKA}	Flip-Flop (Latch) Clock Active Pulse Width	7.4		8.6		ns
t_{WASYN}	Flip-Flop (Latch) Asynchronous Pulse Width	7.4		8.6		ns
t_A	Flip-Flop Clock Input Period	16.4		22.1		ns
t_{INH}	Input Buffer Latch Hold	2.5		2.5		ns
t_{INSU}	Input Buffer Latch Setup	–3.5		–3.5		ns
t_{OUTH}	Output Buffer Latch Hold	0.0		0.0		ns
t_{OUTSU}	Output Buffer Latch Setup	0.5		0.5		ns
f_{MAX}	Flip-Flop (Latch) Clock Frequency		60		41	MHz

Notes:

1. *For dual-module macros, use $t_{PD1} + t_{RD1} + t_{PDn}$, $t_{CO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.*
2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*
3. *Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the DirectTime Analyzer utility.*
4. *Setup and hold timing parameters for the input buffer latch are defined with respect to the PAD and the D input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.*

A1280XL Timing Characteristics (continued)

(Worst-Case Military Conditions, V_{CC} = 4.5V, T_J = 125°C)

		'–1' Speed		'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
TTL Output Module Timing[1]						
t_{DLH}	Data to Pad High		5.3		6.2	ns
t_{DHL}	Data to Pad Low		5.7		6.6	ns
t_{ENZH}	Enable Pad Z to High		5.3		6.2	ns
t_{ENZL}	Enable Pad Z to Low		5.8		6.8	ns
t_{ENHZ}	Enable Pad High to Z		7.5		8.9	ns
t_{ENLZ}	Enable Pad Low to Z		7.5		8.9	ns
t_{GLH}	G to Pad High		5.9		6.9	ns
t_{GHL}	G to Pad Low		6.6		7.8	ns
d_{TLH}	Delta Low to High		0.05		0.06	ns/pF
d_{THL}	Delta High to Low		0.05		0.09	ns/pF
CMOS Output Module Timing[1]						
t_{DLH}	Data to Pad High		6.6		7.9	ns
t_{DHL}	Data to Pad Low		4.7		5.5	ns
t_{ENZH}	Enable Pad Z to High		5.3		6.2	ns
t_{ENZL}	Enable Pad Z to Low		5.8		6.8	ns
t_{ENHZ}	Enable Pad High to Z		7.5		8.9	ns
t_{ENLZ}	Enable Pad Low to Z		7.5		8.9	ns
t_{GLH}	G to Pad High		5.9		6.9	ns
t_{GHL}	G to Pad Low		6.6		7.8	ns
d_{TLH}	Delta Low to High		0.07		0.09	ns/pF
d_{THL}	Delta High to Low		0.06		0.09	ns/pF

Notes:

1. *Delays based on 50 pF loading.*
2. *SSO information can be found in the* Simultaneously Switching Output Limits for Actel FPGAs *application note at http://www.actel.com/appnotes.*

A1460A Timing Characteristics (continued)

(Worst-Case Military Conditions, V_{CC} = 4.5V, T_J = 125°C)

		'–1' Speed		'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
I/O Module Sequential Timing						
t_{INH}	Input F-F Data Hold (w.r.t. IOCLK Pad)	0.0		0.0		ns
t_{INSU}	Input F-F Data Setup (w.r.t. IOCLK Pad)	2.1		2.4		ns
t_{IDEH}	Input Data Enable Hold (w.r.t. IOCLK Pad)	0.0		0.0		ns
t_{IDESU}	Input Data Enable Setup (w.r.t. IOCLK Pad)	8.7		10.0		ns
t_{OUTH}	Output F-F Data Hold (w.r.t. IOCLK Pad)	1.1		1.2		ns
t_{OUTSU}	Output F-F Data Setup (w.r.t. IOCLK Pad)	1.1		1.2		ns
t_{ODEH}	Output Data Enable Hold (w.r.t. IOCLK Pad)	0.5		0.6		ns
t_{ODESU}	Output Data Enable Setup (w.r.t. IOCLK Pad)	2.0		2.4		ns
TTL Output Module Timing[1]						
t_{DHS}	Data to Pad, High Slew		7.5		8.9	ns
t_{DLS}	Data to Pad, Low Slew		11.9		14.0	ns
t_{ENZHS}	Enable to Pad, Z to H/L, High Slew		6.0		7.0	ns
t_{ENZLS}	Enable to Pad, Z to H/L, Low Slew		10.9		12.8	ns
t_{ENHSZ}	Enable to Pad, H/L to Z, High Slew		11.5		13.5	ns
t_{ENLSZ}	Enable to Pad, H/L to Z, Low Slew		10.9		12.8	ns
t_{CKHS}	IOCLK Pad to Pad H/L, High Slew		11.6		13.4	ns
t_{CKLS}	IOCLK Pad to Pad H/L, Low Slew		17.8		19.8	ns
d_{TLHHS}	Delta Low to High, High Slew		0.04		0.04	ns/pF
d_{TLHLS}	Delta Low to High, Low Slew		0.07		0.08	ns/pF
d_{THLHS}	Delta High to Low, High Slew		0.05		0.06	ns/pF
d_{THLLS}	Delta High to Low, Low Slew		0.07		0.08	ns/pF

Note:

1. Delays based on 35 pF loading.

A14100A Timing Characteristics (continued)

(Worst-Case Military Conditions, V_{CC} = 4.5V, T_J = 125°C)

		'–1' Speed		'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
CMOS Output Module Timing[1]						
t_{DHS}	Data to Pad, High Slew		9.2		10.8	ns
t_{DLS}	Data to Pad, Low Slew		17.3		20.3	ns
t_{ENZHS}	Enable to Pad, Z to H/L, High Slew		7.7		9.1	ns
t_{ENZLS}	Enable to Pad, Z to H/L, Low Slew		13.1		15.5	ns
t_{ENHSZ}	Enable to Pad, H/L to Z, High Slew		11.6		14.0	ns
t_{ENLSZ}	Enable to Pad, H/L to Z, Low Slew		10.9		12.8	ns
t_{CKHS}	IOCLK Pad to Pad H/L, High Slew		14.4		16.0	ns
t_{CKLS}	IOCLK Pad to Pad H/L, Low Slew		20.2		22.4	ns
d_{TLHHS}	Delta Low to High, High Slew		0.06		0.07	ns/pF
d_{TLHLS}	Delta Low to High, Low Slew		0.11		0.13	ns/pF
d_{THLHS}	Delta High to Low, High Slew		0.04		0.05	ns/pF
d_{THLLS}	Delta High to Low, Low Slew		0.05		0.06	ns/pF
Dedicated (Hard-Wired) I/O Clock Network						
t_{IOCKH}	Input Low to High (Pad to I/O Module Input)		3.5		4.1	ns
t_{IOPWH}	Minimum Pulse Width High	4.8		5.7		ns
t_{IOPWL}	Minimum Pulse Width Low	4.8		5.7		ns
t_{IOSAPW}	Minimum Asynchronous Pulse Width	3.9		4.4		ns
t_{IOCKSW}	Maximum Skew		0.9		1.0	ns
t_{IOP}	Minimum Period	9.9		11.6		ns
f_{IOMAX}	Maximum Frequency		100		85	MHz
Dedicated (Hard-Wired) Array Clock Network						
t_{HCKH}	Input Low to High (Pad to S-Module Input)		5.5		6.4	ns
t_{HCKL}	Input High to Low (Pad to S-Module Input)		5.5		6.4	ns
t_{HPWH}	Minimum Pulse Width High	4.8		5.7		ns
t_{HPWL}	Minimum Pulse Width Low	4.8		5.7		ns
t_{HCKSW}	Maximum Skew		0.9		1.0	ns
t_{HP}	Minimum Period	9.9		11.6		ns
f_{HMAX}	Maximum Frequency		100		85	MHz

Notes:

1. *Delays based on 35 pF loading.*
2. *SSO information can be found in the* Simultaneously Switching Output Limits for Actel FPGAs *application note at http://www.actel.com/appnotes.*

A14100A Timing Characteristics (continued)

(Worst-Case Military Conditions, V_{CC} = 4.5V, T_J = 125°C)

		'–1' Speed		'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
Routed Array Clock Networks						
t_{RCKH}	Input Low to High (FO=256)		9.0		10.5	ns
t_{RCKL}	Input High to Low (FO=256)		9.0		10.5	ns
t_{RPWH}	Min. Pulse Width High (FO=256)	6.3		7.1		ns
t_{RPWL}	Min. Pulse Width Low (FO=256)	6.3		7.1		ns
t_{RCKSW}	Maximum Skew (FO=128)		1.9		2.1	ns
t_{RP}	Minimum Period (FO=256)	12.9		14.5		ns
f_{RMAX}	Maximum Frequency (FO=256)		75		65	MHz
Clock-to-Clock Skews						
$t_{IOHCKSW}$	I/O Clock to H-Clock Skew	0.0	3.5	0.0	3.5	ns
$t_{IORCKSW}$	I/O Clock to R-Clock Skew	0.0	5.0	0.0	5.0	ns
t_{HRCKSW}	H-Clock to R-Clock Skew (FO = 64) (FO = 50% max.)	 0.0 0.0	 1.0 3.0	 0.0 0.0	 1.0 3.0	ns

A32100DX Timing Characteristics (continued)

(Worst-Case Military Conditions, V_{CC} = 4.5V, T_J = 125°C)

		'–1' Speed		'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
Synchronous SRAM Operations						
t_{RC}	Read Cycle Time	8.8		11.8		ns
t_{WC}	Write Cycle Time	8.8		11.8		ns
t_{RCKHL}	Clock High/Low Time	4.4		5.9		ns
t_{RCO}	Data Valid After Clock High/Low		4.4		5.9	ns
t_{ADSU}	Address/Data Setup Time	2.1		2.8		ns
t_{ADH}	Address/Data Hold Time	0.0		0.0		ns
t_{RENSU}	Read Enable Setup	0.8		1.1		ns
t_{RENH}	Read Enable Hold	4.4		5.9		ns
t_{WENSU}	Write Enable Setup	3.5		4.7		ns
t_{WENH}	Write Enable Hold	0.0		0.0		ns
t_{BENS}	Block Enable Setup	3.6		4.8		ns
t_{BENH}	Block Enable Hold	0.0		0.0		ns
Asynchronous SRAM Operations						
t_{RPD}	Asynchronous Access Time		10.6		14.1	ns
t_{RDADV}	Read Address Valid	11.5		15.3		ns
t_{ADSU}	Address/Data Setup Time	2.1		2.8		ns
t_{ADH}	Address/Data Hold Time	0.0		0.0		ns
t_{RENSUA}	Read Enable Setup to Address Valid	0.8		1.1		ns
t_{RENHA}	Read Enable Hold	4.4		5.9		ns
t_{WENSU}	Write Enable Setup	3.5		4.7		ns
t_{WENH}	Write Enable Hold	0.0		0.0		ns
t_{DOH}	Data Out Hold Time		1.6		2.1	ns

A32100DX Timing Characteristics (continued)

(Worst-Case Military Conditions, V_{CC} = 4.5V, T_J = 125°C)

		'–1' Speed		'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
TTL Output Module Timing[1]						
t_{DLH}	Data to Pad High		5.1		6.8	ns
t_{DHL}	Data to Pad Low		6.3		8.3	ns
t_{ENZH}	Enable Pad Z to High		6.6		8.8	ns
t_{ENZL}	Enable Pad Z to Low		7.1		9.4	ns
t_{ENHZ}	Enable Pad High to Z		11.5		15.3	ns
t_{ENLZ}	Enable Pad Low to Z		11.5		15.3	ns
t_{GLH}	G to Pad High		11.5		15.3	ns
t_{GHL}	G to Pad Low		12.4		16.6	ns
t_{LSU}	I/O Latch Output Setup	0.4		0.5		ns
t_{LH}	I/O Latch Output Hold	0.0		0.0		ns
t_{LCO}	I/O Latch Clock-Out (Pad-to-Pad) 32 I/O		11.5		15.4	ns
t_{ACO}	Array Latch Clock-Out (Pad-to-Pad) 32 I/O		16.3		21.7	ns
d_{TLH}	Capacitive Loading, Low to High		0.04		0.06	ns/pF
d_{THL}	Capacitive Loading, High to Low		0.06		0.08	ns/pF
t_{WDO}	Hard-Wired Wide Decode Output		0.05		0.07	ns
CMOS Output Module Timing[1]						
t_{DLH}	Data to Pad High		6.3		8.3	ns
t_{DHL}	Data to Pad Low		5.1		6.8	ns
t_{ENZH}	Enable Pad Z to High		6.6		8.8	ns
t_{ENZL}	Enable Pad Z to Low		7.1		9.4	ns
t_{ENHZ}	Enable Pad High to Z		11.5		15.3	ns
t_{ENLZ}	Enable Pad Low to Z		11.5		15.3	ns
t_{GLH}	G to Pad High		11.5		15.3	ns
t_{GHL}	G to Pad Low		12.4		16.6	ns
t_{LSU}	I/O Latch Setup	0.4		0.5		ns
t_{LH}	I/O Latch Hold	0.0		0.0		ns
t_{LCO}	I/O Latch Clock-Out (Pad-to-Pad) 32 I/O		13.7		18.2	ns
t_{ACO}	Array Latch Clock-Out (Pad-to-Pad) 32 I/O		19.2		25.6	ns
d_{TLH}	Capacitive Loading, Low to High		0.06		0.08	ns/pF
d_{THL}	Capacitive Loading, High to Low		0.05		0.07	ns/pF
t_{WDO}	Hard-Wired Wide Decode Output		0.05		0.07	ns

Notes:

1. *Delays based on 35 pF loading.*
2. *SSO information can be found in the* Simultaneously Switching Output Limits for Actel FPGAs *application note at http://www.actel.com/appnotes.*

A32200DX Timing Characteristics

(Worst-Case Military Conditions, V_{CC} = 4.5V, T_J = 125°C)

		'–1' Speed		'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
Logic Module Combinatorial Functions						
t_{PD}	Internal Array Module Delay		2.8		3.8	ns
t_{PDD}	Internal Decode Module Delay		3.4		4.6	ns
Logic Module Predicted Routing Delays[1]						
t_{RD1}	FO=1 Routing Delay		1.6		2.1	ns
t_{RD2}	FO=2 Routing Delay		2.3		3.1	ns
t_{RD3}	FO=3 Routing Delay		2.9		3.9	ns
t_{RD4}	FO=4 Routing Delay		3.5		4.7	ns
t_{RD5}	FO=8 Routing Delay		6.2		8.2	ns
t_{RDD}	Decode-to-Output Routing Delay		0.8		1.1	ns
Logic Module Sequential Timing Characteristics						
t_{CO}	Flip-Flop Clock-to-Output		3.2		4.2	ns
t_{GO}	Latch Gate-to-Output		2.8		3.8	ns
t_{SU}	Flip-Flop (Latch) Setup Time	0.5		0.6		ns
t_{H}	Flip-Flop (Latch) Hold Time	0.0		0.0		ns
t_{RO}	Flip-Flop (Latch) Reset to Output		3.2		4.2	ns
t_{SUENA}	Flip-Flop (Latch) Enable Setup	0.9		1.2		ns
t_{HENA}	Flip-Flop (Latch) Enable Hold	0.0		0.0		ns
t_{WCLKA}	Flip-Flop (Latch) Clock Active Pulse Width	4.3		5.8		ns
t_{WASYN}	Flip-Flop (Latch) Asynchronous Pulse Width	5.7		7.6		ns

Note:

1. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.

A32200DX Timing Characteristics (continued)

(Worst-Case Military Conditions, V_{CC} = 4.5V, T_J = 125°C)

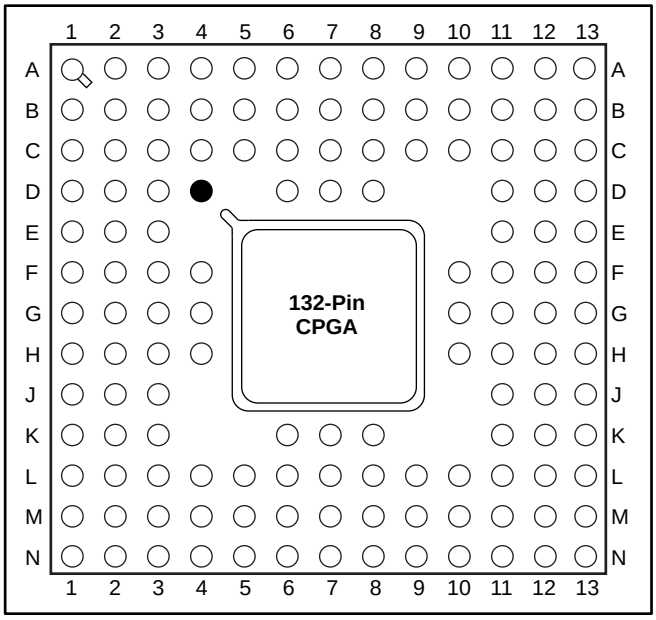
			‘–1’ Speed		‘Std’ Speed		
Parameter	**Description**		**Min.**	**Max.**	**Min.**	**Max.**	**Units**
Input Module Propagation Delays							
t_{INPY}	Input Data Pad to Y			1.9		2.6	ns
t_{INGO}	Input Latch Gate-to-Output			4.6		6.0	ns
t_{INH}	Input Latch Hold		0.0		0.0		ns
t_{INSU}	Input Latch Setup		0.7		0.9		ns
t_{ILA}	Latch Active Pulse Width		6.1		8.1		ns
Input Module Predicted Routing Delays[1]							
t_{IRD1}	FO=1 Routing Delay			2.6		3.5	ns
t_{IRD2}	FO=2 Routing Delay			3.4		4.6	ns
t_{IRD3}	FO=3 Routing Delay			4.6		6.1	ns
t_{IRD4}	FO=4 Routing Delay			5.4		7.2	ns
t_{IRD5}	FO=8 Routing Delay			7.0		9.3	ns
Global Clock Network							
t_{CKH}	Input Low to High	FO=32		7.3		9.8	ns
		FO=635		8.5		11.3	ns
t_{CKL}	Input High to Low	FO=32		7.2		9.6	ns
		FO=635		9.3		12.5	ns
t_{PWH}	Minimum Pulse Width High	FO=32	3.2		4.3		ns
		FO=635	3.9		5.2		ns
t_{PWL}	Minimum Pulse Width Low	FO=32	3.2		4.3		ns
		FO=635	3.9		5.2		ns
t_{CKSW}	Maximum Skew	FO=32		1.8		2.4	ns
		FO=635		1.8		2.4	ns
t_{SUEXT}	Input Latch External Setup	FO=32	0.0		0.0		ns
		FO=635	0.0		0.0		ns
t_{HEXT}	Input Latch External Hold	FO=32	3.0		4.0		ns
		FO=635	3.8		5.1		ns
t_P	Minimum Period (1/fmax)	FO=32	5.8		7.7		ns
		FO=635	6.8		9.1		ns
f_{HMAX}	Maximum Datapath Frequency	FO=32		172		130	MHz
		FO=635		147		110	MHz

Note:

1. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment. Optimization techniques may further reduce delays by 0 to 4 ns.

Package Pin Assignments (continued)

132-Pin CPGA (Top View)

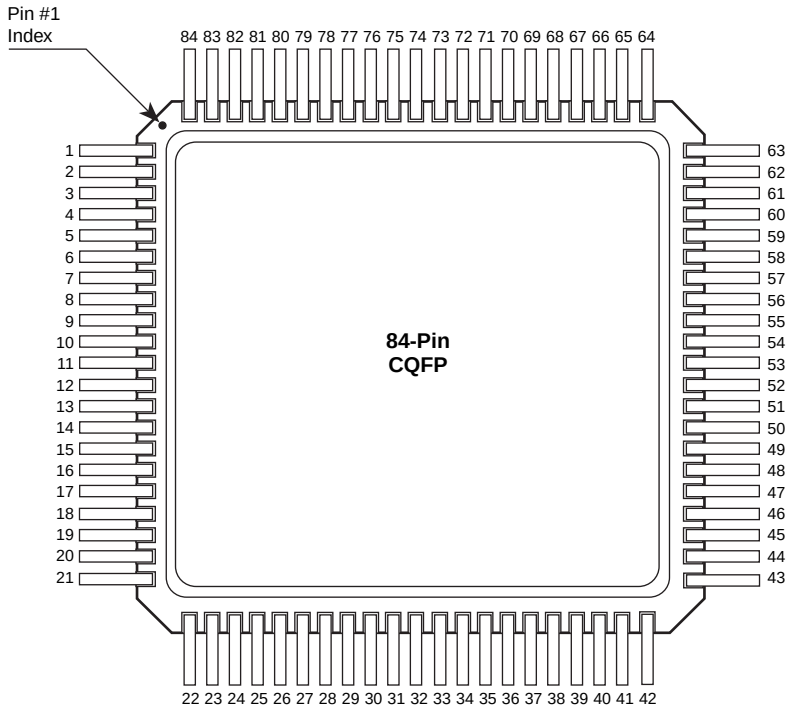


133-Pin CPGA

Pin Number	A1425A Function
A1	NC
A2	GND
A3	I/O
A4	I/O
A5	I/O
A6	PRA, I/O
A7	NC
A8	I/O
A9	I/O
A10	I/O
A11	I/O
A12	I/O
A13	NC
B1	I/O
B2	V_{CC}
B3	I/O
B4	I/O
B5	I/O
B6	CLKB, I/O
B7	V_{CC}
B8	I/O
B9	I/O
B10	I/O
B11	I/O
B12	V_{CC}
B13	I/O
C1	I/O
C2	SDI, I/O
C3	GND
C4	I/O
C5	I/O
C6	I/O
C7	GND
C8	I/O
C9	I/O
C10	IOCLK, I/O
C11	GND
C12	GND
C13	I/O
D1	I/O
D2	I/O
D3	I/O
D4	DCLK, I/O
D6	CLKA, I/O
D7	I/O
D8	I/O
D11	I/O
D12	I/O
D13	I/O
E1	I/O
E2	I/O
E3	MODE
E11	V_{CC}
E12	I/O
E13	I/O
F1	I/O
F2	I/O
F3	I/O
F4	I/O
F10	GND
F11	I/O
F12	I/O
F13	I/O
G1	NC
G2	V_{CC}
G3	GND
G4	I/O
G10	I/O
G11	GND
G12	V_{CC}
G13	NC
H1	I/O
H2	I/O
H3	I/O
H4	I/O
H10	I/O
H11	I/O
H12	I/O
H13	I/O
J1	I/O
J2	V_{CC}
J3	I/O
J11	I/O
J12	V_{CC}
J13	I/O
K1	I/O
K2	I/O
K3	I/O
K6	I/O
K7	HCLKA, I/O
K8	I/O
K11	I/O
K12	I/O
K13	I/O
L1	I/O
L2	I/O
L3	GND
L4	I/O
L5	I/O
L6	PRB, I/O
L7	GND
L8	I/O
L9	I/O
L10	IOPCL, I/O
L11	GND
L12	I/O
L13	I/O
M1	I/O
M2	V_{CC}
M3	GND
M4	I/O
M5	I/O
M6	I/O
M7	V_{CC}
M8	I/O
M9	I/O
M10	I/O
M11	I/O
M12	V_{CC}
M13	I/O
N1	NC
N2	I/O
N3	I/O
N4	I/O
N5	I/O
N6	I/O
N7	NC
N8	I/O
N9	I/O
N10	I/O
N11	I/O
N12	GND
N13	NC

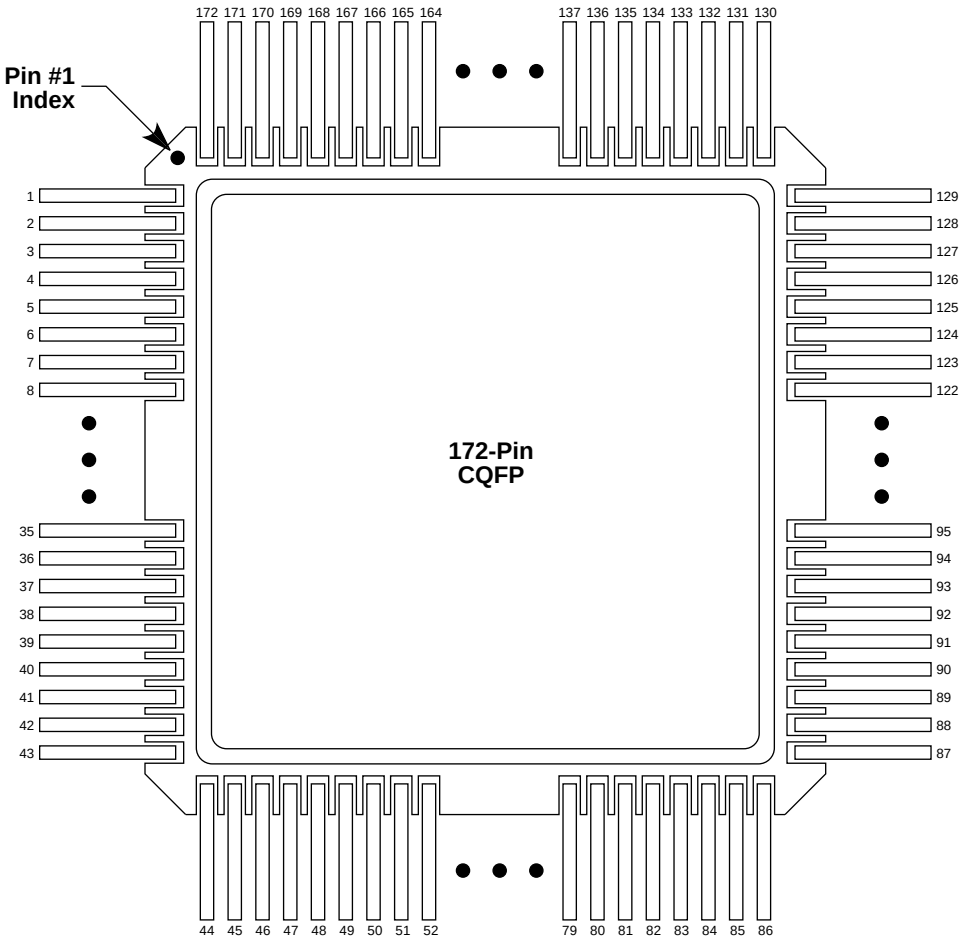
Package Pin Assignments (continued)

84-Pin CQFP (Top View)



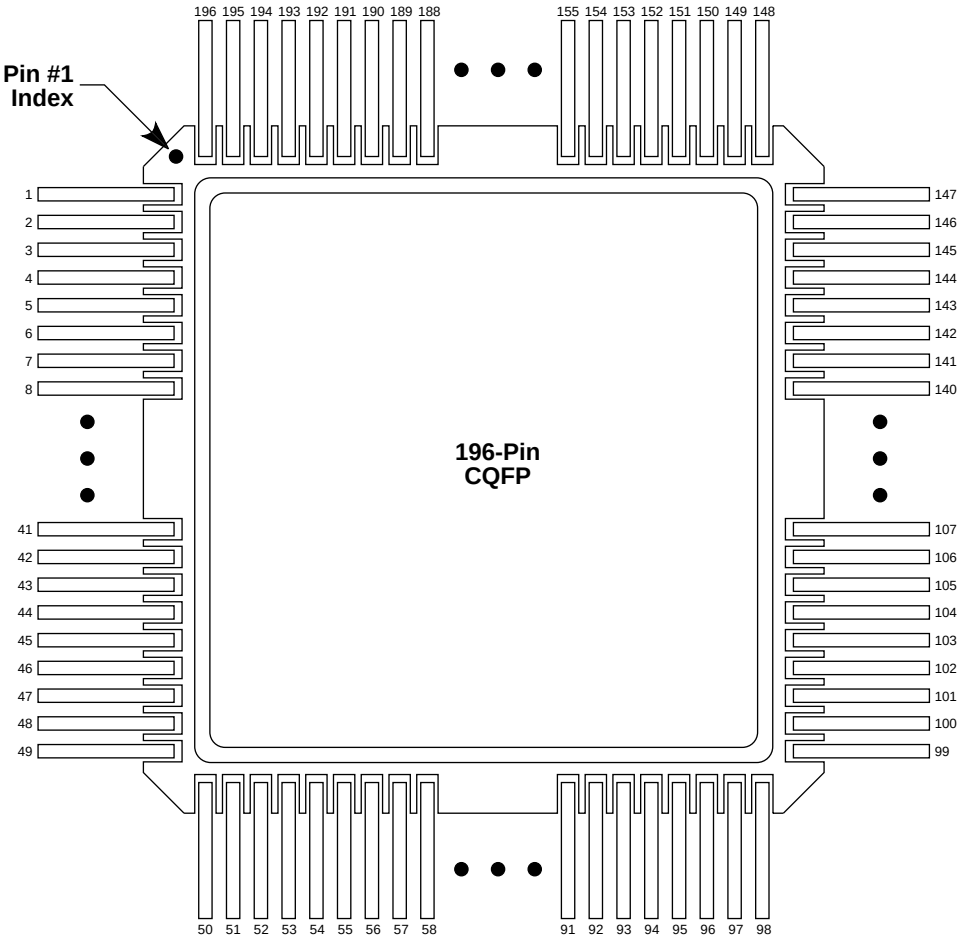
Package Pin Assignments (continued)

172-Pin CQFP (Top View)



Package Pin Assignments (continued)

196-Pin CQFP (Top View)

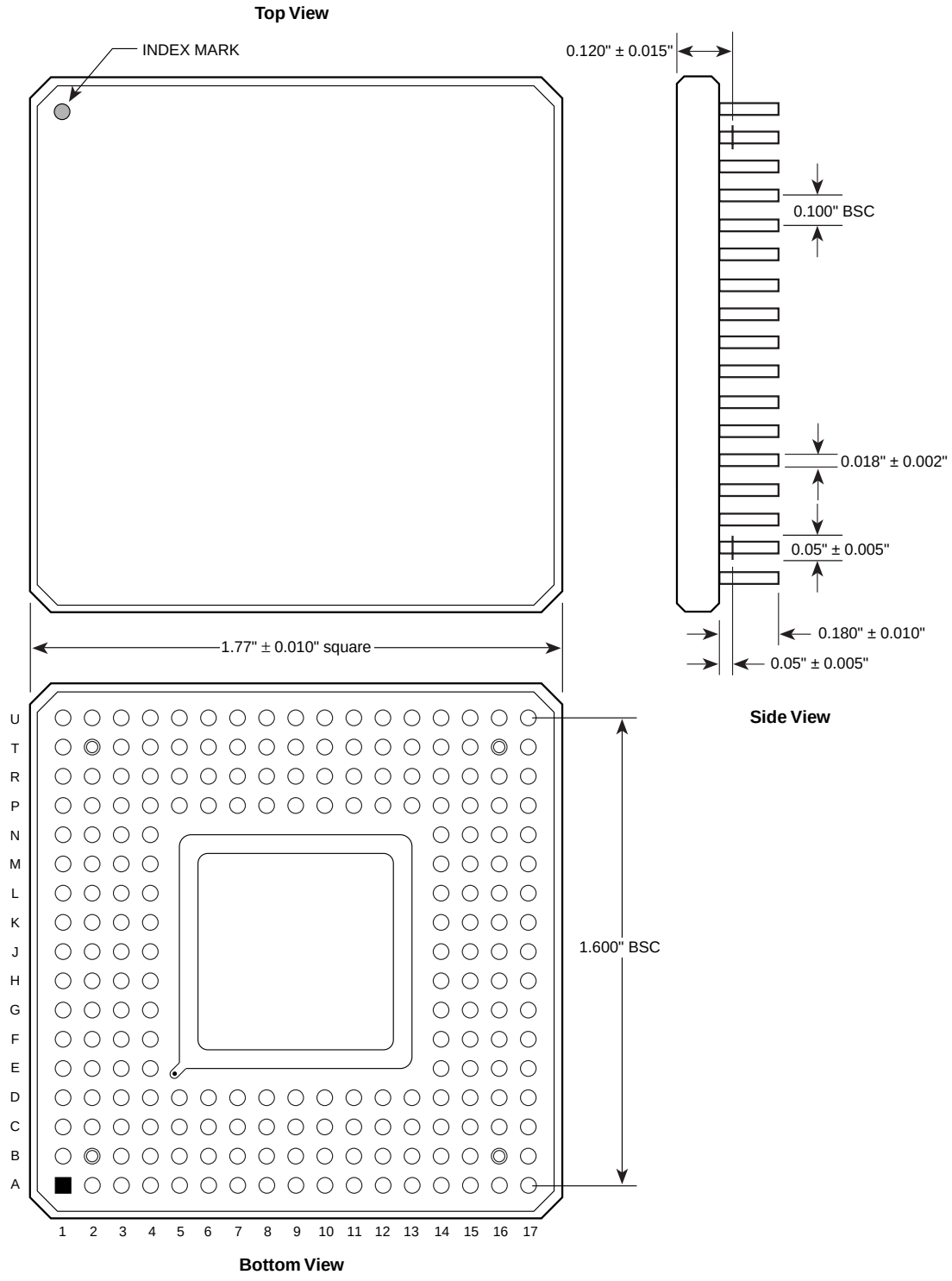


256-Pin CQFP (Continued)

Pin Number	A14100A Function	A32200DX Function
133	I/O	I/O
134	I/O	I/O
135	I/O	I/O
136	I/O	I/O
137	I/O	I/O
138	I/O	I/O
139	I/O	GND
140	I/O	I/O
141	V_{CC}	I/O
142	I/O	I/O
143	I/O	I/O
144	I/O	I/O
145	I/O	I/O
146	I/O	I/O
147	I/O	I/O
148	I/O	I/O
149	I/O	I/O
150	I/O	I/O
151	I/O	I/O
152	I/O	I/O
153	I/O	I/O
154	I/O	I/O
155	I/O	V_{CC}
156	I/O	I/O
157	I/O	I/O
158	GND	V_{CC}
159	V_{CC}	V_{CC}
160	GND	GND
161	V_{CC}	I/O
162	I/O	I/O
163	I/O	I/O
164	I/O	I/O
165	I/O	GND
166	I/O	I/O
167	I/O	I/O
168	I/O	I/O
169	I/O	I/O
170	I/O	V_{CC}
171	I/O	I/O
172	I/O	I/O
173	I/O	I/O
174	V_{CC}	I/O
175	GND	I/O
176	GND	I/O
177	I/O	I/O
178	I/O	I/O
179	I/O	I/O
180	I/O	GND
181	I/O	I/O
182	I/O	I/O
183	I/O	I/O
184	I/O	I/O
185	I/O	I/O
186	I/O	I/O
187	I/O	I/O
188	IOCLK, I/O	MODE
189	GND	V_{CC}
190	I/O	GND
191	I/O	NC
192	I/O	NC
193	I/O	NC
194	I/O	I/O
195	I/O	DCLK, I/O
196	I/O	I/O
197	I/O	I/O
198	I/O	I/O
199	I/O	I/O (WD)
200	I/O	I/O (WD)
201	I/O	V_{CC}
202	I/O	I/O
203	I/O	I/O
204	I/O	I/O
205	I/O	I/O
206	I/O	GND
207	I/O	I/O
208	I/O	I/O
209	I/O	QCLKC, I/O
210	I/O	I/O
211	I/O	I/O (WD)
212	I/O	I/O (WD)
213	I/O	I/O
214	I/O	I/O
215	I/O	I/O (WD)
216	I/O	I/O (WD)
217	I/O	I/O
218	I/O	PRB, I/O
219	CLKA, I/O	I/O
220	CLKB, I/O	CLKB, I/O
221	V_{CC}	I/O
222	GND	GND
223	V_{CC}	GND
224	GND	V_{CC}
225	PRA, I/O	V_{CC}
226	I/O	I/O
227	I/O	CLKA, I/O
228	I/O	I/O
229	I/O	PRA, I/O
230	I/O	I/O
231	I/O	I/O
232	I/O	I/O (WD)
233	I/O	I/O (WD)
234	I/O	I/O
235	I/O	I/O
236	I/O	I/O
237	I/O	I/O
238	I/O	I/O
239	I/O	I/O
240	GND	QCLKD, I/O
241	I/O	I/O
242	I/O	I/O (WD)
243	I/O	GND
244	I/O	I/O (WD)
245	I/O	I/O
246	I/O	I/O
247	I/O	I/O
248	I/O	V_{CC}
249	I/O	I/O
250	I/O	I/O (WD)
251	I/O	I/O (WD)
252	I/O	I/O
253	I/O	SDI, I/O
254	I/O	I/O
255	I/O	GND
256	DCLK, I/O	NC

Package Mechanical Drawings (continued)

207-Pin CPGA

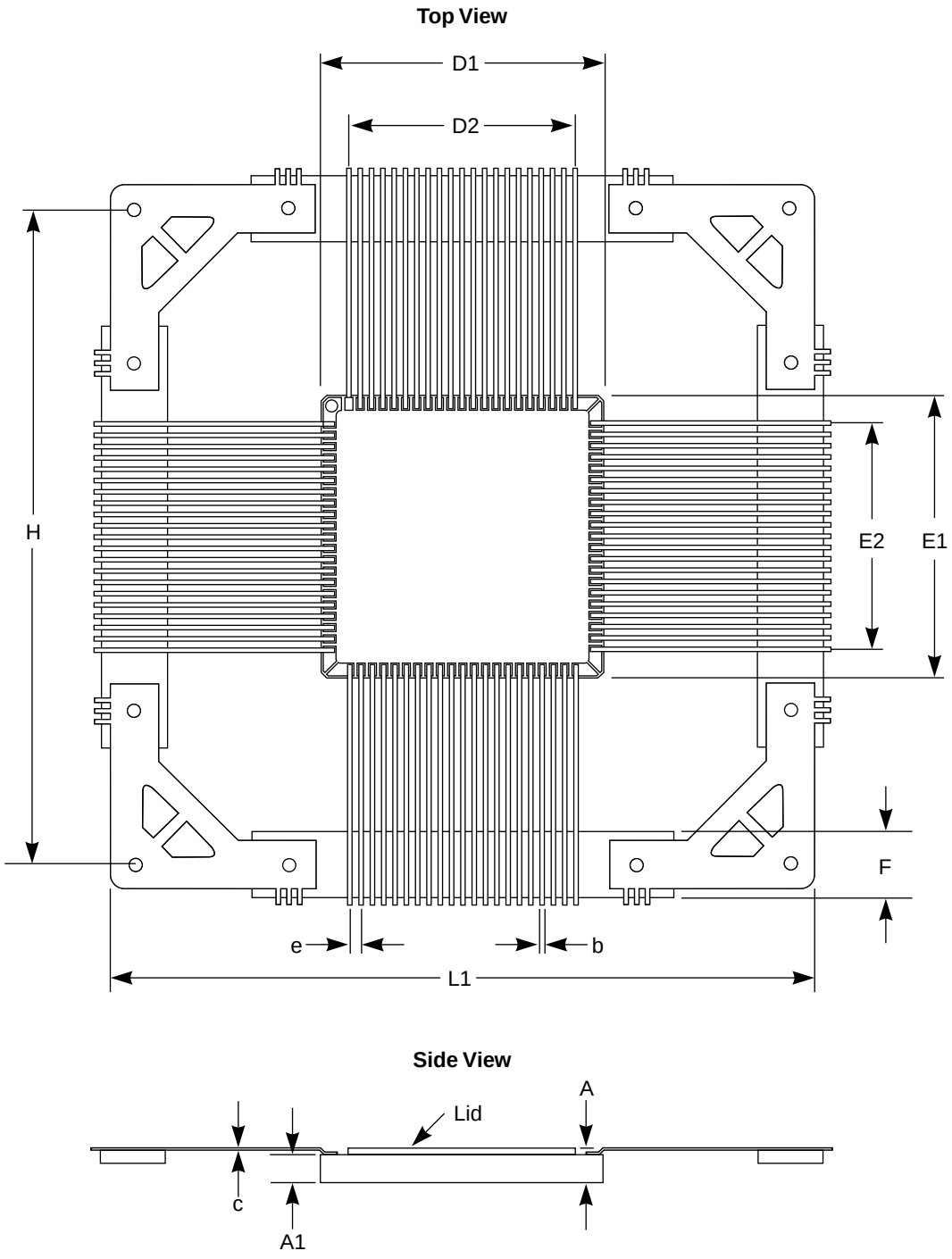


Notes:

1. *All dimensions are in inches unless otherwise stated.*
2. *BSC—Basic Spacing between Centers. This is a theoretical true position dimension and so has no tolerance.*

Package Mechanical Drawings (continued)

84-Pin CQFP



Notes:

1. *Seal ring and lid are connected to Ground.*
2. *Lead material is Kovar with minimum 50 microinches gold plate over nickel.*
3. *Packages are shipped unformed with the ceramic tie bar in a test carrier.*