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Understanding Embedded - FPGAs (Field Programmable Gate Array)

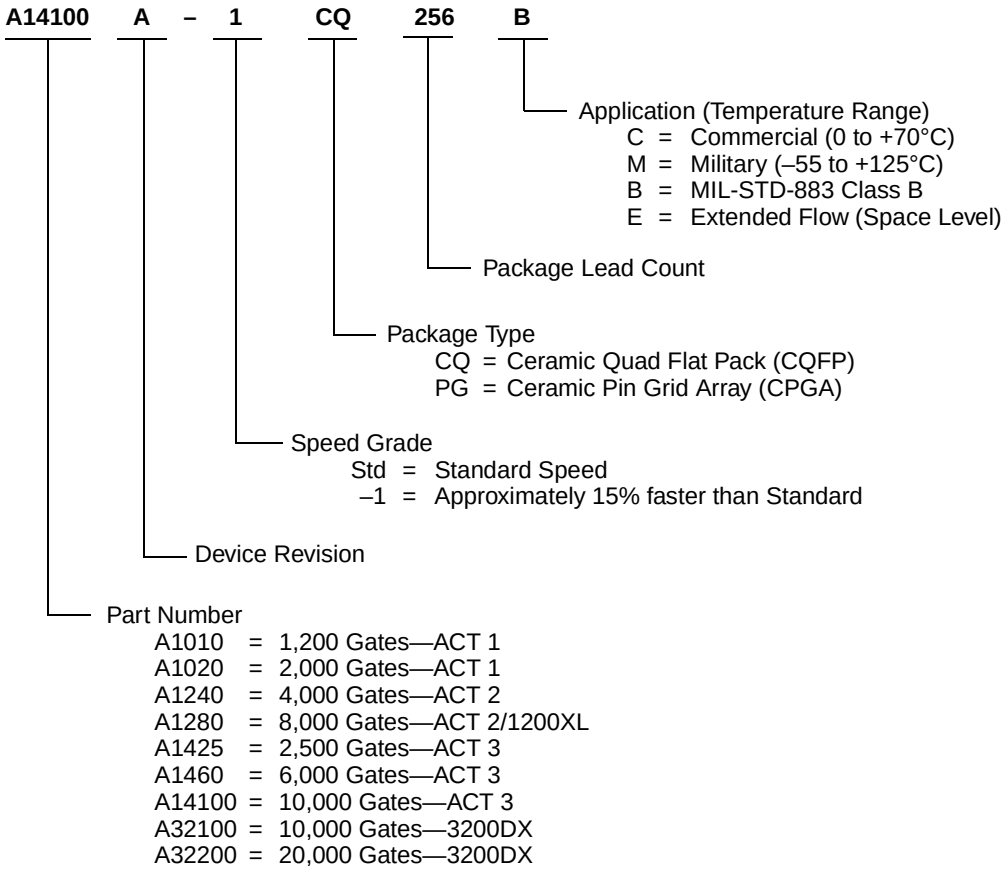
Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	547
Number of Logic Elements/Cells	-
Total RAM Bits	-
Number of I/O	69
Number of Gates	2000
Voltage - Supply	4.5V ~ 5.5V
Mounting Type	Through Hole
Operating Temperature	-55°C ~ 125°C (TJ)
Package / Case	84-BCPGA
Supplier Device Package	84-CPGA (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/microsemi/a1020b-pg84b

Military Device Ordering Information



DESC SMD/Actel Part Number Cross Reference

Actel Part Number (Gold Leads)	DSCC SMD (Gold Leads)	DSCC SMD (Solder Dipped)
A1010B-PG84B	5962-9096403MXC	5962-9096403MXA
A1010B-1PG84B	5962-9096404MXC	5962-9096404MXA
A1020B-PG84B	5962-9096503MUC	5962-9096503MUA
A1020B-1PG84B	5962-9096504MUC	5962-9096504MUA
A1020B-CQ84B	5962-9096503MTC	5962-9096503MTA
A1020B-1CQ84B	5962-9096504MTC	5962-9096504MTA
A1240A-PG132B	5962-9322101MXC	5962-9322101MXA
A1240A-1PG132B	5962-9322102MXC	5962-9322102MXA
A1280A-PG176B	5962-9215601MXC	5962-9215601MXA
A1280A-1PG176B	5962-9215602MXC	5962-9215602MXA
A1280A-CQ172B	5962-9215601MYC	5962-9215601MYA
A1280A-1CQ172B	5962-9215602MYC	5962-9215602MYA
A1425A-PG133B	5962-9552001MXC	N/A
A1425A-1PG133B	5962-9552002MXC	N/A
A1425A-CQ132B	5962-9552001MYC	N/A
A1425A-1CQ132B	5962-9552002MYC	N/A
A1460A-PG207B	5962-9550801MXC	N/A
A1460A-1PG207B	5962-9550802MXC	N/A
A1460A-CQ196B	5962-9550801MYC	N/A
A1460A-1CQ196B	5962-9550802MYC	N/A
A14100A-PG257B	5962-9552101MXC	N/A
A14100A-1PG257B	5962-9552102MXC	N/A
A14100A-CQ256B	5962-9552101MYC	N/A
A14100A-1CQ256B	5962-9552102MYC	N/A
A32100DX-CQ84B	5962-9875901QXC	N/A
A32100DX-1CQ84B	5962-9857902QXC	N/A
A32200DX-CQ256B	5962-9952701QXC	N/A
A32200DX-1CQ256B	5962-9952702QXC	N/A
A32200DX-CQ208B	5962-9952701QYC	N/A
A32200DX-1CQ208B	5962-9952702QYC	N/A

Actel Extended Flow[1]

Step	Screen	Method	Require-ment
1.	Wafer Lot Acceptance[2]	5007 with Step Coverage Waiver	All Lots
2.	Destructive In-Line Bond Pull[3]	2011, Condition D	Sample
3.	Internal Visual	2010, Condition A	100%
4.	Serialization		100%
5.	Temperature Cycling	1010, Condition C	100%
6.	Constant Acceleration	2001, Condition D or E, Y_1 Orientation Only	100%
7.	Particle Impact Noise Detection	2020, Condition A	100%
8.	Radiographic	2012 (one view only)	100%
9.	Pre-Burn-In Test	In accordance with applicable Actel device specification	100%
10.	Burn-in Test	1015, Condition D, 240 hours @ 125°C minimum	100%
11.	Interim (Post-Burn-In) Electrical Parameters	In accordance with applicable Actel device specification	100%
12.	Reverse Bias Burn-In	1015, Condition C, 72 hours @ 150°C minimum	100%
13.	Interim (Post-Burn-In) Electrical Parameters	In accordance with applicable Actel device specification	100%
14.	Percent Defective Allowable (PDA) Calculation	5%, 3% Functional Parameters @ 25°C	All Lots
15.	Final Electrical Test	In accordance with Actel applicable device specification which includes a, b, and c:	100%
	a. Static Tests		100%
	(1) 25°C (Subgroup 1, Table1)	5005	
	(2) –55°C and +125°C (Subgroups 2, 3, Table 1)	5005	
	b. Functional Tests		100%
	(1) 25°C (Subgroup 7, Table 15)	5005	
	(2) –55°C and +125°C (Subgroups 8A and B, Table 1)	5005	
	c. Switching Tests at 25°C (Subgroup 9, Table 1)	5005	100%
16.	Seal	1014	100%
	a. Fine		
	b. Gross		
17.	External Visual	2009	100%

Notes:

1. *Actel offers the extended flow for customers who require additional screening beyond the requirements of the MIL-STD-833, Class B. Actel is compliant to the requirements of MIL-STD-883, Paragraph 1.2.1, and MIL-I-38535, Appendix A. Actel is offering this extended flow incorporating the majority of the screening procedures as outlined in Method 5004 of MIL-STD-883, Class S. The exceptions to Method 5004 are shown in notes 2 and 3 below.*
2. *Wafer lot acceptance is performed to Method 5007; however, the step coverage requirement as specified in Method 2018 must be waived.*
3. *MIL-STD-883, Method 5004 requires 100 percent Radiation latch-up testing (Method 1020). Actel will not be performing any radiation testing, and this requirement must be waived in its entirety.*

Absolute Maximum Ratings[1]

Free air temperature range

Symbol	Parameter	Limits	Units
V_{CC}	DC Supply Voltage[2, 3, 4]	–0.5 to +7.0	V
V_I	Input Voltage	–0.5 to V_{CC} +0.5	V
V_O	Output Voltage	–0.5 to V_{CC} +0.5	V
I_{IO}	I/O Source Sink Current[5]	±20	mA
T_{STG}	Storage Temperature	–65 to +150	°C

Notes:

1. *Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. Devices should not be operated outside the recommended operating conditions.*
2. *$V_{PP} = V_{CC}$, except during device programming.*
3. *$V_{SV} = V_{CC}$, except during device programming.*
4. *$V_{KS} = GND$, except during device programming.*
5. *Device inputs are normally high impedance and draw extremely low current. However, when input voltage is greater than V_{CC} + 0.5V or less than GND – 0.5V, the internal protection diode will be forward biased and can draw excessive current.*

Recommended Operating Conditions

Parameter	Commercial	Military	Units
Temperature Range[1]	0 to +70	–55 to +125	°C
Power Supply Tolerance[2]	±5	±10	%V_{CC}

Notes:

1. *Ambient temperature (T_A) is used for commercial and industrial; case temperature (T_C) is used for military.*
2. *All power supplies must be in the recommended operating range. For more information, refer to the* Power-Up Design Considerations *application note at http://www.actel.com/appnotes.*

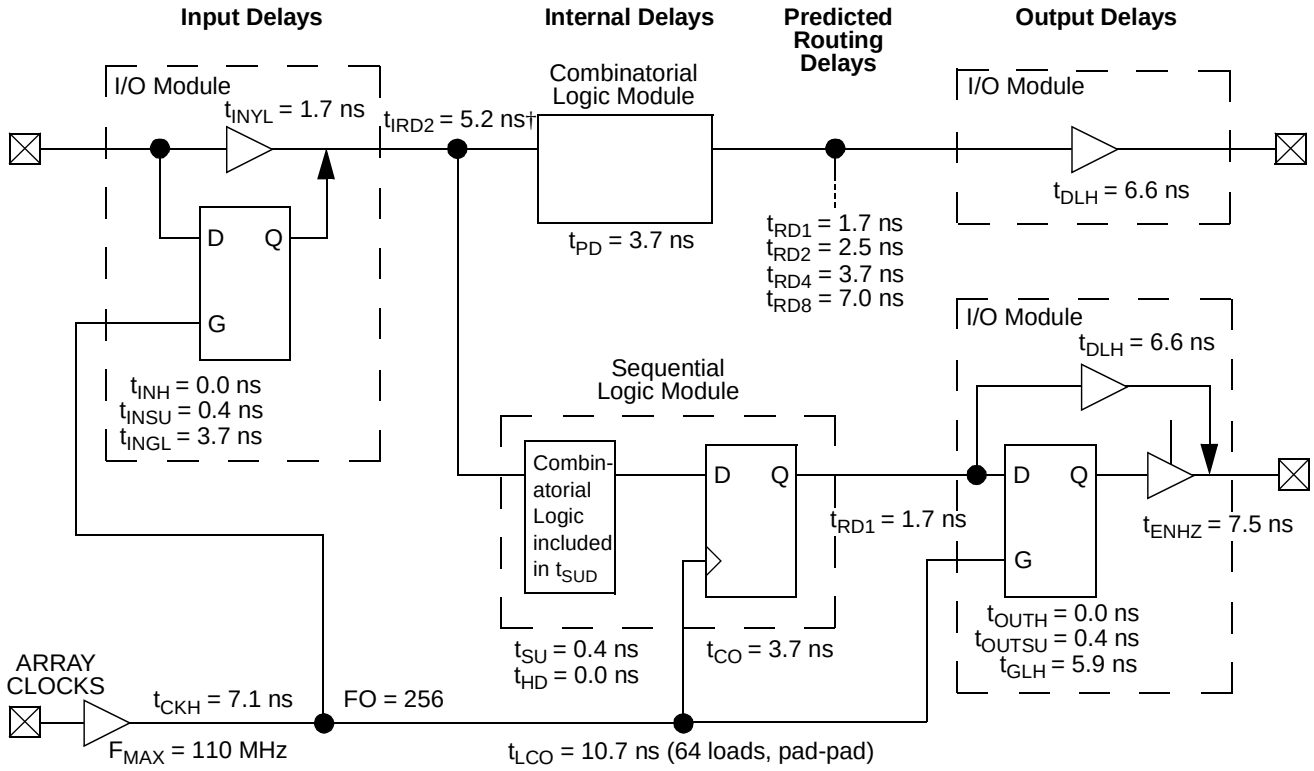
Electrical Specifications

Symbol	Parameter	Test Condition	Commercial		Military		Units
			Min.	Max.	Min.	Max.	
V_{OH}[1, 2]	HIGH Level Output	I_{OH} = –4 mA (CMOS)			3.7		V
		I_{OH} = –6 mA (CMOS)	3.84				V
V_{OL}[1, 2]	LOW Level Output	I_{OL} = +6 mA (CMOS)		0.33		0.4	V
V_{IH}	HIGH Level Input	TTL Inputs	2.0	V_{CC} + 0.3	2.0	V_{CC} + 0.3	V
V_{IL}	LOW Level Input	TTL Inputs	–0.3	0.8	–0.3	0.8	V
I_{IN}	Input Leakage	$V_I = V_{CC}$ or GND	–10	+10	–10	+10	µA
I_{OZ}	3-state Output Leakage	$V_O = V_{CC}$ or GND	–10	+10	–10	+10	µA
C_{IO}	I/O Capacitance[3, 4]			10		10	pF
$I_{CC(S)}$	Standby V_{CC} Supply Current	$V_I = V_{CC}$ or GND, I_O = 0 mA					
		ACT 1		3		20	mA
		ACT 2/3/1200XL/3200DX		2		20	mA
$I_{CC(D)}$	Dynamic V_{CC} Supply Current	See the "Power Dissipation" section on page 11.					

Notes:

1. *Actel devices can drive and receive either CMOS or TTL signal levels. No assignment of I/Os as TTL or CMOS is required.*
2. *Tested one output at a time, V_{CC} = min.*
3. *Not tested; for information only.*
4. *V_{OUT} = 0V, f = 1 MHz*

1200XL Timing Model*

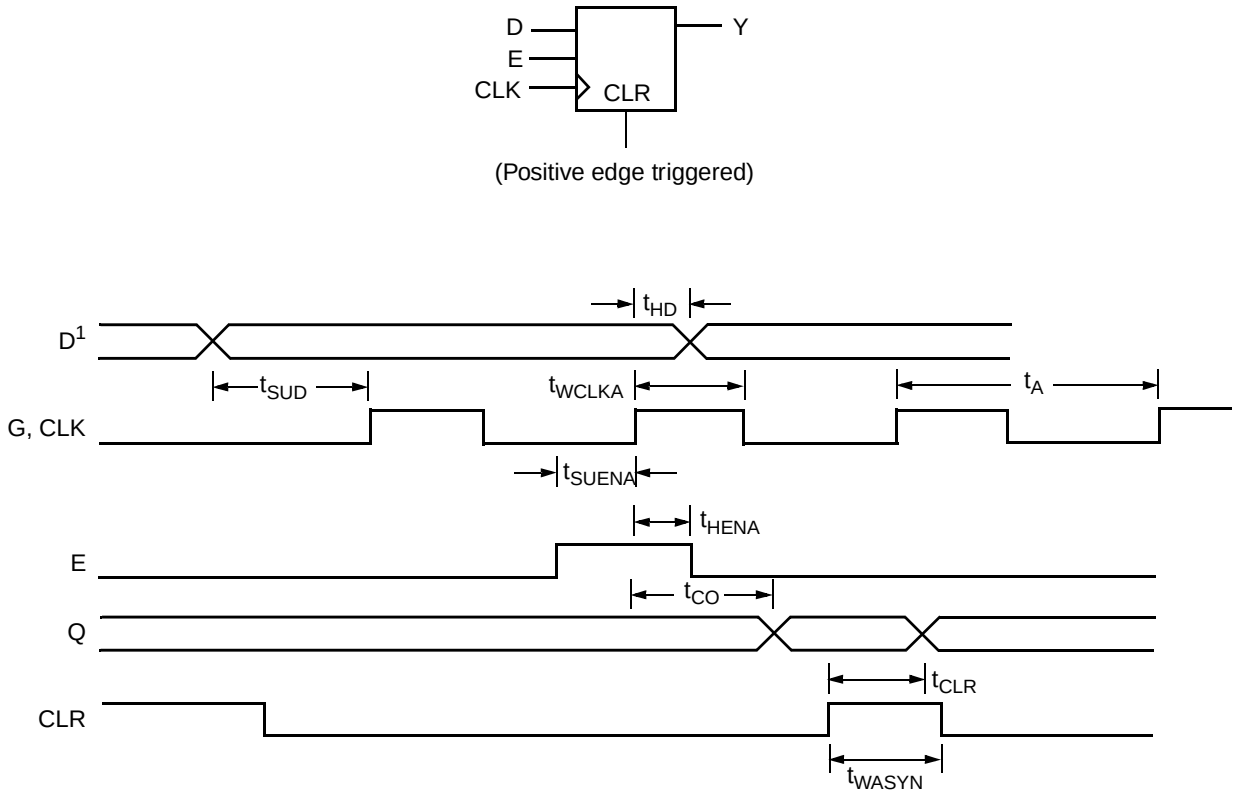


**Values shown for A1280XL–1 at worst-case military conditions.*

† Input module predicted routing delay.

Sequential Timing Characteristics

Flip-Flops and Latches (ACT 3)

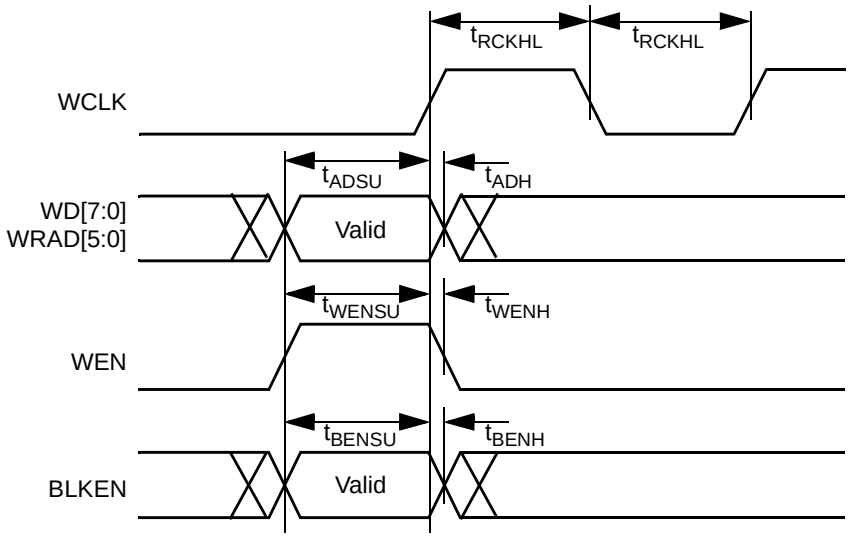


Note:

1. D represents all data functions involving A, B, and S for multiplexed flip-flops.

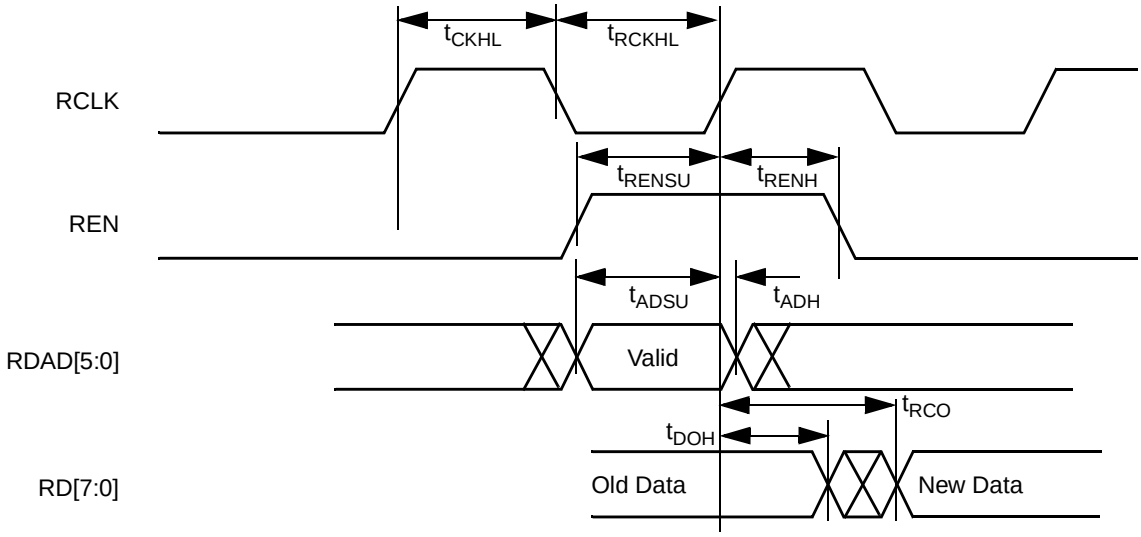
Dual-Port SRAM Timing Waveforms

3200DX SRAM Write Operation



Note: *Identical timing for falling-edge clock.*

3200DX SRAM Synchronous Read Operation



Note: *Identical timing for falling-edge clock.*

A1240A Timing Characteristics

(Worst-Case Military Conditions, V_{CC} = 4.5V, T_J = 125°C)

		'–1' Speed		'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
Logic Module Propagation Delays[1]						
t_{PD1}	Single Module		5.2		6.1	ns
t_{CO}	Sequential Clk to Q		5.2		6.1	ns
t_{GO}	Latch G to Q		5.2		6.1	ns
t_{RS}	Flip-Flop (Latch) Reset to Q		5.2		6.1	ns
Logic Module Predicted Routing Delays[2]						
t_{RD1}	FO=1 Routing Delay		1.9		2.2	ns
t_{RD2}	FO=2 Routing Delay		2.4		2.8	ns
t_{RD3}	FO=3 Routing Delay		3.1		3.7	ns
t_{RD4}	FO=4 Routing Delay		4.3		5.0	ns
t_{RD8}	FO=8 Routing Delay		6.6		7.7	ns
Logic Module Sequential Timing[3, 4]						
t_{SUD}	Flip-Flop (Latch) Data Input Setup	0.5		0.5		ns
t_{HD}	Flip-Flop (Latch) Data Input Hold	0.0		0.0		ns
t_{SUENA}	Flip-Flop (Latch) Enable Setup	1.3		1.3		ns
t_{HENA}	Flip-Flop (Latch) Enable Hold	0.0		0.0		ns
t_{WCLKA}	Flip-Flop (Latch) Clock Active Pulse Width	7.4		8.1		ns
t_{WASYN}	Flip-Flop (Latch) Asynchronous Pulse Width	7.4		8.1		ns
t_A	Flip-Flop Clock Input Period	14.8		18.6		ns
t_{INH}	Input Buffer Latch Hold	2.5		2.5		ns
t_{INSU}	Input Buffer Latch Setup	–3.5		–3.5		ns
t_{OUTH}	Output Buffer Latch Hold	0.0		0.0		ns
t_{OUTSU}	Output Buffer Latch Setup	0.5		0.5		ns
f_{MAX}	Flip-Flop (Latch) Clock Frequency		63		54	MHz

Notes:

1. *For dual-module macros, use $t_{PD1} + t_{RD1} + t_{PDn}$, $t_{CO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.*
2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*
3. *Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the DirectTime Analyzer utility.*
4. *Setup and hold timing parameters for the Input Buffer Latch are defined with respect to the PAD and the D input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.*

A1240A Timing Characteristics (continued)

(Worst-Case Military Conditions, V_{CC} = 4.5V, T_J = 125°C)

			'–1' Speed		'Std' Speed		
Parameter	**Description**		**Min.**	**Max.**	**Min.**	**Max.**	**Units**
Input Module Propagation Delays							
t_{INYH}	Pad to Y High			4.0		4.7	ns
t_{INYL}	Pad to Y Low			3.6		4.3	ns
t_{INGH}	G to Y High			6.9		8.1	ns
t_{INGL}	G to Y Low			6.6		7.7	ns
Input Module Predicted Routing Delays[1]							
t_{IRD1}	FO=1 Routing Delay			5.8		6.9	ns
t_{IRD2}	FO=2 Routing Delay			6.7		7.8	ns
t_{IRD3}	FO=3 Routing Delay			7.5		8.8	ns
t_{IRD4}	FO=4 Routing Delay			8.2		9.7	ns
t_{IRD8}	FO=8 Routing Delay			10.9		12.9	ns
Global Clock Network							
t_{CKH}	Input Low to High	FO = 32 FO = 256		13.3 16.3		15.7 19.2	ns
t_{CKL}	Input High to Low	FO = 32 FO = 256		13.3 16.5		15.7 19.5	ns
t_{PWH}	Minimum Pulse Width High	FO = 32 FO = 256	5.7 6.0		6.7 7.1		ns
t_{PWL}	Minimum Pulse Width Low	FO = 32 FO = 256	5.7 6.0		6.7 7.1		ns
t_{CKSW}	Maximum Skew	FO = 32 FO = 256		0.6 3.1		0.6 3.1	ns
t_{SUEXT}	Input Latch External Setup	FO = 32 FO = 256	0.0 0.0		0.0 0.0		ns
t_{HEXT}	Input Latch External Hold	FO = 32 FO = 256	8.6 13.8		8.6 13.8		ns
t_P	Minimum Period	FO = 32 FO = 256	11.5 12.2		13.5 14.3		ns
f_{MAX}	Maximum Frequency	FO = 32 FO = 256		87 82		74 70	MHz

Note:

1. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment. Optimization techniques may further reduce delays by 0 to 4 ns.

A1240A Timing Characteristics (continued)

(Worst-Case Military Conditions, V_{CC} = 4.5V, T_J = 125°C)

		'–1' Speed		'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
TTL Output Module Timing[1]						
t_{DLH}	Data to Pad High		11.0		13.0	ns
t_{DHL}	Data to Pad Low		13.9		16.4	ns
t_{ENZH}	Enable Pad Z to High		12.3		14.4	ns
t_{ENZL}	Enable Pad Z to Low		16.1		19.0	ns
t_{ENHZ}	Enable Pad High to Z		9.8		11.5	ns
t_{ENLZ}	Enable Pad Low to Z		11.5		13.6	ns
t_{GLH}	G to Pad High		12.4		14.6	ns
t_{GHL}	G to Pad Low		15.5		18.2	ns
d_{TLH}	Delta Low to High		0.09		0.11	ns/pF
d_{THL}	Delta High to Low		0.17		0.20	ns/pF
CMOS Output Module Timing[1]						
t_{DLH}	Data to Pad High		14.0		16.5	ns
t_{DHL}	Data to Pad Low		11.7		13.7	ns
t_{ENZH}	Enable Pad Z to High		12.3		14.4	ns
t_{ENZL}	Enable Pad Z to Low		16.1		19.0	ns
t_{ENHZ}	Enable Pad High to Z		9.8		11.5	ns
t_{ENLZ}	Enable Pad Low to Z		11.5		13.6	ns
t_{GLH}	G to Pad High		12.4		14.6	ns
t_{GHL}	G to Pad Low		15.5		18.2	ns
d_{TLH}	Delta Low to High		0.17		0.20	ns/pF
d_{THL}	Delta High to Low		0.12		0.15	ns/pF

Notes:

1. *Delays based on 50 pF loading.*
2. *SSO information can be found in the* Simultaneously Switching Output Limits for Actel FPGAs *application note at http://www.actel.com/appnotes.*

A1280A Timing Characteristics

(Worst-Case Military Conditions, V_{CC} = 4.5V, T_J = 125°C)

		'–1' Speed		'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
Logic Module Propagation Delays[1]						
t_{PD1}	Single Module		5.2		6.1	ns
t_{CO}	Sequential Clk to Q		5.2		6.1	ns
t_{GO}	Latch G to Q		5.2		6.1	ns
t_{RS}	Flip-Flop (Latch) Reset to Q		5.2		6.1	ns
Logic Module Predicted Routing Delays[2]						
t_{RD1}	FO=1 Routing Delay		2.4		2.8	ns
t_{RD2}	FO=2 Routing Delay		3.4		4.0	ns
t_{RD3}	FO=3 Routing Delay		4.2		4.9	ns
t_{RD4}	FO=4 Routing Delay		5.1		6.0	ns
t_{RD8}	FO=8 Routing Delay		9.2		10.8	ns
Logic Module Sequential Timing[3, 4]						
t_{SUD}	Flip-Flop (Latch) Data Input Setup	0.5		0.5		ns
t_{HD}	Flip-Flop (Latch) Data Input Hold	0.0		0.0		ns
t_{SUENA}	Flip-Flop (Latch) Enable Setup	1.3		1.3		ns
t_{HENA}	Flip-Flop (Latch) Enable Hold	0.0		0.0		ns
t_{WCLKA}	Flip-Flop (Latch) Clock Active Pulse Width	7.4		8.6		ns
t_{WASYN}	Flip-Flop (Latch) Asynchronous Pulse Width	7.4		8.6		ns
t_A	Flip-Flop Clock Input Period	16.4		22.1		ns
t_{INH}	Input Buffer Latch Hold	2.5		2.5		ns
t_{INSU}	Input Buffer Latch Setup	–3.5		–3.5		ns
t_{OUTH}	Output Buffer Latch Hold	0.0		0.0		ns
t_{OUTSU}	Output Buffer Latch Setup	0.5		0.5		ns
f_{MAX}	Flip-Flop (Latch) Clock Frequency		60		41	MHz

Notes:

1. *For dual-module macros, use $t_{PD1} + t_{RD1} + t_{PDn}$, $t_{CO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.*
2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*
3. *Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the DirectTime Analyzer utility.*
4. *Setup and hold timing parameters for the input buffer latch are defined with respect to the PAD and the D input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.*

A1425A Timing Characteristics

(Worst-Case Military Conditions, V_{CC} = 4.5V, T_J = 125°C)

		'–1' Speed		'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
Logic Module Propagation Delays[1]						
t_{PD}	Internal Array Module		3.0		3.5	ns
t_{CO}	Sequential Clock to Q		3.0		3.5	ns
t_{CLR}	Asynchronous Clear to Q		3.0		3.5	ns
Logic Module Predicted Routing Delays[2]						
t_{RD1}	FO=1 Routing Delay		1.3		1.5	ns
t_{RD2}	FO=2 Routing Delay		1.9		2.1	ns
t_{RD3}	FO=3 Routing Delay		2.1		2.5	ns
t_{RD4}	FO=4 Routing Delay		2.6		2.9	ns
t_{RD8}	FO=8 Routing Delay		4.2		4.9	ns
Logic Module Sequential Timing						
t_{SUD}	Flip-Flop (Latch) Data Input Setup	0.9		1.0		ns
t_{HD}	Flip-Flop (Latch) Data Input Hold	0.0		0.0		ns
t_{SUENA}	Flip-Flop (Latch) Enable Setup	0.9		1.0		ns
t_{HENA}	Flip-Flop (Latch) Enable Hold	0.0		0.0		ns
t_{WASYN}	Asynchronous Pulse Width	3.8		4.4		ns
t_{WCLKA}	Flip-Flop Clock Pulse Width	3.8		4.4		ns
t_A	Flip-Flop Clock Input Period	7.9		9.3		ns
f_{MAX}	Flip-Flop Clock Frequency		125		100	MHz
Input Module Propagation Delays						
t_{INY}	Input Data Pad to Y		4.2		4.9	ns
t_{ICKY}	Input Reg IOCLK Pad to Y		7.0		8.2	ns
t_{OCKY}	Output Reg IOCLK Pad to Y		7.0		8.2	ns
t_{ICLRY}	Input Asynchronous Clear to Y		7.0		8.2	ns
t_{OCLRY}	Output Asynchronous Clear to Y		7.0		8.2	ns
Input Module Predicted Routing Delays[1, 3]						
t_{IRD1}	FO=1 Routing Delay		1.3		1.5	ns
t_{IRD2}	FO=2 Routing Delay		1.9		2.1	ns
t_{IRD3}	FO=3 Routing Delay		2.1		2.5	ns
t_{IRD4}	FO=4 Routing Delay		2.6		2.9	ns
t_{IRD8}	FO=8 Routing Delay		4.2		4.9	ns

Notes:

1. *For dual-module macros, use $t_{PD} + t_{RD1} + t_{PDn}$, $t_{CO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.*
2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*
3. *Optimization techniques may further reduce delays by 0 to 4 ns.*

A1460A Timing Characteristics (continued)

(Worst-Case Military Conditions, V_{CC} = 4.5V, T_J = 125°C)

		'–1' Speed		'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
CMOS Output Module Timing[1]						
t_{DHS}	Data to Pad, High Slew		9.2		10.8	ns
t_{DLS}	Data to Pad, Low Slew		17.3		20.3	ns
t_{ENZHS}	Enable to Pad, Z to H/L, High Slew		7.7		9.1	ns
t_{ENZLS}	Enable to Pad, Z to H/L, Low Slew		13.1		15.5	ns
t_{ENHSZ}	Enable to Pad, H/L to Z, High Slew		10.9		12.8	ns
t_{ENLSZ}	Enable to Pad, H/L to Z, Low Slew		10.9		12.8	ns
t_{CKHS}	IOCLK Pad to Pad H/L, High Slew		14.1		16.0	ns
t_{CKLS}	IOCLK Pad to Pad H/L, Low Slew		20.2		22.4	ns
d_{TLHHS}	Delta Low to High, High Slew		0.06		0.07	ns/pF
d_{TLHLS}	Delta Low to High, Low Slew		0.11		0.13	ns/pF
d_{THLHS}	Delta High to Low, High Slew		0.04		0.05	ns/pF
d_{THLLS}	Delta High to Low, Low Slew		0.05		0.06	ns/pF
Dedicated (Hard-Wired) I/O Clock Network						
t_{IOCKH}	Input Low to High (Pad to I/O Module Input)		3.5		4.1	ns
t_{IOPWH}	Minimum Pulse Width High	4.8		5.7		ns
t_{IOPWL}	Minimum Pulse Width Low	4.8		5.7		ns
t_{IOSAPW}	Minimum Asynchronous Pulse Width	3.9		4.4		ns
t_{IOCKSW}	Maximum Skew		0.9		1.0	ns
t_{IOP}	Minimum Period	9.9		11.6		ns
f_{IOMAX}	Maximum Frequency		100		85	MHz
Dedicated (Hard-Wired) Array Clock Network						
t_{HCKH}	Input Low to High (Pad to S-Module Input)		5.5		6.4	ns
t_{HCKL}	Input High to Low (Pad to S-Module Input)		5.5		6.4	ns
t_{HPWH}	Minimum Pulse Width High	4.8		5.7		ns
t_{HPWL}	Minimum Pulse Width Low	4.8		5.7		ns
t_{HCKSW}	Maximum Skew		0.9		1.0	ns
t_{HP}	Minimum Period	9.9		11.6		ns
f_{HMAX}	Maximum Frequency		100		85	MHz

Notes:

1. *Delays based on 35 pF loading.*
2. *SSO information can be found in the* Simultaneously Switching Output Limits for Actel FPGAs *application note at http://www.actel.com/appnotes.*

A14100A Timing Characteristics

(Worst-Case Military Conditions, V_{CC} = 4.5V, T_J = 125°C)

		'–1' Speed		'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
Logic Module Propagation Delays[1]						
t_{PD}	Internal Array Module		3.0		3.5	ns
t_{CO}	Sequential Clock to Q		3.0		3.5	ns
t_{CLR}	Asynchronous Clear to Q		3.0		3.5	ns
Logic Module Predicted Routing Delays[2]						
t_{RD1}	FO=1 Routing Delay		1.3		1.5	ns
t_{RD2}	FO=2 Routing Delay		1.9		2.1	ns
t_{RD3}	FO=3 Routing Delay		2.1		2.5	ns
t_{RD4}	FO=4 Routing Delay		2.6		2.9	ns
t_{RD8}	FO=8 Routing Delay		4.2		4.9	ns
Logic Module Sequential Timing						
t_{SUD}	Flip-Flop (Latch) Data Input Setup	1.0		1.0		ns
t_{HD}	Flip-Flop (Latch) Data Input Hold	0.6		0.6		ns
t_{SUENA}	Flip-Flop (Latch) Enable Setup	1.0		1.0		ns
t_{HENA}	Flip-Flop (Latch) Enable Hold	0.6		0.6		ns
t_{WASYN}	Asynchronous Pulse Width	4.8		5.6		ns
t_{WCLKA}	Flip-Flop Clock Pulse Width	4.8		5.6		ns
t_{A}	Flip-Flop Clock Input Period	9.9		11.6		ns
f_{MAX}	Flip-Flop Clock Frequency		100		85	MHz
Input Module Propagation Delays						
t_{INY}	Input Data Pad to Y		4.2		4.9	ns
t_{ICKY}	Input Reg IOCLK Pad to Y		7.0		8.2	ns
t_{OCKY}	Output Reg IOCLK Pad to Y		7.0		8.2	ns
t_{ICLRY}	Input Asynchronous Clear to Y		7.0		8.2	ns
t_{OCLRY}	Output Asynchronous Clear to Y		7.0		8.2	ns
Input Module Predicted Routing Delays[2, 3]						
t_{IRD1}	FO=1 Routing Delay		1.3		1.5	ns
t_{IRD2}	FO=2 Routing Delay		1.9		2.1	ns
t_{IRD3}	FO=3 Routing Delay		2.1		2.5	ns
t_{IRD4}	FO=4 Routing Delay		2.6		2.9	ns
t_{IRD8}	FO=8 Routing Delay		4.2		4.9	ns

Notes:

1. *For dual-module macros, use $t_{PD} + t_{RD1} + t_{PDn}$, $t_{CO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.*
2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*
3. *Optimization techniques may further reduce delays by 0 to 4 ns.*

A32100DX Timing Characteristics (continued)

(Worst-Case Military Conditions, V_{CC} = 4.5V, T_J = 125°C)

		'–1' Speed		'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
Synchronous SRAM Operations						
t_{RC}	Read Cycle Time	8.8		11.8		ns
t_{WC}	Write Cycle Time	8.8		11.8		ns
t_{RCKHL}	Clock High/Low Time	4.4		5.9		ns
t_{RCO}	Data Valid After Clock High/Low		4.4		5.9	ns
t_{ADSU}	Address/Data Setup Time	2.1		2.8		ns
t_{ADH}	Address/Data Hold Time	0.0		0.0		ns
t_{RENSU}	Read Enable Setup	0.8		1.1		ns
t_{RENH}	Read Enable Hold	4.4		5.9		ns
t_{WENSU}	Write Enable Setup	3.5		4.7		ns
t_{WENH}	Write Enable Hold	0.0		0.0		ns
t_{BENS}	Block Enable Setup	3.6		4.8		ns
t_{BENH}	Block Enable Hold	0.0		0.0		ns
Asynchronous SRAM Operations						
t_{RPD}	Asynchronous Access Time		10.6		14.1	ns
t_{RDADV}	Read Address Valid	11.5		15.3		ns
t_{ADSU}	Address/Data Setup Time	2.1		2.8		ns
t_{ADH}	Address/Data Hold Time	0.0		0.0		ns
t_{RENSUA}	Read Enable Setup to Address Valid	0.8		1.1		ns
t_{RENHA}	Read Enable Hold	4.4		5.9		ns
t_{WENSU}	Write Enable Setup	3.5		4.7		ns
t_{WENH}	Write Enable Hold	0.0		0.0		ns
t_{DOH}	Data Out Hold Time		1.6		2.1	ns

A32200DX Timing Characteristics (continued)

(Worst-Case Military Conditions, V_{CC} = 4.5V, T_J = 125°C)

			‘–1’ Speed		‘Std’ Speed		
Parameter	**Description**		**Min.**	**Max.**	**Min.**	**Max.**	**Units**
Input Module Propagation Delays							
t_{INPY}	Input Data Pad to Y			1.9		2.6	ns
t_{INGO}	Input Latch Gate-to-Output			4.6		6.0	ns
t_{INH}	Input Latch Hold		0.0		0.0		ns
t_{INSU}	Input Latch Setup		0.7		0.9		ns
t_{ILA}	Latch Active Pulse Width		6.1		8.1		ns
Input Module Predicted Routing Delays[1]							
t_{IRD1}	FO=1 Routing Delay			2.6		3.5	ns
t_{IRD2}	FO=2 Routing Delay			3.4		4.6	ns
t_{IRD3}	FO=3 Routing Delay			4.6		6.1	ns
t_{IRD4}	FO=4 Routing Delay			5.4		7.2	ns
t_{IRD5}	FO=8 Routing Delay			7.0		9.3	ns
Global Clock Network							
t_{CKH}	Input Low to High	FO=32		7.3		9.8	ns
		FO=635		8.5		11.3	ns
t_{CKL}	Input High to Low	FO=32		7.2		9.6	ns
		FO=635		9.3		12.5	ns
t_{PWH}	Minimum Pulse Width High	FO=32	3.2		4.3		ns
		FO=635	3.9		5.2		ns
t_{PWL}	Minimum Pulse Width Low	FO=32	3.2		4.3		ns
		FO=635	3.9		5.2		ns
t_{CKSW}	Maximum Skew	FO=32		1.8		2.4	ns
		FO=635		1.8		2.4	ns
t_{SUEXT}	Input Latch External Setup	FO=32	0.0		0.0		ns
		FO=635	0.0		0.0		ns
t_{HEXT}	Input Latch External Hold	FO=32	3.0		4.0		ns
		FO=635	3.8		5.1		ns
t_P	Minimum Period (1/fmax)	FO=32	5.8		7.7		ns
		FO=635	6.8		9.1		ns
f_{HMAX}	Maximum Datapath Frequency	FO=32		172		130	MHz
		FO=635		147		110	MHz

Note:

1. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment. Optimization techniques may further reduce delays by 0 to 4 ns.

257-Pin CPGA

Pin Number	A14100A Function
A1	I/O
A2	I/O
A3	I/O
A4	I/O
A5	MODE
A6	I/O
A7	I/O
A8	I/O
A9	I/O
A10	I/O
A11	I/O
A12	I/O
A13	I/O
A14	I/O
A15	I/O
A16	I/O
A17	I/O
A18	I/O
A19	I/O
B1	I/O
B2	I/O
B3	I/O
B4	SDI, I/O
B5	I/O
B6	I/O
B7	I/O
B8	I/O
B9	I/O
B10	I/O
B11	I/O
B12	I/O
B13	I/O
B14	I/O
B15	I/O
B16	GND
B17	I/O
B18	I/O
B19	I/O
C1	I/O
C2	I/O
C3	V_{CC}
C4	GND
C5	I/O
C6	I/O

Pin Number	A14100A Function
C7	I/O
C8	I/O
C9	I/O
C10	V_{CC}
C11	I/O
C12	I/O
C13	V_{CC}
C14	I/O
C15	I/O
C16	I/O
C17	V_{CC}
C18	I/O
C19	I/O
D1	I/O
D2	I/O
D3	I/O
D4	GND
D5	I/O
D6	I/O
D7	I/O
D8	I/O
D9	I/O
D10	GND
D11	I/O
D12	I/O
D13	I/O
D14	I/O
D15	I/O
D16	GND
D17	I/O
D18	I/O
D19	I/O
E1	I/O
E2	I/O
E3	I/O
E4	DCLK, I/O
E5	NC
E7	I/O
E9	I/O
E11	GND
E13	I/O
E16	I/O
E17	I/O
E18	I/O

Pin Number	A14100A Function
E19	I/O
F1	I/O
F2	I/O
F3	I/O
F4	I/O
F16	I/O
F17	I/O
F18	I/O
F19	I/O
G1	I/O
G2	I/O
G3	I/O
G4	I/O
G5	I/O
G15	I/O
G16	I/O
G17	I/O
G18	I/O
G19	I/O
H1	I/O
H2	I/O
H3	I/O
H4	I/O
H16	I/O
H17	I/O
H18	I/O
H19	I/O
J1	PRA, I/O
J2	I/O
J3	I/O
J4	I/O
J5	GND
J15	I/O
J16	HCLK, I/O
J17	PRB, I/O
J18	I/O
J19	I/O
K1	I/O
K2	I/O
K3	V_{CC}
K4	GND
K16	GND
K17	V_{CC}
K18	I/O

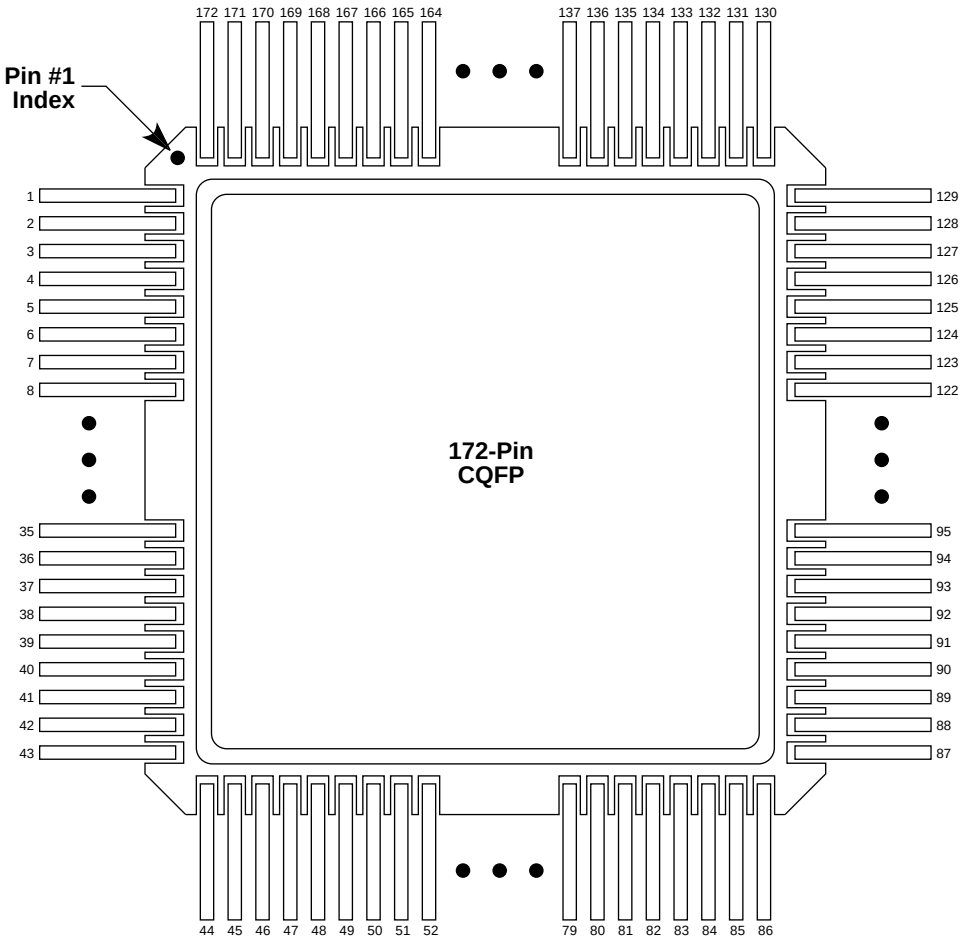
84-Pin CQFP

Pin Number	A1020B Function	A32100DX Function
1	NC	GND
2	I/O	MODE
3	I/O	I/O
4	I/O	I/O
5	I/O	I/O
6	I/O	I/O
7	GND	V_{CC}
8	GND	I/O
9	I/O	I/O
10	I/O	GND
11	I/O	V_{CC}
12	I/O	V_{CC}
13	I/O	I/O
14	V_{CC}	I/O
15	V_{CC}	I/O
16	I/O	I/O
17	I/O	GND
18	I/O	I/O
19	I/O	I/O
20	I/O	I/O
21	I/O	I/O
22	V_{CC}	GND
23	I/O	I/O
24	I/O	I/O
25	I/O	I/O (WD)
26	I/O	I/O (WD)
27	I/O	I/O
28	I/O	QCLKA, I/O
29	GND	GND
30	I/O	I/O (WD)
31	I/O	I/O
32	I/O	GND
33	I/O	V_{CC}
34	I/O	I/O (WD)
35	V_{CC}	I/O (WD)
36	I/O	QCLKB, I/O
37	I/O	I/O (WD)
38	I/O	GND
39	I/O	I/O (WD)
40	I/O	I/O (WD)
41	I/O	I/O (WD)
42	I/O	SDO, I/O

Pin Number	A1020B Function	A32100DX Function
43	I/O	GND
44	I/O	I/O
45	I/O	I/O
46	I/O	I/O
47	I/O	I/O
48	I/O	I/O
49	GND	I/O
50	GND	GND
51	I/O	TCK, I/O
52	I/O	GND
53	CLKA, I/O	V_{CC}
54	I/O	V_{CC}
55	MODE	V_{CC}
56	V_{CC}	V_{CC}
57	V_{CC}	I/O
58	I/O	I/O
59	I/O	GND
60	I/O	I/O
61	SDI, I/O	I/O
62	DCLK, I/O	I/O
63	PRA, I/O	GND
64	PRB, I/O	SDI, I/O
65	I/O	I/O (WD)
66	I/O	I/O (WD)
67	I/O	I/O (WD)
68	I/O	I/O (WD)
69	I/O	QCLKD, I/O
70	I/O	I/O (WD)
71	GND	I/O (WD)
72	I/O	PRA, I/O
73	I/O	CLKA, I/O
74	I/O	V_{CC}
75	I/O	GND
76	I/O	CLKB, I/O
77	V_{CC}	PRB, I/O
78	I/O	I/O (WD)
79	I/O	I/O (WD)
80	I/O	QCLKC, I/O
81	I/O	GND
82	I/O	I/O (WD)
83	I/O	I/O (WD)
84	I/O	DCLK, I/O

Package Pin Assignments (continued)

172-Pin CQFP (Top View)



256-Pin CQFP (Continued)

Pin Number	A14100A Function	A32200DX Function
133	I/O	I/O
134	I/O	I/O
135	I/O	I/O
136	I/O	I/O
137	I/O	I/O
138	I/O	I/O
139	I/O	GND
140	I/O	I/O
141	V_{CC}	I/O
142	I/O	I/O
143	I/O	I/O
144	I/O	I/O
145	I/O	I/O
146	I/O	I/O
147	I/O	I/O
148	I/O	I/O
149	I/O	I/O
150	I/O	I/O
151	I/O	I/O
152	I/O	I/O
153	I/O	I/O
154	I/O	I/O
155	I/O	V_{CC}
156	I/O	I/O
157	I/O	I/O
158	GND	V_{CC}
159	V_{CC}	V_{CC}
160	GND	GND
161	V_{CC}	I/O
162	I/O	I/O
163	I/O	I/O
164	I/O	I/O
165	I/O	GND
166	I/O	I/O
167	I/O	I/O
168	I/O	I/O
169	I/O	I/O
170	I/O	V_{CC}
171	I/O	I/O
172	I/O	I/O
173	I/O	I/O
174	V_{CC}	I/O
175	GND	I/O
176	GND	I/O
177	I/O	I/O
178	I/O	I/O
179	I/O	I/O
180	I/O	GND
181	I/O	I/O
182	I/O	I/O
183	I/O	I/O
184	I/O	I/O
185	I/O	I/O
186	I/O	I/O
187	I/O	I/O
188	IOCLK, I/O	MODE
189	GND	V_{CC}
190	I/O	GND
191	I/O	NC
192	I/O	NC
193	I/O	NC
194	I/O	I/O
195	I/O	DCLK, I/O
196	I/O	I/O
197	I/O	I/O
198	I/O	I/O
199	I/O	I/O (WD)
200	I/O	I/O (WD)
201	I/O	V_{CC}
202	I/O	I/O
203	I/O	I/O
204	I/O	I/O
205	I/O	I/O
206	I/O	GND
207	I/O	I/O
208	I/O	I/O
209	I/O	QCLKC, I/O
210	I/O	I/O
211	I/O	I/O (WD)
212	I/O	I/O (WD)
213	I/O	I/O
214	I/O	I/O
215	I/O	I/O (WD)
216	I/O	I/O (WD)
217	I/O	I/O
218	I/O	PRB, I/O
219	CLKA, I/O	I/O
220	CLKB, I/O	CLKB, I/O
221	V_{CC}	I/O
222	GND	GND
223	V_{CC}	GND
224	GND	V_{CC}
225	PRA, I/O	V_{CC}
226	I/O	I/O
227	I/O	CLKA, I/O
228	I/O	I/O
229	I/O	PRA, I/O
230	I/O	I/O
231	I/O	I/O
232	I/O	I/O (WD)
233	I/O	I/O (WD)
234	I/O	I/O
235	I/O	I/O
236	I/O	I/O
237	I/O	I/O
238	I/O	I/O
239	I/O	I/O
240	GND	QCLKD, I/O
241	I/O	I/O
242	I/O	I/O (WD)
243	I/O	GND
244	I/O	I/O (WD)
245	I/O	I/O
246	I/O	I/O
247	I/O	I/O
248	I/O	V_{CC}
249	I/O	I/O
250	I/O	I/O (WD)
251	I/O	I/O (WD)
252	I/O	I/O
253	I/O	SDI, I/O
254	I/O	I/O
255	I/O	GND
256	DCLK, I/O	NC