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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	547
Number of Logic Elements/Cells	-
Total RAM Bits	-
Number of I/O	69
Number of Gates	2000
Voltage - Supply	4.5V ~ 5.5V
Mounting Type	Through Hole
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	84-BCPGA
Supplier Device Package	84-CPGA (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/microsemi/a1020b-pg84c

unique architecture offers gate array flexibility, high performance, and quick turnaround through user programming. Device utilization is typically 95 percent of available logic modules. All Actel devices include on-chip clock drivers and a hard-wired distribution network.

User-definable I/Os are capable of driving at both TTL and CMOS drive levels. Available packages for the military are the Ceramic Quad Flat Pack (CQFP) and the Ceramic Pin Grid Array (CPGA). See the "Product Plan" section on page 6 for details.

QML Certification

Actel has achieved full QML certification, demonstrating that quality management, procedures, processes, and controls are in place and comply with MIL-PRF-38535, the performance specification used by the Department of Defense for monolithic integrated circuits. QML certification is a good example of Actel's commitment to supplying the highest quality products for all types of high-reliability, military and space applications.

Many suppliers of microelectronics components have implemented QML as their primary worldwide business system. Appropriate use of this system not only helps in the implementation of advanced technologies, but also allows for a quality, reliable and cost-effective logistics support throughout QML products' life cycles.

Development Tool Support

The HiRel devices are fully supported by Actel's line of FPGA development tools, including the Actel DeskTOP series and Designer Advantage tools. The Actel DeskTOP Series is an integrated design environment for PCs that includes design entry, simulation, synthesis, and place and route tools. Designer Advantage is Actel's suite of FPGA development point tools for PCs and Workstations that includes the ACTgen Macro Builder, Designer with DirectTime timing driven place and route and analysis tools, and device programming software.

In addition, the HiRel devices contain ActionProbe circuitry that provides built-in access to every node in a design, enabling 100 percent real-time observation and analysis of a device's internal logic nodes without design iteration. The probe circuitry is accessed by Silicon Explorer, an easy to use integrated verification and logic analysis tool that can sample data at 100 MHz (asynchronous) or 66 MHz (synchronous). Silicon Explorer attaches to a PC's standard COM port, turning the PC into a fully functional 18 channel logic analyzer. Silicon Explorer allows designers to complete the design verification process at their desks and reduces verification time from several hours per cycle to a few seconds.

ACT 3 Description

The ACT 3 family is the third-generation Actel FPGA family. This family offers the highest-performance and highest-capacity devices, ranging from 2,500 to 10,000 gates, with system performance up to 60 MHz over the military temperature range. The devices have four clock distribution networks, including dedicated array and I/O clocks. In addition, the ACT 3 family offers the highest I/O-to-gate ratio available. ACT 3 devices are manufactured using 0.8µ CMOS technology.

1200XL/3200DX Description

3200DX and 1200XL FPGAs were designed to integrate system logic which is typically implemented in multiple CPLDs, PALs, and FPGAs. These devices provide the features and performance required for today's complex, high-speed digital logic systems. The 3200DX family offers the industry's fastest dual-port SRAM for implementing fast FIFOs, LIFOs, and temporary data storage.

ACT 2 Description

The ACT 2 family is the second-generation Actel FPGA family. This family offers the best-value, high-capacity devices, ranging from 4,000 to 8,000 gates, with system performance up to 40 MHz over the military temperature range. The devices have two routed array clock distribution networks. ACT 2 devices are manufactured using 1.0µ CMOS technology.

ACT 1 Description

The ACT 1 family is the first Actel FPGA family and the first antifuse-based FPGA. This family offers the lowest-cost logic integration, with devices ranging from 1,200 to 2,000 gates, with system performance up to 20 MHz over the military temperature range. The devices have one routed array clock distribution network. ACT 1 devices are manufactured using 1.0µ CMOS technology.

Actel MIL-STD-883 Product Flow

Step	Screen	883 Method	883—Class B Requirement
1.	Internal Visual	2010, Test Condition B	100%
2.	Temperature Cycling	1010, Test Condition C	100%
3.	Constant Acceleration	2001, Test Condition D or E, Y_1, Orientation Only	100%
4.	Seal	1014	
	a. Fine		100%
	b. Gross		100%
5.	Visual Inspection	2009	100%
6.	Pre-Burn-In Electrical Parameters	In accordance with applicable Actel device specification	100%
7.	Burn-in Test	1015, Condition D, 160 hours @ 125°C or 80 hours @ 150°C	100%
8.	Interim (Post-Burn-In) Electrical Parameters	In accordance with applicable Actel device specification	100%
9.	Percent Defective Allowable	5%	All Lots
10.	Final Electrical Test	In accordance with applicable Actel device specification, which includes a, b, and c:	
	a. Static Tests		100%
	(1) 25°C (Subgroup 1, Table I)	5005	
	(2) –55°C and +125°C (Subgroups 2, 3, Table I)	5005	
	b. Functional Tests		100%
	(1) 25°C (Subgroup 7, Table I)	5005	
	(2) –55°C and +125°C (Subgroups 8A and 8B, Table I)	5005	
	c. Switching Tests at 25°C (Subgroup 9, Table I)	5005	100%
11.	External Visual	2009	100%

Note: *When Destructive Physical Analysis (DPA) is performed on Class B devices, the step coverage requirement as specified in Method 2018 must be waived.*

Actel Extended Flow[1]

Step	Screen	Method	Require-ment
1.	Wafer Lot Acceptance[2]	5007 with Step Coverage Waiver	All Lots
2.	Destructive In-Line Bond Pull[3]	2011, Condition D	Sample
3.	Internal Visual	2010, Condition A	100%
4.	Serialization		100%
5.	Temperature Cycling	1010, Condition C	100%
6.	Constant Acceleration	2001, Condition D or E, Y_1 Orientation Only	100%
7.	Particle Impact Noise Detection	2020, Condition A	100%
8.	Radiographic	2012 (one view only)	100%
9.	Pre-Burn-In Test	In accordance with applicable Actel device specification	100%
10.	Burn-in Test	1015, Condition D, 240 hours @ 125°C minimum	100%
11.	Interim (Post-Burn-In) Electrical Parameters	In accordance with applicable Actel device specification	100%
12.	Reverse Bias Burn-In	1015, Condition C, 72 hours @ 150°C minimum	100%
13.	Interim (Post-Burn-In) Electrical Parameters	In accordance with applicable Actel device specification	100%
14.	Percent Defective Allowable (PDA) Calculation	5%, 3% Functional Parameters @ 25°C	All Lots
15.	Final Electrical Test	In accordance with Actel applicable device specification which includes a, b, and c:	100%
	a. Static Tests		100%
	(1) 25°C (Subgroup 1, Table1)	5005	
	(2) –55°C and +125°C (Subgroups 2, 3, Table 1)	5005	
	b. Functional Tests		100%
	(1) 25°C (Subgroup 7, Table 15)	5005	
	(2) –55°C and +125°C (Subgroups 8A and B, Table 1)	5005	
	c. Switching Tests at 25°C (Subgroup 9, Table 1)	5005	100%
16.	Seal	1014	100%
	a. Fine		
	b. Gross		
17.	External Visual	2009	100%

Notes:

1. *Actel offers the extended flow for customers who require additional screening beyond the requirements of the MIL-STD-833, Class B. Actel is compliant to the requirements of MIL-STD-883, Paragraph 1.2.1, and MIL-I-38535, Appendix A. Actel is offering this extended flow incorporating the majority of the screening procedures as outlined in Method 5004 of MIL-STD-883, Class S. The exceptions to Method 5004 are shown in notes 2 and 3 below.*
2. *Wafer lot acceptance is performed to Method 5007; however, the step coverage requirement as specified in Method 2018 must be waived.*
3. *MIL-STD-883, Method 5004 requires 100 percent Radiation latch-up testing (Method 1020). Actel will not be performing any radiation testing, and this requirement must be waived in its entirety.*

Fixed Capacitance Values for Actel FPGAs (pF)

Device Type	r_1 routed_Clk1	r_2 routed_Clk2
A1010B	41	n/a
A1020B	69	n/a
A1240A	134	134
A1280A	168	168
A1280XL	168	168
A1425A	75	75
A1460A	165	165
A14100A	195	195
A32100DX	178	178
A32200DX	230	230

Fixed Clock Loads (s_1/s_2—ACT 3 Only)

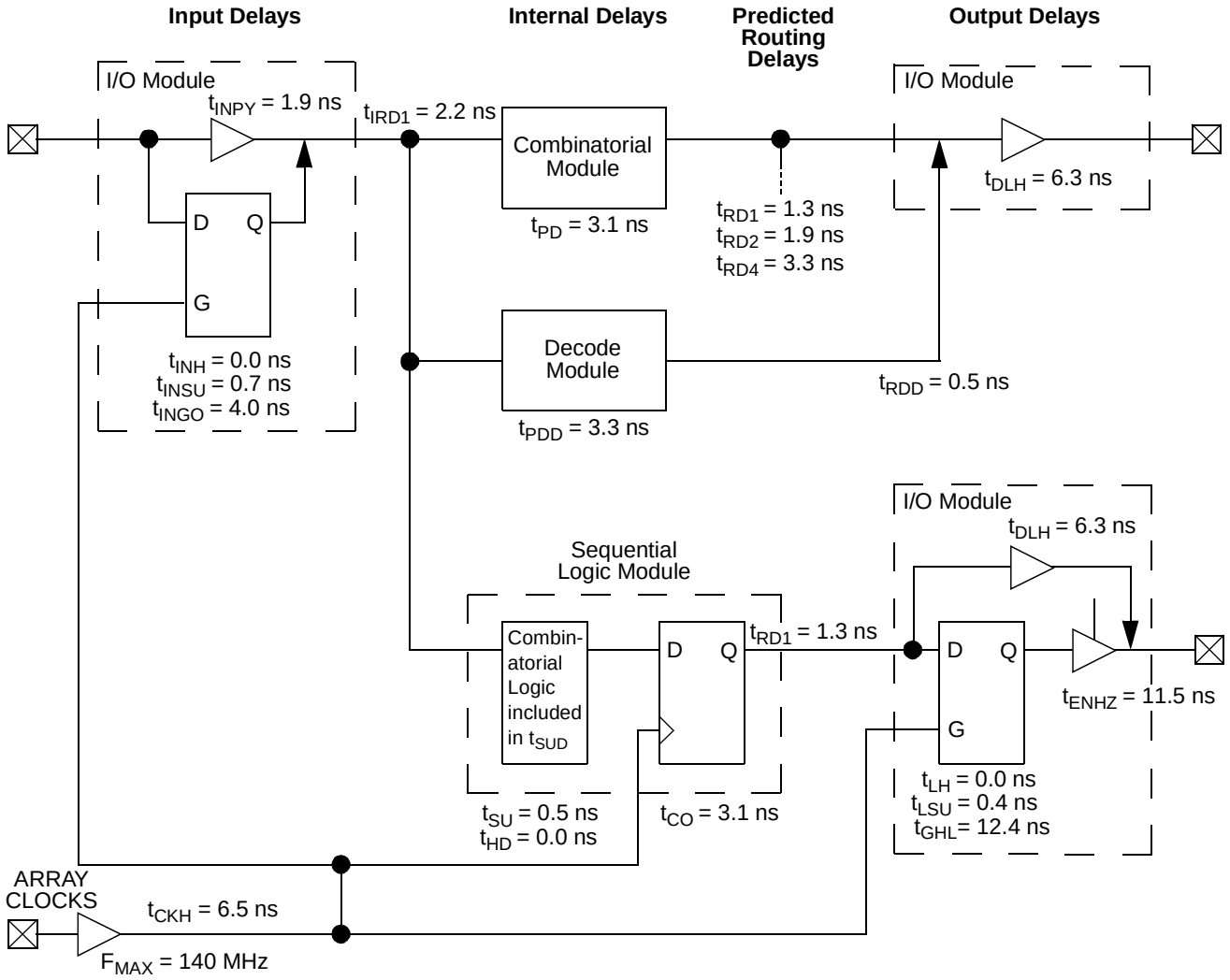
Device Type	s_1 Clock Loads on Dedicated Array Clock	s_2 Clock Loads on Dedicated I/O Clock
A1425A	160	100
A1460A	432	168
A14100A	697	228

Determining Average Switching Frequency

To determine the switching frequency for a design, you must have a detailed understanding of the data values input to the circuit. The guidelines in the table below are meant to represent worst-case scenarios so that they can be generally used to predict the upper limits of power dissipation.

Type	ACT 3	3200DX/ACT 2/1200XL	ACT 1
Logic modules (m)	80% of modules	80% of modules	90% of modules
Input switching (n)	# inputs/4	# inputs/4	# inputs/4
Outputs switching (p)	#outputs/4	#outputs/4	#outputs/4
First routed array clock loads (q_1)	40% of sequential modules	40% of sequential modules	40% of modules
Second routed array clock loads (q_2)	40% of sequential modules	40% of sequential modules	n/a
Load capacitance (C_L)	35 pF	35 pF	35 pF
Average logic module switching rate (f_m)	F/10	F/10	F/10
Average input switching rate (f_n)	F/5	F/5	F/5
Average output switching rate (f_p)	F/10	F/10	F/10
Average first routed array clock rate (f_{q1})	F/2	F	F
Average second routed array clock rate (f_{q2})	F/2	F/2	n/a
Average dedicated array clock rate (f_{s1})	F	n/a	n/a
Average dedicated I/O clock rate (f_{s2})	F	n/a	n/a

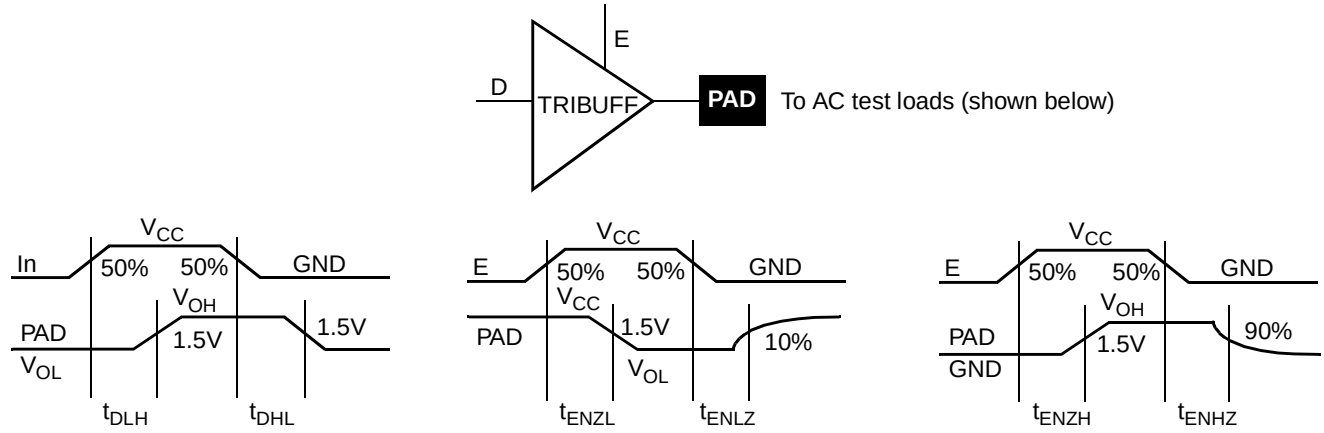
3200DX Timing Model (Logic Functions using Array Clocks)*



**Values shown for A32100DX–1 at worst-case military conditions.*

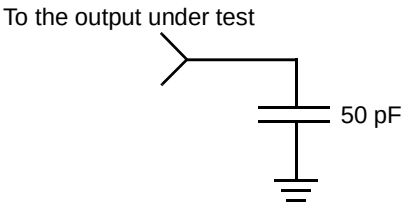
Parameter Measurement

Output Buffer Delays

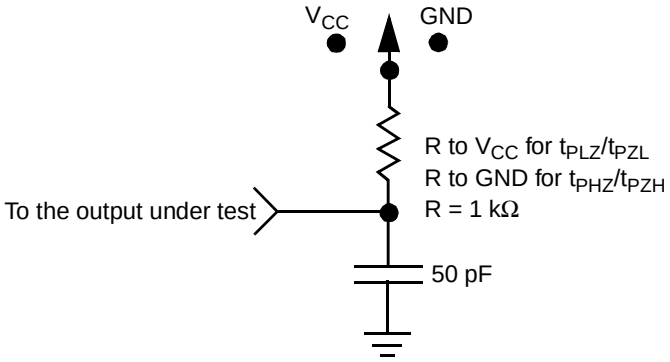


AC Test Load

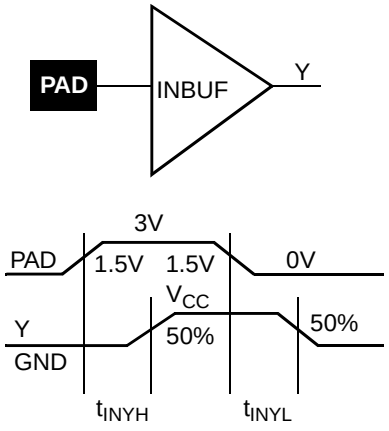
Load 1
(Used to measure propagation delay)



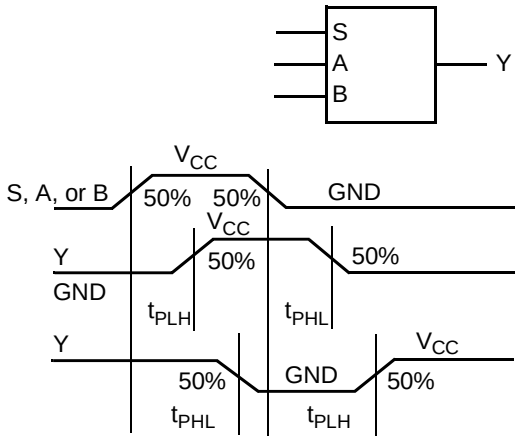
Load 2
(Used to measure rising/falling edges)



Input Buffer Delays

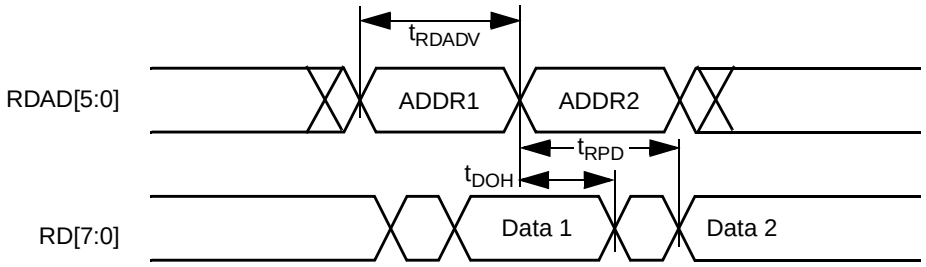


Combinatorial Macro Delays



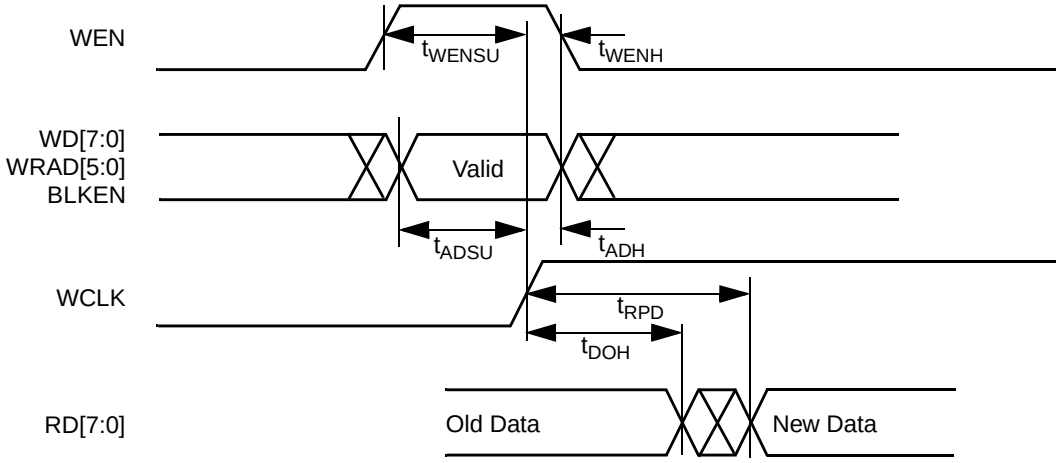
3200DX SRAM Asynchronous Read Operation—Type 1

(Read Address Controlled)



3200DX SRAM Asynchronous Read Operation—Type 2

(Write Address Controlled)



A1280A Timing Characteristics (continued)

(Worst-Case Military Conditions, V_{CC} = 4.5V, T_J = 125°C)

			'–1' Speed		'Std' Speed		
Parameter	**Description**		**Min.**	**Max.**	**Min.**	**Max.**	**Units**
Input Module Propagation Delays							
t_{INYH}	Pad to Y High			4.0		4.7	ns
t_{INYL}	Pad to Y Low			3.6		4.3	ns
t_{INGH}	G to Y High			6.9		8.1	ns
t_{INGL}	G to Y Low			6.6		7.7	ns
Input Module Predicted Routing Delays[1]							
t_{RD1}	FO=1 Routing Delay			6.2		7.3	ns
t_{RD2}	FO=2 Routing Delay			7.2		8.4	ns
t_{RD3}	FO=3 Routing Delay			7.7		9.1	ns
t_{RD4}	FO=4 Routing Delay			8.9		10.5	ns
t_{RD8}	FO=8 Routing Delay			12.9		15.2	ns
Global Clock Network							
t_{CKH}	Input Low to High	FO = 32 FO = 384		13.3 17.9		15.7 21.1	ns
t_{CKL}	Input High to Low	FO = 32 FO = 384		13.3 18.2		15.7 21.4	ns
t_{PWH}	Minimum Pulse Width High	FO = 32 FO = 384	6.9 7.9		8.1 9.3		ns
t_{PWL}	Minimum Pulse Width Low	FO = 32 FO = 384	6.9 7.9		8.1 9.3		ns
t_{CKSW}	Maximum Skew	FO = 32 FO = 384		0.6 3.1		0.6 3.1	ns
t_{SUEXT}	Input Latch External Setup	FO = 32 FO = 384	0.0 0.0		0.0 0.0		ns
t_{HEXT}	Input Latch External Hold	FO = 32 FO = 384	8.6 13.8		8.6 13.8		ns
t_P	Minimum Period	FO = 32 FO = 384	13.7 16.0		16.2 18.9		ns
f_{MAX}	Maximum Frequency	FO = 32 FO = 384		73 63		62 53	MHz

Note:

1. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment. Optimization techniques may further reduce delays by 0 to 4 ns.

A1280XL Timing Characteristics (continued)

(Worst-Case Military Conditions, V_{CC} = 4.5V, T_J = 125°C)

			'–1' Speed		'Std' Speed		
Parameter	**Description**		**Min.**	**Max.**	**Min.**	**Max.**	**Units**
Input Module Propagation Delays							
t_{INYH}	Pad to Y High			1.5		1.7	ns
t_{INYL}	Pad to Y Low			1.7		2.1	ns
t_{INGH}	G to Y High			2.8		3.3	ns
t_{INGL}	G to Y Low			3.7		4.3	ns
Input Module Predicted Routing Delays[1]							
t_{RD1}	FO=1 Routing Delay			4.6		5.3	ns
t_{RD2}	FO=2 Routing Delay			5.2		6.1	ns
t_{RD3}	FO=3 Routing Delay			5.5		6.5	ns
t_{RD4}	FO=4 Routing Delay			6.4		7.5	ns
t_{RD8}	FO=8 Routing Delay			9.2		10.8	ns
Global Clock Network							
t_{CKH}	Input Low to High	FO = 32 FO = 384		7.1 8.0		8.4 9.5	ns
t_{CKL}	Input High to Low	FO = 32 FO = 384		7.0 8.0		8.3 9.5	ns
t_{PWH}	Minimum Pulse Width High	FO = 32 FO = 384	4.3 4.8		5.3 5.7		ns
t_{PWL}	Minimum Pulse Width Low	FO = 32 FO = 384	4.3 4.8		5.3 5.7		ns
t_{CKSW}	Maximum Skew	FO = 32 FO = 384		1.1 1.1		1.2 1.2	ns
t_{SUEXT}	Input Latch External Setup	FO = 32 FO = 384	0.0 0.0		0.0 0.0		ns
t_{HEXT}	Input Latch External Hold	FO = 32 FO = 384	3.6 4.6		4.2 5.3		ns
t_P	Minimum Period	FO = 32 FO = 384	9.1 9.8		10.7 11.8		ns
f_{MAX}	Maximum Frequency	FO = 32 FO = 384		110 100		90 85	MHz

Note:

1. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment. Optimization techniques may further reduce delays by 0 to 4 ns.

A14100A Timing Characteristics (continued)

(Worst-Case Military Conditions, V_{CC} = 4.5V, T_J = 125°C)

		'–1' Speed		'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
CMOS Output Module Timing[1]						
t_{DHS}	Data to Pad, High Slew		9.2		10.8	ns
t_{DLS}	Data to Pad, Low Slew		17.3		20.3	ns
t_{ENZHS}	Enable to Pad, Z to H/L, High Slew		7.7		9.1	ns
t_{ENZLS}	Enable to Pad, Z to H/L, Low Slew		13.1		15.5	ns
t_{ENHSZ}	Enable to Pad, H/L to Z, High Slew		11.6		14.0	ns
t_{ENLSZ}	Enable to Pad, H/L to Z, Low Slew		10.9		12.8	ns
t_{CKHS}	IOCLK Pad to Pad H/L, High Slew		14.4		16.0	ns
t_{CKLS}	IOCLK Pad to Pad H/L, Low Slew		20.2		22.4	ns
d_{TLHHS}	Delta Low to High, High Slew		0.06		0.07	ns/pF
d_{TLHLS}	Delta Low to High, Low Slew		0.11		0.13	ns/pF
d_{THLHS}	Delta High to Low, High Slew		0.04		0.05	ns/pF
d_{THLLS}	Delta High to Low, Low Slew		0.05		0.06	ns/pF
Dedicated (Hard-Wired) I/O Clock Network						
t_{IOCKH}	Input Low to High (Pad to I/O Module Input)		3.5		4.1	ns
t_{IOPWH}	Minimum Pulse Width High	4.8		5.7		ns
t_{IOPWL}	Minimum Pulse Width Low	4.8		5.7		ns
t_{IOSAPW}	Minimum Asynchronous Pulse Width	3.9		4.4		ns
t_{IOCKSW}	Maximum Skew		0.9		1.0	ns
t_{IOP}	Minimum Period	9.9		11.6		ns
f_{IOMAX}	Maximum Frequency		100		85	MHz
Dedicated (Hard-Wired) Array Clock Network						
t_{HCKH}	Input Low to High (Pad to S-Module Input)		5.5		6.4	ns
t_{HCKL}	Input High to Low (Pad to S-Module Input)		5.5		6.4	ns
t_{HPWH}	Minimum Pulse Width High	4.8		5.7		ns
t_{HPWL}	Minimum Pulse Width Low	4.8		5.7		ns
t_{HCKSW}	Maximum Skew		0.9		1.0	ns
t_{HP}	Minimum Period	9.9		11.6		ns
f_{HMAX}	Maximum Frequency		100		85	MHz

Notes:

1. *Delays based on 35 pF loading.*
2. *SSO information can be found in the* Simultaneously Switching Output Limits for Actel FPGAs *application note at http://www.actel.com/appnotes.*

A32100DX Timing Characteristics (continued)

(Worst-Case Military Conditions, V_{CC} = 4.5V, T_J = 125°C)

		'–1' Speed		'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
Synchronous SRAM Operations						
t_{RC}	Read Cycle Time	8.8		11.8		ns
t_{WC}	Write Cycle Time	8.8		11.8		ns
t_{RCKHL}	Clock High/Low Time	4.4		5.9		ns
t_{RCO}	Data Valid After Clock High/Low		4.4		5.9	ns
t_{ADSU}	Address/Data Setup Time	2.1		2.8		ns
t_{ADH}	Address/Data Hold Time	0.0		0.0		ns
t_{RENSU}	Read Enable Setup	0.8		1.1		ns
t_{RENH}	Read Enable Hold	4.4		5.9		ns
t_{WENSU}	Write Enable Setup	3.5		4.7		ns
t_{WENH}	Write Enable Hold	0.0		0.0		ns
t_{BENS}	Block Enable Setup	3.6		4.8		ns
t_{BENH}	Block Enable Hold	0.0		0.0		ns
Asynchronous SRAM Operations						
t_{RPD}	Asynchronous Access Time		10.6		14.1	ns
t_{RDADV}	Read Address Valid	11.5		15.3		ns
t_{ADSU}	Address/Data Setup Time	2.1		2.8		ns
t_{ADH}	Address/Data Hold Time	0.0		0.0		ns
t_{RENSUA}	Read Enable Setup to Address Valid	0.8		1.1		ns
t_{RENHA}	Read Enable Hold	4.4		5.9		ns
t_{WENSU}	Write Enable Setup	3.5		4.7		ns
t_{WENH}	Write Enable Hold	0.0		0.0		ns
t_{DOH}	Data Out Hold Time		1.6		2.1	ns

TDI Test Data In

Serial data input for JTAG instructions and data. Data is shifted in on the rising edge of TCLK. This pin functions as an I/O when the JTAG fuse is not programmed. JTAG pins are only available in the 3200DX device.

TDO Test Data Out

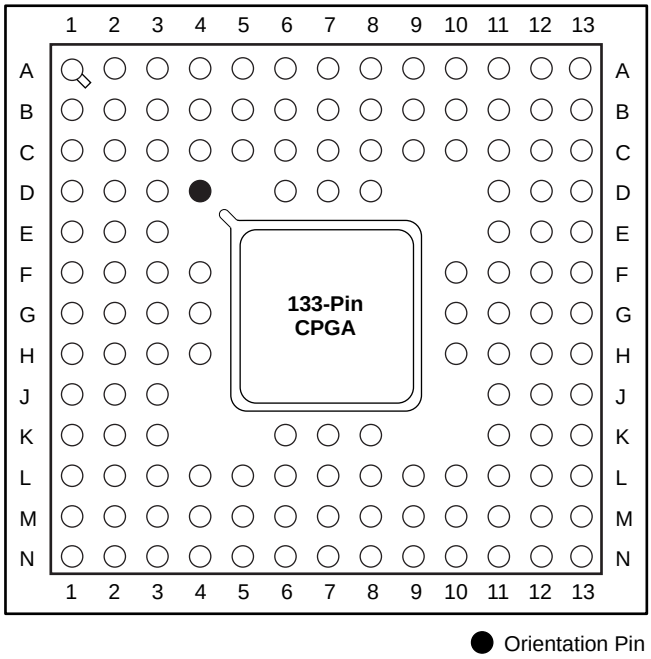
Serial data output for JTAG instructions and test data. This pin functions as an I/O when the JTAG fuse is not programmed. JTAG pins are only available in the 3200DX device.

TMS Test Mode Select

Serial data input for JTAG test mode. Data is shifted in on the rising edge of TCLK. This pin functions as an I/O when the JTAG fuse is not programmed. JTAG pins are only available in the 3200DX device.

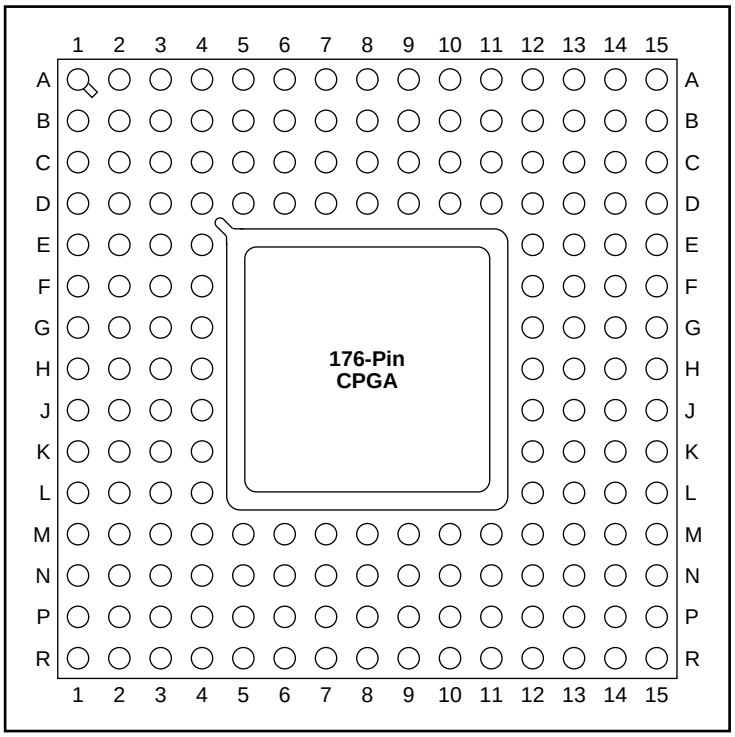
Package Pin Assignments (continued)

133-Pin CPGA (Top View)



Package Pin Assignments (continued)

176-Pin CPGA (Top View)



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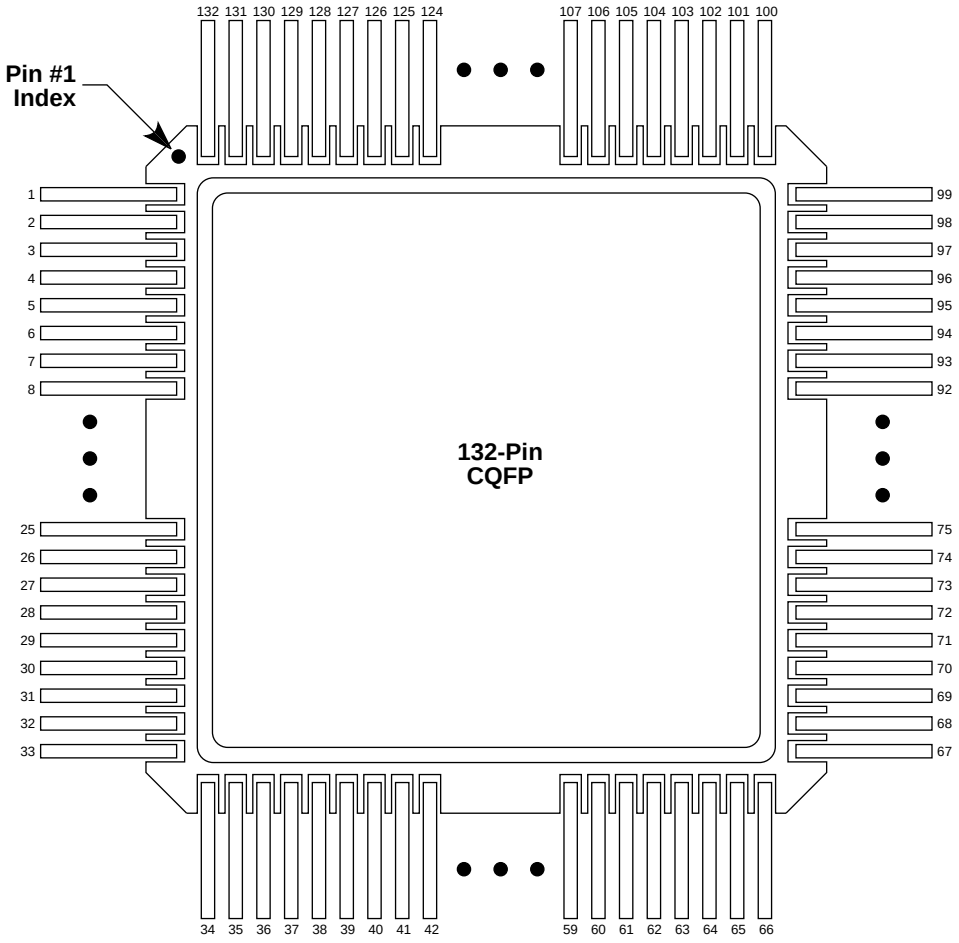
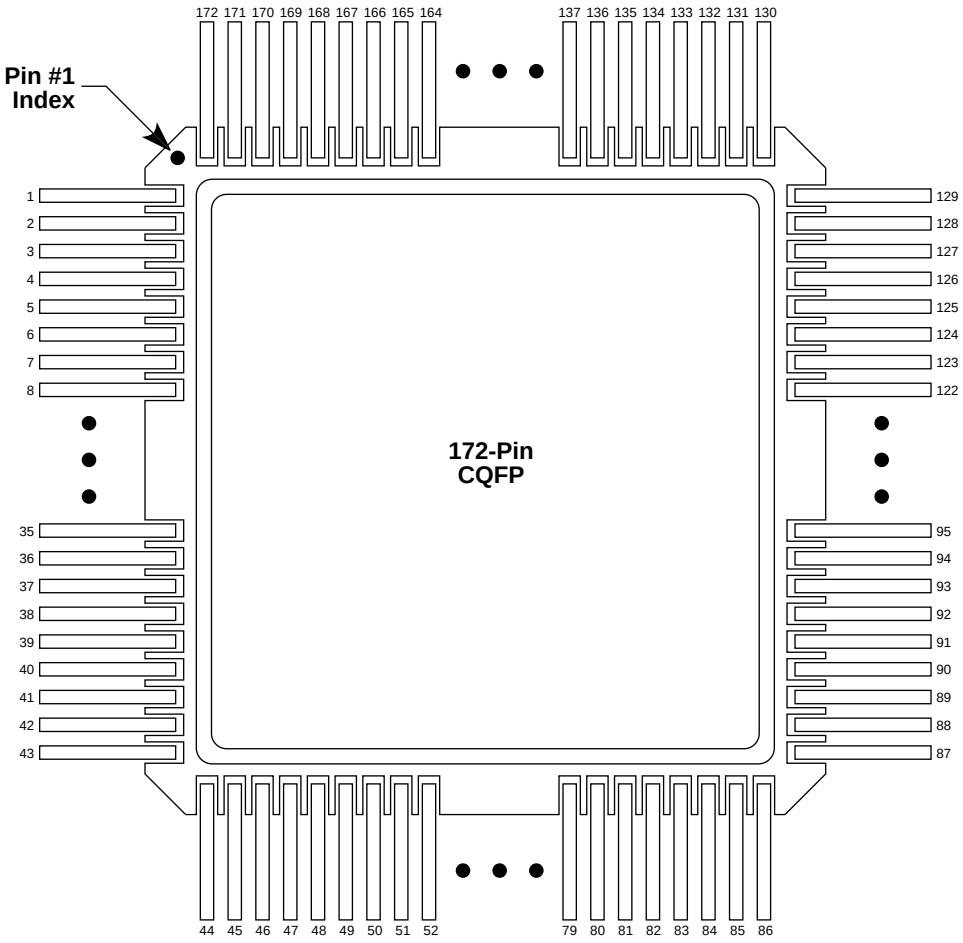
Package Pin Assignments (continued)

132-Pin CQFP (Top View)



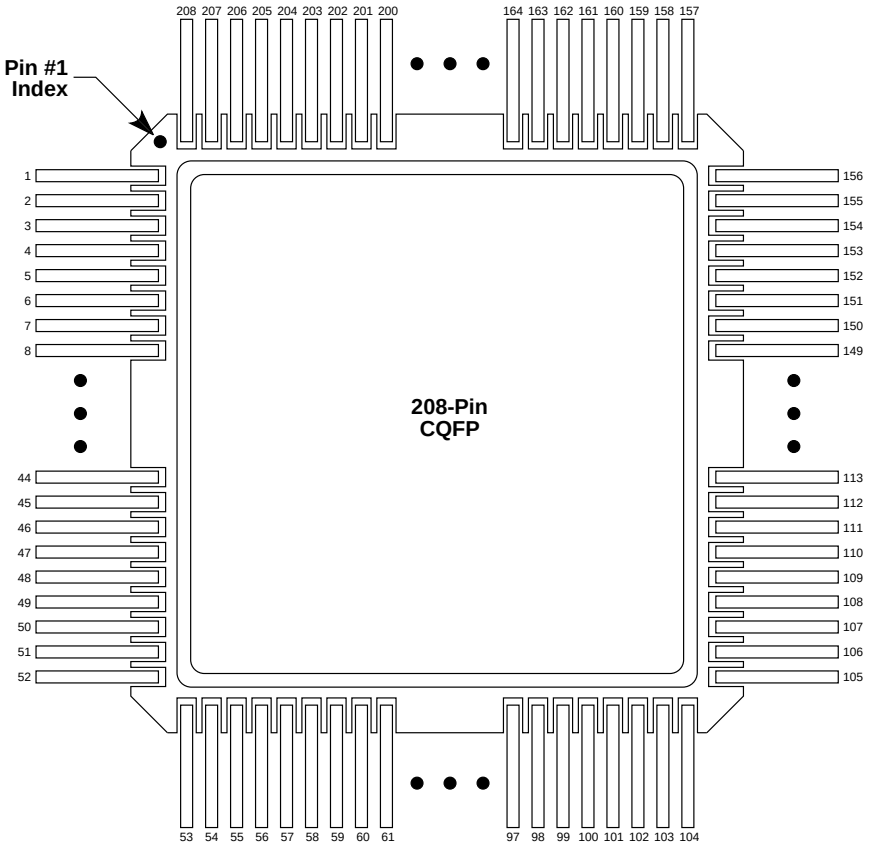
Package Pin Assignments (continued)

172-Pin CQFP (Top View)



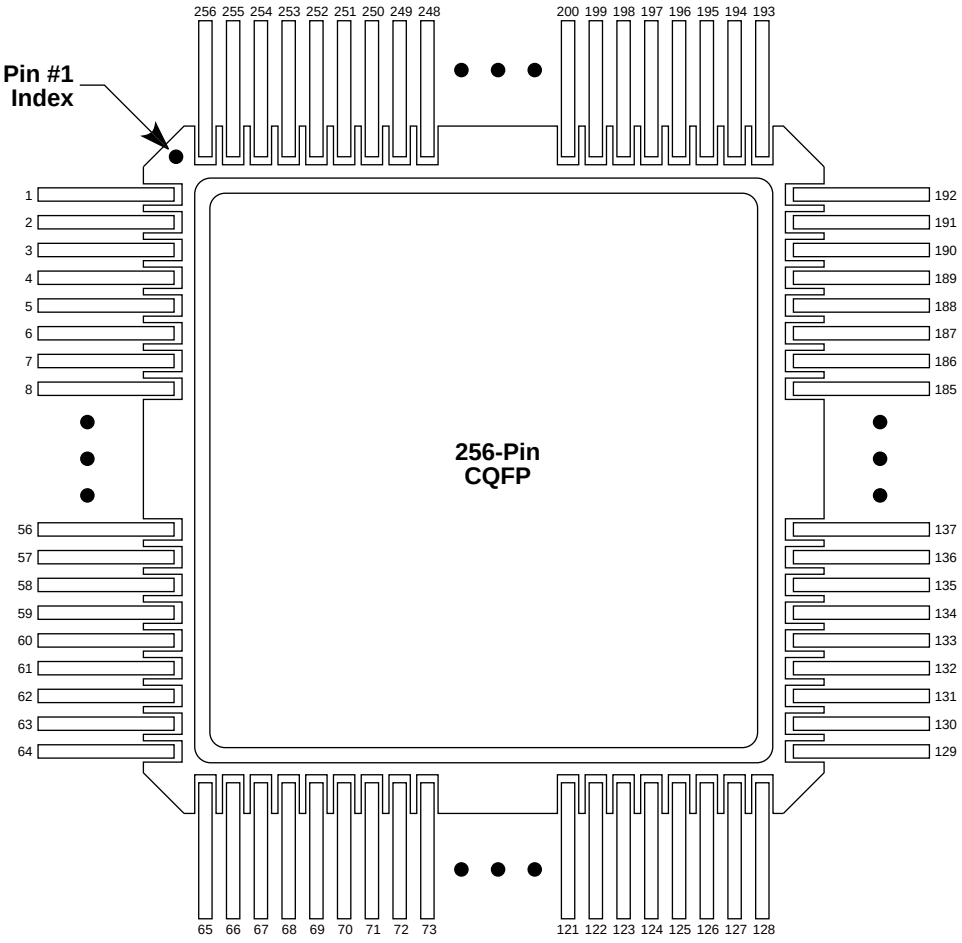
Package Pin Assignments (continued)

208-Pin CQFP (Top View)



Package Pin Assignments (continued)

256-Pin CQFP (Top View)



256-Pin CQFP

Pin Number	A14100A Function	A32200DX Function
1	GND	NC
2	SDI, I/O	GND
3	I/O	I/O
4	I/O	I/O
5	I/O	I/O
6	I/O	I/O
7	I/O	I/O
8	I/O	I/O
9	I/O	I/O
10	I/O	GND
11	MODE	I/O
12	I/O	I/O
13	I/O	I/O
14	I/O	I/O
15	I/O	I/O
16	I/O	I/O
17	I/O	I/O
18	I/O	I/O
19	I/O	I/O
20	I/O	I/O
21	I/O	I/O
22	I/O	I/O
23	I/O	I/O
24	I/O	I/O
25	I/O	I/O
26	I/O	V_{CC}
27	I/O	I/O
28	V_{CC}	I/O
29	GND	V_{CC}
30	V_{CC}	V_{CC}
31	GND	GND
32	I/O	V_{CC}
33	I/O	GND
34	I/O	TCK, I/O
35	I/O	I/O
36	I/O	GND
37	I/O	I/O
38	I/O	I/O
39	I/O	I/O
40	I/O	I/O
41	I/O	I/O
42	I/O	I/O
43	I/O	I/O
44	I/O	I/O
45	I/O	I/O
46	V_{CC}	I/O
47	I/O	I/O
48	I/O	GND
49	I/O	I/O
50	I/O	I/O
51	I/O	I/O
52	I/O	I/O
53	I/O	I/O
54	I/O	I/O
55	I/O	I/O
56	I/O	I/O
57	I/O	I/O
58	I/O	I/O
59	GND	I/O
60	I/O	V_{CC}
61	I/O	GND
62	I/O	GND
63	I/O	NC
64	I/O	NC
65	I/O	NC
66	I/O	I/O
67	I/O	SDO, I/O
68	I/O	I/O
69	I/O	I/O (WD)
70	I/O	I/O (WD)
71	I/O	I/O
72	I/O	V_{CC}
73	I/O	I/O
74	I/O	I/O
75	I/O	I/O
76	I/O	I/O (WD)
77	I/O	GND
78	I/O	I/O (WD)
79	I/O	I/O
80	I/O	QCLKB, I/O
81	I/O	I/O
82	I/O	I/O
83	I/O	I/O
84	I/O	I/O
85	I/O	I/O
86	I/O	I/O
87	I/O	I/O (WD)
88	I/O	I/O (WD)
89	I/O	I/O
90	PRB, I/O	I/O
91	GND	I/O
92	V_{CC}	I/O
93	GND	I/O
94	V_{CC}	I/O
95	I/O	V_{CC}
96	HCLK, I/O	V_{CC}
97	I/O	GND
98	I/O	GND
99	I/O	I/O
100	I/O	I/O
101	I/O	I/O
102	I/O	I/O
103	I/O	I/O
104	I/O	I/O
105	I/O	I/O (WD)
106	I/O	I/O (WD)
107	I/O	I/O
108	I/O	I/O
109	I/O	I/O (WD)
110	GND	I/O (WD)
111	I/O	I/O
112	I/O	QCLKA, I/O
113	I/O	I/O
114	I/O	GND
115	I/O	I/O
116	I/O	I/O
117	I/O	I/O
118	I/O	I/O
119	I/O	V_{CC}
120	I/O	I/O
121	I/O	I/O (WD)
122	I/O	I/O (WD)
123	I/O	I/O
124	I/O	I/O
125	I/O	TDI, I/O
126	I/O	TMS, I/O
127	IOPCL, I/O	GND
128	GND	NC
129	I/O	NC
130	I/O	NC
131	I/O	GND
132	I/O	I/O

256-Pin CQFP (Continued)

Pin Number	A14100A Function	A32200DX Function
133	I/O	I/O
134	I/O	I/O
135	I/O	I/O
136	I/O	I/O
137	I/O	I/O
138	I/O	I/O
139	I/O	GND
140	I/O	I/O
141	V_{CC}	I/O
142	I/O	I/O
143	I/O	I/O
144	I/O	I/O
145	I/O	I/O
146	I/O	I/O
147	I/O	I/O
148	I/O	I/O
149	I/O	I/O
150	I/O	I/O
151	I/O	I/O
152	I/O	I/O
153	I/O	I/O
154	I/O	I/O
155	I/O	V_{CC}
156	I/O	I/O
157	I/O	I/O
158	GND	V_{CC}
159	V_{CC}	V_{CC}
160	GND	GND
161	V_{CC}	I/O
162	I/O	I/O
163	I/O	I/O
164	I/O	I/O
165	I/O	GND
166	I/O	I/O
167	I/O	I/O
168	I/O	I/O
169	I/O	I/O
170	I/O	V_{CC}
171	I/O	I/O
172	I/O	I/O
173	I/O	I/O
174	V_{CC}	I/O
175	GND	I/O
176	GND	I/O
177	I/O	I/O
178	I/O	I/O
179	I/O	I/O
180	I/O	GND
181	I/O	I/O
182	I/O	I/O
183	I/O	I/O
184	I/O	I/O
185	I/O	I/O
186	I/O	I/O
187	I/O	I/O
188	IOCLK, I/O	MODE
189	GND	V_{CC}
190	I/O	GND
191	I/O	NC
192	I/O	NC
193	I/O	NC
194	I/O	I/O
195	I/O	DCLK, I/O
196	I/O	I/O
197	I/O	I/O
198	I/O	I/O
199	I/O	I/O (WD)
200	I/O	I/O (WD)
201	I/O	V_{CC}
202	I/O	I/O
203	I/O	I/O
204	I/O	I/O
205	I/O	I/O
206	I/O	GND
207	I/O	I/O
208	I/O	I/O
209	I/O	QCLKC, I/O
210	I/O	I/O
211	I/O	I/O (WD)
212	I/O	I/O (WD)
213	I/O	I/O
214	I/O	I/O
215	I/O	I/O (WD)
216	I/O	I/O (WD)
217	I/O	I/O
218	I/O	PRB, I/O
219	CLKA, I/O	I/O
220	CLKB, I/O	CLKB, I/O
221	V_{CC}	I/O
222	GND	GND
223	V_{CC}	GND
224	GND	V_{CC}
225	PRA, I/O	V_{CC}
226	I/O	I/O
227	I/O	CLKA, I/O
228	I/O	I/O
229	I/O	PRA, I/O
230	I/O	I/O
231	I/O	I/O
232	I/O	I/O (WD)
233	I/O	I/O (WD)
234	I/O	I/O
235	I/O	I/O
236	I/O	I/O
237	I/O	I/O
238	I/O	I/O
239	I/O	I/O
240	GND	QCLKD, I/O
241	I/O	I/O
242	I/O	I/O (WD)
243	I/O	GND
244	I/O	I/O (WD)
245	I/O	I/O
246	I/O	I/O
247	I/O	I/O
248	I/O	V_{CC}
249	I/O	I/O
250	I/O	I/O (WD)
251	I/O	I/O (WD)
252	I/O	I/O
253	I/O	SDI, I/O
254	I/O	I/O
255	I/O	GND
256	DCLK, I/O	NC