Welcome to E-XFL.COM

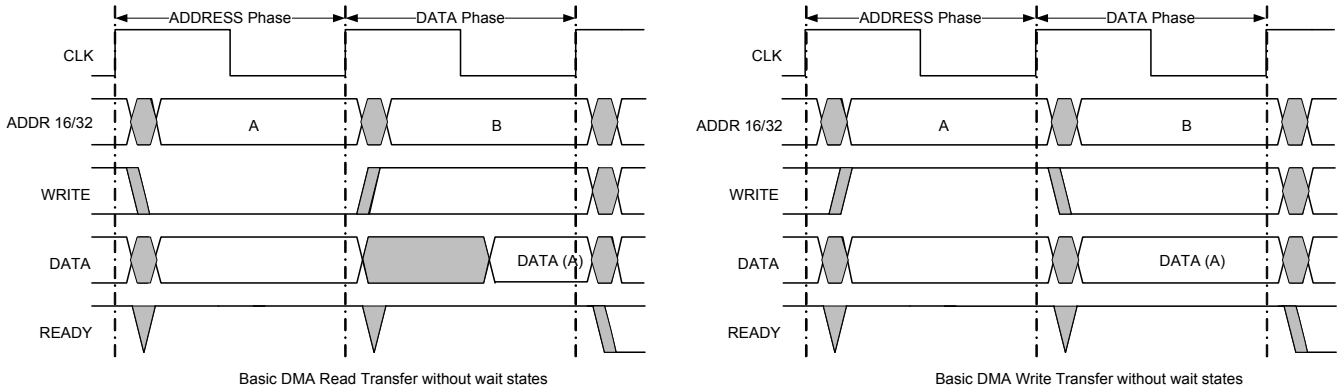
What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	67MHz
Connectivity	CANbus, I²C, LINbus, SPI, UART/USART, USB
Peripherals	CapSense, DMA, LCD, POR, PWM, WDT
Number of I/O	62
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 5.5V
Data Converters	A/D 1x20b, 1x12b; D/A 4x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c5866axi-lp020

Figure 4-2. DMA Timing Diagram



4.3.4.2 Auto Repeat DMA

Auto repeat DMA is typically used when a static pattern is repetitively read from system memory and written to a peripheral. This is done with a single TD that chains to itself.

4.3.4.3 Ping Pong DMA

A ping pong DMA case uses double buffering to allow one buffer to be filled by one client while another client is consuming the data previously received in the other buffer. In its simplest form, this is done by chaining two TDs together so that each TD calls the opposite TD when complete.

4.3.4.4 Circular DMA

Circular DMA is similar to ping pong DMA except it contains more than two buffers. In this case there are multiple TDs; after the last TD is complete it chains back to the first TD.

4.3.4.5 Indexed DMA

In an indexed DMA case, an external master requires access to locations on the system bus as if those locations were shared memory. As an example, a peripheral may be configured as an SPI or I^2C slave where an address is received by the external master. That address becomes an index or offset into the internal system bus memory space. This is accomplished with an initial “address fetch” TD that reads the target address location from the peripheral and writes that value into a subsequent TD in the chain. This modifies the TD chain on the fly. When the “address fetch” TD completes it moves on to the next TD, which has the new address information embedded in it. This TD then carries out the data transfer with the address location required by the external master.

4.3.4.6 Scatter Gather DMA

In the case of scatter gather DMA, there are multiple noncontiguous sources or destinations that are required to effectively carry out an overall DMA transaction. For example, a packet may need to be transmitted off of the device and the packet elements, including the header, payload, and trailer, exist in various noncontiguous locations in memory. Scatter gather DMA allows the segments to be concatenated together by using multiple TDs in a chain. The chain gathers the data from the multiple locations. A similar concept applies for the reception of data onto the device. Certain parts of the received data may need to be scattered to various locations in memory for software processing convenience. Each TD in the chain specifies the location for each discrete element in the chain.

4.3.4.7 Packet Queuing DMA

Packet queuing DMA is similar to scatter gather DMA but specifically refers to packet protocols. With these protocols, there may be separate configuration, data, and status phases associated with sending or receiving a packet.

For instance, to transmit a packet, a memory mapped configuration register can be written inside a peripheral, specifying the overall length of the ensuing data phase. The CPU can set up this configuration information anywhere in system memory and copy it with a simple TD to the peripheral. After the configuration phase, a data phase TD (or a series of data phase TDs) can begin (potentially using scatter gather). When the data phase TD(s) finish, a status phase TD can be invoked that reads some memory mapped status information from the peripheral and copies it to a location in system memory specified by the CPU for later inspection. Multiple sets of configuration, data, and status phase “subchains” can be strung together to create larger chains that transmit multiple packets in this way. A similar concept exists in the opposite direction to receive the packets.

4.3.4.8 Nested DMA

One TD may modify another TD, as the TD configuration space is memory mapped similar to any other peripheral. For example, a first TD loads a second TD’s configuration and then calls the second TD. The second TD moves data as required by the application. When complete, the second TD calls the first TD, which again updates the second TD’s configuration. This process repeats as often as necessary.

6.4 I/O System and Routing

PSoC I/Os are extremely flexible. Every GPIO has analog and digital I/O capability. All I/Os have a large number of drive modes, which are set at POR. PSoC also provides up to four individual I/O voltage domains through the VDDIO pins.

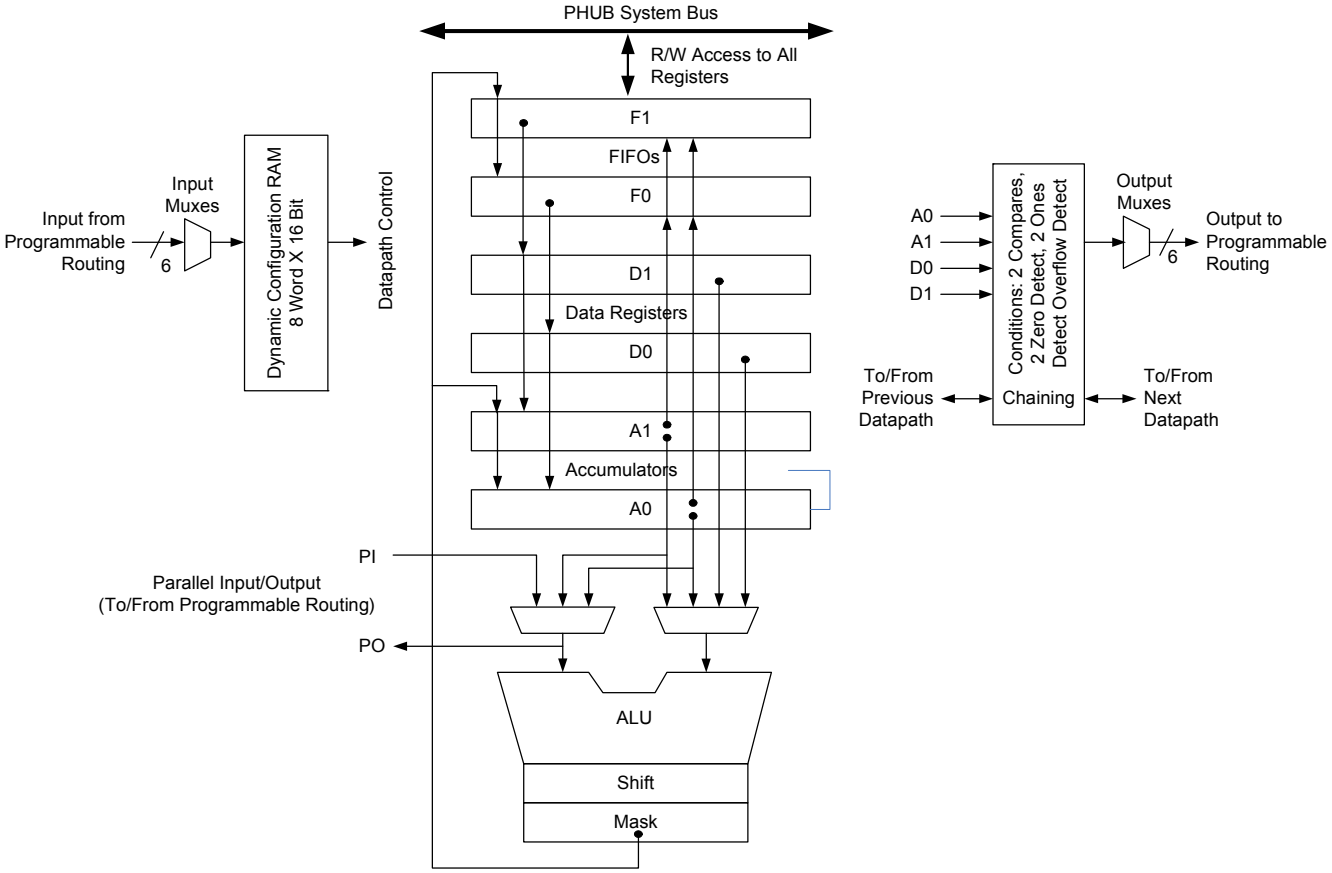
There are two types of I/O pins on every device; those with USB provide a third type. Both general purpose I/O (GPIO) and special I/O (SIO) provide similar digital functionality. The primary differences are their analog capability and drive strength. Devices that include USB also provide two USBIO pins that support specific USB functionality as well as limited GPIO capability.

All I/O pins are available for use as digital inputs and outputs for both the CPU and digital peripherals. In addition, all I/O pins can generate an interrupt. The flexible and advanced capabilities of the PSoC I/O, combined with any signal to any pin routability, greatly simplify circuit design and board layout. All GPIO pins can be used for analog input, CapSense[9], and LCD segment drive, while SIO pins are used for voltages in excess of VDDA and for programmable output voltages.

- Features supported by both GPIO and SIO:
  - User programmable port reset state
  - Separate I/O supplies and voltages for up to four groups of I/O
  - Digital peripherals use DSI to connect the pins
  - Input or output or both for CPU and DMA
  - Eight drive modes
  - Every pin can be an interrupt source configured as rising edge, falling edge or both edges. If required, level sensitive interrupts are supported through the DSI
  - Dedicated port interrupt vector for each port
  - Slew rate controlled digital output drive mode
  - Access port control and configuration registers on either port basis or pin basis
  - Separate port read (PS) and write (DR) data registers to avoid read modify write errors
  - Special functionality on a pin by pin basis
- Additional features only provided on the GPIO pins:
  - LCD segment drive on LCD equipped devices
  - CapSense[9]
  - Analog input and output capability
  - Continuous 100 µA clamp current capability
  - Standard drive strength down to 1.71 V
- Additional features only provided on SIO pins:
  - Higher drive strength than GPIO
  - Hot swap capability (5 V tolerance at any operating VDD)
  - Programmable and regulated high input and output drive levels down to 1.2 V
  - No analog input, CapSense, or LCD capability
  - Over voltage tolerance up to 5.5 V
  - SIO can act as a general purpose analog comparator
- USBIO features:
  - Full speed USB 2.0 compliant I/O
  - Highest drive strength for general purpose use
  - Input, output, or both for CPU and DMA
  - Input, output, or both for digital peripherals
  - Digital output (CMOS) drive mode
  - Each pin can be an interrupt source configured as rising edge, falling edge, or both edges

Note
9. GPIOs with opamp outputs are not recommended for use with CapSense.

Figure 7-4. Datapath Top Level



7.2.2.1 Working Registers

The datapath contains six primary working registers, which are accessed by CPU firmware or DMA during normal operation.

Table 7-1. Working Datapath Registers

Name	Function	Description
A0 and A1	Accumulators	These are sources and sinks for the ALU and also sources for the compares.
D0 and D1	Data Registers	These are sources for the ALU and sources for the compares.
F0 and F1	FIFOs	These are the primary interface to the system bus. They can be a data source for the data registers and accumulators or they can capture data from the accumulators or ALU. Each FIFO is four bytes deep.

7.2.2.2 Dynamic Configuration RAM

Dynamic configuration is the ability to change the datapath function and internal configuration on a cycle-by-cycle basis, under sequencer control. This is implemented using the 8-word x 16-bit configuration RAM, which stores eight unique 16-bit wide configurations. The address input to this RAM controls the sequence, and can be routed from any block connected to the UDB routing matrix, most typically PLD logic, I/O pins, or from the outputs of this or other datapath blocks.

ALU

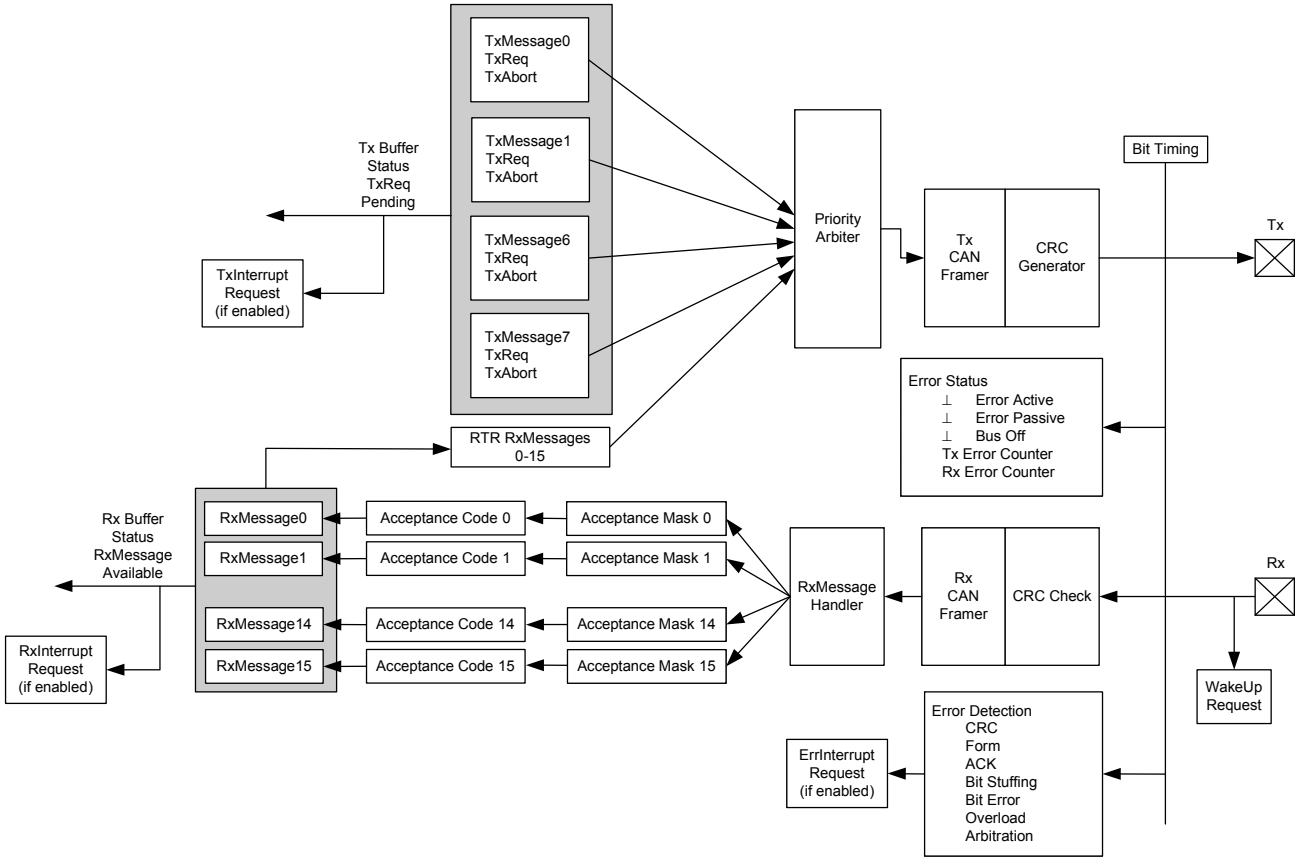
The ALU performs eight general purpose functions. They are:

- Increment
- Decrement
- Add
- Subtract
- Logical AND
- Logical OR
- Logical XOR
- Pass, used to pass a value through the ALU to the shift register, mask, or another UDB register

Independent of the ALU operation, these functions are available:

- Shift left
- Shift right
- Nibble swap
- Bitwise OR mask

Figure 7-15. CAN Controller Block Diagram



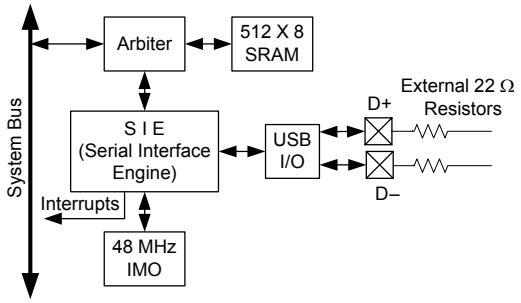
7.6 USB

PSoC includes a dedicated Full-Speed (12 Mbps) USB 2.0 transceiver supporting all four USB transfer types: control, interrupt, bulk, and isochronous. PSoC Creator provides full configuration support. USB interfaces to hosts through two dedicated USBIO pins, which are detailed in the I/O System and Routing on page 33.

USB includes the following features:

- Eight unidirectional data endpoints
- One bidirectional control endpoint 0 (EP0)
- Shared 512-byte buffer for the eight data endpoints
- Dedicated 8-byte buffer for EP0
- Three memory modes
  - Manual Memory Management with No DMA Access
  - Manual Memory Management with Manual DMA Access
  - Automatic Memory Management with Automatic DMA Access
- Internal 3.3 V regulator for transceiver
- Internal 48 MHz oscillator that auto locks to USB bus clock, requiring no external crystal for USB (USB equipped parts only)
- Interrupts on bus and each endpoint event, with device wakeup
- USB Reset, Suspend, and Resume operations
- Bus powered and self powered modes

Figure 7-16. USB



9.2 SWD Interface

The SWD interface is the preferred alternative to the JTAG interface. It requires only two pins instead of the four or five needed by JTAG. SWD provides all of the programming and debugging features of JTAG at the same speed. SWD does not provide access to scan chains or device chaining. The SWD clock frequency can be up to 1/3 of the CPU clock frequency.

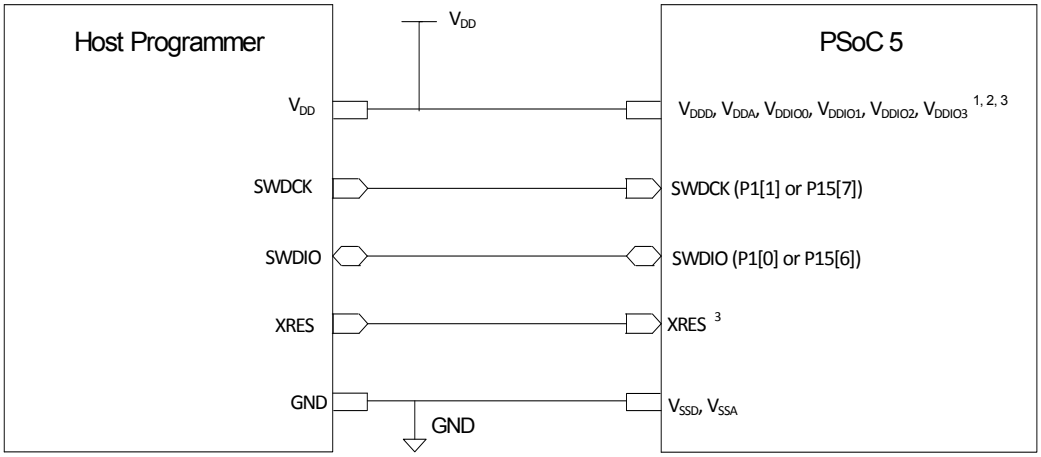
SWD uses two pins, either two of the JTAG pins (TMS and TCK) or the USBIO D+ and D- pins. The USBIO pins are useful for in system programming of USB solutions that would otherwise require a separate programming connector. One pin is used for the data clock and the other is used for data input and output.

SWD can be enabled on only one of the pin pairs at a time. This only happens if, within 8 µs (key window) after reset, that pin pair (JTAG or USB) receives a predetermined acquire sequence of 1s and 0s. If the NVL latches are set for SWD (see *Section 5.5*), this sequence need not be applied to the JTAG pin pair. The acquire sequence must always be applied to the USB pin pair.

SWD is used for debugging or for programming the flash memory.

The SWD interface can be enabled from the JTAG interface or disabled, allowing its pins to be used as GPIO. Unlike JTAG, the SWD interface can always be reacquired on any device during the key window. It can then be used to reenable the JTAG interface, if desired. When using SWD or JTAG pins as standard GPIO, make sure that the GPIO functionality and PCB circuits do not interfere with SWD or JTAG use.

Figure 9-2. SWD Interface Connections between PSoC 5LP and Programmer



[1] The voltage levels of the Host Programmer and the PSoC 5 voltage domains involved in programming should be the same. The XRES pin is powered by V_{DDIO1}. The USB SWD pins are powered by V_{DDD}. So for Programming using the USB SWD pins with XRES pin, the V_{DDD}, V_{DDIO1} of PSoC 5 should be at the same voltage level as Host V_{DD}. Rest of PSoC 5 voltage domains (V_{DDA}, V_{DDIO0}, V_{DDIO2}, V_{DDIO3}) need not be at the same voltage level as host Programmer. The Port 1 SWD pins are powered by V_{DDIO1}. So V_{DDIO1} of PSoC 5 should be at same voltage level as host V_{DD} for Port 1 SWD programming. Rest of PSoC 5 voltage domains (V_{DDD}, V_{DDA}, V_{DDIO0}, V_{DDIO2}, V_{DDIO3}) need not be at the same voltage level as host Programmer.

[2] Vdda must be greater than or equal to all other power supplies (Vddd, Vddio's) in PSoC 5.

[3] For Power cycle mode Programming, XRES pin is not required. But the Host programmer must have the capability to toggle power (Vddd, Vdda, All Vddio's) to PSoC 5. This may typically require external interface circuitry to toggle power which will depend on the programming setup. The power supplies can be brought up in any sequence, however, once stable, VDDA must be greater than or equal to all other supplies.

9.3 Debug Features

The CY8C58LP supports the following debug features:

- Halt and single-step the CPU
- View and change CPU and peripheral registers, and RAM addresses
- Six program address breakpoints and two literal access breakpoints
- Data watchpoint events to CPU
- Patch and remap instruction from flash to SRAM
- Debugging at the full speed of the CPU
- Compatible with PSoC Creator and MiniProg3 programmer and debugger
- Standard JTAG programming and debugging interfaces make CY8C58LP compatible with other popular third-party tools (for example, ARM / Keil)

9.4 Trace Features

The following trace features are supported:

- Instruction trace
- Data watchpoint on access to data address, address range, or data value
- Trace trigger on data watchpoint
- Debug exception trigger
- Code profiling
- Counters for measuring clock cycles, folded instructions, load/store operations, sleep cycles, cycles per instruction, interrupt overhead
- Interrupt events trace
- Software event monitoring, “printf-style” debugging

9.5 SWV and TRACEPORT Interfaces

The SWV and TRACEPORT interfaces provide trace data to a debug host via the Cypress MiniProg3 or an external trace port analyzer. The 5 pin TRACEPORT is used for rapid transmission of large trace streams. The single pin SWV mode is used to minimize the number of trace pins. SWV is shared with a JTAG pin. If debugging and tracing are done at the same time then SWD may be used with either SWV or TRACEPORT, or JTAG may be used with TRACEPORT, as shown in Table 9-1.

Table 9-1. Debug Configurations

Debug and Trace Configuration	GPIO Pins Used
All debug and trace disabled	0
JTAG	4 or 5
SWD	2
SWV	1
TRACEPORT	5
JTAG + TRACEPORT	9 or 10
SWD + SWV	3
SWD + TRACEPORT	7

9.6 Programming Features

The JTAG and SWD interfaces provide full programming support. The entire device can be erased, programmed, and verified. Designers can increase flash protection levels to protect firmware IP. Flash protection can only be reset after a full device erase. Individual flash blocks can be erased, programmed, and verified, if block security settings permit.

9.7 Device Security

PSoC 5LP offers an advanced security feature called device security, which permanently disables all test, programming, and debug ports, protecting your application from external access. The device security is activated by programming a 32-bit key (0x50536F43) to a Write Once Latch (WOL).

The WOL is a type of nonvolatile latch (NVL). The cell itself is an NVL with additional logic wrapped around it. Each WOL device contains four bytes (32 bits) of data. The wrapper outputs a ‘1’ if a super-majority (28 of 32) of its bits match a pre-determined pattern (0x50536F43); it outputs a ‘0’ if this majority is not reached. When the output is 1, the Write Once NV latch locks the part out of Debug and Test modes; it also permanently gates off the ability to erase or alter the contents of the latch. Matching all bits is intentionally not required, so that single (or few) bit failures do not deassert the WOL output. The state of the NVL bits after wafer processing is truly random with no tendency toward 1 or 0.

The WOL only locks the part after the correct 32-bit key (0x50536F43) is loaded into the NVL's volatile memory, programmed into the NVL's nonvolatile cells, and the part is reset. The output of the WOL is only sampled on reset and used to disable the access. This precaution prevents anyone from reading, erasing, or altering the contents of the internal memory.

The user can write the key into the WOL to lock out external access only if no flash protection is set (see “Flash Security” section on page 19). However, after setting the values in the WOL, a user still has access to the part until it is reset. Therefore, a user can write the key into the WOL, program the flash protection data, and then reset the part to lock it.

If the device is protected with a WOL setting, Cypress cannot perform failure analysis and, therefore, cannot accept RMAs from customers. The WOL can be read out via SWD port to electrically identify protected parts. The user can write the key in WOL to lock out external access only if no flash protection is set. For more information on how to take full advantage of the security features in PSoC see the PSoC 5 TRM.

Disclaimer

Note the following details of the flash code protection features on Cypress devices.

Cypress products meet the specifications contained in their particular Cypress datasheets. Cypress believes that its family of products is one of the most secure families of its kind on the market today, regardless of how they are used. There may be methods, unknown to Cypress, that can breach the code protection features. Any of these methods, to our knowledge, would be dishonest and possibly illegal. Neither Cypress nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as “unbreakable.”

Cypress is willing to work with the customer who is concerned about the integrity of their code. Code protection is constantly evolving. We at Cypress are committed to continuously improving the code protection features of our products.

9.8 CSP Package Bootloader

A factory-installed bootloader program is included in all devices with CSP packages. The bootloader is compatible with PSoC Creator 3.0 bootloadable project files, and has the following features:

- I2C-based
- SCLK and SDAT available at P1[6] and P1[7], respectively
- External pull-up resistors required
- I2C slave, address 4, data rate = 100 kbps
- Single application
- Wait 2 seconds for bootload command
- Other bootloader options are as set by the PSoC Creator 3.0 Bootloader Component default
- Occupies the bottom 9 Kbytes of flash

For more information on this bootloader, see the following Cypress application notes:

- AN73854, PSoC 3 and PSoC 5 LP Introduction to Bootloaders
- AN60317, PSoC 3 and PSoC 5 LP I2C Bootloader

Note that a PSoC Creator bootloadable project must be associated with .hex and .elf files for a bootloader project that is configured for the target device. Bootloader .hex and .elf files can be found at www.cypress.com/go/PSoC5LPdatasheet.

The factory-installed bootloader can be overwritten using JTAG or SWD programming.

11.4.2 SIO

Table 11-10. SIO DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
Vinmax	Maximum input voltage	All allowed values of Vddio and V_{DDD}, see Absolute Maximum Ratings on page 67	–	–	5.5	V
Vinref	Input voltage reference (differential input mode)		0.5	–	$0.52 \times V_{DDIO}$	V
Voutref	Output voltage reference (regulated output mode)					
		$V_{DDIO} > 3.7$	1	–	$V_{DDIO} - 1$	V
		$V_{DDIO} < 3.7$	1	–	$V_{DDIO} - 0.5$	V
V_{IH}	Input voltage high threshold					
	GPIO mode	CMOS input	$0.7 \times V_{DDIO}$	–	–	V
	Differential input mode[37]	Hysteresis disabled	SIO_ref + 0.2	–	–	V
V_{IL}	Input voltage low threshold					
	GPIO mode	CMOS input	–	–	$0.3 \times V_{DDIO}$	V
	Differential input mode[37]	Hysteresis disabled	–	–	SIO_ref – 0.2	V
V_{OH}	Output voltage high					
	Unregulated mode	I_{OH} = 4 mA, V_{DDIO} = 3.3 V	$V_{DDIO} - 0.4$	–	–	V
	Regulated mode[37]	I_{OH} = 1 mA	SIO_ref – 0.65	–	SIO_ref + 0.2	V
		I_{OH} = 0.1 mA	SIO_ref – 0.3	–	SIO_ref + 0.2	V
		no load, I_{OH} = 0	SIO_ref – 0.1	–	SIO_ref + 0.1	V
V_{OL}	Output voltage low	V_{DDIO} = 3.30 V, I_{OL} = 25 mA	–	–	0.8	V
		V_{DDIO} = 3.30 V, I_{OL} = 20 mA	–	–	0.4	V
		V_{DDIO} = 1.80 V, I_{OL} = 4 mA	–	–	0.4	V
Rpullup	Pull-up resistor		3.5	5.6	8.5	kΩ
Rpulldown	Pull-down resistor		3.5	5.6	8.5	kΩ
I_{IL}	Input leakage current (absolute value)[38]					
	$V_{IH} \leq$ Vddsio	25 °C, Vddsio = 3.0 V, V_{IH} = 3.0 V	–	–	14	nA
	V_{IH} > Vddsio	25 °C, Vddsio = 0 V, V_{IH} = 3.0 V	–	–	10	µA
C_{IN}	Input Capacitance[38]		–	–	9	pF
V_H	Input voltage hysteresis (Schmitt-Trigger)[38]	Single ended mode (GPIO mode)	–	115	–	mV
		Differential mode	–	50	–	mV
Idiode	Current through protection diode to V_{SSIO}		–	–	100	µA

Notes
37. See Figure 6-9 on page 35 and Figure 6-12 on page 38 for more information on SIO reference.
38. Based on device characterization (Not production tested).

11.5 Analog Peripherals

Specifications are valid for –40 °C ≤ T_A ≤ 105 °C and T_J ≤ 120 °C, except where noted. Specifications are valid for 1.71 V to 5.5 V, except where noted.

11.5.1 Opamp

Table 11-18. Opamp DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
V_I	Input voltage range		V_{SSA}	–	V_{DDA}	V
Vos	Input offset voltage		–	–	2.5	mV
		Operating temperature –40 °C to 70 °C	–	–	2	mV
TCVos	Input offset voltage drift with temperature	Power mode = high	–	–	±30	µV / °C
Ge1	Gain error, unity gain buffer mode	Rload = 1 kΩ	–	–	±0.1	%
Cin	Input capacitance	Routing from pin	–	–	18	pF
Vo	Output voltage range	1 mA, source or sink, power mode = high	V_{SSA} + 0.05	–	V_{DDA} – 0.05	V
Iout	Output current capability, source or sink	V_{SSA} + 500 mV ≤ V_{OUT} ≤ V_{DDA} –500 mV, V_{DDA} > 2.7 V	25	–	–	mA
		V_{SSA} + 500 mV ≤ V_{OUT} ≤ V_{DDA} –500 mV, 1.7 V = V_{DDA} ≤ 2.7 V	16	–	–	mA
Idd	Quiescent current[43]	Power mode = min	–	250	400	uA
		Power mode = low	–	250	400	uA
		Power mode = med	–	330	950	uA
		Power mode = high	–	1000	2500	uA
CMRR	Common mode rejection ratio[43]		80	–	–	dB
PSRR	Power supply rejection ratio[43]	V_{DDA} ≥ 2.7 V	85	–	–	dB
		V_{DDA} < 2.7 V	70	–	–	dB
I_{IB}	Input bias current[43]	25 °C	–	10	–	pA

Figure 11-25. Opamp Vos Histogram, 7020 samples/1755 parts, 30 °C, VDDA = 3.3 V

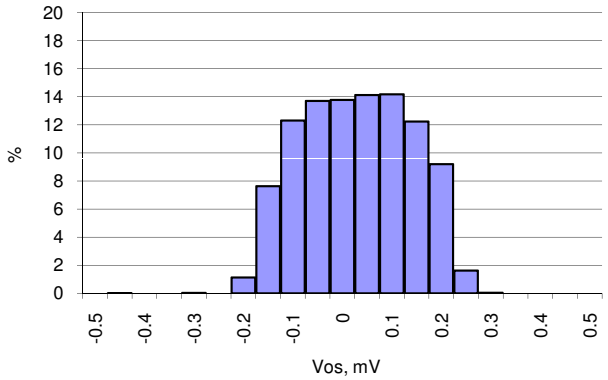
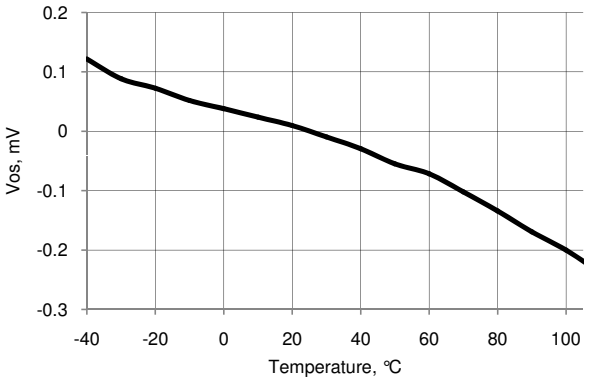


Figure 11-26. Opamp Vos vs Temperature, V_{DDA} = 5 V



Note
43. Based on device characterization (Not production tested).

Table 11-22. Delta-sigma ADC Sample Rates, Range = ±1.024 V

Resolution, Bits	Continuous		Multi-Sample		Multi-Sample Turbo	
	Min	Max	Min	Max	Min	Max
8	8000	384000	1911	91701	1829	87771
9	6400	307200	1543	74024	1489	71441
10	5566	267130	1348	64673	1307	62693
11	4741	227555	1154	55351	1123	53894
12	4000	192000	978	46900	956	45850
13	3283	157538	806	38641	791	37925
14	2783	133565	685	32855	674	32336
15	2371	113777	585	28054	577	27675
16	2000	48000	495	11861	489	11725
17	500	12000	124	2965	282	6766
18	125	3000	31	741	105	2513
19	16	375	4	93	15	357
20	8	187.5	2	46	8	183

Figure 11-33. Delta-sigma ADC IDD vs sps, Range = ±1.024 V, Continuous Sample Mode, Input Buffer Bypassed

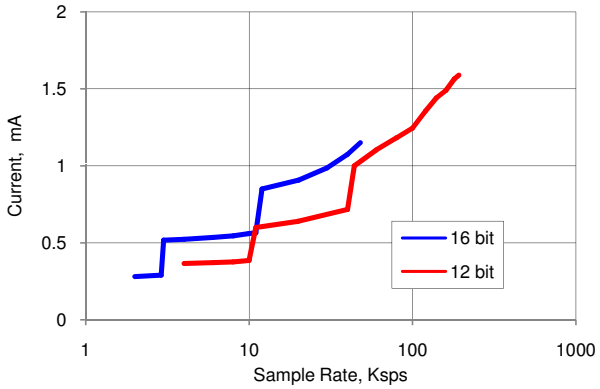


Figure 11-34. Delta-sigma ADC Noise Histogram, 1000 Samples, 20-Bit, 187 sps, Ext Ref, $V_{IN} = V_{REF}/2$, Range = ±1.024 V

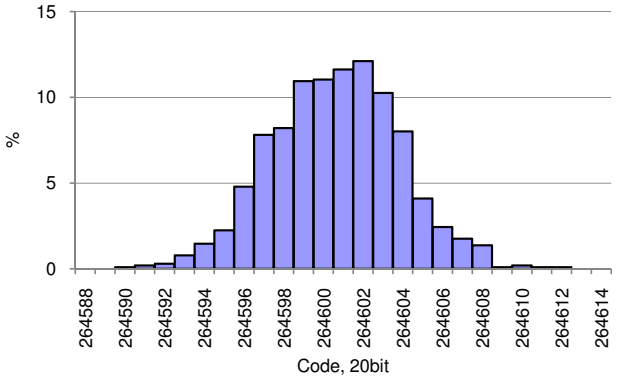


Figure 11-35. Delta-sigma ADC Noise Histogram, 1000 Samples, 16-bit, 48 ksps, Ext Ref, $V_{IN} = V_{REF}/2$, Range = ±1.024 V

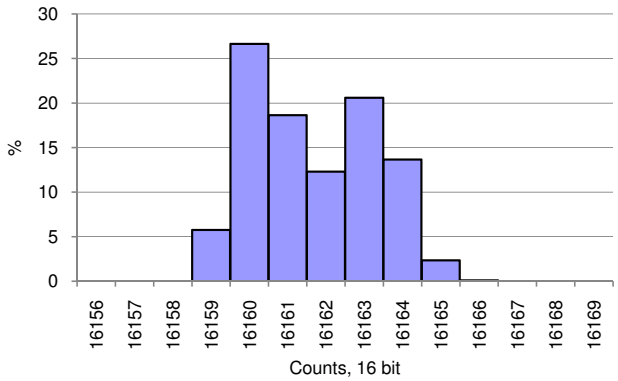
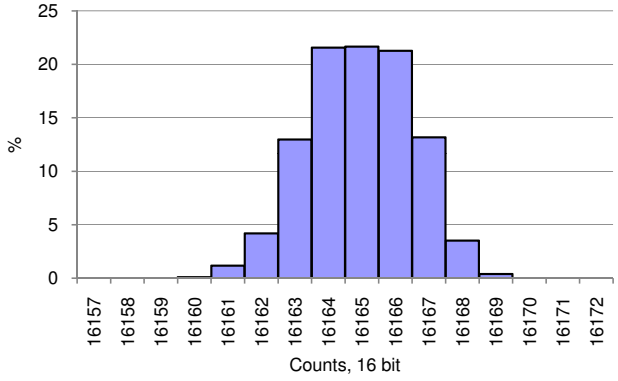


Figure 11-36. Delta-sigma ADC Noise Histogram, 1000 Samples, 16-bit, 48 ksps, Int Ref, $V_{IN} = V_{REF}/2$, Range = ±1.024 V



11.5.4 SAR ADC

Table 11-28. SAR ADC DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Resolution		–	–	12	bits
	Number of channels – single-ended		–	–	No of GPIO	
	Number of channels – differential	Differential pair is formed using a pair of neighboring GPIO.	–	–	No of GPIO/2	
	Monotonicity[52]		Yes	–	–	
Ge	Gain error[53]	External reference	–	–	±0.1	%
V_{OS}	Input offset voltage		–	–	±2	mV
I_{DD}	Current consumption[52]		–	–	1	mA
	Input voltage range – single-ended[52]		V_{SSA}	–	V_{DDA}	V
	Input voltage range – differential[52]		V_{SSA}	–	V_{DDA}	V
PSRR	Power supply rejection ratio[52]		70	–	–	dB
CMRR	Common mode rejection ratio		70	–	–	dB
INL	Integral non linearity[52]	V_{DDA} 1.71 to 5.5 V, 1 Msps, V_{REF} 1 to 5.5 V, bypassed at ExtRef pin	–	–	+2/–1.5	LSB
		V_{DDA} 2.0 to 3.6 V, 1 Msps, V_{REF} 2 to V_{DDA}, bypassed at ExtRef pin	–	–	±1.2	LSB
		V_{DDA} 1.71 to 5.5 V, 500 ksps, V_{REF} 1 to 5.5 V, bypassed at ExtRef pin	–	–	±1.3	LSB
DNL	Differential non linearity[52]	V_{DDA} 1.71 to 5.5 V, 1 Msps, V_{REF} 1 to 5.5 V, bypassed at ExtRef pin	–	–	+2/–1	LSB
		V_{DDA} 2.0 to 3.6 V, 1 Msps, V_{REF} 2 to V_{DDA}, bypassed at ExtRef pin No missing codes	–	–	1.7/–0.99	LSB
		V_{DDA} 1.71 to 5.5 V, 500 ksps, V_{REF} 1 to 5.5 V, bypassed at ExtRef pin No missing codes	–	–	+2/–0.99	LSB
R_{IN}	Input resistance[52]		–	180	–	kΩ

Notes
52. Based on device characterization (Not production tested).
53. For total analog system Idd < 5 mA, depending on package used. With higher total analog system currents it is recommended that the SAR ADC be used in differential mode.

Figure 11-41. SAR ADC DNL vs Output Code, Bypassed Internal Reference Mode

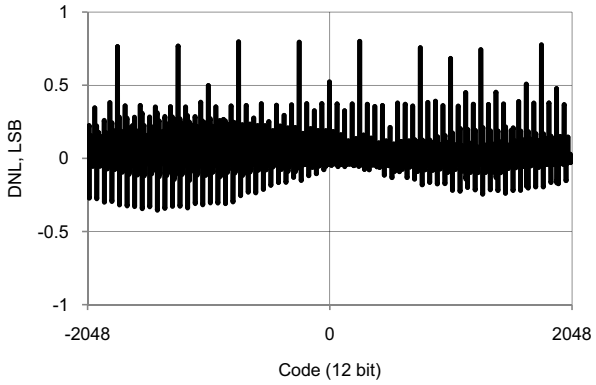


Figure 11-42. SAR ADC INL vs Output Code, Bypassed Internal Reference Mode

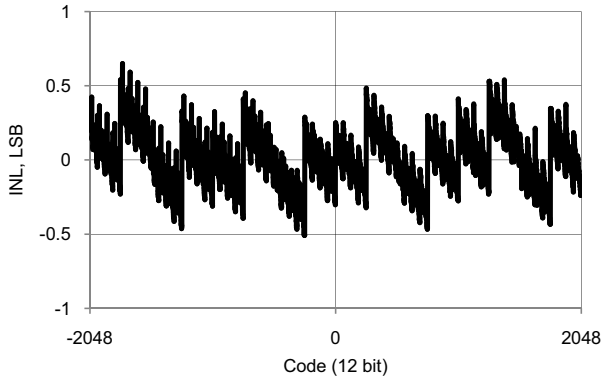
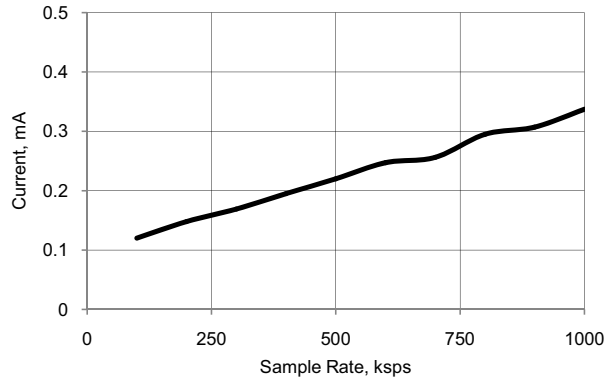


Figure 11-43. SAR ADC I_{DD} vs sps, V_{DDA} = 5 V, Continuous Sample Mode, External Reference Mode



11.5.5 Analog Globals

Table 11-30. Analog Globals DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
Rppag	Resistance pin-to-pin through P2[4], AGL0, DSM INP, AGL1, P2[5][55, 57]	V_{DDA} = 3.0 V	–	1500	2200	Ω
		V_{DDA} = 1.71 V	–	1200	1700	Ω
Rppmuxbus	Resistance pin-to-pin through P2[3], amuxbusL, P2[4][55, 57]	V_{DDA} = 3.0 V	–	700	1100	Ω
		V_{DDA} = 1.71 V	–	600	900	Ω

Table 11-31. Analog Globals AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Inter-pair crosstalk for analog routes[56]		106	–	–	dB
BWag	Analog globals 3 db bandwidth[56]	V_{DDA} = 3.0 V, 25 °C	–	26	–	MHz

Notes
55. Based on device characterization (Not production tested).
56. Pin P6[4] to del-sig ADC input; calculated, not measured.
57. The resistance of the analog global and analog mux bus is high if $V_{DDA} \leq 2.7$ V, and the chip is in either sleep or hibernate mode. Use of analog global and analog mux bus under these conditions is not recommended.

Figure 11-47. IDAC INL vs Input Code, Range = 255 µA, Source Mode

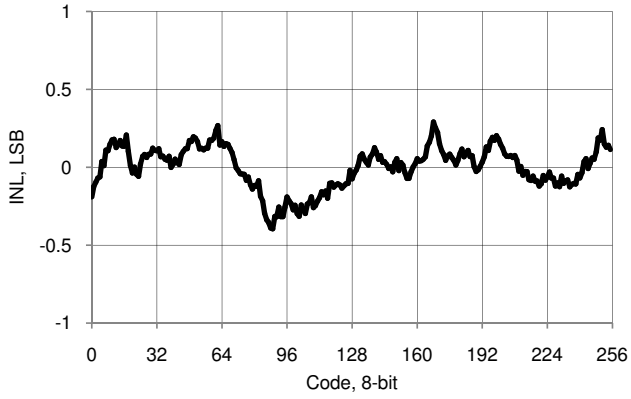


Figure 11-48. IDAC INL vs Input Code, Range = 255 µA, Sink Mode

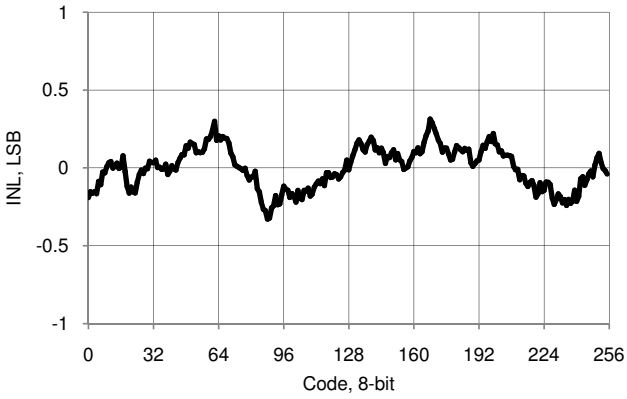


Figure 11-49. IDAC DNL vs Input Code, Range = 255 µA, Source Mode

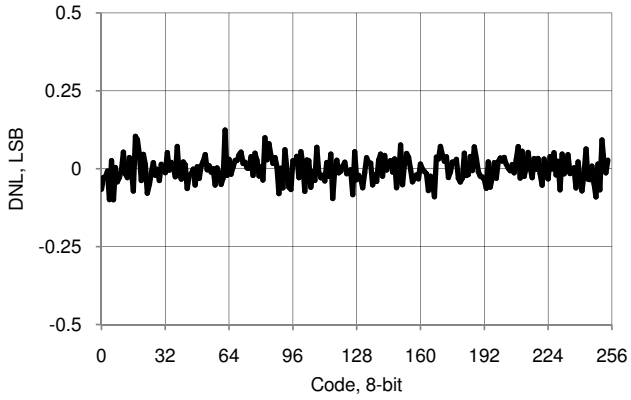


Figure 11-50. IDAC DNL vs Input Code, Range = 255 µA, Sink Mode

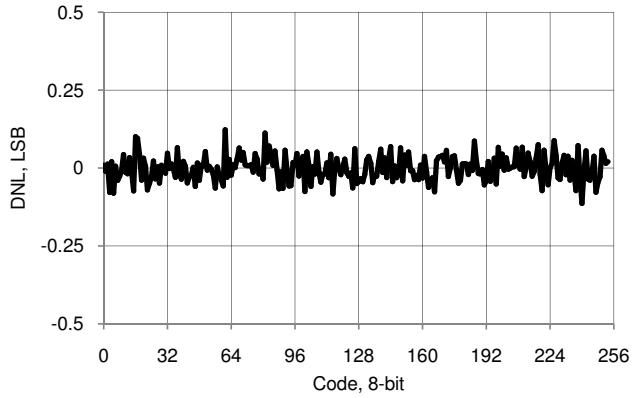


Figure 11-51. IDAC INL vs Temperature, Range = 255 µA, Fast Mode

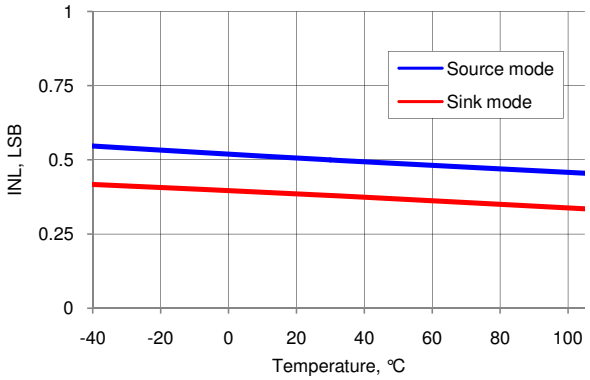


Figure 11-52. IDAC DNL vs Temperature, Range = 255 µA, Fast Mode

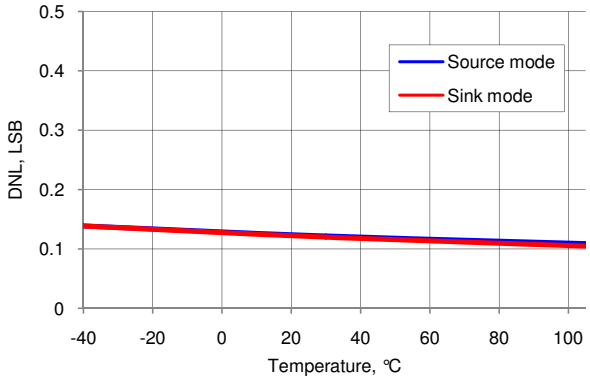


Figure 11-63. VDAC INL vs Temperature, 1 V Mode

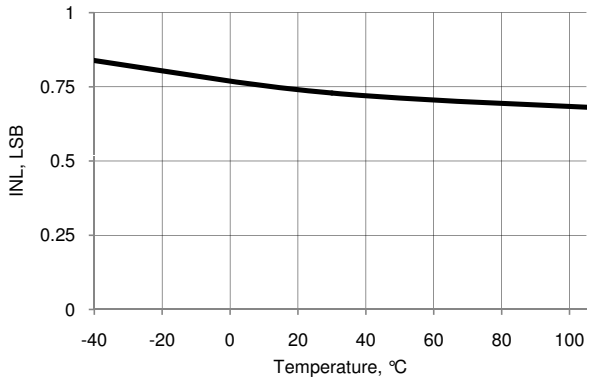


Figure 11-64. VDAC DNL vs Temperature, 1 V Mode

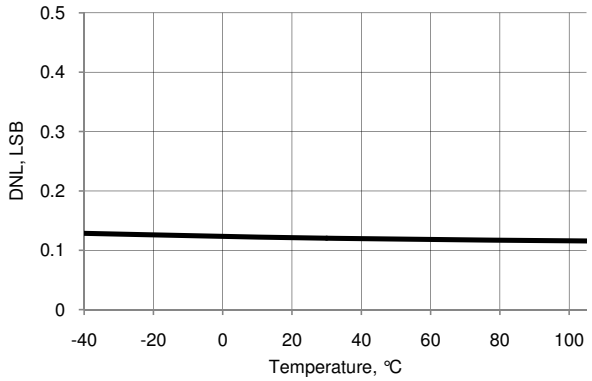


Figure 11-65. VDAC Full Scale Error vs Temperature, 1 V Mode

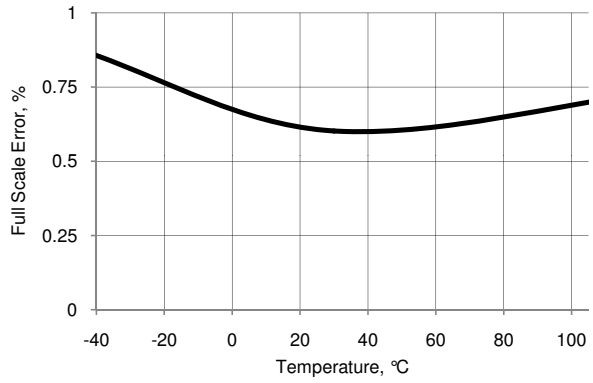


Figure 11-66. VDAC Full Scale Error vs Temperature, 4 V Mode

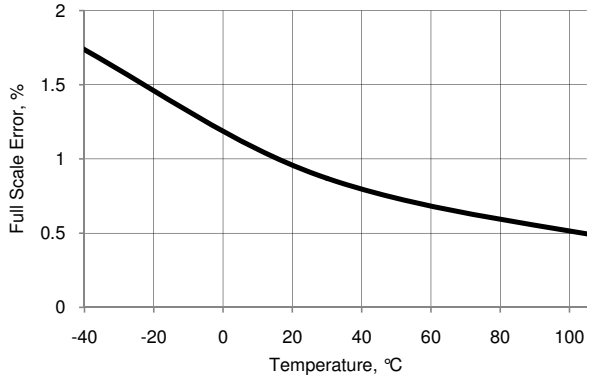


Figure 11-67. VDAC Operating Current vs Temperature, 1V Mode, Slow Mode

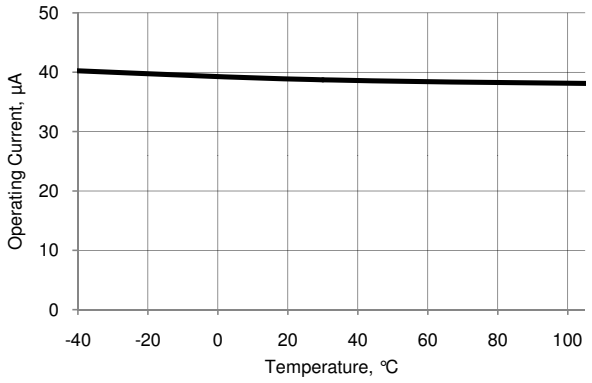
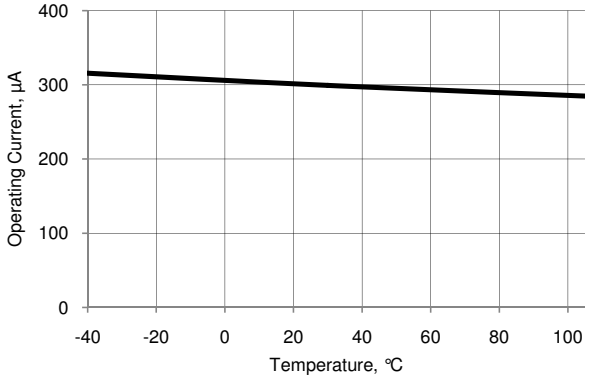


Figure 11-68. VDAC Operating Current vs Temperature, 1 V Mode, Fast Mode



11.6.6 Digital Filter Block

Table 11-57. DFB DC Specifications[78]

Parameter	Description	Conditions	Min	Typ	Max	Units
	DFB operating current	64-tap FIR at F_{DFB}				
		500 kHz (6.7 ksps)	–	0.16	0.27	mA
		1 MHz (13.4 ksps)	–	0.33	0.53	mA
		10 MHz (134 ksps)	–	3.3	5.3	mA
		48 MHz (644 ksps)	–	15.7	25.5	mA
		80 MHz (1.07 Msps)	–	26.0	42.5	mA

Table 11-58. DFB AC Specifications[78]

Parameter	Description	Conditions	Min	Typ	Max	Units
F_{DFB}	DFB operating frequency		DC	–	80.01	MHz

11.6.7 USB

Table 11-59. USB DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
V_{USB_5}	Device supply (V_{DDD}) for USB operation	USB configured, USB regulator enabled	4.35	–	5.25	V
$V_{USB\_3.3}$		USB configured, USB regulator bypassed	3.15	–	3.6	V
V_{USB_3}		USB configured, USB regulator bypassed[78]	2.85	–	3.6	V
$I_{USB\_Configured}$	Device supply current in device active mode, bus clock and IMO = 24 MHz	V_{DDD} = 5 V, F_{CPU} = 1.5 MHz	–	10	–	mA
		V_{DDD} = 3.3 V, F_{CPU} = 1.5 MHz	–	8	–	mA
$I_{USB\_Suspended}$	Device supply current in device sleep mode	V_{DDD} = 5 V, connected to USB host, PICU configured to wake on USB resume signal	–	0.5	–	mA
		V_{DDD} = 5 V, disconnected from USB host	–	0.3	–	mA
		V_{DDD} = 3.3 V, connected to USB host, PICU configured to wake on USB resume signal	–	0.5	–	mA
		V_{DDD} = 3.3 V, disconnected from USB host	–	0.3	–	mA

Note
78. Rise/fall time matching (TR) not guaranteed, see Table 11-15 on page 84.

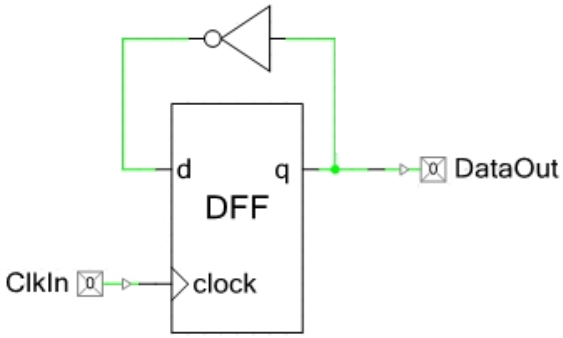
11.6.8 Universal Digital Blocks (UDBs)

PSoC Creator provides a library of pre-built and tested standard digital peripherals (UART, SPI, LIN, PRS, CRC, timer, counter, PWM, AND, OR, and so on) that are mapped to the UDB array. See the component datasheets in PSoC Creator for full AC/DC specifications, APIs, and example code.

Table 11-60. UDB AC Specifications[79]

Parameter	Description	Conditions	Min	Typ	Max	Units
Datapath Performance						
F_{MAX_TIMER}	Maximum frequency of 16-bit timer in a UDB pair		–	–	67.01	MHz
F_{MAX_ADDER}	Maximum frequency of 16-bit adder in a UDB pair		–	–	67.01	MHz
F_{MAX_CRC}	Maximum frequency of 16-bit CRC/PRS in a UDB pair		–	–	67.01	MHz
PLD Performance						
F_{MAX_PLD}	Maximum frequency of a two-pass PLD function in a UDB pair		–	–	67.01	MHz
Clock to Output Performance						
t_{CLK_OUT}	Propagation delay for clock in to data out, see Figure 11-76.	25 °C, $V_{DDD} \geq 2.7$ V	–	20	25	ns
t_{CLK_OUT}	Propagation delay for clock in to data out, see Figure 11-76.	Worst-case placement, routing, and pin selection	–	–	55	ns

Figure 11-76. Clock to Output Performance



Note
79. Based on device characterization (Not production tested).

11.8 PSoC System Resources

Specifications are valid for –40 °C ≤ T_A ≤ 105 °C and T_J ≤ 120 °C, except where noted. Specifications are valid for 1.71 V to 5.5 V, except where noted.

11.8.1 POR with Brown Out

For brown out detect in regulated mode, V_{DDD} and V_{DDA} must be ≥ 2.0 V. Brown out detect is not available in externally regulated mode.

Table 11-71. Precise Low-Voltage Reset (PRES) with Brown Out DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
PRESR	Rising trip voltage	Factory trim	1.64	–	1.68	V
PRESF	Falling trip voltage		1.62	–	1.66	V

Table 11-72. Power-On-Reset (POR) with Brown Out AC Specifications[90]

Parameter	Description	Conditions	Min	Typ	Max	Units
PRES_TR[91]	Response time		–	–	0.5	µs
	V_{DDD}/V_{DDA} droop rate	Sleep mode	–	5	–	V/sec

11.8.2 Voltage Monitors

Table 11-73. Voltage Monitors DC Specifications

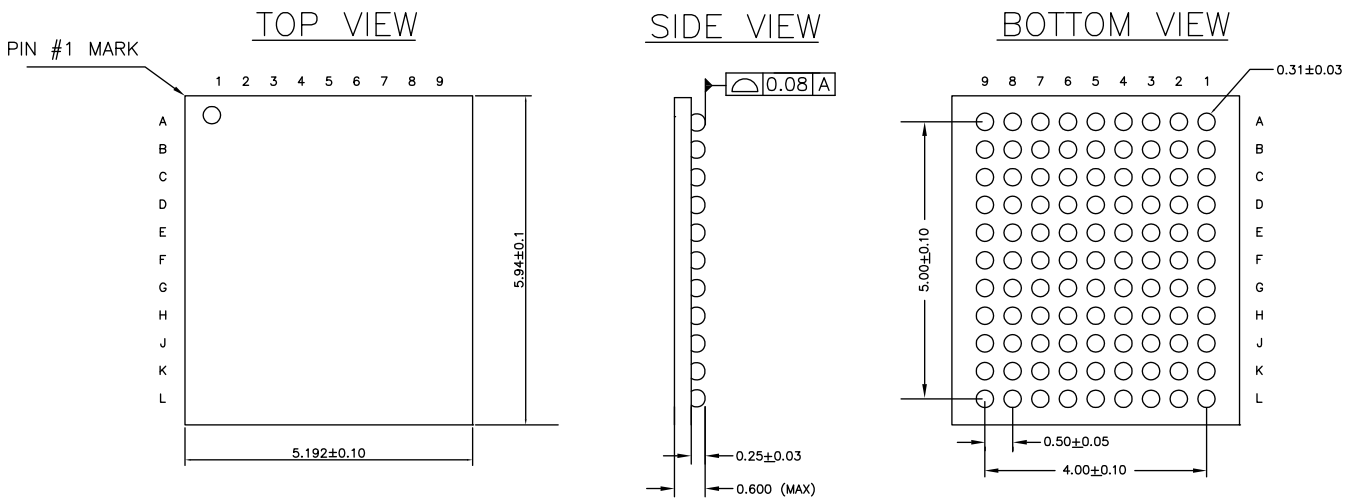
Parameter	Description	Conditions	Min	Typ	Max	Units
LVI	Trip voltage					
	LVI_A/D_SEL[3:0] = 0000b		1.68	1.73	1.77	V
	LVI_A/D_SEL[3:0] = 0001b		1.89	1.95	2.01	V
	LVI_A/D_SEL[3:0] = 0010b		2.14	2.20	2.27	V
	LVI_A/D_SEL[3:0] = 0011b		2.38	2.45	2.53	V
	LVI_A/D_SEL[3:0] = 0100b		2.62	2.71	2.79	V
	LVI_A/D_SEL[3:0] = 0101b		2.87	2.95	3.04	V
	LVI_A/D_SEL[3:0] = 0110b		3.11	3.21	3.31	V
	LVI_A/D_SEL[3:0] = 0111b		3.35	3.46	3.56	V
	LVI_A/D_SEL[3:0] = 1000b		3.59	3.70	3.81	V
	LVI_A/D_SEL[3:0] = 1001b		3.84	3.95	4.07	V
	LVI_A/D_SEL[3:0] = 1010b		4.08	4.20	4.33	V
	LVI_A/D_SEL[3:0] = 1011b		4.32	4.45	4.59	V
	LVI_A/D_SEL[3:0] = 1100b		4.56	4.70	4.84	V
	LVI_A/D_SEL[3:0] = 1101b		4.83	4.98	5.13	V
	LVI_A/D_SEL[3:0] = 1110b		5.05	5.21	5.37	V
	LVI_A/D_SEL[3:0] = 1111b		5.30	5.47	5.63	V
HVI	Trip voltage		5.57	5.75	5.92	V

Table 11-74. Voltage Monitors AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
LVI_tr[91]	Response time		–	–	1	µs

Notes
90. Based on device characterization (Not production tested).
91. This value is calculated, not measured.

Figure 13-3. WLCSP Package (5.192 × 5.940 × 0.6 mm) Package Outline



NOTES:

1. REFERENCE JEDEC Publication 95: Design Guide 4.18
2. ALL DIMENSIONS ARE IN MILLIMETERS

001-88034 *B

Document History Page (continued)

Description Title: PSoC® 5LP: CY8C58LP Family Datasheet Programmable System-on-Chip (PSoC®) Document Number: 001-84932				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
*H	4698847	AVER / MKEA / GJV	03/24/2015	Updated Features: Added “Extended temperature parts: –40 to 105 °C” as indented under “Temperature range (ambient)” under “Operating characteristics”. Updated System Integration: Updated Power System: Updated Boost Converter: Updated entire section. Updated Electrical Specifications: Replaced “Specifications are valid for –40 °C ≤ T_A ≤ 85 °C and T_J ≤ 100 °C, except where noted.” with “Specifications are valid for –40 °C ≤ T_A ≤ 105 °C and T_J ≤ 120 °C, except where noted.” in all instances. Updated Device Level Specifications: Updated Table 11-2: Added details of I_{DD} parameter corresponding to “T = 105 °C”. Updated Figure 11-3 and Figure 11-4. Updated Power Regulators: Updated Inductive Boost Regulator: Updated Table 11-6: Updated details of V_{BAT}, I_{OUT}, V_{OUT}, Reg_{LOAD}, Reg_{LINE} parameters. Removed V_{OUT}: V_{BAT} parameter and its details. Removed Table “Inductive Boost Regulator AC Specifications”. Updated Table 11-7: Updated details of L_{BOOST}, C_{BOOST} parameters. Added C_{BAT} parameter and its details. Added Figure 11-8, Figure 11-9, Figure 11-10, Figure 11-11, Figure 11-12, Figure 11-13, Figure 11-14. Removed Figure “Efficiency vs I_{OUT} V_{BOOST} = 3.3 V, L_{BOOST} = 10 µH”. Removed Figure “Efficiency vs I_{OUT} V_{BOOST} = 3.3 V, L_{BOOST} = 22 µH”. Updated Analog Peripherals: Updated Opamp: Updated Figure 11-26. Updated Delta-Sigma ADC: Updated Table 11-20: Added details of CMRRb parameter corresponding to condition “T_A ≤ 105 °C”. Updated Table 11-21: Added details of SINAD16int parameter corresponding to condition “T_A ≤ 105 °C”. Updated Voltage Reference: Updated Table 11-27: Added details of V_{REF} parameter corresponding to condition “105 °C”. Updated Figure 11-39. Updated Current Digital-to-analog Converter (IDAC): Updated Figure 11-51, Figure 11-52, Figure 11-53, Figure 11-54, Figure 11-55, Figure 11-56. Updated Voltage Digital to Analog Converter (VDAC): Updated Figure 11-63, Figure 11-64, Figure 11-65, Figure 11-66, Figure 11-67, Figure 11-68. Updated Programmable Gain Amplifier: Updated Table 11-43: Added details of BW1 parameter corresponding to condition “T_A ≤ 105 °C”. Updated Figure 11-74. Updated Temperature Sensor: Updated Table 11-44: Replaced 85 °C with 105 °C.