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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	67MHz
Connectivity	I²C, LINbus, SPI, UART/USART, USB
Peripherals	CapSense, DMA, LCD, POR, PWM, WDT
Number of I/O	62
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 5.5V
Data Converters	A/D 1x20b, 1x12b; D/A 4x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c5866axi-lp021

1. Architectural Overview

Introducing the CY8C58LP family of ultra low power, flash Programmable System-on-Chip (PSoC) devices, part of a scalable 8-bit PSoC 3 and 32-bit PSoC 5LP platform. The CY8C58LP family provides configurable blocks of analog, digital, and interconnect circuitry around a CPU subsystem. The combination of a CPU with a flexible analog subsystem, digital subsystem, routing, and I/O enables a high level of integration in a wide variety of consumer, industrial, and medical applications.

Figure 1-1. Simplified Block Diagram

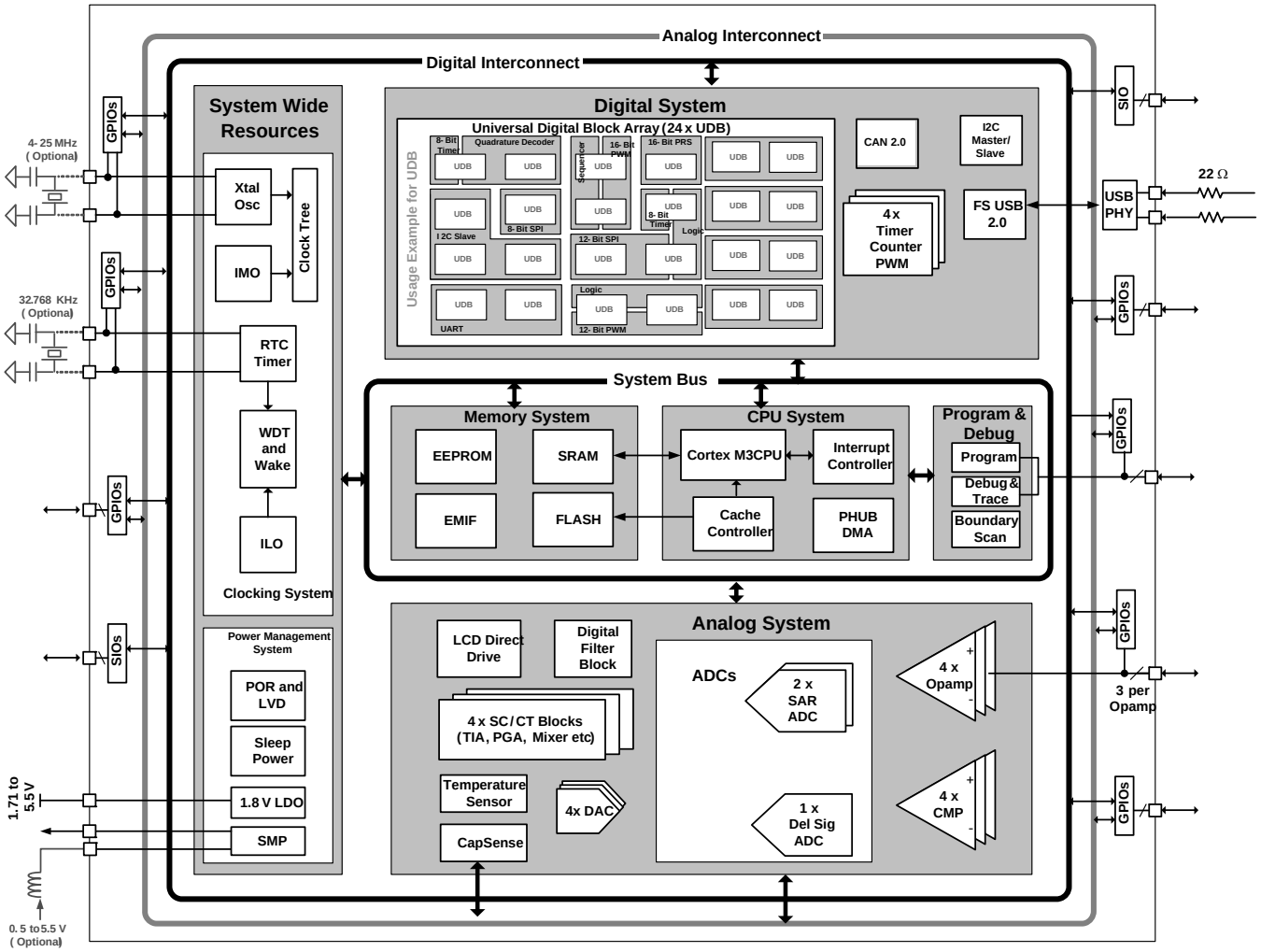
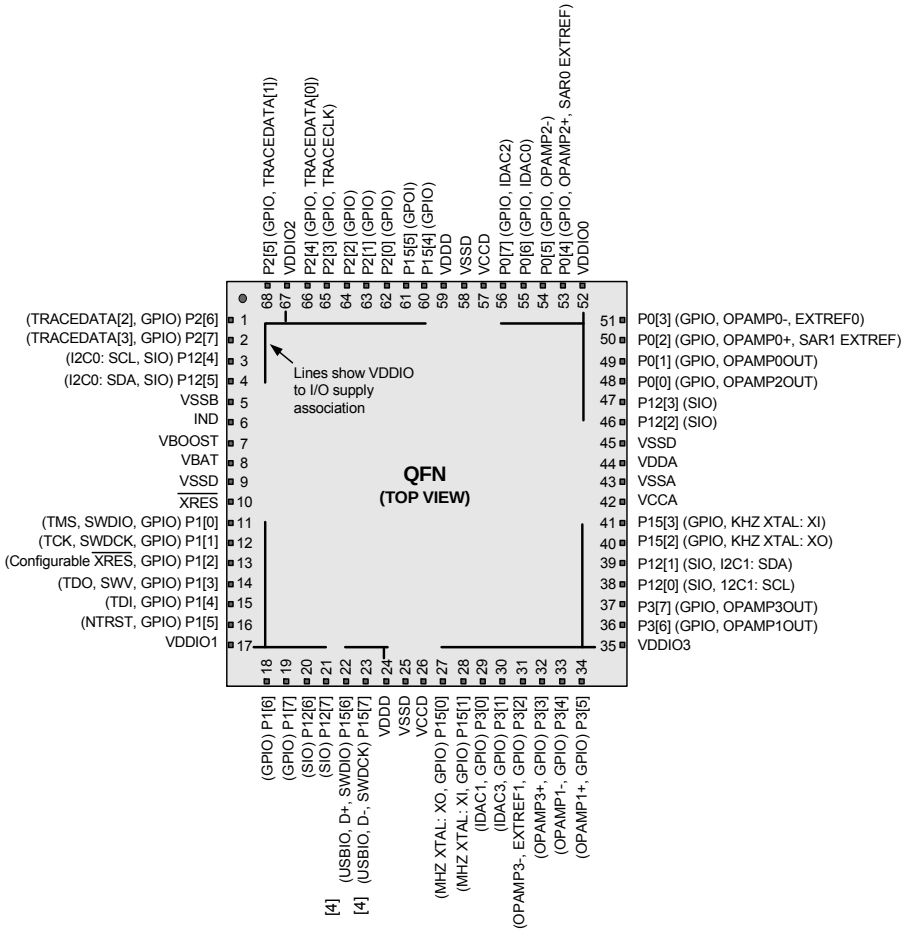


Figure 1-1 illustrates the major components of the CY8C58LP family. They are:

- ARM Cortex-M3 CPU subsystem
- Nonvolatile subsystem
- Programming, debug, and test subsystem
- Inputs and outputs
- Clocking
- Power
- Digital subsystem
- Analog subsystem

PSoC's digital subsystem provides half of its unique configurability. It connects a digital signal from any peripheral to any pin through the digital system interconnect (DSI). It also provides functional flexibility through an array of small, fast, low power UDBs. PSoC Creator provides a library of pre-built and tested standard digital peripherals (UART, SPI, LIN, PRS, CRC, timer, counter, PWM, AND, OR, and so on) that are mapped to the UDB array. You can also easily create a digital circuit using boolean primitives by means of graphical design entry. Each UDB contains programmable array logic (PAL)/programmable logic device (PLD) functionality, together with a small state machine engine to support a wide variety of peripherals.

Figure 2-3. 68-pin QFN Part Pinout [3]



Notes
3. The center pad on the QFN package should be connected to digital ground (VSSD) for best mechanical, thermal, and electrical performance. If not connected to ground, it should be electrically floated and not connected to any other signal. For more information, see AN72845, Design Guidelines for QFN Devices.
4. Pins are Do Not Use (DNU) on devices without USB. The pin must be left floating.

Table 2-2 shows the pinout for the 99-pin CSP package. Since there are four V_{DDIO} pins, the set of I/O pins associated with any V_{DDIO} may sink up to 100 mA total, same as for the 100-pin and 68-pin devices.

Table 2-2. CSP Pinout

Ball	Name	Ball	Name	Ball	Name	Ball	Name
E5	P2[5]	L2	VIO1	B2	P3[6]	C8	VIO0
G6	P2[6]	K2	P1[6]	B3	P3[7]	D7	P0[4]
G5	P2[7]	C9	P4[2]	C3	P12[0]	E7	P0[5]
H6	P12[4]	E8	P4[3]	C4	P12[1]	B9	P0[6]
K7	P12[5]	K1	P1[7]	E3	P15[2]	D8	P0[7]
L8	P6[4]	H2	P12[6]	E4	P15[3]	D9	P4[4]
J6	P6[5]	F4	P12[7]	A1	NC	F8	P4[5]
H5	P6[6]	J1	P5[4]	A9	NC	F7	P4[6]
J5	P6[7]	H1	P5[5]	L1	NC	E6	P4[7]
L7	VSSB	F3	P5[6]	L9	NC	E9	VCCD
K6	Ind	G1	P5[7]	A3	VCCA	F9	VSSD
L6	VBOOST	G2	P15[6]	A4	VSSA	G9	VDDD
K5	VBAT	F2	P15[7]	B7	VSSA	H9	P6[0]
L5	VSSD	E2	VDDD	B8	VSSA	G8	P6[1]
L4	XRES	F1	VSSD	C7	VSSA	H8	P6[2]
J4	P5[0]	E1	VCCD	A5	VDDA	J9	P6[3]
K4	P5[1]	D1	P15[0]	A6	VSSD	G7	P15[4]
K3	P5[2]	D2	P15[1]	B5	P12[2]	F6	P15[5]
L3	P5[3]	C1	P3[0]	A7	P12[3]	F5	P2[0]
H4	P1[0]	C2	P3[1]	C5	P4[0]	J7	P2[1]
J3	P1[1]	D3	P3[2]	D5	P4[1]	J8	P2[2]
H3	P1[2]	D4	P3[3]	B6	P0[0]	K9	P2[3]
J2	P1[3]	B4	P3[4]	C6	P0[1]	H7	P2[4]
G4	P1[4]	A2	P3[5]	A8	P0[2]	K8	VIO2
G3	P1[5]	B1	VIO3	D6	P0[3]		

Figure 2-5 on page 10 and Figure 2-6 on page 11 show an example schematic and an example PCB layout, for the 100-pin TQFP part, for optimal analog performance on a two-layer board.

- The two pins labeled VDDD must be connected together.
- The two pins labeled VCCD must be connected together, with capacitance added, as shown in Figure 2-5 and Power System on page 26. The trace between the two VCCD pins should be as short as possible.
- The two pins labeled VSSD must be connected together.

For information on circuit board layout issues for mixed signals, refer to the application note, AN57821 - Mixed Signal Circuit Board Layout Considerations for PSoC® 3 and PSoC 5.

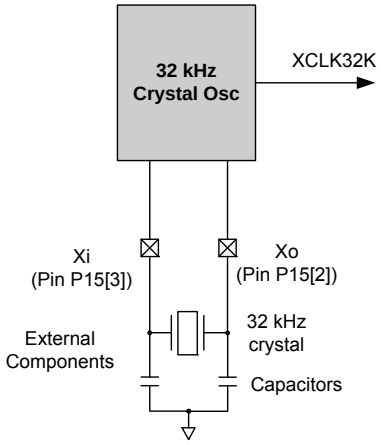
Note
6. Pins are Do Not Use (DNU) on devices without USB. The pin must be left floating.

6.1.2.2 32.768 kHz ECO

The 32.768-kHz external crystal oscillator (32kHzECO) provides precision timing with minimal power consumption using an external 32.768-kHz watch crystal (see Figure 6-3). The 32kHzECO also connects directly to the sleep timer and provides the source for the RTC. The RTC uses a 1 second interrupt to implement the RTC functionality in firmware.

The oscillator works in two distinct power modes. This allows users to trade off power consumption with noise immunity from neighboring circuits. The GPIO pins connected to the external crystal and capacitors are fixed.

Figure 6-3. 32kHzECO Block Diagram



It is recommended that the external 32.768-kHz watch crystal have a load capacitance (CL) of 6 pF or 12.5 pF. Check the crystal manufacturer's datasheet. The two external capacitors, CL1 and CL2, are typically of the same value, and their total capacitance, CL1CL2 / (CL1 + CL2), including pin and trace capacitance, should equal the crystal CL value. For more information, refer to application note AN54439: PSoC 3 and PSoC 5 External Oscillators. See also pin capacitance specifications in the "GPIO" section on page 76.

6.1.2.3 Digital System Interconnect

The DSI provides routing for clocks taken from external clock oscillators connected to I/O. The oscillators can also be generated within the device in the digital system and UDBs.

While the primary DSI clock input provides access to all clocking resources, up to eight other DSI clocks (internally or externally generated) may be routed directly to the eight digital clock dividers. This is only possible if there are multiple precision clock sources.

6.1.3 Clock Distribution

All seven clock sources are inputs to the central clock distribution system. The distribution system is designed to create multiple high precision clocks. These clocks are customized for the design's requirements and eliminate the common problems found with limited resolution prescalers attached to peripherals. The clock distribution system generates several types of clock trees.

- The system clock is used to select and supply the fastest clock in the system for general system clock requirements and clock synchronization of the PSoC device.
- Bus clock 16-bit divider uses the system clock to generate the system's bus clock used for data transfers and the CPU. The CPU clock is directly derived from the bus clock.
- Eight fully programmable 16-bit clock dividers generate digital system clocks for general use in the digital system, as configured by the design's requirements. Digital system clocks can generate custom clocks derived from any of the seven clock sources for any purpose. Examples include baud rate generators, accurate PWM periods, and timer clocks, and many others. If more than eight digital clock dividers are required, the UDBs and fixed function timer/counter/PWMs can also generate clocks.
- Four 16-bit clock dividers generate clocks for the analog system components that require clocking, such as ADCs and mixers. The analog clock dividers include skew control to ensure that critical analog events do not occur simultaneously with digital switching events. This is done to reduce analog system noise.

Each clock divider consists of an 8-input multiplexer, a 16-bit clock divider (divide by 2 and higher) that generates ~50% duty cycle clocks, system clock resynchronization logic, and deglitch logic. The outputs from each digital clock tree can be routed into the digital system interconnect and then brought back into the clock system as an input, allowing clock chaining of up to 32 bits.

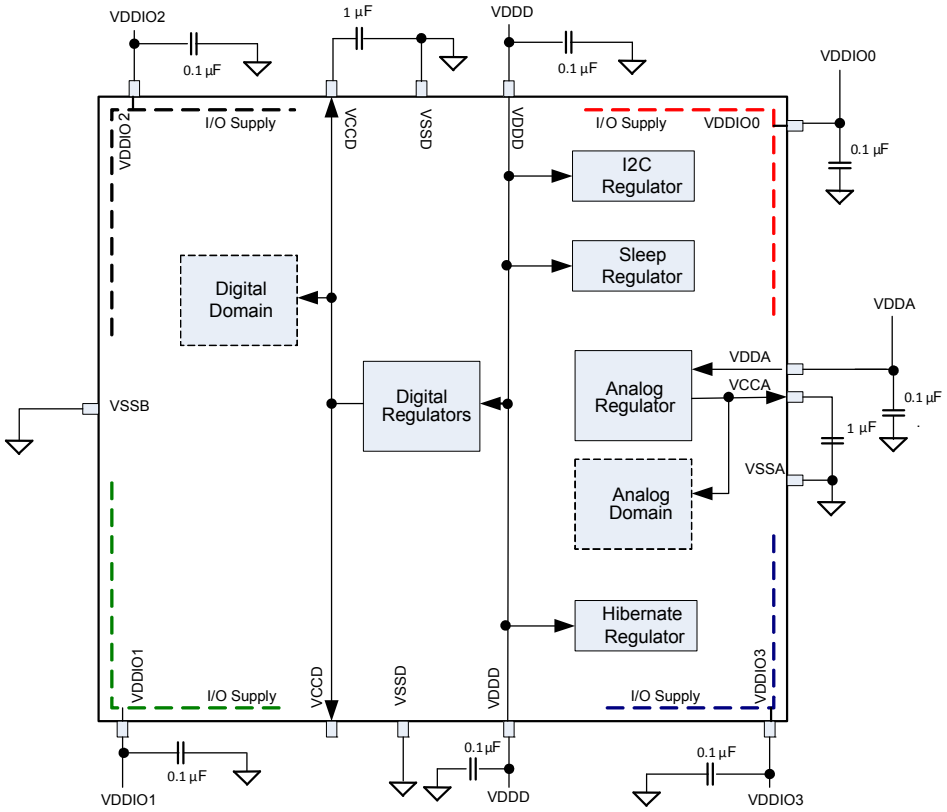
6.1.4 USB Clock Domain

The USB clock domain is unique in that it operates largely asynchronously from the main clock network. The USB logic contains a synchronous bus interface to the chip, while running on an asynchronous clock to process USB data. The USB logic requires a 48-MHz frequency. This frequency can be generated from different sources, including DSI clock at 48 MHz or doubled value of 24 MHz from internal oscillator, DSI signal, or crystal oscillator.

6.2 Power System

The power system consists of separate analog, digital, and I/O supply pins, labeled VDDA, VDDD, and VDDIOX, respectively. It also includes two internal 1.8 V regulators that provide the digital (VCCD) and analog (VCCA) supplies for the internal core logic. The output pins of the regulators (VCCD and VCCA) and the VDDIO pins must have capacitors connected as shown in Figure 6-4. The two V_{CCD} pins must be shorted together, with as short a trace as possible, and connected to a 1 µF ±10% X5R capacitor. The power system also contains a sleep regulator, an I^2C regulator, and a hibernate regulator.

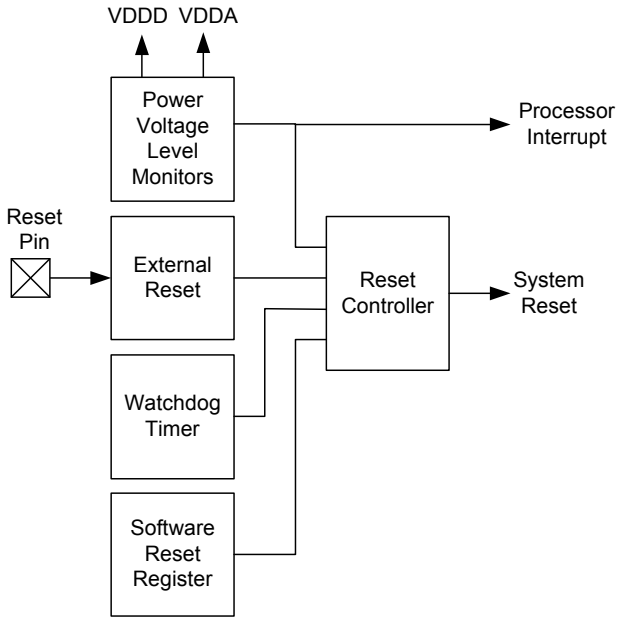
Figure 6-4. PSoC Power System



Notes

- The two V_{CCD} pins must be connected together with as short a trace as possible. A trace under the device is recommended, as shown in Figure 2-6.
- You can power the device in internally regulated mode, where the voltage applied to the V_{DDx} pins is as high as 5.5 V, and the internal regulators provide the core voltages. **In this mode, do not apply power to the V_{CCx} pins, and do not tie the V_{DDx} pins to the V_{CCx} pins.**
- You can also power the device in externally regulated mode, that is, by directly powering the V_{CCD} and V_{CCA} pins. In this configuration, the V_{DDD} pins should be shorted to the V_{CCD} pins and the V_{DDA} pin should be shorted to the V_{CCA} pin. The allowed supply range in this configuration is 1.71 V to 1.89 V. After power up in this configuration, the internal regulators are on by default, and should be disabled to reduce power consumption.
- It is good practice to check the datasheets for your bypass capacitors, specifically the working voltage and the DC bias specifications. With some capacitors, the actual capacitance can decrease considerably when the DC bias (V_{DDX} or V_{CCX} in Figure 6-4) is a significant percentage of the rated working voltage.

Figure 6-7. Resets



The term **system reset** indicates that the processor as well as analog and digital peripherals and registers are reset.

A reset status register shows some of the resets or power voltage monitoring interrupts. The program may examine this register to detect and report certain exception conditions. This register is cleared after a power-on reset. For details see the Technical Reference Manual.

6.3.1 Reset Sources

6.3.1.1 Power Voltage Level Monitors

- IPOR - Initial Power-on-Reset

  At initial power on, IPOR monitors the power voltages V_{DDD}, V_{DDA}, V_{CCD} and V_{CCA}. The trip level is not precise. It is set to approximately 1 volt (0.75 V to 1.45 V). This is below the lowest specified operating voltage but high enough for the internal circuits to be reset and to hold their reset state. The monitor generates a reset pulse that is at least 150 ns wide. It may be much wider if one or more of the voltages ramps up slowly.

  After boot, the IPOR circuit is disabled and voltage supervision is handed off to the precise low-voltage reset (PRES) circuit.

- PRES - Precise Low-Voltage Reset

  This circuit monitors the outputs of the analog and digital internal regulators after power up. The regulator outputs are compared to a precise reference voltage. The response to a PRES trip is identical to an IPOR reset.

  In normal operating mode, the program cannot disable the digital PRES circuit. The analog regulator can be disabled, which also disables the analog portion of the PRES. The PRES circuit is disabled automatically during sleep and hibernate modes, with one exception: During sleep mode the regulators are periodically activated (buzzed) to provide supervisory services and to reduce wakeup time. At these times the PRES circuit is also buzzed to allow periodic voltage monitoring.

- ALVI, DLVI, AHVI - Analog/Digital Low Voltage Interrupt, Analog High Voltage Interrupt

  Interrupt circuits are available to detect when VDDA and VDDD go outside a voltage range. For AHVI, VDDA is compared to a fixed trip level. For ALVI and DLVI, VDDA and VDDD are compared to trip levels that are programmable, as listed in Table 6-5. ALVI and DLVI can also be configured to generate a device reset instead of an interrupt.

Table 6-5. Analog/Digital Low Voltage Interrupt, Analog High Voltage Interrupt

Interrupt	Supply	Normal Voltage Range	Available Trip Settings
DLVI	VDDD	1.71 V-5.5 V	1.70 V-5.45 V in 250 mV increments
ALVI	VDDA	1.71 V-5.5 V	1.70 V-5.45 V in 250 mV increments
AHVI	VDDA	1.71 V-5.5 V	5.75 V

The monitors are disabled until after IPOR. During sleep mode these circuits are periodically activated (buzzed). If an interrupt occurs during buzzing then the system first enters its wakeup sequence. The interrupt is then recognized and may be serviced.

The buzz frequency is adjustable, and should be set to be less than the minimum time that any voltage is expected to be out of range. For details on how to adjust the buzz frequency, see the TRM.

6.3.1.2 Other Reset Sources

- XRES - External Reset

  PSoC 5LP has a dedicated XRES pin, which holds the part in reset while held active (low). The response to an XRES is the same as to an IPOR reset. The external reset is active low. It includes an internal pull-up resistor. XRES is active during sleep and hibernate modes.

  After XRES has been deasserted, at least 10 µs must elapse before it can be reasserted.

- SRES - Software Reset

  A reset can be commanded under program control by setting a bit in the software reset register. This is done either directly by the program or indirectly by DMA access. The response to a SRES is the same as after an IPOR reset.

  Another register bit exists to disable this function.

- WRES - Watchdog Timer Reset

  The watchdog reset detects when the software program is no longer being executed correctly. To indicate to the watchdog timer that it is running correctly, the program must periodically reset the timer. If the timer is not reset before a user-specified amount of time, then a reset is generated.

  Note IPOR disables the watchdog function. The program must enable the watchdog function at an appropriate point in the code by setting a register bit. When this bit is set, it cannot be cleared again except by an IPOR power on reset event.

6.4 I/O System and Routing

PSoC I/Os are extremely flexible. Every GPIO has analog and digital I/O capability. All I/Os have a large number of drive modes, which are set at POR. PSoC also provides up to four individual I/O voltage domains through the VDDIO pins.

There are two types of I/O pins on every device; those with USB provide a third type. Both general purpose I/O (GPIO) and special I/O (SIO) provide similar digital functionality. The primary differences are their analog capability and drive strength. Devices that include USB also provide two USBIO pins that support specific USB functionality as well as limited GPIO capability.

All I/O pins are available for use as digital inputs and outputs for both the CPU and digital peripherals. In addition, all I/O pins can generate an interrupt. The flexible and advanced capabilities of the PSoC I/O, combined with any signal to any pin routability, greatly simplify circuit design and board layout. All GPIO pins can be used for analog input, CapSense[9], and LCD segment drive, while SIO pins are used for voltages in excess of VDDA and for programmable output voltages.

- Features supported by both GPIO and SIO:
  - User programmable port reset state
  - Separate I/O supplies and voltages for up to four groups of I/O
  - Digital peripherals use DSI to connect the pins
  - Input or output or both for CPU and DMA
  - Eight drive modes
  - Every pin can be an interrupt source configured as rising edge, falling edge or both edges. If required, level sensitive interrupts are supported through the DSI
  - Dedicated port interrupt vector for each port
  - Slew rate controlled digital output drive mode
  - Access port control and configuration registers on either port basis or pin basis
  - Separate port read (PS) and write (DR) data registers to avoid read modify write errors
  - Special functionality on a pin by pin basis
- Additional features only provided on the GPIO pins:
  - LCD segment drive on LCD equipped devices
  - CapSense[9]
  - Analog input and output capability
  - Continuous 100 µA clamp current capability
  - Standard drive strength down to 1.71 V
- Additional features only provided on SIO pins:
  - Higher drive strength than GPIO
  - Hot swap capability (5 V tolerance at any operating VDD)
  - Programmable and regulated high input and output drive levels down to 1.2 V
  - No analog input, CapSense, or LCD capability
  - Over voltage tolerance up to 5.5 V
  - SIO can act as a general purpose analog comparator
- USBIO features:
  - Full speed USB 2.0 compliant I/O
  - Highest drive strength for general purpose use
  - Input, output, or both for CPU and DMA
  - Input, output, or both for digital peripherals
  - Digital output (CMOS) drive mode
  - Each pin can be an interrupt source configured as rising edge, falling edge, or both edges

Note
9. GPIOs with opamp outputs are not recommended for use with CapSense.

7. Digital Subsystem

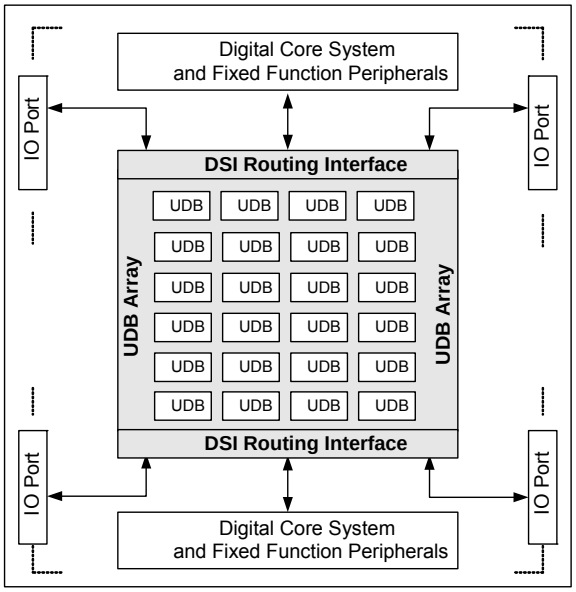
The digital programmable system creates application specific combinations of both standard and advanced digital peripherals and custom logic functions. These peripherals and logic are then interconnected to each other and to any pin on the device, providing a high level of design flexibility and IP security.

The features of the digital programmable system are outlined here to provide an overview of capabilities and architecture. You do not need to interact directly with the programmable digital system at the hardware and register level. PSoC Creator provides a high level schematic capture graphical interface to automatically place and route resources similar to PLDs.

The main components of the digital programmable system are:

- Universal Digital Blocks (UDB) - These form the core functionality of the digital programmable system. UDBs are a collection of uncommitted logic (PLD) and structural logic (Datapath) optimized to create all common embedded peripherals and customized functionality that are application or design specific.
- Universal Digital Block array - UDB blocks are arrayed within a matrix of programmable interconnect. The UDB array structure is homogeneous and allows for flexible mapping of digital functions onto the array. The array supports extensive and flexible routing interconnects between UDBs and the Digital System Interconnect.
- Digital System Interconnect (DSI) - Digital signals from Universal Digital Blocks (UDBs), fixed function peripherals, I/O pins, interrupts, DMA, and other system core signals are attached to the Digital System Interconnect to implement full featured device connectivity. The DSI allows any digital function to any pin or other feature routability when used with the Universal Digital Block array.

Figure 7-1. CY8C58LP Digital Programmable Architecture



7.1 Example Peripherals

The flexibility of the CY8C58LP family's UDBs and analog blocks allow the user to create a wide range of components (peripherals). The most common peripherals were built and characterized by Cypress and are shown in the PSoC Creator component catalog, however, users may also create their own custom components using PSoC Creator. Using PSoC Creator, users may also create their own components for reuse within their organization, for example sensor interfaces, proprietary algorithms, and display interfaces.

The number of components available through PSoC Creator is too numerous to list in the datasheet, and the list is always growing. An example of a component available for use in CY8C58LP family, but, not explicitly called out in this datasheet is the UART component.

7.1.1 Example Digital Components

The following is a sample of the digital components available in PSoC Creator for the CY8C58LP family. The exact amount of hardware resources (UDBs, routing, RAM, flash) used by a component varies with the features selected in PSoC Creator for the component.

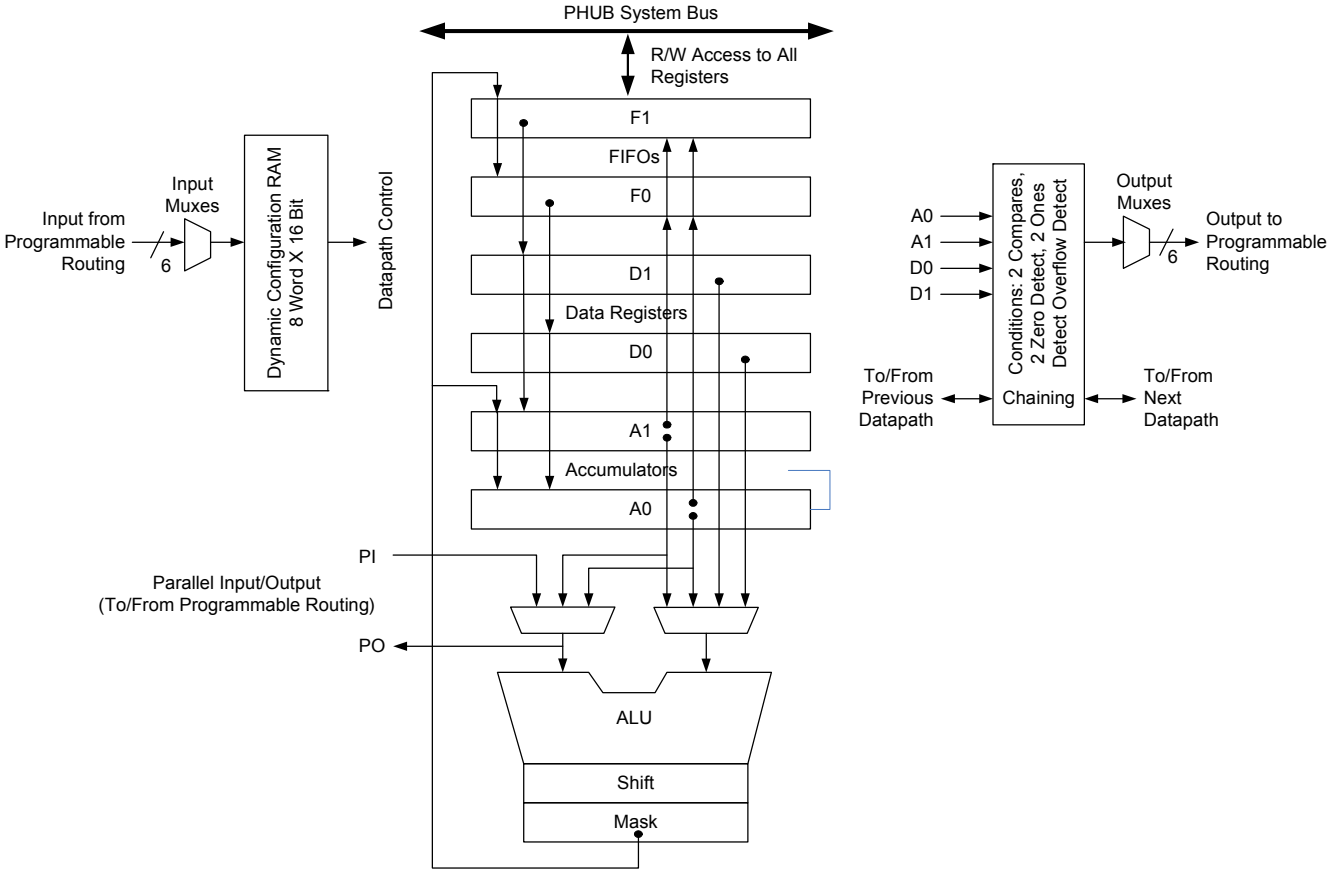
- Communications
  - I^2C
  - UART
  - SPI
- Functions
  - EMIF
  - PWMs
  - Timers
  - Counters
- Logic
  - NOT
  - OR
  - XOR
  - AND

7.1.2 Example Analog Components

The following is a sample of the analog components available in PSoC Creator for the CY8C58LP family. The exact amount of hardware resources (SC/CT blocks, routing, RAM, flash) used by a component varies with the features selected in PSoC Creator for the component.

- Amplifiers
  - TIA
  - PGA
  - opamp
- ADCs
  - Delta-Sigma
  - Successive Approximation (SAR)
- DACs
  - Current
  - Voltage
  - PWM
- Comparators
- Mixers

Figure 7-4. Datapath Top Level



7.2.2.1 Working Registers

The datapath contains six primary working registers, which are accessed by CPU firmware or DMA during normal operation.

Table 7-1. Working Datapath Registers

Name	Function	Description
A0 and A1	Accumulators	These are sources and sinks for the ALU and also sources for the compares.
D0 and D1	Data Registers	These are sources for the ALU and sources for the compares.
F0 and F1	FIFOs	These are the primary interface to the system bus. They can be a data source for the data registers and accumulators or they can capture data from the accumulators or ALU. Each FIFO is four bytes deep.

7.2.2.2 Dynamic Configuration RAM

Dynamic configuration is the ability to change the datapath function and internal configuration on a cycle-by-cycle basis, under sequencer control. This is implemented using the 8-word x 16-bit configuration RAM, which stores eight unique 16-bit wide configurations. The address input to this RAM controls the sequence, and can be routed from any block connected to the UDB routing matrix, most typically PLD logic, I/O pins, or from the outputs of this or other datapath blocks.

ALU

The ALU performs eight general purpose functions. They are:

- Increment
- Decrement
- Add
- Subtract
- Logical AND
- Logical OR
- Logical XOR
- Pass, used to pass a value through the ALU to the shift register, mask, or another UDB register

Independent of the ALU operation, these functions are available:

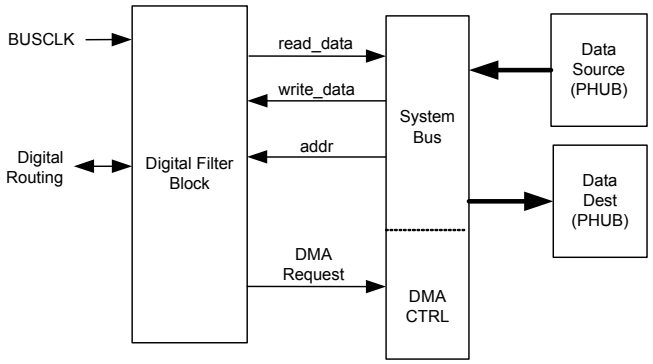
- Shift left
- Shift right
- Nibble swap
- Bitwise OR mask

7.9 Digital Filter Block

Some devices in the CY8C58LP family of devices have a dedicated HW accelerator block used for digital filtering. The DFB has a dedicated multiplier and accumulator that calculates a 24-bit by 24-bit multiply accumulate in one system clock cycle. This enables the mapping of a direct form FIR filter that approaches a computation rate of one FIR tap for each clock cycle. The MCU can implement any of the functions performed by this block, but at a slower rate that consumes significant MCU bandwidth.

The PSoC Creator interface provides a wizard to implement FIR and IIR digital filters with coefficients for LPF, BPF, HPF, Notch and arbitrary shape filters. 64 pairs of data and coefficients are stored. This enables a 64 tap FIR filter or up to 4 16 tap filters of either FIR or IIR formulation.

Figure 7-20. DFB Application Diagram (pwr/gnd not shown)



The typical use model is for data to be supplied to the DFB over the system bus from another on-chip system data source such as an ADC. The data typically passes through main memory or is directly transferred from another chip resource through DMA. The DFB processes this data and passes the result to another on chip resource such as a DAC or main memory through DMA on the system bus.

Data movement in or out of the DFB is typically controlled by the system DMA controller but can be moved directly by the MCU.

8. Analog Subsystem

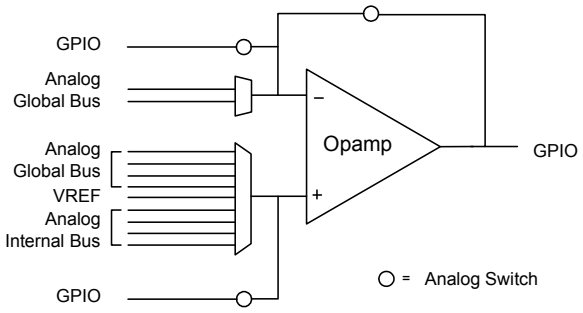
The analog programmable system creates application specific combinations of both standard and advanced analog signal processing blocks. These blocks are then interconnected to each other and also to any pin on the device, providing a high level of design flexibility and IP security. The features of the analog subsystem are outlined here to provide an overview of capabilities and architecture.

- Flexible, configurable analog routing architecture provided by analog globals, analog mux bus, and analog local buses
- High resolution Delta-Sigma ADC
- Two successive approximation (SAR) ADCs
- Four 8-bit DACs that provide either voltage or current output
- Four comparators with optional connection to configurable LUT outputs
- Four configurable switched capacitor/continuos time (SC/CT) blocks for functions that include opamp, unity gain buffer, programmable gain amplifier, transimpedance amplifier, and mixer
- Four opamps for internal use and connection to GPIO that can be used as high current output buffers
- CapSense subsystem to enable capacitive touch sensing
- Precision reference for generating an accurate analog voltage for internal analog blocks

8.5 Opamps

The CY8C58LP family of devices contain four general purpose opamps.

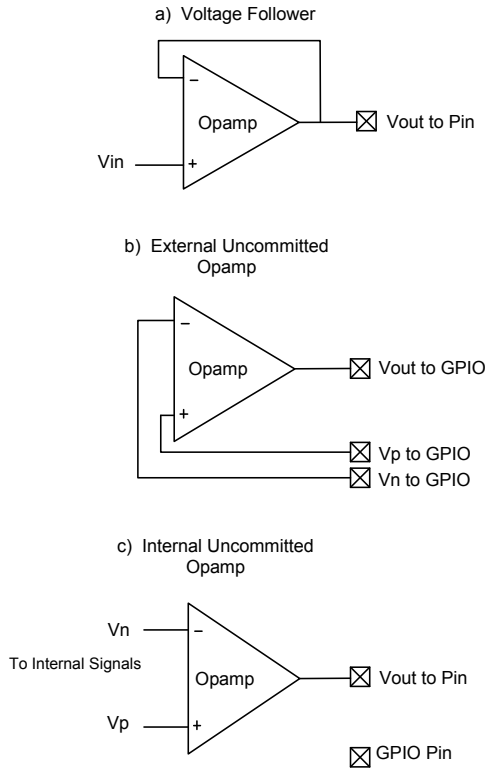
Figure 8-7. Opamp



The opamp is uncommitted and can be configured as a gain stage or voltage follower on external or internal signals.

See Figure 8-8. In any configuration, the input and output signals can all be connected to the internal global signals and monitored with an ADC, or comparator. The configurations are implemented with switches between the signals and GPIO pins.

Figure 8-8. Opamp Configurations



The opamp has three speed modes, slow, medium, and fast. The slow mode consumes the least amount of quiescent power and the fast mode consumes the most power. The inputs are able to swing rail-to-rail. The output swing is capable of rail-to-rail operation at low current output, within 50 mV of the rails. When driving high current loads (about 25 mA) the output voltage may only get within 500 mV of the rails.

8.6 Programmable SC/CT Blocks

The CY8C58LP family of devices contains four switched capacitor/continuous time (SC/CT) blocks. Each switched capacitor/continuous time block is built around a single rail-to-rail high bandwidth opamp.

Switched capacitor is a circuit design technique that uses capacitors plus switches instead of resistors to create analog functions. These circuits work by moving charge between capacitors by opening and closing different switches. Nonoverlapping in phase clock signals control the switches, so that not all switches are ON simultaneously.

The PSoC Creator tool offers a user friendly interface, which allows you to easily program the SC/CT blocks. Switch control and clock phase control configuration is done by PSoC Creator so users only need to determine the application use parameters such as gain, amplifier polarity, V_{REF} connection, and so on.

The same opamps and block interfaces are also connectable to an array of resistors which allows the construction of a variety of continuous time functions.

The opamp and resistor array is programmable to perform various analog functions including

- Naked Operational Amplifier - Continuous Mode
- Unity-Gain Buffer - Continuous Mode
- Programmable Gain Amplifier (PGA) - Continuous Mode
- Transimpedance Amplifier (TIA) - Continuous Mode
- Up/Down Mixer - Continuous Mode
- Sample and Hold Mixer (NRZ S/H) - Switched Cap Mode
- First Order Analog to Digital Modulator - Switched Cap Mode

8.6.1 Naked Opamp

The Naked Opamp presents both inputs and the output for connection to internal or external signals. The opamp has a unity gain bandwidth greater than 6.0 MHz and output drive current up to 650 µA. This is sufficient for buffering internal signals (such as DAC outputs) and driving external loads greater than 7.5 kohms.

8.6.2 Unity Gain

The Unity Gain buffer is a Naked Opamp with the output directly connected to the inverting input for a gain of 1.00. It has a -3 dB bandwidth greater than 6.0 MHz.

8.6.3 PGA

The PGA amplifies an external or internal signal. The PGA can be configured to operate in inverting mode or noninverting mode. The PGA function may be configured for both positive and negative gains as high as 50 and 49 respectively. The gain is adjusted by changing the values of R1 and R2 as illustrated in Figure 8-9. The schematic in Figure 8-9 shows the configuration and possible resistor settings for the PGA. The gain is switched from inverting and non inverting by changing the shared select value of the both the input muxes. The bandwidth for each gain case is listed in Table 8-3.

8.7.1 LCD Segment Pin Driver

Each GPIO pin contains an LCD driver circuit. The LCD driver buffers the appropriate output of the LCD DAC to directly drive the glass of the LCD. A register setting determines whether the pin is a common or segment. The pin's LCD driver then selects one of the six bias voltages to drive the I/O pin, as appropriate for the display data.

8.7.2 Display Data Flow

The LCD segment driver system reads display data and generates the proper output voltages to the LCD glass to produce the desired image. Display data resides in a memory buffer in the system SRAM. Each time you need to change the common and segment driver voltages, the next set of pixel data moves from the memory buffer into the Port Data Registers via DMA.

8.7.3 UDB and LCD Segment Control

A UDB is configured to generate the global LCD control signals and clocking. This set of signals is routed to each LCD pin driver through a set of dedicated LCD global routing channels. In addition to generating the global LCD control signals, the UDB also produces a DMA request to initiate the transfer of the next frame of LCD data.

8.7.4 LCD DAC

The LCD DAC generates the contrast control and bias voltage for the LCD system. The LCD DAC produces up to five LCD drive voltages plus ground, based on the selected bias ratio. The bias voltages are driven out to GPIO pins on a dedicated LCD bias bus, as required.

8.8 CapSense

The CapSense system provides a versatile and efficient means for measuring capacitance in applications such as touch sense buttons, sliders, proximity detection, etc. The CapSense system uses a configuration of system resources, including a few hardware functions primarily targeted for CapSense. Specific resource usage is detailed in the CapSense component in PSoC Creator.

A capacitive sensing method using a Delta-Sigma Modulator (CSD) is used. It provides capacitance sensing using a switched capacitor technique with a delta-sigma modulator to convert the sensing current to a digital code.

8.9 Temp Sensor

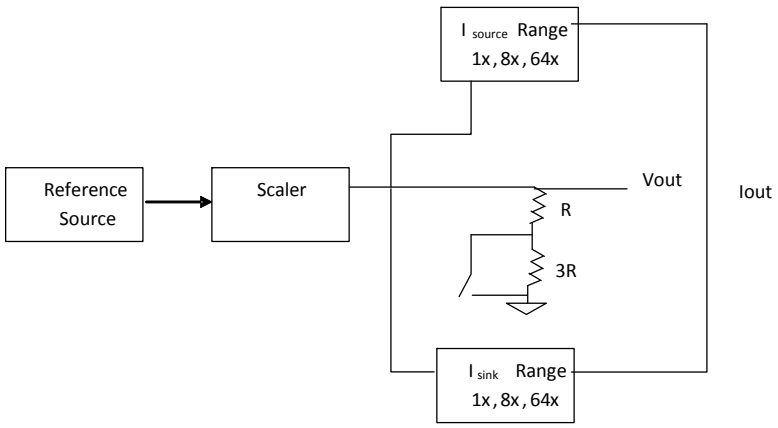
Die temperature is used to establish programming parameters for writing flash. Die temperature is measured using a dedicated sensor based on a forward biased transistor. The temperature sensor has its own auxiliary ADC.

8.10 DAC

The CY8C58LP parts contain four Digital to Analog Convertors (DACs). Each DAC is 8-bit and can be configured for either voltage or current output. The DACs support CapSense, power supply regulation, and waveform generation. Each DAC has the following features.

- Adjustable voltage or current output in 255 steps
- Programmable step size (range selection)
- Eight bits of calibration to correct ± 25% of gain error
- Source and sink option for current output
- 8 Msps conversion rate for current output
- 1 Msps conversion rate for voltage output
- Monotonic in nature
- Data and strobe inputs can be provided by the CPU or DMA, or routed directly from the DSI
- Dedicated low-resistance output pin for high-current mode

Figure 8-12. DAC Block Diagram



8.10.1 Current DAC

The current DAC (IDAC) can be configured for the ranges 0 to 31.875 µA, 0 to 255 µA, and 0 to 2.04 mA. The IDAC can be configured to source or sink current.

8.10.2 Voltage DAC

For the voltage DAC (VDAC), the current DAC output is routed through resistors. The two ranges available for the VDAC are 0 to 1.02 V and 0 to 4.08 V. In voltage mode any load connected to the output of a DAC should be purely capacitive (the output of the VDAC is not buffered).

11. Electrical Specifications

Specifications are valid for –40 °C ≤ T_A ≤ 105 °C and T_J ≤ 120 °C, except where noted. Specifications are valid for 1.71 V to 5.5 V, except where noted. The unique flexibility of the PSoC UDBs and analog blocks enable many functions to be implemented in PSoC Creator components, see the component datasheets for full AC/DC specifications of individual functions. See the Example Peripherals on page 40 for further explanation of PSoC Creator components.

11.1 Absolute Maximum Ratings

Table 11-1. Absolute Maximum Ratings DC Specifications[14]

Parameter	Description	Conditions	Min	Typ	Max	Units
V_{DDA}	Analog supply voltage relative to V_{SSA}		–0.5	–	6	V
V_{DDD}	Digital supply voltage relative to V_{SSD}		–0.5	–	6	V
V_{DDIO}	I/O supply voltage relative to V_{SSD}		–0.5	–	6	V
V_{CCA}	Direct analog core voltage input		–0.5	–	1.95	V
V_{CCD}	Direct digital core voltage input		–0.5	–	1.95	V
V_{SSA}	Analog ground voltage		V_{SSD} – 0.5	–	V_{SSD} + 0.5	V
V_{GPIO}[15]	DC input voltage on GPIO	Includes signals sourced by V_{DDA} and routed internal to the pin.	V_{SSD} – 0.5	–	V_{DDIO} + 0.5	V
V_{SIO}	DC input voltage on SIO	Output disabled	V_{SSD} – 0.5	–	7	V
		Output enabled	V_{SSD} – 0.5	–	6	V
V_{IND}	Voltage at boost converter input		0.5	–	5.5	V
V_{BAT}	Boost converter supply		V_{SSD} – 0.5	–	5.5	V
I_{VDDIO}	Current per V_{DDIO} supply pin		–	–	100	mA
I_{GPIO}	GPIO current		–30	–	41	mA
I_{SIO}	SIO current		–49	–	28	mA
I_{USBIO}	USBIO current		–56	–	59	mA
V_{EXTREF}	ADC external reference inputs	Pins P0[3], P3[2]	–	–	2	V
LU	Latch up current[16]		–140	–	140	mA
ESD_{HBM}	Electrostatic discharge voltage	Human body model	2000	–	–	V
ESD_{CDM}	ESD voltage	Charge device model	500	–	–	V

Notes
14. Usage above the absolute maximum conditions listed in Table 11-1 may cause permanent damage to the device. Exposure to Absolute Maximum conditions for extended periods of time may affect device reliability. The Maximum Storage Temperature is 150 °C in compliance with JEDEC Standard JESD22-A103, High Temperature Storage Life. When used below Absolute Maximum conditions but above normal operating conditions, the device may not operate to specification.
15. The V_{DDIO} supply voltage must be greater than the maximum voltage on the associated GPIO pins. Maximum voltage on GPIO pin ≤ V_{DDIO} ≤ V_{DDA}.
16. Meets or exceeds JEDEC Spec EIA/JESD78 IC Latch-up Test.

11.5 Analog Peripherals

Specifications are valid for –40 °C ≤ T_A ≤ 105 °C and T_J ≤ 120 °C, except where noted. Specifications are valid for 1.71 V to 5.5 V, except where noted.

11.5.1 Opamp

Table 11-18. Opamp DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
V_I	Input voltage range		V_{SSA}	–	V_{DDA}	V
Vos	Input offset voltage		–	–	2.5	mV
		Operating temperature –40 °C to 70 °C	–	–	2	mV
TCVos	Input offset voltage drift with temperature	Power mode = high	–	–	±30	µV / °C
Ge1	Gain error, unity gain buffer mode	Rload = 1 kΩ	–	–	±0.1	%
Cin	Input capacitance	Routing from pin	–	–	18	pF
Vo	Output voltage range	1 mA, source or sink, power mode = high	V_{SSA} + 0.05	–	V_{DDA} – 0.05	V
Iout	Output current capability, source or sink	V_{SSA} + 500 mV ≤ V_{OUT} ≤ V_{DDA} –500 mV, V_{DDA} > 2.7 V	25	–	–	mA
		V_{SSA} + 500 mV ≤ V_{OUT} ≤ V_{DDA} –500 mV, 1.7 V = V_{DDA} ≤ 2.7 V	16	–	–	mA
Idd	Quiescent current[43]	Power mode = min	–	250	400	uA
		Power mode = low	–	250	400	uA
		Power mode = med	–	330	950	uA
		Power mode = high	–	1000	2500	uA
CMRR	Common mode rejection ratio[43]		80	–	–	dB
PSRR	Power supply rejection ratio[43]	V_{DDA} ≥ 2.7 V	85	–	–	dB
		V_{DDA} < 2.7 V	70	–	–	dB
I_{IB}	Input bias current[43]	25 °C	–	10	–	pA

Figure 11-25. Opamp Vos Histogram, 7020 samples/1755 parts, 30 °C, VDDA = 3.3 V

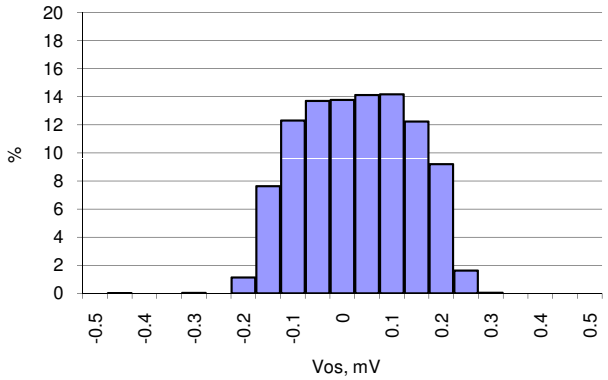
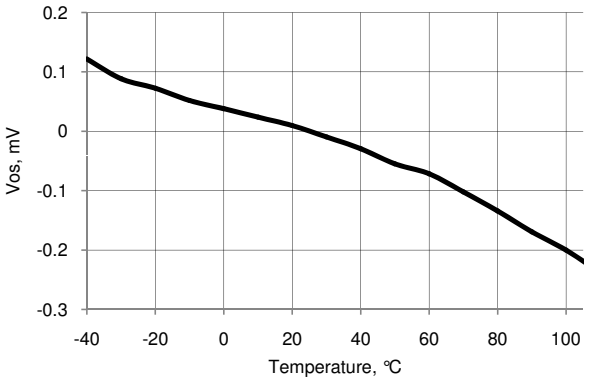


Figure 11-26. Opamp Vos vs Temperature, V_{DDA} = 5 V



Note
43. Based on device characterization (Not production tested).

Table 11-34. IDAC DC Specifications (continued)

Parameter	Description	Conditions	Min	Typ	Max	Units
DNL	Differential nonlinearity	Sink mode, range = 255 µA, Rload = 2.4 kΩ, Cload = 15 pF	–	±0.3	±1	LSB
		Source mode, range = 255 µA, Rload = 2.4 kΩ, Cload = 15 pF	–	±0.3	±1	LSB
		Source mode, range = 31.875 µA, Rload = 20 kΩ, Cload = 15 pF[61]	–	±0.2	±1	LSB
		Sink mode, range = 31.875 µA, Rload = 20 kΩ, Cload = 15 pF[61]	–	±0.2	±1	LSB
		Source mode, range = 2.0 4 mA, Rload = 600 Ω, Cload = 15 pF[61]	–	±0.2	±1	LSB
		Sink mode, range = 2.0 4 mA, Rload = 600 Ω, Cload = 15 pF[61]	–	±0.2	±1	LSB
Vcompliance	Dropout voltage, source or sink mode	Voltage headroom at max current, Rload to V_{DDA} or Rload to V_{SSA}, V_{DIFF} from V_{DDA}	1	–	–	V
I_{DD}	Operating current, code = 0	Slow mode, source mode, range = 31.875 µA	–	44	100	µA
		Slow mode, source mode, range = 255 µA,	–	33	100	µA
		Slow mode, source mode, range = 2.04 mA	–	33	100	µA
		Slow mode, sink mode, range = 31.875 µA	–	36	100	µA
		Slow mode, sink mode, range = 255 µA	–	33	100	µA
		Slow mode, sink mode, range = 2.04 mA	–	33	100	µA
		Fast mode, source mode, range = 31.875 µA	–	310	500	µA
		Fast mode, source mode, range = 255 µA	–	305	500	µA
		Fast mode, source mode, range = 2.04 mA	–	305	500	µA
		Fast mode, sink mode, range = 31.875 µA	–	310	500	µA
		Fast mode, sink mode, range = 255 µA	–	300	500	µA
		Fast mode, sink mode, range = 2.04 mA	–	300	500	µA

Note
61. Based on device characterization (Not production tested).

11.6.6 Digital Filter Block

Table 11-57. DFB DC Specifications[78]

Parameter	Description	Conditions	Min	Typ	Max	Units
	DFB operating current	64-tap FIR at F_{DFB}				
		500 kHz (6.7 ksps)	–	0.16	0.27	mA
		1 MHz (13.4 ksps)	–	0.33	0.53	mA
		10 MHz (134 ksps)	–	3.3	5.3	mA
		48 MHz (644 ksps)	–	15.7	25.5	mA
		80 MHz (1.07 Msps)	–	26.0	42.5	mA

Table 11-58. DFB AC Specifications[78]

Parameter	Description	Conditions	Min	Typ	Max	Units
F_{DFB}	DFB operating frequency		DC	–	80.01	MHz

11.6.7 USB

Table 11-59. USB DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
V_{USB_5}	Device supply (V_{DDD}) for USB operation	USB configured, USB regulator enabled	4.35	–	5.25	V
$V_{USB\_3.3}$		USB configured, USB regulator bypassed	3.15	–	3.6	V
V_{USB_3}		USB configured, USB regulator bypassed[78]	2.85	–	3.6	V
$I_{USB\_Configured}$	Device supply current in device active mode, bus clock and IMO = 24 MHz	V_{DDD} = 5 V, F_{CPU} = 1.5 MHz	–	10	–	mA
		V_{DDD} = 3.3 V, F_{CPU} = 1.5 MHz	–	8	–	mA
$I_{USB\_Suspended}$	Device supply current in device sleep mode	V_{DDD} = 5 V, connected to USB host, PICU configured to wake on USB resume signal	–	0.5	–	mA
		V_{DDD} = 5 V, disconnected from USB host	–	0.3	–	mA
		V_{DDD} = 3.3 V, connected to USB host, PICU configured to wake on USB resume signal	–	0.5	–	mA
		V_{DDD} = 3.3 V, disconnected from USB host	–	0.3	–	mA

Note
78. Rise/fall time matching (TR) not guaranteed, see Table 11-15 on page 84.

11.8.5 SWD Interface

Figure 11-80. SWD Interface Timing

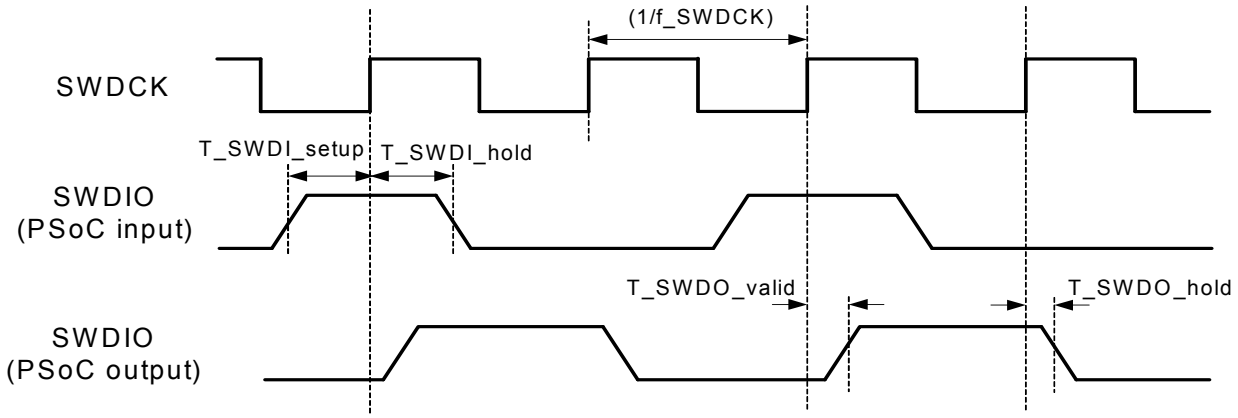


Table 11-77. SWD Interface AC Specifications[95]

Parameter	Description	Conditions	Min	Typ	Max	Units
f_SWDCK	SWDCLK frequency	3.3 V ≤ V_{DDD} ≤ 5 V	–	–	12[96]	MHz
		1.71 V ≤ V_{DDD} < 3.3 V	–	–	7[96]	MHz
		1.71 V ≤ V_{DDD} < 3.3 V, SWD over USBIO pins	–	–	5.5[96]	MHz
T_SWDI_setup	SWDIO input setup before SWDCK high	T = 1/f_SWDCK max	T/4	–	–	
T_SWDI_hold	SWDIO input hold after SWDCK high	T = 1/f_SWDCK max	T/4	–	–	
T_SWDO_valid	SWDCK high to SWDIO output	T = 1/f_SWDCK max	–	–	T/2	
T_SWDO_hold	SWDIO output hold after SWDCK high	T = 1/f_SWDCK max	1	–	–	ns

11.8.6 TPIU Interface

Table 11-78. TPIU Interface AC Specifications[95]

Parameter	Description	Conditions	Min	Typ	Max	Units
	TRACEPORT (TRACECLK) frequency		–	–	33[97]	MHz
	SWV bit rate		–	–	33[97]	Mbit

Notes
95. Based on device characterization (Not production tested).
96. f_SWDCK must also be no more than 1/3 CPU clock frequency.
97. TRACEPORT signal frequency and bit rate are limited by GPIO output frequency, see Table 11-9 on page 77.

11.9.3 MHz External Crystal Oscillator

For more information on crystal or ceramic resonator selection for the MHzECO, refer to application note AN54439: PSoC 3 and PSoC 5 External Oscillators.

Table 11-83. MHzECO DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
I_{CC}	Operating current[104]	13.56 MHz crystal	–	3.8	–	mA

Table 11-84. MHzECO AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
F	Crystal frequency range		4	–	25	MHz

11.9.4 kHz External Crystal Oscillator

Table 11-85. kHzECO DC Specifications[104]

Parameter	Description	Conditions	Min	Typ	Max	Units
I_{CC}	Operating current	Low power mode; CL = 6 pF	–	0.25	1.0	µA
DL	Drive level		–	–	1	µW

Table 11-86. kHzECO AC Specifications[104]

Parameter	Description	Conditions	Min	Typ	Max	Units
F	Frequency		–	32.768	–	kHz
T_{ON}	Startup time	High power mode	–	1	–	s

11.9.5 External Clock Reference

Table 11-87. External Clock Reference AC Specifications[104]

Parameter	Description	Conditions	Min	Typ	Max	Units
	External frequency range		0	–	33	MHz
	Input duty cycle range	Measured at $V_{DDIO}/2$	30	50	70	%
	Input edge rate	V_{IL} to V_{IH}	0.5	–	–	V/ns

11.9.6 Phase-Locked Loop

Table 11-88. PLL DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
I_{DD}	PLL operating current	In = 3 MHz, Out = 80 MHz	–	650	–	µA
		In = 3 MHz, Out = 67 MHz	–	400	–	µA
		In = 3 MHz, Out = 24 MHz	–	200	–	µA

Table 11-89. PLL AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
Fpllin	PLL input frequency[105]		1	–	48	MHz
	PLL intermediate frequency[106]	Output of prescaler	1	–	3	MHz
Fpllout	PLL output frequency[105]		24	–	80	MHz
	Lock time at startup		–	–	250	µs
Jperiod-rms	Jitter (rms)[104]		–	–	250	ps

Notes
104.Based on device characterization (Not production tested).
105.This specification is guaranteed by testing the PLL across the specified range using the IMO as the source for the PLL.
106.PLL input divider, Q, must be set so that the input frequency is divided down to the intermediate frequency range. Value for Q ranges from 1 to 16.

12. Ordering Information

In addition to the features listed in Table 12-1, every CY8C58LP device includes: up to 256 KB flash, 64 KB SRAM, 2 KB EEPROM, a precision on-chip voltage reference, precision oscillators, flash, ECC, DMA, a fixed function I^2C, JTAG/SWD programming and debug, external memory interface, boost, and more. In addition to these features, the flexible UDBs and analog subsection support a wide range of peripherals. To assist you in selecting the ideal part, PSoC Creator makes a part recommendation after you choose the components required by your application. All CY8C58LP derivatives incorporate device and flash security in user-selectable security levels; see the TRM for details.

Table 12-1. CY8C58LP Family with ARM Cortex-M3 CPU

Part Number	MCU Core				Analog								Digital				I/O[109]				Package	JTAG ID[110]
	CPU SPEED (MHZ)	FLASH (KB)	SRAM (KB)	EEPROM (KB)	LCD SEGMENT DRIVE	ADCS	DAC	COMPARATORS	SC/CT ANALOG BLOCKS[107]	OPAMPS	DFB	CAPSENSE	UDBS[108]	16-BIT TIMER/PWM	FS USB	CAN 2.0B	TOTAL I/O	GPIO	SIO	USBIO		
CY8C5868AXI-LP031	67	256	64	2	✔	1x20-bit Del-Sig 2x12-bit SAR	4	4	4	4	✔	✔	24	4	–	–	70	62	8	0	100-TQFP	0x2E11F069
CY8C5868AXI-LP032	67	256	64	2	✔	1x20-bit Del-Sig 2x12-bit SAR	4	4	4	4	✔	✔	24	4	✔	–	72	62	8	2	100-TQFP	0x2E120069
CY8C5868AXI-LP035	67	256	64	2	✔	1x20-bit Del-Sig 2x12-bit SAR	4	4	4	4	✔	✔	24	4	✔	✔	72	62	8	2	100-TQFP	0x2E123069
CY8C5868LTI-LP036	67	256	64	2	✔	1x20-bit Del-Sig 2x12-bit SAR	4	4	4	4	✔	✔	24	4	–	–	46	38	8	0	68-QFN	0x2E124069
CY8C5868LTI-LP038	67	256	64	2	✔	1x20-bit Del-Sig 2x12-bit SAR	4	4	4	4	✔	✔	24	4	✔	–	48	38	8	2	68-QFN	0x2E126069
CY8C5868LTI-LP039	67	256	64	2	✔	1x20-bit Del-Sig 2x12-bit SAR	4	4	4	4	✔	✔	24	4	✔	✔	48	38	8	2	68-QFN	0x2E127069
CY8C5867AXI-LP023	67	128	32	2	✔	1x20-bit Del-Sig 1x12-bit SAR	4	4	4	4	✔	✔	24	4	–	–	70	62	8	0	100-TQFP	0x2E117069
CY8C5867AXI-LP024	67	128	32	2	✔	1x20-bit Del-Sig 1x12-bit SAR	4	4	4	4	✔	✔	24	4	✔	–	72	62	8	2	100-TQFP	0x2E118069
CY8C5867LTI-LP025	67	128	32	2	✔	1x20-bit Del-Sig 1x12-bit SAR	4	4	4	4	✔	✔	24	4	–	–	46	38	8	0	68-QFN	0x2E119069
CY8C5867LTI-LP028	67	128	32	2	✔	1x20-bit Del-Sig 1x12-bit SAR	4	4	4	4	✔	✔	24	4	✔	–	48	38	8	2	68-QFN	0x2E11C069
CY8C5866AXI-LP020	67	64	16	2	✔	1x20-bit Del-Sig 1x12-bit SAR	4	4	4	4	✔	✔	20	4	✔	✔	72	62	8	2	100-TQFP	0x2E114069
CY8C5866AXI-LP021	67	64	16	2	✔	1x20-bit Del-Sig 1x12-bit SAR	4	4	4	4	✔	✔	20	4	✔	–	72	62	8	2	100-TQFP	0x2E115069
CY8C5866LTI-LP022	67	64	16	2	✔	1x20-bit Del-Sig 1x12-bit SAR	4	4	4	4	✔	✔	20	4	✔	–	48	38	8	2	68-QFN	0x2E116069
CY8C5888AXI-LP096	80	256	64	2	✔	1x20-bit Del-Sig 2x12-bit SAR	4	4	4	4	✔	✔	24	4	✔	✔	72	62	8	2	100-TQFP	0x2E160069
CY8C5888AXQ-LP096	80	256	64	2	✔	1x20-bit Del-Sig 2x12-bit SAR	4	4	4	4	✔	✔	24	4	✔	✔	72	62	8	2	100-TQFP	0x2E160069
CY8C5888LTI-LP097	80	256	64	2	✔	1x20-bit Del-Sig 2x12-bit SAR	4	4	4	4	✔	✔	24	4	✔	✔	48	38	8	2	68-QFN	0x2E161069
CY8C5888LTQ-LP097	80	256	64	2	✔	1x20-bit Del-Sig 2x12-bit SAR	4	4	4	4	✔	✔	24	4	✔	✔	48	38	8	2	68-QFN	0x2E161069
CY8C5888FNI-LP210	80	256	64	2	✔	1x20-bit Del-Sig 2x12-bit SAR	4	4	4	4	✔	✔	24	4	✔	✔	72	62	8	2	99-WLCSP	0x2E1D2069
CY8C5888FNI-LP214	80	256	64	2	✔	1x20-bit Del-Sig 2x12-bit SAR	4	4	4	4	✔	✔	24	4	✔	–	72	62	8	2	99-WLCSP	0x2E1D6069

Notes

107. Analog blocks support a wide variety of functionality including TIA, PGA, and mixers. See Example Peripherals on page 40 for more information on how analog blocks can be used.
108. UDBs support a wide variety of functionality including SPI, LIN, UART, timer, counter, PWM, PRS, and others. Individual functions may use a fraction of a UDB or multiple UDBs. Multiple functions can share a single UDB. See Example Peripherals on page 40 for more information on how UDBs can be used.
109. The I/O Count includes all types of digital I/O: GPIO, SIO, and the two USB I/O. See "I/O System and Routing" section on page 33 for details on the functionality of each of these types of I/O.
110. The JTAG ID has three major fields. The most significant nibble (left digit) is the version, followed by a 2 byte part number and a 3 nibble manufacturer ID.

Document History Page (continued)

Description Title: PSoC® 5LP: CY8C58LP Family Datasheet Programmable System-on-Chip (PSoC®) Document Number: 001-84932				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
*J	5030641	MKEA	11/30/2015	Added Table 2-1. Removed the configurable XRES information. Updated *Section 5.6* Updated *Section 6.3.1.1*. Updated values for DSI Fmax, Fgpioin max, and Fsioin max. Corrected the web link for the PSoC 5 Device Programming Specifications in *Section 9.* Updated CSP Package Bootloader section. Added MHzECO DC Specifications. Updated 99-WLCSP and 100-pin TQFP package drawings. Added a footnote reference for the "CY8C5287AXI-LP095" part in Table 12-1 clarifying that it has 256 KB flash. Added the CY8C5667AXQ-LP040 part in Table 12-1.
*K	5478402	MKEA	10/25/2016	Updated More Information. Add Links to CAD Libraries in *Section 2.* Corrected typos in External Electrical Connections.
*L	5703770	GNKK	04/20/2017	Updated the Cypress logo and copyright information.