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### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	67MHz
Connectivity	I <sup>2</sup> C, LINbus, SPI, UART/USART, USB
Peripherals	CapSense, DMA, LCD, POR, PWM, WDT
Number of I/O	62
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 5.5V
Data Converters	A/D 1x20b, 1x12b; D/A 4x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/infineon-technologies/cy8c5867axi-lp024">https://www.e-xfl.com/product-detail/infineon-technologies/cy8c5867axi-lp024</a>

### More Information

Cypress provides a wealth of data at [www.cypress.com](http://www.cypress.com) to help you to select the right PSoC device for your design, and to help you to quickly and effectively integrate the device into your design. For a comprehensive list of resources, see the knowledge base article [KBA86521](#), [How to Design with PSoC 3](#), [PSoC 4](#), and [PSoC 5LP](#). Following is an abbreviated list for PSoC 5LP:

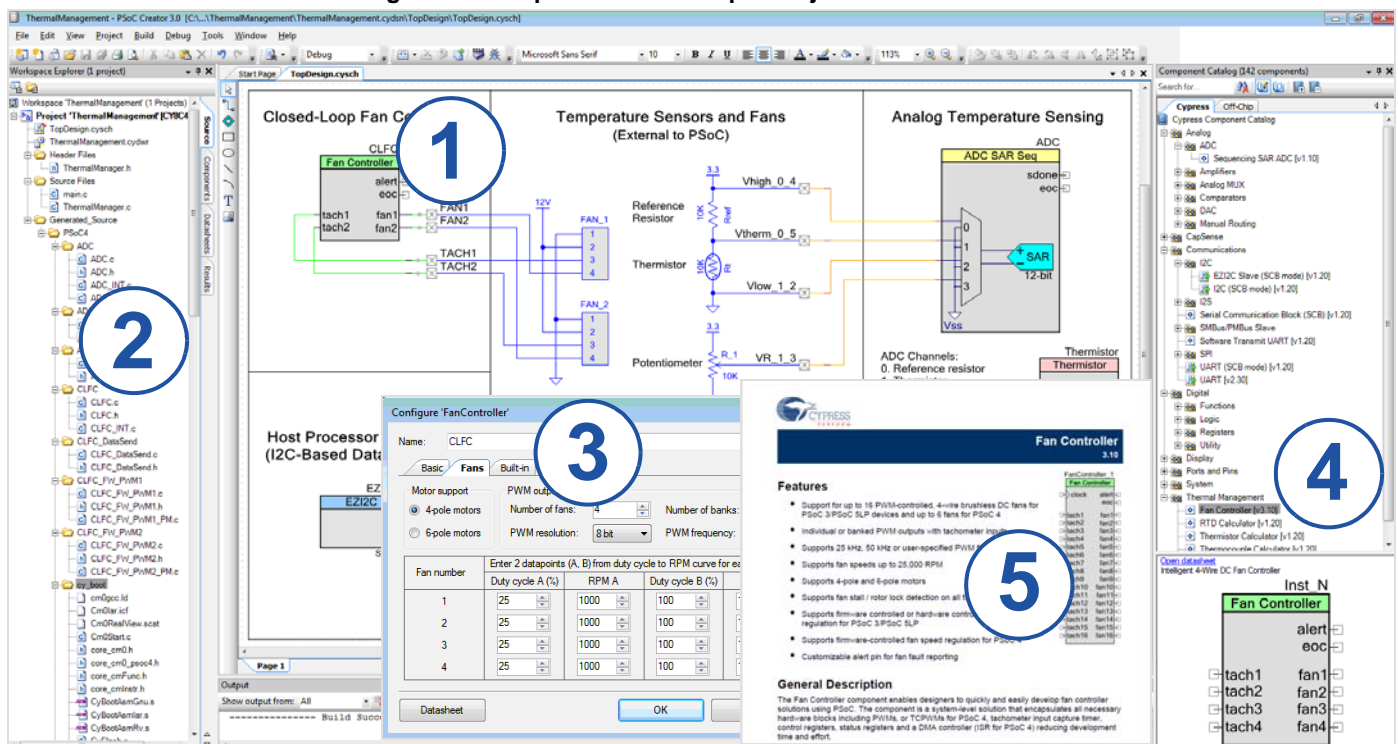
- Overview: [PSoC Portfolio](#), [PSoC Roadmap](#)
- Product Selectors: [PSoC 1](#), [PSoC 3](#), [PSoC 4](#), [PSoC 5LP](#)  
In addition, PSoC Creator includes a device selection tool.
- Application notes: Cypress offers a large number of PSoC application notes and [code examples](#) covering a broad range of topics, from basic to advanced level. Recommended application notes for getting started with PSoC 5LP are:
  - [AN77759](#): Getting Started With PSoC 5LP
  - [AN77835](#): PSoC 3 to PSoC 5LP Migration Guide
  - [AN61290](#): Hardware Design Considerations
  - [AN57821](#): Mixed Signal Circuit Board Layout
  - [AN58304](#): Pin Selection for Analog Designs
  - [AN81623](#): Digital Design Best Practices
  - [AN73854](#): Introduction To Bootloaders
- Development Kits:
  - [CY8CKIT-059](#) is a low-cost platform for prototyping, with a unique snap-away programmer and debugger on the USB connector.
  - [CY8CKIT-050](#) is designed for analog performance, for developing high-precision analog, low-power, and low-voltage applications.
  - [CY8CKIT-001](#) provides a common development platform for any one of the PSoC 1, PSoC 3, PSoC 4, or PSoC 5LP families of devices.
  - The [MiniProg3](#) device provides an interface for flash programming and debug.
- Technical Reference Manuals (TRM)
  - [Architecture TRM](#)
  - [Registers TRM](#)
- [Programming Specification](#)

### PSoC Creator

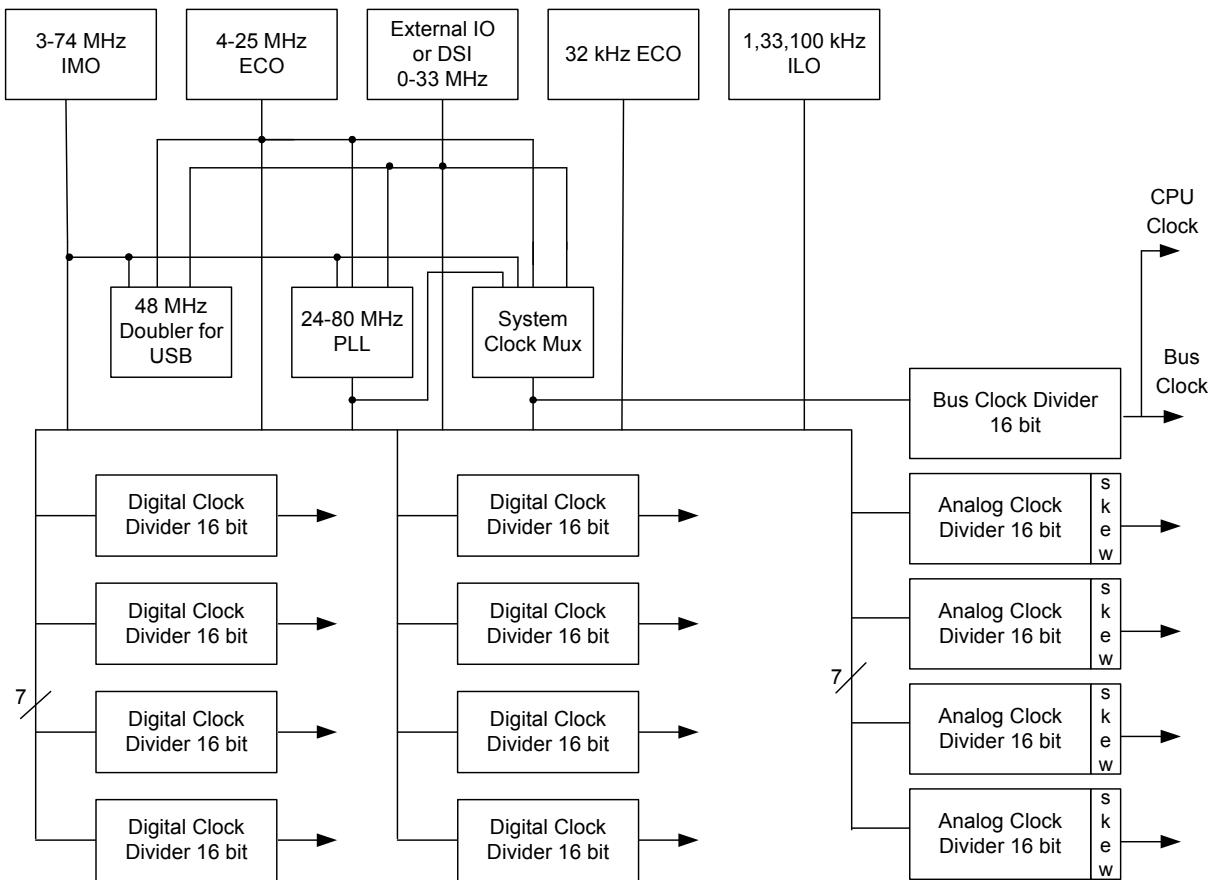
[PSoC Creator](#) is a free Windows-based Integrated Design Environment (IDE). It enables concurrent hardware and firmware design of PSoC 3, PSoC 4, and PSoC 5LP based systems. Create designs using classic, familiar schematic capture supported by over 100 pre-verified, production-ready PSoC Components; see the [list of component datasheets](#). With PSoC Creator, you can:

1. Drag and drop component icons to build your hardware system design in the main design workspace
2. Codesign your application firmware with the PSoC hardware, using the PSoC Creator IDE C compiler
3. Configure components using the configuration tools
4. Explore the library of 100+ components
5. Review component datasheets

**Figure 1. Multiple-Sensor Example Project in PSoC Creator**



**Figure 6-1. Clocking Subsystem**

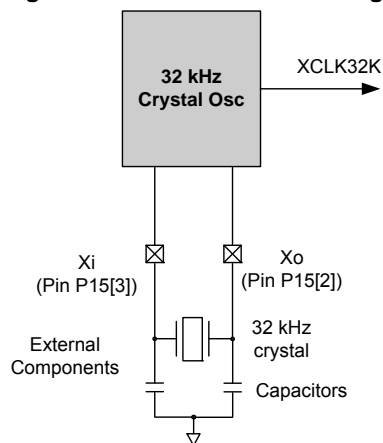


### 6.1.2.2 32.768 kHz ECO

The 32.768-kHz external crystal oscillator (32kHzECO) provides precision timing with minimal power consumption using an external 32.768-kHz watch crystal (see [Figure 6-3](#)). The 32kHzECO also connects directly to the sleep timer and provides the source for the RTC. The RTC uses a 1 second interrupt to implement the RTC functionality in firmware.

The oscillator works in two distinct power modes. This allows users to trade off power consumption with noise immunity from neighboring circuits. The GPIO pins connected to the external crystal and capacitors are fixed.

**Figure 6-3. 32kHzECO Block Diagram**



It is recommended that the external 32.768-kHz watch crystal have a load capacitance (CL) of 6 pF or 12.5 pF. Check the crystal manufacturer's datasheet. The two external capacitors, CL1 and CL2, are typically of the same value, and their total capacitance,  $CL1CL2 / (CL1 + CL2)$ , including pin and trace capacitance, should equal the crystal CL value. For more information, refer to application note [AN54439: PSoC 3 and PSoC 5 External Oscillators](#). See also pin capacitance specifications in the "GPIO" section on page 76.

### 6.1.2.3 Digital System Interconnect

The DSI provides routing for clocks taken from external clock oscillators connected to I/O. The oscillators can also be generated within the device in the digital system and UDBs.

While the primary DSI clock input provides access to all clocking resources, up to eight other DSI clocks (internally or externally generated) may be routed directly to the eight digital clock dividers. This is only possible if there are multiple precision clock sources.

### 6.1.3 Clock Distribution

All seven clock sources are inputs to the central clock distribution system. The distribution system is designed to create multiple high precision clocks. These clocks are customized for the design's requirements and eliminate the common problems found with limited resolution prescalers attached to peripherals. The clock distribution system generates several types of clock trees.

- The system clock is used to select and supply the fastest clock in the system for general system clock requirements and clock synchronization of the PSoC device.
- Bus clock 16-bit divider uses the system clock to generate the system's bus clock used for data transfers and the CPU. The CPU clock is directly derived from the bus clock.
- Eight fully programmable 16-bit clock dividers generate digital system clocks for general use in the digital system, as configured by the design's requirements. Digital system clocks can generate custom clocks derived from any of the seven clock sources for any purpose. Examples include baud rate generators, accurate PWM periods, and timer clocks, and many others. If more than eight digital clock dividers are required, the UDBs and fixed function timer/counter/PWMs can also generate clocks.
- Four 16-bit clock dividers generate clocks for the analog system components that require clocking, such as ADCs and mixers. The analog clock dividers include skew control to ensure that critical analog events do not occur simultaneously with digital switching events. This is done to reduce analog system noise.

Each clock divider consists of an 8-input multiplexer, a 16-bit clock divider (divide by 2 and higher) that generates ~50% duty cycle clocks, system clock resynchronization logic, and deglitch logic. The outputs from each digital clock tree can be routed into the digital system interconnect and then brought back into the clock system as an input, allowing clock chaining of up to 32 bits.

### 6.1.4 USB Clock Domain

The USB clock domain is unique in that it operates largely asynchronously from the main clock network. The USB logic contains a synchronous bus interface to the chip, while running on an asynchronous clock to process USB data. The USB logic requires a 48-MHz frequency. This frequency can be generated from different sources, including DSI clock at 48 MHz or doubled value of 24 MHz from internal oscillator, DSI signal, or crystal oscillator.

## 6.2 Power System

The power system consists of separate analog, digital, and I/O supply pins, labeled VDDA, VDDD, and VDDIOX, respectively. It also includes two internal 1.8 V regulators that provide the digital (VCCD) and analog (VCCA) supplies for the internal core logic. The output pins of the regulators (VCCD and VCCA) and the VDDIO pins must have capacitors connected as shown in [Figure 6-4](#). The two V<sub>CCD</sub> pins must be shorted together, with as short a trace as possible, and connected to a 1 μF ±10% X5R capacitor. The power system also contains a sleep regulator, an I<sup>2</sup>C regulator, and a hibernate regulator.

### 6.4 I/O System and Routing

PSoC I/Os are extremely flexible. Every GPIO has analog and digital I/O capability. All I/Os have a large number of drive modes, which are set at POR. PSoC also provides up to four individual I/O voltage domains through the VDDIO pins.

There are two types of I/O pins on every device; those with USB provide a third type. Both general purpose I/O (GPIO) and special I/O (SIO) provide similar digital functionality. The primary differences are their analog capability and drive strength. Devices that include USB also provide two USBIO pins that support specific USB functionality as well as limited GPIO capability.

All I/O pins are available for use as digital inputs and outputs for both the CPU and digital peripherals. In addition, all I/O pins can generate an interrupt. The flexible and advanced capabilities of the PSoC I/O, combined with any signal to any pin routability, greatly simplify circuit design and board layout. All GPIO pins can be used for analog input, CapSense<sup>[9]</sup>, and LCD segment drive, while SIO pins are used for voltages in excess of VDDA and for programmable output voltages.

#### ■ Features supported by both GPIO and SIO:

- User programmable port reset state
- Separate I/O supplies and voltages for up to four groups of I/O
- Digital peripherals use DSI to connect the pins
- Input or output or both for CPU and DMA
- Eight drive modes
- Every pin can be an interrupt source configured as rising edge, falling edge or both edges. If required, level sensitive interrupts are supported through the DSI
- Dedicated port interrupt vector for each port

- Slew rate controlled digital output drive mode
- Access port control and configuration registers on either port basis or pin basis
- Separate port read (PS) and write (DR) data registers to avoid read modify write errors
- Special functionality on a pin by pin basis

#### ■ Additional features only provided on the GPIO pins:

- LCD segment drive on LCD equipped devices
- CapSense<sup>[9]</sup>
- Analog input and output capability
- Continuous 100  $\mu$ A clamp current capability
- Standard drive strength down to 1.71 V

#### ■ Additional features only provided on SIO pins:

- Higher drive strength than GPIO
- Hot swap capability (5 V tolerance at any operating VDD)
- Programmable and regulated high input and output drive levels down to 1.2 V
- No analog input, CapSense, or LCD capability
- Over voltage tolerance up to 5.5 V
- SIO can act as a general purpose analog comparator

#### ■ USBIO features:

- Full speed USB 2.0 compliant I/O
- Highest drive strength for general purpose use
- Input, output, or both for CPU and DMA
- Input, output, or both for digital peripherals
- Digital output (CMOS) drive mode
- Each pin can be an interrupt source configured as rising edge, falling edge, or both edges

#### Note

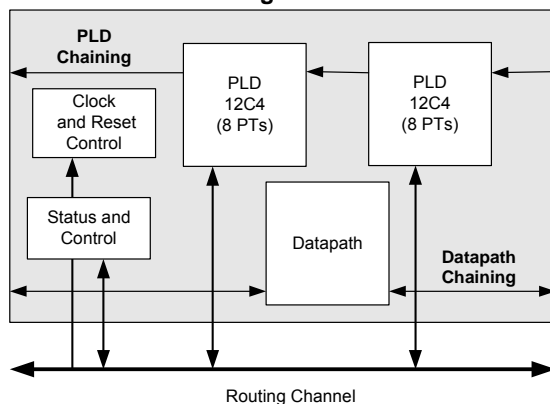
9. GPIOs with opamp outputs are not recommended for use with CapSense.

### 7.2 Universal Digital Block

The Universal Digital Block (UDB) represents an evolutionary step to the next generation of PSoC embedded digital peripheral functionality. The architecture in first generation PSoC digital blocks provides coarse programmability in which a few fixed functions with a small number of options are available. The new UDB architecture is the optimal balance between configuration granularity and efficient implementation. A cornerstone of this approach is to provide the ability to customize the devices digital operation to match application requirements.

To achieve this, UDBs consist of a combination of uncommitted logic (PLD), structured logic (Datapath), and a flexible routing scheme to provide interconnect between these elements, I/O connections, and other peripherals. UDB functionality ranges from simple self contained functions that are implemented in one UDB, or even a portion of a UDB (unused resources are available for other functions), to more complex functions that require multiple UDBs. Examples of basic functions are timers, counters, CRC generators, PWMs, dead band generators, and communications functions, such as UARTs, SPI, and I<sup>2</sup>C. Also, the PLD blocks and connectivity provide full featured general purpose programmable logic within the limits of the available resources.

**Figure 7-2. UDB Block Diagram**



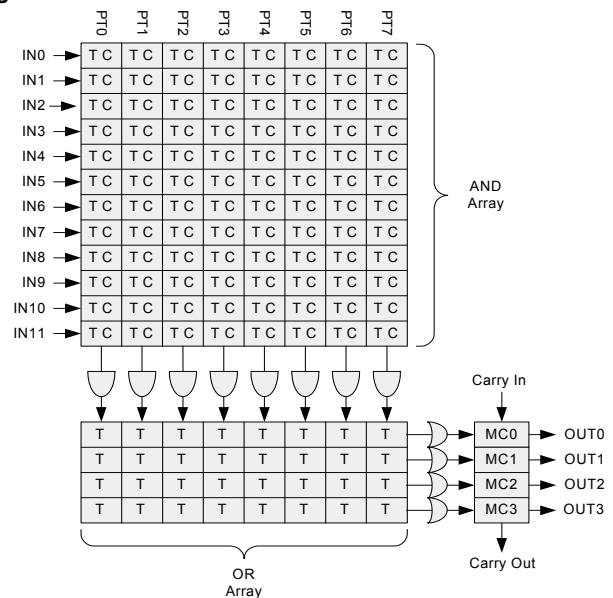
The main component blocks of the UDB are:

- **PLD blocks** - There are two small PLDs per UDB. These blocks take inputs from the routing array and form registered or combinational sum-of-products logic. PLDs are used to implement state machines, state bits, and combinational logic equations. PLD configuration is automatically generated from graphical primitives.
- **Datapath Module** - This 8-bit wide datapath contains structured logic to implement a dynamically configurable ALU, a variety of compare configurations and condition generation. This block also contains input/output FIFOs, which are the primary parallel data interface between the CPU/DMA system and the UDB.
- **Status and Control Module** - The primary role of this block is to provide a way for CPU firmware to interact and synchronize with UDB operation.
- **Clock and Reset Module** - This block provides the UDB clocks and reset selection and control.

#### 7.2.1 PLD Module

The primary purpose of the PLD blocks is to implement logic expressions, state machines, sequencers, look up tables, and decoders. In the simplest use model, consider the PLD blocks as a standalone resource onto which general purpose RTL is synthesized and mapped. The more common and efficient use model is to create digital functions from a combination of PLD and datapath blocks, where the PLD implements only the random logic and state portion of the function while the datapath (ALU) implements the more structured elements.

**Figure 7-3. PLD 12C4 Structure**

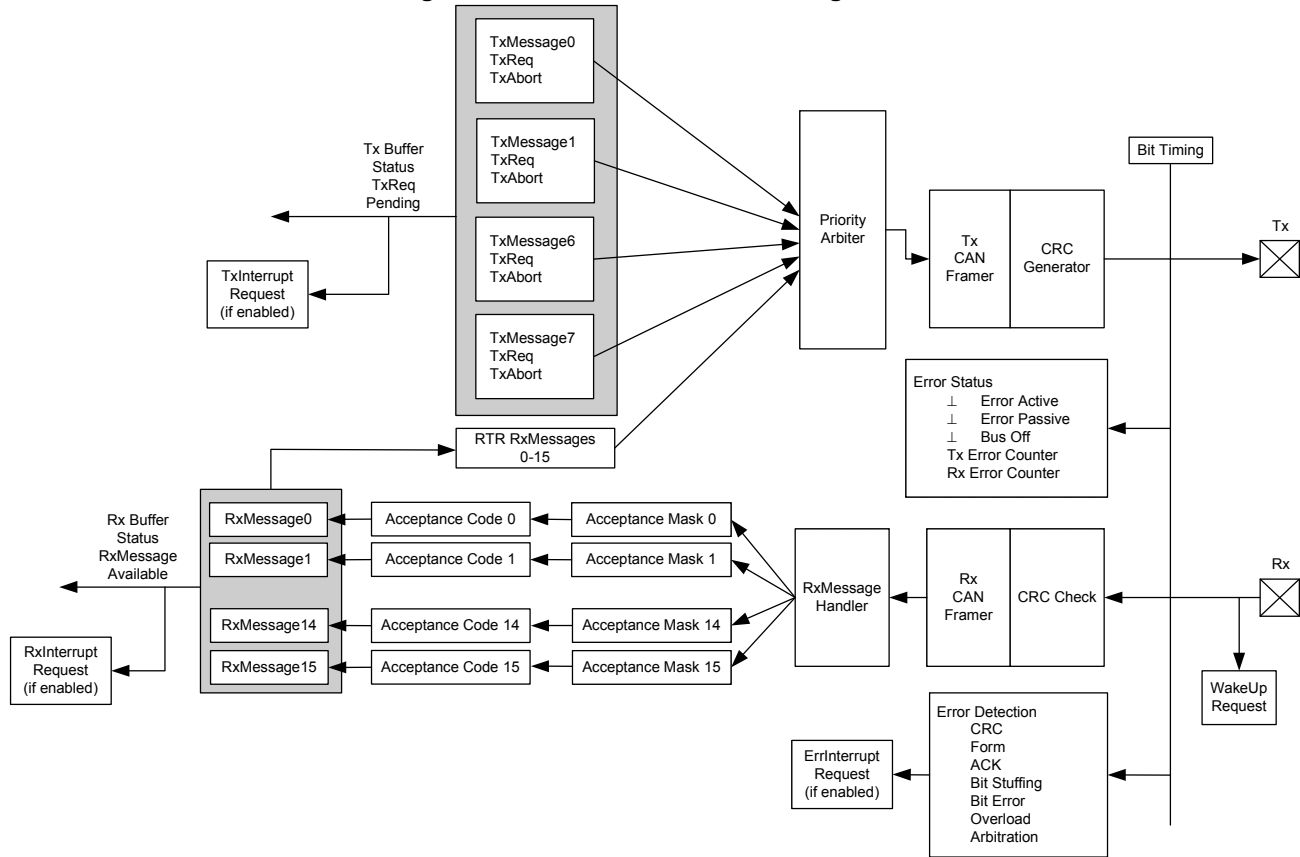


One 12C4 PLD block is shown in Figure 7-3. This PLD has 12 inputs, which feed across eight product terms. Each product term (AND function) can be from 1 to 12 inputs wide, and in a given product term, the true (T) or complement (C) of each input can be selected. The product terms are summed (OR function) to create the PLD outputs. A sum can be from 1 to 8 product terms wide. The 'C' in 12C4 indicates that the width of the OR gate (in this case 8) is constant across all outputs (rather than variable as in a 22V10 device). This PLA like structure gives maximum flexibility and insures that all inputs and outputs are permutable for ease of allocation by the software tools. There are two 12C4 PLDs in each UDB.

#### 7.2.2 Datapath Module

The datapath contains an 8-bit single cycle ALU, with associated compare and condition generation logic. This datapath block is optimized to implement embedded functions, such as timers, counters, integrators, PWMs, PRS, CRC, shifters and dead band generators, and many others.



**Figure 7-15. CAN Controller Block Diagram**


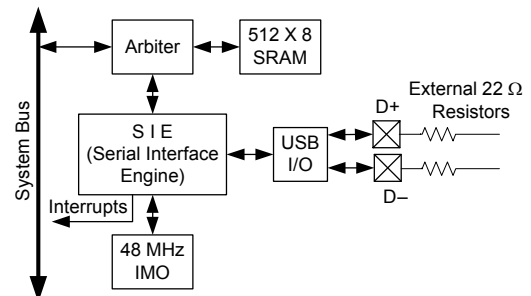
## 7.6 USB

PSoC includes a dedicated Full-Speed (12 Mbps) USB 2.0 transceiver supporting all four USB transfer types: control, interrupt, bulk, and isochronous. PSoC Creator provides full configuration support. USB interfaces to hosts through two dedicated USBIO pins, which are detailed in the [I/O System and Routing](#) on page 33.

USB includes the following features:

- Eight unidirectional data endpoints
- One bidirectional control endpoint 0 (EP0)
- Shared 512-byte buffer for the eight data endpoints
- Dedicated 8-byte buffer for EP0
- Three memory modes
  - Manual Memory Management with No DMA Access
  - Manual Memory Management with Manual DMA Access
  - Automatic Memory Management with Automatic DMA Access

- Internal 3.3 V regulator for transceiver
- Internal 48 MHz oscillator that auto locks to USB bus clock, requiring no external crystal for USB (USB equipped parts only)
- Interrupts on bus and each endpoint event, with device wakeup
- USB Reset, Suspend, and Resume operations
- Bus powered and self powered modes

**Figure 7-16. USB**


### 7.7 Timers, Counters, and PWMs

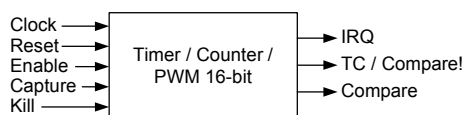
The Timer/Counter/PWM peripheral is a 16-bit dedicated peripheral providing three of the most common embedded peripheral features. As almost all embedded systems use some combination of timers, counters, and PWMs. Four of them have been included on this PSoC device family. Additional and more advanced functionality timers, counters, and PWMs can also be instantiated in Universal Digital Blocks (UDBs) as required. PSoC Creator allows you to choose the timer, counter, and PWM features that you need. The tool set utilizes the most optimal resources available.

The Timer/Counter/PWM peripheral can select from multiple clock sources, with input and output signals connected through the DSI routing. DSI routing allows input and output connections to any device pin and any internal digital signal accessible through the DSI. Each of the four instances has a compare output, terminal count output (optional complementary compare output), and programmable interrupt request line. The Timer/Counter/PWMs are configurable as free running, one shot, or Enable input controlled. The peripheral has timer reset and capture inputs, and a kill input for control of the comparator outputs. The peripheral supports full 16-bit capture.

Timer/Counter/PWM features include:

- 16-bit timer/counter/PWM (down count only)
- Selectable clock source
- PWM comparator (configurable for LT, LTE, EQ, GTE, GT)
- Period reload on start, reset, and terminal count
- Interrupt on terminal count, compare true, or capture
- Dynamic counter reads
- Timer capture mode
- Count while enable signal is asserted mode
- Free run mode
- One-shot mode (stop at end of period)
- Complementary PWM outputs with deadband
- PWM output kill

**Figure 7-17. Timer/Counter/PWM**



### 7.8 I<sup>2</sup>C

PSoC includes a single fixed-function I<sup>2</sup>C peripheral. Additional I<sup>2</sup>C interfaces can be instantiated using Universal Digital Blocks (UDBs) in PSoC Creator, as required.

The I<sup>2</sup>C peripheral provides a synchronous two-wire interface designed to interface the PSoC device with a two-wire I<sup>2</sup>C serial communication bus. It is compatible<sup>[13]</sup> with I<sup>2</sup>C Standard-mode, Fast-mode, and Fast-mode Plus devices as defined in the NXP I<sup>2</sup>C-bus specification and user manual (UM10204). The I<sup>2</sup>C bus I/O may be implemented with GPIO or SIO in open-drain modes.

To eliminate the need for excessive CPU intervention and overhead, I<sup>2</sup>C specific support is provided for status detection and generation of framing bits. I<sup>2</sup>C operates as a slave, a master, or multimaster (Slave and Master)<sup>[13]</sup>. In slave mode, the unit always listens for a start condition to begin sending or receiving data. Master mode supplies the ability to generate the Start and Stop conditions and initiate transactions. Multimaster mode provides clock synchronization and arbitration to allow multiple masters on the same bus. If Master mode is enabled and Slave mode is not enabled, the block does not generate interrupts on externally generated Start conditions. I<sup>2</sup>C interfaces through the DSI routing and allows direct connections to any GPIO or SIO pins.

I<sup>2</sup>C provides hardware address detect of a 7-bit address without CPU intervention. Additionally the device can wake from low power modes on a 7-bit hardware address match. If wakeup functionality is required, I<sup>2</sup>C pin connections are limited to one of two specific pairs of SIO pins. See descriptions of SCL and SDA pins in [Pin Descriptions](#) on page 12.

I<sup>2</sup>C features include:

- Slave and master, transmitter, and receiver operation
- Byte processing for low CPU overhead
- Interrupt or polling CPU interface
- Support for bus speeds up to 1 Mbps
- 7 or 10-bit addressing (10-bit addressing requires firmware support)
- SMBus operation (through firmware support - SMBus supported in hardware in UDBs)
- 7-bit hardware address compare
- Wake from low power modes on address match
- Glitch filtering (active and alternate-active modes only)

Data transfers follow the format shown in [Figure 7-18](#). After the START condition (S), a slave address is sent. This address is 7 bits long followed by an eighth bit which is a data direction bit (R/W) - a 'zero' indicates a transmission (WRITE), a 'one' indicates a request for data (READ). A data transfer is always terminated by a STOP condition (P) generated by the master.

#### Notes

12. The I<sup>2</sup>C peripheral is non-compliant with the NXP I<sup>2</sup>C specification in the following areas: analog glitch filter, I/O V<sub>OL</sub>/I<sub>OL</sub>, I/O hysteresis. The I<sup>2</sup>C Block has a digital glitch filter (not available in sleep mode). The Fast-mode minimum fall-time specification can be met by setting the I/Os to slow speed mode. See the I/O Electrical Specifications in [Inputs and Outputs](#) on page 76 for details.
13. Fixed-block I<sup>2</sup>C does not support undefined bus conditions, nor does it support Repeated Start in Slave mode. These conditions should be avoided, or the UDB-based I<sup>2</sup>C component should be used instead.

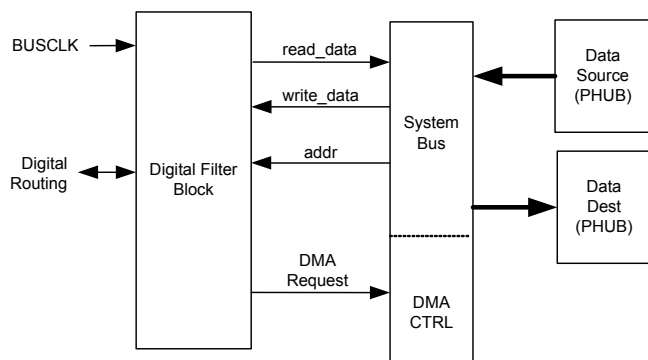


### 7.9 Digital Filter Block

Some devices in the CY8C58LP family of devices have a dedicated HW accelerator block used for digital filtering. The DFB has a dedicated multiplier and accumulator that calculates a 24-bit by 24-bit multiply accumulate in one system clock cycle. This enables the mapping of a direct form FIR filter that approaches a computation rate of one FIR tap for each clock cycle. The MCU can implement any of the functions performed by this block, but at a slower rate that consumes significant MCU bandwidth.

The PSoC Creator interface provides a wizard to implement FIR and IIR digital filters with coefficients for LPF, BPF, HPF, Notch and arbitrary shape filters. 64 pairs of data and coefficients are stored. This enables a 64 tap FIR filter or up to 4 16 tap filters of either FIR or IIR formulation.

**Figure 7-20. DFB Application Diagram (pwr/gnd not shown)**



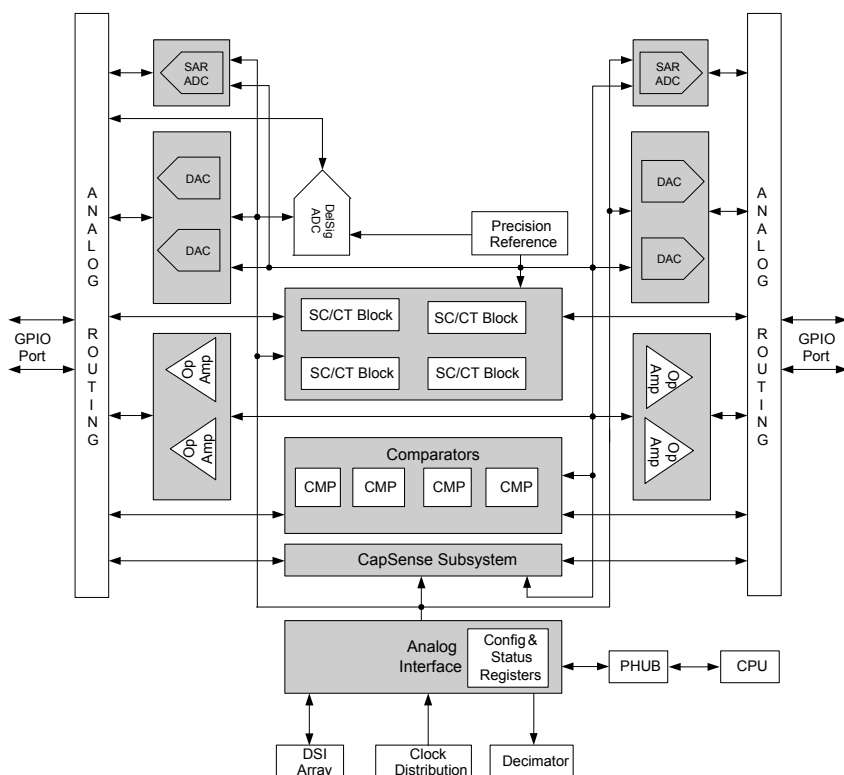
The typical use model is for data to be supplied to the DFB over the system bus from another on-chip system data source such as an ADC. The data typically passes through main memory or is directly transferred from another chip resource through DMA. The DFB processes this data and passes the result to another on-chip resource such as a DAC or main memory through DMA on the system bus.

Data movement in or out of the DFB is typically controlled by the system DMA controller but can be moved directly by the MCU.

### 8. Analog Subsystem

The analog programmable system creates application specific combinations of both standard and advanced analog signal processing blocks. These blocks are then interconnected to each other and also to any pin on the device, providing a high level of design flexibility and IP security. The features of the analog subsystem are outlined here to provide an overview of capabilities and architecture.

- Flexible, configurable analog routing architecture provided by analog globals, analog mux bus, and analog local buses
- High resolution Delta-Sigma ADC
- Two successive approximation (SAR) ADCs
- Four 8-bit DACs that provide either voltage or current output
- Four comparators with optional connection to configurable LUT outputs
- Four configurable switched capacitor/continuous time (SC/CT) blocks for functions that include opamp, unity gain buffer, programmable gain amplifier, transimpedance amplifier, and mixer
- Four opamps for internal use and connection to GPIO that can be used as high current output buffers
- CapSense subsystem to enable capacitive touch sensing
- Precision reference for generating an accurate analog voltage for internal analog blocks

**Figure 8-1. Analog Subsystem Block Diagram**


The PSoC Creator software program provides a user friendly interface to configure the analog connections between the GPIO and various analog resources and also connections from one analog resource to another. PSoC Creator also provides component libraries that allow you to configure the various analog blocks to perform application specific functions (PGA, transimpedance amplifier, voltage DAC, current DAC, and so on). The tool also generates API interface libraries that allow you to write firmware that allows the communication between the analog peripheral and CPU/Memory.

## 8.1 Analog Routing

The PSoC 5LP family of devices has a flexible analog routing architecture that provides the capability to connect GPIOs and different analog blocks, and also route signals between different analog blocks. One of the strong points of this flexible routing architecture is that it allows dynamic routing of input and output connections to the different analog blocks.

For information on how to make pin selections for optimal analog routing, refer to the application note, [AN58304 - PSoC® 3 and PSoC® 5 - Pin Selection for Analog Designs](#).

### 8.1.1 Features

- Flexible, configurable analog routing architecture
- 16 analog globals (AG) and two analog mux buses (AMUXBUS) to connect GPIOs and the analog blocks
- Each GPIO is connected to one analog global and one analog mux bus

- Eight analog local buses (abus) to route signals between the different analog blocks
- Multiplexers and switches for input and output selection of the analog blocks

### 8.1.2 Functional Description

Analog globals (AGs) and analog mux buses (AMUXBUS) provide analog connectivity between GPIOs and the various analog blocks. There are 16 AGs in the PSoC 5LP family. The analog routing architecture is divided into four quadrants as shown in [Figure 8-2](#). Each quadrant has four analog globals (AGL[0..3], AGL[4..7], AGR[0..3], AGR[4..7]). Each GPIO is connected to the corresponding AG through an analog switch. The analog mux bus is a shared routing resource that connects to every GPIO through an analog switch. There are two AMUXBUS routes in PSoC 5LP, one in the left half (AMUXBUSL) and one in the right half (AMUXBUSR), as shown in [Figure 8-2](#).

Analog local buses (abus) are routing resources located within the analog subsystem and are used to route signals between different analog blocks. There are eight abus routes in PSoC 5LP, four in the left half (abusl [0:3]) and four in the right half (abusr [0:3]) as shown in [Figure 8-2](#). Using the abus saves the analog globals and analog mux buses from being used for interconnecting the analog blocks.

Multiplexers and switches exist on the various buses to direct signals into and out of the analog blocks. A multiplexer can have only one connection on at a time, whereas a switch can have multiple connections on simultaneously. In [Figure 8-2](#), multiplexers are indicated by grayed ovals and switches are indicated by transparent ovals.

### 8.7.1 LCD Segment Pin Driver

Each GPIO pin contains an LCD driver circuit. The LCD driver buffers the appropriate output of the LCD DAC to directly drive the glass of the LCD. A register setting determines whether the pin is a common or segment. The pin's LCD driver then selects one of the six bias voltages to drive the I/O pin, as appropriate for the display data.

### 8.7.2 Display Data Flow

The LCD segment driver system reads display data and generates the proper output voltages to the LCD glass to produce the desired image. Display data resides in a memory buffer in the system SRAM. Each time you need to change the common and segment driver voltages, the next set of pixel data moves from the memory buffer into the Port Data Registers via DMA.

### 8.7.3 UDB and LCD Segment Control

A UDB is configured to generate the global LCD control signals and clocking. This set of signals is routed to each LCD pin driver through a set of dedicated LCD global routing channels. In addition to generating the global LCD control signals, the UDB also produces a DMA request to initiate the transfer of the next frame of LCD data.

### 8.7.4 LCD DAC

The LCD DAC generates the contrast control and bias voltage for the LCD system. The LCD DAC produces up to five LCD drive voltages plus ground, based on the selected bias ratio. The bias voltages are driven out to GPIO pins on a dedicated LCD bias bus, as required.

## 8.8 CapSense

The CapSense system provides a versatile and efficient means for measuring capacitance in applications such as touch sense buttons, sliders, proximity detection, etc. The CapSense system

uses a configuration of system resources, including a few hardware functions primarily targeted for CapSense. Specific resource usage is detailed in the CapSense component in PSoC Creator.

A capacitive sensing method using a Delta-Sigma Modulator (CSD) is used. It provides capacitance sensing using a switched capacitor technique with a delta-sigma modulator to convert the sensing current to a digital code.

## 8.9 Temp Sensor

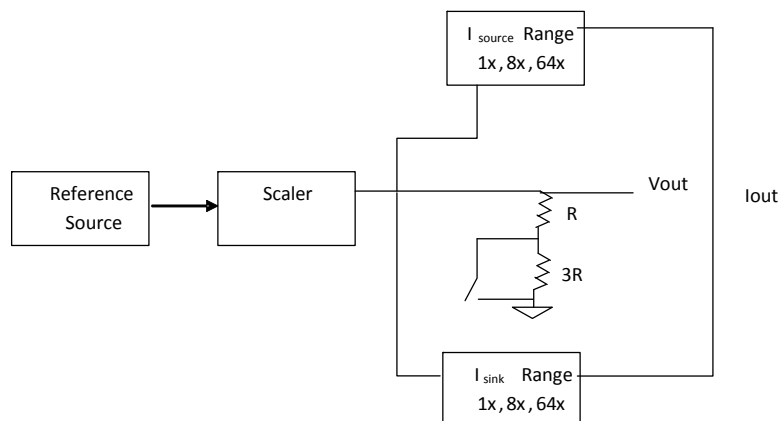
Die temperature is used to establish programming parameters for writing flash. Die temperature is measured using a dedicated sensor based on a forward biased transistor. The temperature sensor has its own auxiliary ADC.

## 8.10 DAC

The CY8C58LP parts contain four Digital to Analog Convertors (DACs). Each DAC is 8-bit and can be configured for either voltage or current output. The DACs support CapSense, power supply regulation, and waveform generation. Each DAC has the following features.

- Adjustable voltage or current output in 255 steps
- Programmable step size (range selection)
- Eight bits of calibration to correct  $\pm 25\%$  of gain error
- Source and sink option for current output
- 8 Msps conversion rate for current output
- 1 Msps conversion rate for voltage output
- Monotonic in nature
- Data and strobe inputs can be provided by the CPU or DMA, or routed directly from the DSI
- Dedicated low-resistance output pin for high-current mode

**Figure 8-12. DAC Block Diagram**

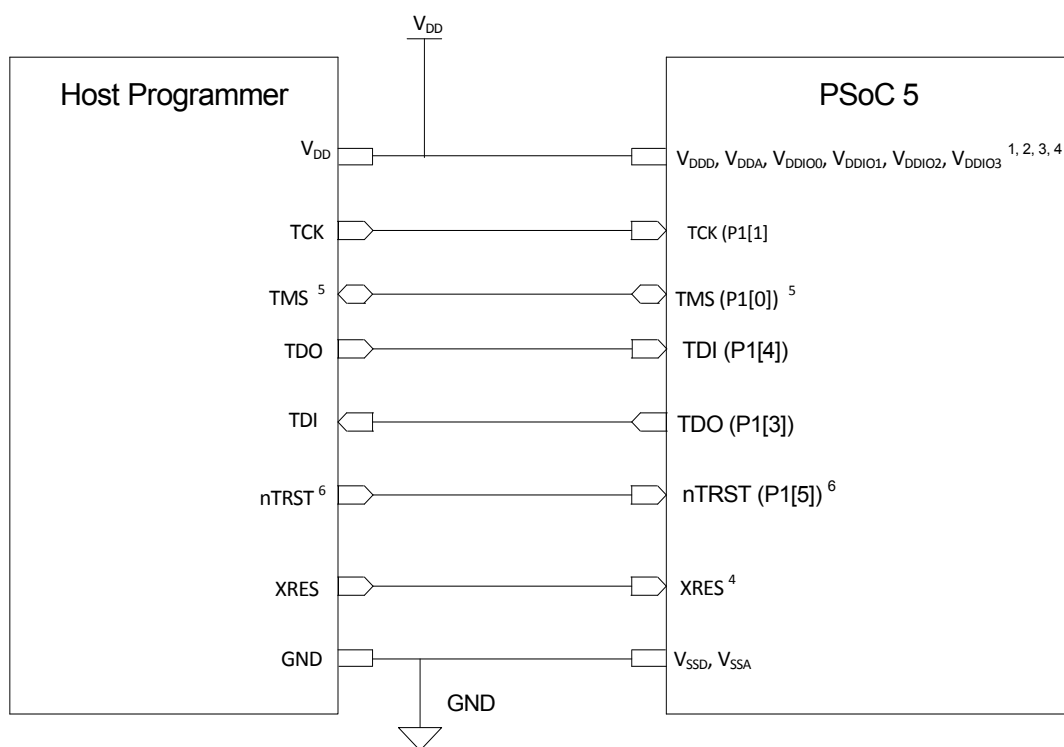


### 8.10.1 Current DAC

The current DAC (IDAC) can be configured for the ranges 0 to 31.875  $\mu\text{A}$ , 0 to 255  $\mu\text{A}$ , and 0 to 2.04 mA. The IDAC can be configured to source or sink current.

### 8.10.2 Voltage DAC

For the voltage DAC (VDAC), the current DAC output is routed through resistors. The two ranges available for the VDAC are 0 to 1.02 V and 0 to 4.08 V. In voltage mode any load connected to the output of a DAC should be purely capacitive (the output of the VDAC is not buffered).

**Figure 9-1. JTAG Interface Connections between PSoC 5LP and Programmer**


<sup>1</sup> The voltage levels of Host Programmer and the PSoC 5 voltage domains involved in Programming should be same. The Port 1 JTAG pins and XRES pin are powered by VDDIO1. So, VDDIO1 of PSoC 5 should be at same voltage level as host VDD. Rest of PSoC 5 voltage domains (VDD, VDDA, VDDIO0, VDDIO2, VDDIO3) need not be at the same voltage level as host Programmer.

<sup>2</sup> Vdda must be greater than or equal to all other power supplies (Vddd, Vddio's) in PSoC 5.

<sup>3</sup> For Power cycle mode Programming, XRES pin is not required. But the Host programmer must have the capability to toggle power (Vddd, Vdda, All Vddio's) to PSoC 5. This may typically require external interface circuitry to toggle power which will depend on the programming setup. The power supplies can be brought up in any sequence, however, once stable, VDDA must be greater than or equal to all other supplies.

<sup>4</sup> For JTAG Programming, Device reset can also be done without connecting to the XRES pin or Power cycle mode by using the TMS, TCK, TDI, TDO pins of PSoC 5, and writing to a specific register. But this requires that the DPS setting in NVL is not equal to "Debug Ports Disabled".

<sup>5</sup> By default, PSoC 5 is configured for 4-wire JTAG mode unless user changes the DPS setting. So the TMS pin is unidirectional. But if the DPS setting is changed to non-JTAG mode, the TMS pin in JTAG is bi-directional as the SWD Protocol has to be used for acquiring the PSoC 5 device initially. After switching from SWD to JTAG mode, the TMS pin will be uni-directional. In such a case, unidirectional buffer should not be used on TMS line.

<sup>6</sup> nTRST JTAG pin (P1[5]) cannot be used to reset the JTAG TAP controller during first time programming of PSoC 5 as the default setting is 4-wire JTAG (nTRST disabled). Use the TMS, TCK pins to do a reset of JTAG TAP controller.

## 10. Development Support

The CY8C58LP family has a rich set of documentation, development tools, and online resources to assist you during your development process. Visit [psoc.cypress.com/getting-started](http://psoc.cypress.com/getting-started) to find out more.

### 10.1 Documentation

A suite of documentation, to ensure that you can find answers to your questions quickly, supports the CY8C58LP family. This section contains a list of some of the key documents.

**Software User Guide:** A step-by-step guide for using PSoC Creator. The software user guide shows you how the PSoC Creator build process works in detail, how to use source control with PSoC Creator, and much more.

**Component Datasheets:** The flexibility of PSoC allows the creation of new peripherals (components) long after the device has gone into production. Component datasheets provide all of the information needed to select and use a particular component, including a functional description, API documentation, example code, and AC/DC specifications.

**Application Notes:** PSoC application notes discuss a particular application of PSoC in depth; examples include brushless DC motor control and on-chip filtering. Application notes often include example projects in addition to the application note document.

**Technical Reference Manual:** PSoC Creator makes designing with PSoC as easy as dragging a peripheral onto a schematic, but, when low level details of the PSoC device are required, use the technical reference manual (TRM) as your guide.

**Note** Visit [www.arm.com](http://www.arm.com) for detailed documentation about the Cortex-M3 CPU.

### 10.2 Online

In addition to print documentation, the Cypress PSoC forums connect you with fellow PSoC users and experts in PSoC from around the world, 24 hours a day, 7 days a week.

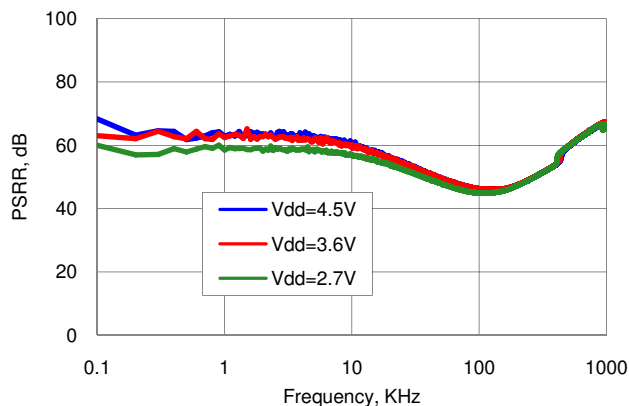
### 10.3 Tools

With industry standard cores, programming, and debugging interfaces, the CY8C58LP family is part of a development tool ecosystem. Visit us at [www.cypress.com/go/psoccreator](http://www.cypress.com/go/psoccreator) for the latest information on the revolutionary, easy to use PSoC Creator IDE, supported third party compilers, programmers, debuggers, and development kits.

### 11.3.2 Analog Core Regulator

**Table 11-5. Analog Core Regulator DC Specifications**

Parameter	Description	Conditions	Min	Typ	Max	Units
V <sub>DDA</sub>	Input voltage		1.8	–	5.5	V
V <sub>CCA</sub>	Output voltage		–	1.80	–	V
	Regulator output capacitor	±10%, X5R ceramic or better	0.9	1	1.1	μF

**Figure 11-7. Analog Regulator PSRR vs Frequency and V<sub>DD</sub>**


### 11.3.3 Inductive Boost Regulator

Unless otherwise specified, operating conditions are: V<sub>BAT</sub> = 0.5 V–3.6 V, V<sub>OUT</sub> = 1.8 V–5.0 V, I<sub>OUT</sub> = 0 mA–50 mA, L<sub>BOOST</sub> = 4.7 μH–22 μH, C<sub>BOOST</sub> = 22 μF || 3 × 1.0 μF || 3 × 0.1 μF, C<sub>BAT</sub> = 22 μF, I<sub>F</sub> = 1.0 A, excludes 99-pin CSP package. For information on using boost with 99-pin CSP package, contact Cypress support. Unless otherwise specified, all charts and graphs show typical values.

**Table 11-6. Inductive Boost Regulator DC Specifications**

Parameter	Description	Conditions		Min	Typ	Max	Units
V <sub>OUT</sub>	Boost output voltage <sup>[29]</sup>	vsel = 1.8 V in register BOOST_CR0		1.71	1.8	1.89	V
		vsel = 1.9 V in register BOOST_CR0		1.81	1.90	2.00	V
		vsel = 2.0 V in register BOOST_CR0		1.90	2.00	2.10	V
		vsel = 2.4 V in register BOOST_CR0		2.16	2.40	2.64	V
		vsel = 2.7 V in register BOOST_CR0		2.43	2.70	2.97	V
		vsel = 3.0 V in register BOOST_CR0		2.70	3.00	3.30	V
		vsel = 3.3 V in register BOOST_CR0		2.97	3.30	3.63	V
		vsel = 3.6 V in register BOOST_CR0		3.24	3.60	3.96	V
		vsel = 5.0 V in register BOOST_CR0		4.50	5.00	5.50	V
V <sub>BAT</sub>	Input voltage to boost <sup>[30]</sup>	I <sub>OUT</sub> = 0 mA–5 mA	vsel = 1.8 V–2.0 V, T <sub>A</sub> = 0 °C–70 °C	0.5	–	0.8	V
		I <sub>OUT</sub> = 0 mA–15 mA	vsel = 1.8 V–5.0 V <sup>[31]</sup> , T <sub>A</sub> = –10 °C–85 °C	1.6	–	3.6	V
		I <sub>OUT</sub> = 0 mA–25 mA	vsel = 1.8 V–2.7 V, T <sub>A</sub> = –10 °C–85 °C	0.8	–	1.6	V
		I <sub>OUT</sub> = 0 mA–50 mA	vsel = 1.8 V–3.3 V <sup>[31]</sup> , T <sub>A</sub> = –40 °C–85 °C	1.8	–	2.5	V
			vsel = 1.8 V–3.3 V <sup>[31]</sup> , T <sub>A</sub> = –10 °C–85 °C	1.3	–	2.5	V
			vsel = 2.5 V–5.0 V <sup>[31]</sup> , T <sub>A</sub> = –10 °C–85 °C	2.5	–	3.6	V



## 11.4 Inputs and Outputs

Specifications are valid for  $-40\text{ }^{\circ}\text{C} \leq T_A \leq 105\text{ }^{\circ}\text{C}$  and  $T_J \leq 120\text{ }^{\circ}\text{C}$ , except where noted. Specifications are valid for 1.71 V to 5.5 V, except where noted. Unless otherwise specified, all charts and graphs show typical values.

When the power supplies ramp up, there are low-impedance connections between each GPIO pin and its  $V_{DDIO}$  supply. This causes the pin voltages to track  $V_{DDIO}$  until both  $V_{DDIO}$  and  $V_{DDA}$  reach the IPOR voltage, which can be as high as 1.45 V. At that point, the low-impedance connections no longer exist and the pins change to their normal NVL settings.

Also, if  $V_{DDA}$  is less than  $V_{DDIO}$ , a low-impedance path may exist between a GPIO and  $V_{DDA}$ , causing the GPIO to track  $V_{DDA}$  until  $V_{DDA}$  becomes greater than or equal to  $V_{DDIO}$ .

### 11.4.1 GPIO

**Table 11-8. GPIO DC Specifications**

Parameter	Description	Conditions	Min	Typ	Max	Units
$V_{IH}$	Input voltage high threshold	CMOS Input, $PRT[x]CTL = 0$	$0.7 \times V_{DDIO}$	—	—	V
$V_{IL}$	Input voltage low threshold	CMOS Input, $PRT[x]CTL = 0$	—	—	$0.3 \times V_{DDIO}$	V
$V_{IH}$	Input voltage high threshold	LVTTL Input, $PRT[x]CTL = 1$ , $V_{DDIO} < 2.7\text{ V}$	$0.7 \times V_{DDIO}$	—	—	V
$V_{IH}$	Input voltage high threshold	LVTTL Input, $PRT[x]CTL = 1$ , $V_{DDIO} \geq 2.7\text{ V}$	2.0	—	—	V
$V_{IL}$	Input voltage low threshold	LVTTL Input, $PRT[x]CTL = 1$ , $V_{DDIO} < 2.7\text{ V}$	—	—	$0.3 \times V_{DDIO}$	V
$V_{IL}$	Input voltage low threshold	LVTTL Input, $PRT[x]CTL = 1$ , $V_{DDIO} \geq 2.7\text{ V}$	—	—	0.8	V
$V_{OH}$	Output voltage high	$I_{OH} = 4\text{ mA}$ at $3.3\text{ V}_{DDIO}$	$V_{DDIO} - 0.6$	—	—	V
		$I_{OH} = 1\text{ mA}$ at $1.8\text{ V}_{DDIO}$	$V_{DDIO} - 0.5$	—	—	V
$V_{OL}$	Output voltage low	$I_{OL} = 8\text{ mA}$ at $3.3\text{ V}_{DDIO}$	—	—	0.6	V
		$I_{OL} = 3\text{ mA}$ at $3.3\text{ V}_{DDIO}$	—	—	0.4	V
		$I_{OL} = 4\text{ mA}$ at $1.8\text{ V}_{DDIO}$	—	—	0.6	V
$R_{pullup}$	Pull-up resistor		3.5	5.6	8.5	k $\Omega$
$R_{pulldown}$	Pull-down resistor		3.5	5.6	8.5	k $\Omega$
$I_{IL}$	Input leakage current (absolute value) <sup>[34]</sup>	25 °C, $V_{DDIO} = 3.0\text{ V}$	—	—	2	nA
$C_{IN}$	Input capacitance <sup>[34]</sup>	P0.0, P0.1, P0.2, P3.6, P3.7	—	17	20	pF
		P0.3, P0.4, P3.0, P3.1, P3.2	—	10	15	pF
		P0.6, P0.7, P15.0, P15.6, P15.7 <sup>[35]</sup>	—	7	12	pF
		All other GPIOs	—	5	9	pF
$V_H$	Input voltage hysteresis (Schmitt-Trigger) <sup>[34]</sup>		—	40	—	mV
$I_{diode}$	Current through protection diode to $V_{DDIO}$ and $V_{SSIO}$		—	—	100	$\mu\text{A}$
$R_{global}$	Resistance pin to analog global bus	25 °C, $V_{DDIO} = 3.0\text{ V}$	—	320	—	$\Omega$
$R_{mux}$	Resistance pin to analog mux bus	25 °C, $V_{DDIO} = 3.0\text{ V}$	—	220	—	$\Omega$

#### Notes

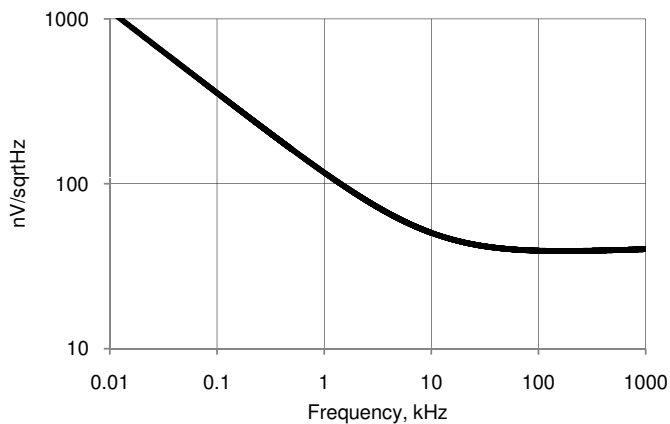
34. Based on device characterization (Not production tested).

35. For information on designing with PSoC oscillators, refer to the application note, [AN54439 - PSoC® 3 and PSoC 5 External Oscillator](#).

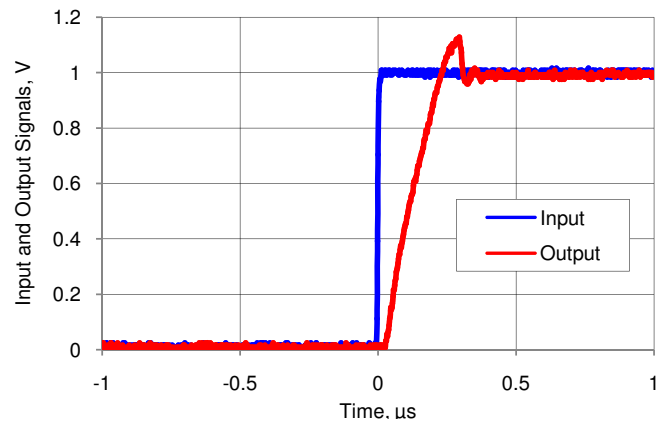
**Table 11-19. Opamp AC Specifications<sup>[44]</sup>**

Parameter	Description	Conditions	Min	Typ	Max	Units
GBW	Gain-bandwidth product	Power mode = minimum, 15 pF load	1	—	—	MHz
		Power mode = low, 15 pF load	2	—	—	MHz
		Power mode = medium, 200 pF load	1	—	—	MHz
		Power mode = high, 200 pF load	3	—	—	MHz
SR	Slew rate, 20% - 80%	Power mode = minimum, 15 pF load	1.1	—	—	V/μs
		Power mode = low, 15 pF load	1.1	—	—	V/μs
		Power mode = medium, 200 pF load	0.9	—	—	V/μs
		Power mode = high, 200 pF load	3	—	—	V/μs
e <sub>n</sub>	Input noise density	Power mode = high, V <sub>dda</sub> = 5 V, at 100 kHz	—	45	—	nV/sqrtHz

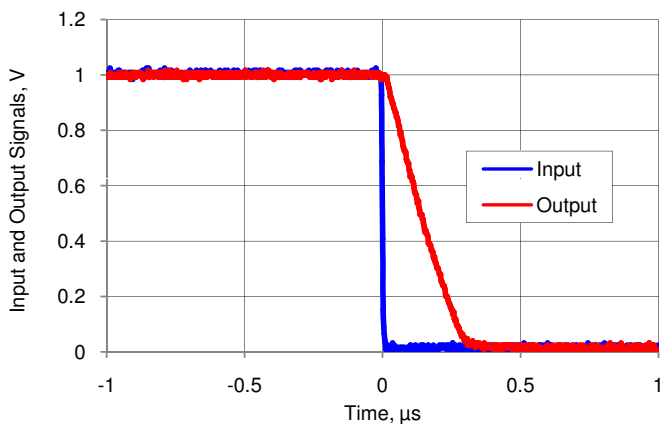
**Figure 11-30. Opamp Noise vs Frequency, Power Mode = High, V<sub>dda</sub> = 5V**



**Figure 11-31. Opamp Step Response, Rising**



**Figure 11-32. Opamp Step Response, Falling**



**Note**

44. Based on device characterization (Not production tested).

## 11.8 PSoC System Resources

Specifications are valid for  $-40\text{ }^{\circ}\text{C} \leq T_A \leq 105\text{ }^{\circ}\text{C}$  and  $T_J \leq 120\text{ }^{\circ}\text{C}$ , except where noted. Specifications are valid for 1.71 V to 5.5 V, except where noted.

### 11.8.1 POR with Brown Out

For brown out detect in regulated mode,  $V_{DDD}$  and  $V_{DDA}$  must be  $\geq 2.0\text{ V}$ . Brown out detect is not available in externally regulated mode.

**Table 11-71. Precise Low-Voltage Reset (PRES) with Brown Out DC Specifications**

Parameter	Description	Conditions	Min	Typ	Max	Units
PRESR	Rising trip voltage	Factory trim	1.64	–	1.68	V
PRESF	Falling trip voltage		1.62	–	1.66	V

**Table 11-72. Power-On-Reset (POR) with Brown Out AC Specifications<sup>[90]</sup>**

Parameter	Description	Conditions	Min	Typ	Max	Units
PRES_TR <sup>[91]</sup>	Response time		–	–	0.5	$\mu\text{s}$
	$V_{DDD}/V_{DDA}$ droop rate	Sleep mode	–	5	–	V/sec

### 11.8.2 Voltage Monitors

**Table 11-73. Voltage Monitors DC Specifications**

Parameter	Description	Conditions	Min	Typ	Max	Units
LVI	Trip voltage					
	LVI_A/D_SEL[3:0] = 0000b		1.68	1.73	1.77	V
	LVI_A/D_SEL[3:0] = 0001b		1.89	1.95	2.01	V
	LVI_A/D_SEL[3:0] = 0010b		2.14	2.20	2.27	V
	LVI_A/D_SEL[3:0] = 0011b		2.38	2.45	2.53	V
	LVI_A/D_SEL[3:0] = 0100b		2.62	2.71	2.79	V
	LVI_A/D_SEL[3:0] = 0101b		2.87	2.95	3.04	V
	LVI_A/D_SEL[3:0] = 0110b		3.11	3.21	3.31	V
	LVI_A/D_SEL[3:0] = 0111b		3.35	3.46	3.56	V
	LVI_A/D_SEL[3:0] = 1000b		3.59	3.70	3.81	V
	LVI_A/D_SEL[3:0] = 1001b		3.84	3.95	4.07	V
	LVI_A/D_SEL[3:0] = 1010b		4.08	4.20	4.33	V
	LVI_A/D_SEL[3:0] = 1011b		4.32	4.45	4.59	V
	LVI_A/D_SEL[3:0] = 1100b		4.56	4.70	4.84	V
	LVI_A/D_SEL[3:0] = 1101b		4.83	4.98	5.13	V
	LVI_A/D_SEL[3:0] = 1110b		5.05	5.21	5.37	V
	LVI_A/D_SEL[3:0] = 1111b		5.30	5.47	5.63	V
HVI	Trip voltage		5.57	5.75	5.92	V

**Table 11-74. Voltage Monitors AC Specifications**

Parameter	Description	Conditions	Min	Typ	Max	Units
LVI_tr <sup>[91]</sup>	Response time		–	–	1	$\mu\text{s}$

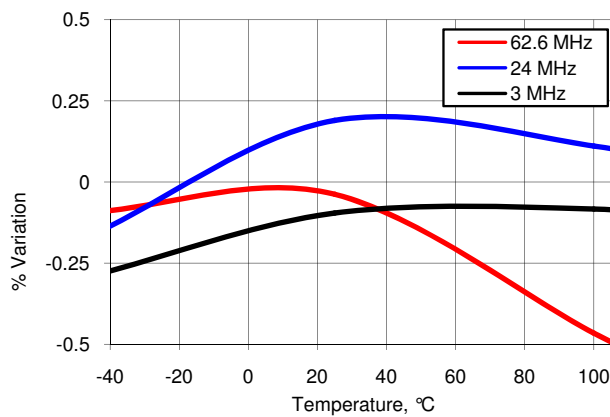
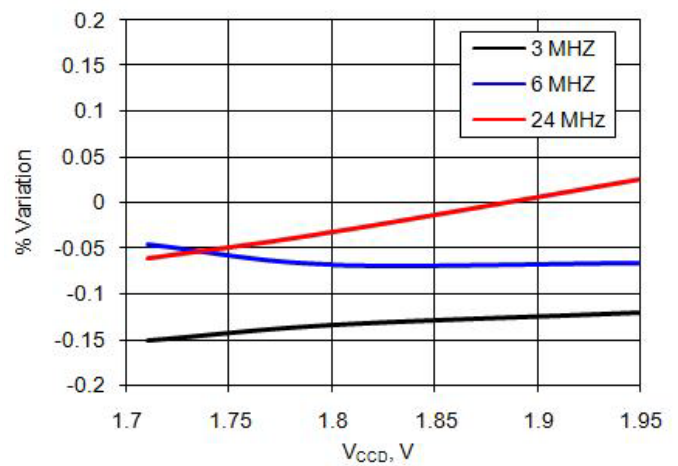
#### Notes

90. Based on device characterization (Not production tested).

91. This value is calculated, not measured.

**Table 11-80. IMO AC Specifications (continued)**

Parameter	Description	Conditions	Min	Typ	Max	Units
Tstart_imo	Startup time <sup>[100]</sup>	From enable (during normal system operation)	–	–	13	μs
Jp-p	Jitter (peak to peak) <sup>[100]</sup>					
	F = 24 MHz		–	0.9	–	ns
	F = 3 MHz		–	1.6	–	ns
Jperiod	Jitter (long term) <sup>[101]</sup>					
	F = 24 MHz		–	0.9	–	ns
	F = 3 MHz		–	12	–	ns

**Figure 11-82. IMO Frequency Variation vs. Temperature**

**Figure 11-83. IMO Frequency Variation vs. V<sub>CC</sub>**


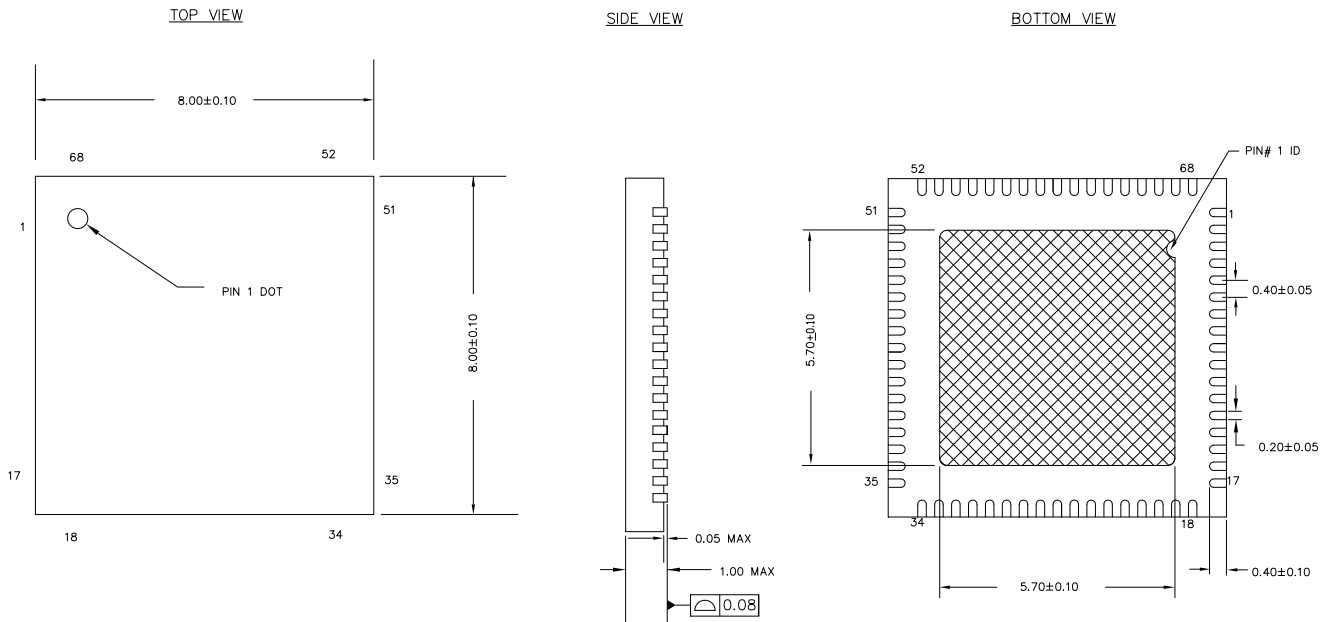
### Notes

99. F<sub>IMO</sub> is measured after packaging, and thus accounts for substrate and die attach stresses.


100. Based on device characterization (Not production tested).

101. Based on device characterization (Not production tested). USBIO pins tied to ground (VSSD).

**Figure 13-1. 68-pin QFN 8x8 with 0.4 mm Pitch Package Outline (Sawn Version)**

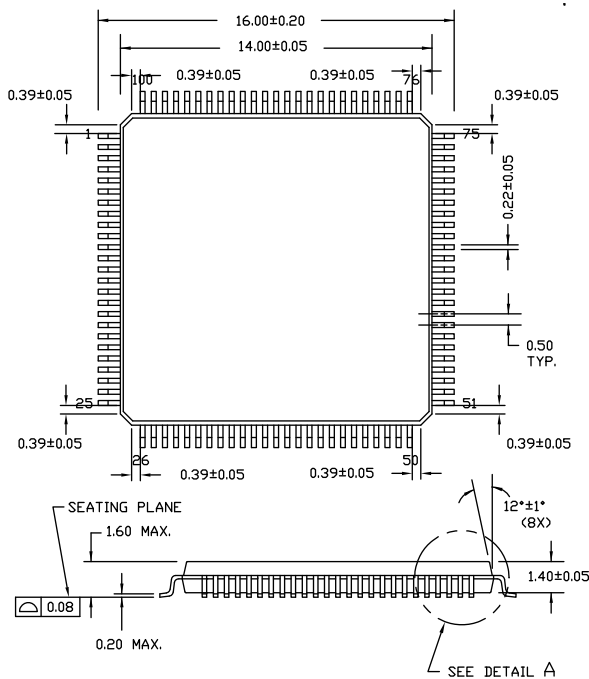


**NOTES:**

1.  HATCH AREA IS SOLDERABLE EXPOSED METAL.
2. REFERENCE JEDEC#: MO-220
3. PACKAGE WEIGHT: 17 ± 2mg
4. ALL DIMENSIONS ARE IN MILLIMETERS

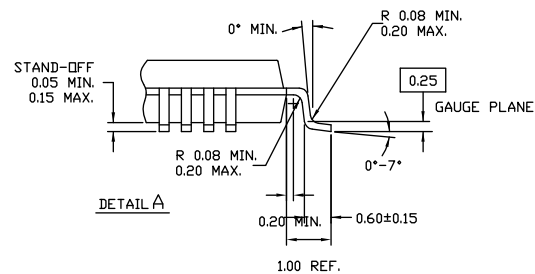
001-09618 \*E

**Figure 13-2. 100-pin TQFP (14 x 14 x 1.4 mm) Package Outline**

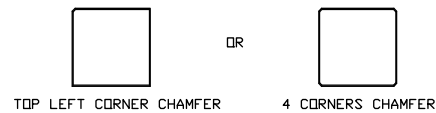


**NOTE:**

1. JEDEC STD REF MS-026
2. BODY LENGTH DIMENSION DOES NOT INCLUDE MOLD PROTRUSION/END FLASH  
MOLD PROTRUSION/END FLASH SHALL NOT EXCEED 0.0098 in (0.25 mm) PER SIDE  
BODY LENGTH DIMENSIONS ARE MAX PLASTIC BODY SIZE INCLUDING MOLD MISMATCH
3. DIMENSIONS IN MILLIMETERS

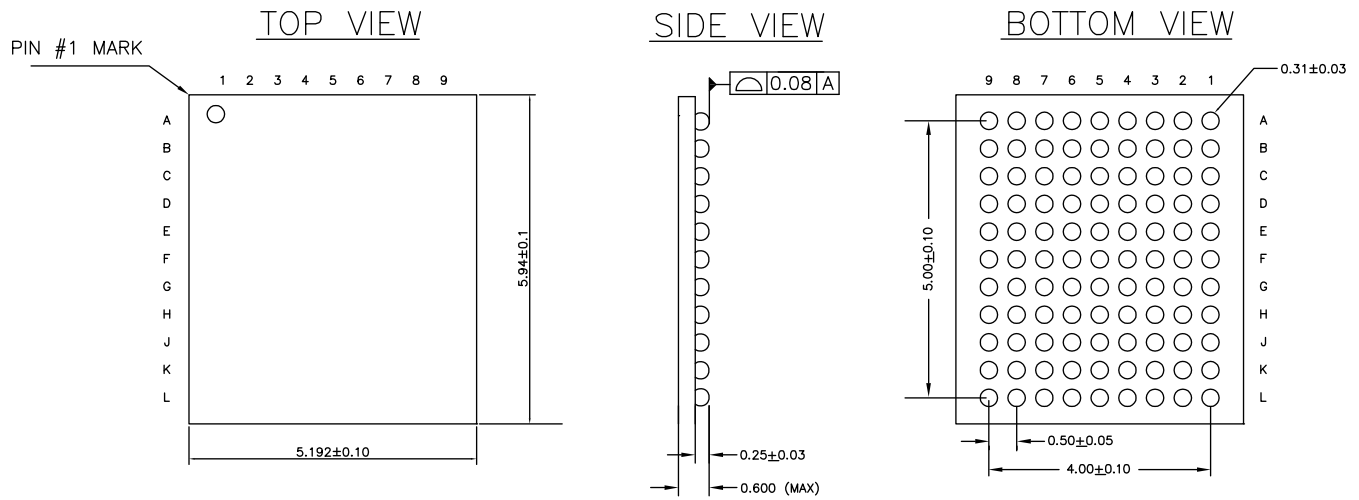


**NOTE:** PKG. CAN HAVE



51-85048 \*J

**Figure 13-3. WLCSP Package (5.192 x 5.940 x 0.6 mm) Package Outline**



**NOTES:**

1. REFERENCE JEDEC Publication 95: Design Guide 4.18
2. ALL DIMENSIONS ARE IN MILLIMETERS

001-88034 \*B



## 15. Document Conventions

### 15.1 Units of Measure

**Table 15-1. Units of Measure**

Symbol	Unit of Measure
°C	degrees Celsius
dB	decibels
fF	femtofarads
Hz	hertz
KB	1024 bytes
kbps	kilobits per second
Khr	kilohours
kHz	kilohertz
kΩ	kilohms
ksps	kilosamples per second
LSB	least significant bit
Mbps	megabits per second
MHz	megahertz
MΩ	megaohms
Msps	megasamples per second
μA	microamperes
μF	microfarads
μH	microhenrys
μs	microseconds
μV	microvolts
μW	microwatts
mA	milliamperes
ms	milliseconds
mV	millivolts
nA	nanoamperes
ns	nanoseconds
nV	nanovolts
Ω	ohms
pF	picofarads
ppm	parts per million
ps	picoseconds
s	seconds
sps	samples per second
sqrtHz	square root of hertz
V	volts