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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	67MHz
Connectivity	I²C, LINbus, SPI, UART/USART, USB
Peripherals	CapSense, DMA, LCD, POR, PWM, WDT
Number of I/O	62
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 5.5V
Data Converters	A/D 1x20b, 2x12b; D/A 4x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c5868axi-lp032

In addition to the flexibility of the UDB array, PSoC also provides configurable digital blocks targeted at specific functions. For the CY8C58LP family, these blocks can include four 16-bit timers, counters, and PWM blocks; I^2C slave, master, and multimaster; Full-Speed USB; and Full CAN 2.0.

For more details on the peripherals see the Example Peripherals on page 40 of this datasheet. For information on UDBs, DSI, and other digital blocks, see the Digital Subsystem on page 40 of this datasheet.

PSoC's analog subsystem is the second half of its unique configurability. All analog performance is based on a highly accurate absolute voltage reference with less than 0.1% error over temperature and voltage. The configurable analog subsystem includes:

- Analog muxes
- Comparators
- Analog mixers
- Voltage references
- ADCs
- DACs
- Digital filter block (DFB)

All GPIO pins can route analog signals into and out of the device using the internal analog bus. This allows the device to interface up to 62 discrete analog signals. One of the ADCs in the analog subsystem is a fast, accurate, configurable delta-sigma ADC with these features:

- Less than 100-µV offset
- A gain error of 0.2%
- Integral non linearity (INL) less than ±2 LSB
- Differential non linearity (DNL) less than ±1 LSB
- SINAD better than 84 dB in 16-bit mode

This converter addresses a wide variety of precision analog applications including some of the most demanding sensors.

The CY8C58LP family also offers up to two SAR ADCs. Featuring 12-bit conversions at up to 1 M samples per second, they also offer low nonlinearity and offset errors and SNR better than 70 dB. They are well-suited for a variety of higher speed analog applications.

The output of any of the ADCs can optionally feed the programmable DFB via DMA without CPU intervention. You can configure the DFB to perform IIR and FIR digital filters and several user defined custom functions. The DFB can implement filters with up to 64 taps. It can perform a 48-bit multiply-accumulate (MAC) operation in one clock cycle.

Four high-speed voltage or current DACs support 8-bit output signals at an update rate of up to 8 Msps. They can be routed out of any GPIO pin. You can create higher resolution voltage PWM DAC outputs using the UDB array. This can be used to create a pulse width modulated (PWM) DAC of up to 10 bits, at up to 48 kHz. The digital DACs in each UDB support PWM, PRS, or delta-sigma algorithms with programmable widths.

In addition to the ADCs, DACs, and DFB, the analog subsystem provides multiple:

- Comparators
- Uncommitted opamps
- Configurable switched capacitor/continuous time (SC/CT) blocks. These support:
  - Transimpedance amplifiers
  - Programmable gain amplifiers
  - Mixers
  - Other similar analog components

See the "Analog Subsystem" section on page 51 of this datasheet for more details.

PSoC's CPU subsystem is built around a 32-bit three-stage pipelined ARM Cortex-M3 processor running at up to 80 MHz. The Cortex-M3 includes a tightly integrated nested vectored interrupt controller (NVIC) and various debug and trace modules. The overall CPU subsystem includes a DMA controller, flash cache, and RAM. The NVIC provides low latency, nested interrupts, and tail-chaining of interrupts and other features to increase the efficiency of interrupt handling. The DMA controller enables peripherals to exchange data without CPU involvement. This allows the CPU to run slower (saving power) or use those CPU cycles to improve the performance of firmware algorithms. The flash cache also reduces system power consumption by allowing less frequent flash access.

PSoC's nonvolatile subsystem consists of flash, byte-writeable EEPROM, and nonvolatile configuration options. It provides up to 256 KB of on-chip flash. The CPU can reprogram individual blocks of flash, enabling boot loaders. You can enable an ECC for high reliability applications. A powerful and flexible protection model secures the user's sensitive information, allowing selective memory block locking for read and write protection. Two KB of byte-writable EEPROM is available on-chip to store application data. Additionally, selected configuration options such as boot speed and pin drive mode are stored in nonvolatile memory. This allows settings to activate immediately after POR.

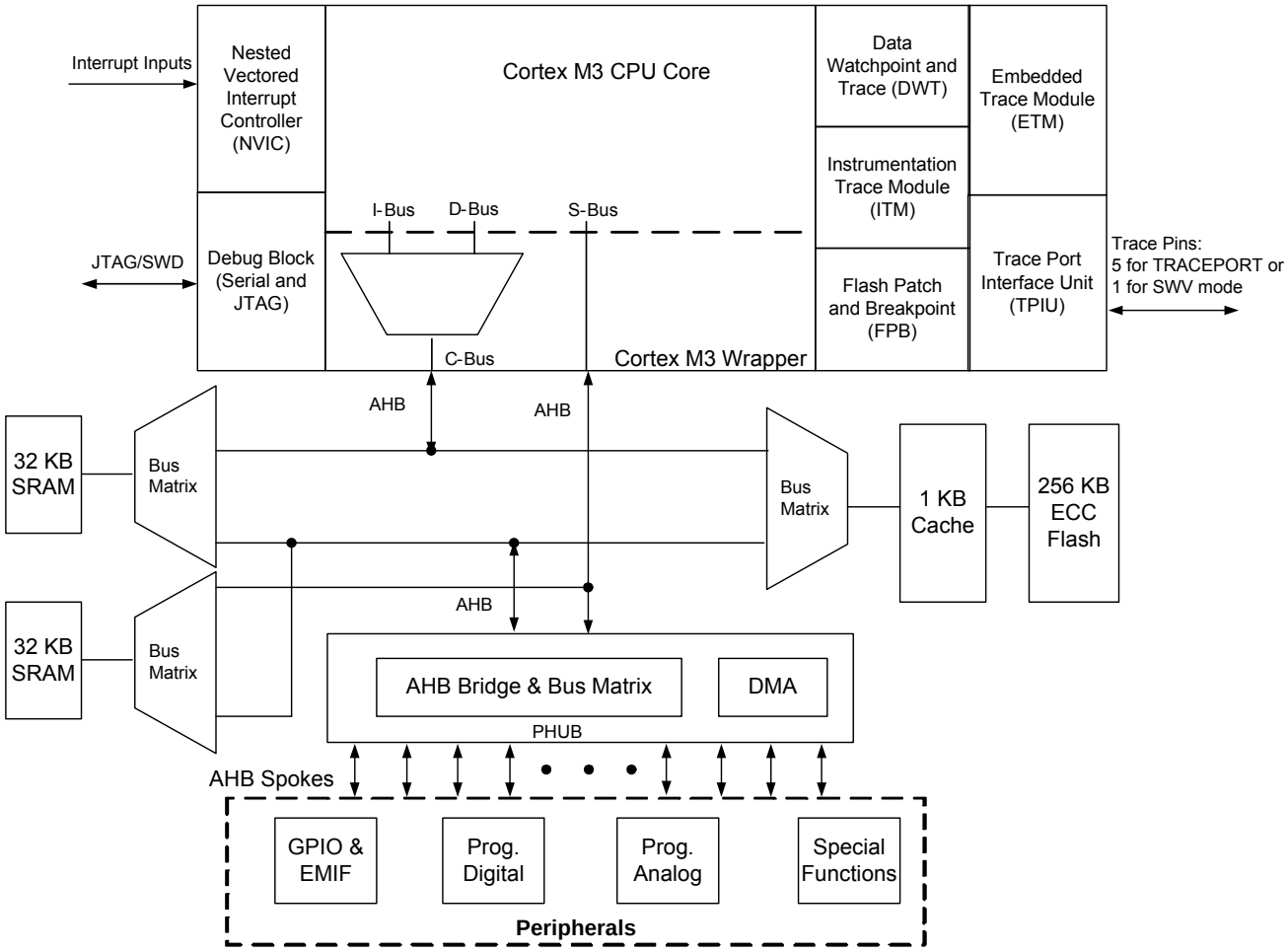
The three types of PSoC I/O are extremely flexible. All I/Os have many drive modes that are set at POR. PSoC also provides up to four I/O voltage domains through the V_{DDIO} pins. Every GPIO has analog I/O, LCD drive, CapSense, flexible interrupt generation, slew rate control, and digital I/O capability. The SIOs on PSoC allow V_{OH} to be set independently of V_{DDIO} when used as outputs. When SIOs are in input mode they are high impedance. This is true even when the device is not powered or when the pin voltage goes above the supply voltage. This makes the SIO ideally suited for use on an I^2C bus where the PSoC may not be powered when other devices on the bus are. The SIO pins also have high current sink capability for applications such as LED drives. The programmable input threshold feature of the SIO can be used to make the SIO function as a general purpose analog comparator. For devices with FS USB, the USB physical interface is also provided (USBIO). When not using USB, these pins may also be used for limited digital functionality and device programming. All the features of the PSoC I/Os are covered in detail in the I/O System and Routing on page 33 of this datasheet.

4. CPU

4.1 ARM Cortex-M3 CPU

The CY8C58LP family of devices has an ARM Cortex-M3 CPU core. The Cortex-M3 is a low-power 32-bit three-stage pipelined Harvard-architecture CPU that delivers 1.25 DMIPS/MHz. It is intended for deeply embedded applications that require fast interrupt handling features.

Figure 4-1. ARM Cortex-M3 Block Diagram



The Cortex-M3 CPU subsystem includes these features:

- ARM Cortex-M3 CPU
- Programmable nested vectored interrupt controller (NVIC), tightly integrated with the CPU core
- Full featured debug and trace modules, tightly integrated with the CPU core
- Up to 256 KB of flash memory, 2 KB of EEPROM, and 64 KB of SRAM
- Cache controller
- Peripheral HUB (PHUB)
- DMA controller
- External memory interface (EMIF)

4.1.1 Cortex-M3 Features

The Cortex-M3 CPU features include:

- 4 GB address space. Predefined address regions for code, data, and peripherals. Multiple buses for efficient and simultaneous accesses of instructions, data, and peripherals.
- The Thumb®-2 instruction set, which offers ARM-level performance at Thumb-level code density. This includes 16-bit and 32-bit instructions. Advanced instructions include:
  - Bit-field control
  - Hardware multiply and divide
  - Saturation
  - If-Then
  - Wait for events and interrupts
  - Exclusive access and barrier
  - Special register access

4.4 Interrupt Controller

The Cortex-M3 NVIC supports 16 system exceptions and 32 interrupts from peripherals, as shown in Table 4-5.

Table 4-5. Cortex-M3 Exceptions and Interrupts

Exception Number	Exception Type	Priority	Exception Table Address Offset	Function
			0x00	Starting value of R13 / MSP
1	Reset	-3 (highest)	0x04	Reset
2	NMI	-2	0x08	Non maskable interrupt
3	Hard fault	-1	0x0C	All classes of fault, when the corresponding fault handler cannot be activated because it is currently disabled or masked
4	MemManage	Programmable	0x10	Memory management fault, for example, instruction fetch from a nonexecutable region
5	Bus fault	Programmable	0x14	Error response received from the bus system; caused by an instruction prefetch abort or data access error
6	Usage fault	Programmable	0x18	Typically caused by invalid instructions or trying to switch to ARM mode
7–10	-	-	0x1C–0x28	Reserved
11	SVC	Programmable	0x2C	System service call via SVC instruction
12	Debug monitor	Programmable	0x30	Debug monitor
13	-	-	0x34	Reserved
14	PendSV	Programmable	0x38	Deferred request for system service
15	SYSTICK	Programmable	0x3C	System tick timer
16–47	IRQ	Programmable	0x40–0x3FC	Peripheral interrupt request #0 - #31

Bit 0 of each exception vector indicates whether the exception is executed using ARM or Thumb instructions. Because the Cortex-M3 only supports Thumb instructions, this bit must always be 1. The Cortex-M3 non maskable interrupt (NMI) input can be routed to any pin, via the DSI, or disconnected from all pins. See DSI Routing Interface Description on page 45.

The Nested Vectored Interrupt Controller (NVIC) handles interrupts from the peripherals, and passes the interrupt vectors to the CPU. It is closely integrated with the CPU for low latency interrupt handling. Features include:

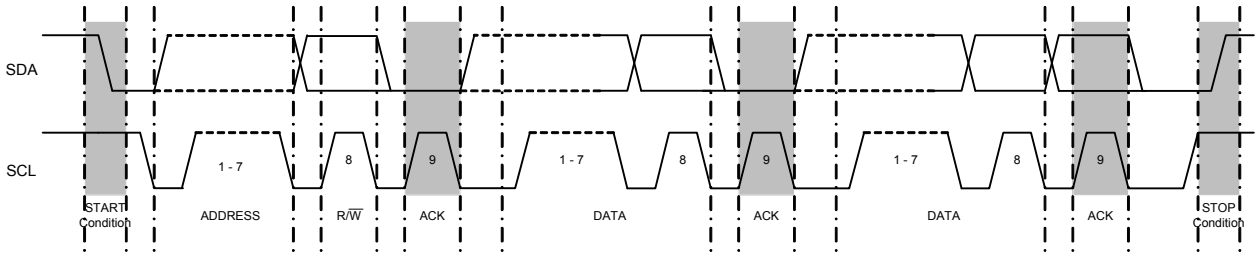
- 32 interrupts. Multiple sources for each interrupt.
- Eight priority levels, with dynamic priority control.
- Priority grouping. This allows selection of preempting and non preempting interrupt levels.
- Support for tail-chaining, and late arrival, of interrupts. This enables back-to-back interrupt processing without the overhead of state saving and restoration between interrupts.
- Processor state automatically saved on interrupt entry, and restored on interrupt exit, with no instruction overhead.

If the same priority level is assigned to two or more interrupts, the interrupt with the lower vector number is executed first. Each interrupt vector may choose from three interrupt sources: Fixed Function, DMA, and UDB. The fixed function interrupts are direct connections to the most common interrupt sources and provide the lowest resource cost connection. The DMA interrupt sources provide direct connections to the two DMA interrupt sources provided per DMA channel. The third interrupt source for vectors is from the UDB digital routing array. This allows any digital signal available to the UDB array to be used as an interrupt source. All interrupt sources may be routed to any interrupt vector using the UDB interrupt source connections.

Table 4-6. Interrupt Vector Table

Interrupt #	Cortex-M3 Exception #	Fixed Function	DMA	UDB
0	16	Low voltage detect (LVD)	phub_termout0[0]	udb_intr[0]
1	17	Cache/ECC	phub_termout0[1]	udb_intr[1]
2	18	Reserved	phub_termout0[2]	udb_intr[2]
3	19	Sleep (Pwr Mgr)	phub_termout0[3]	udb_intr[3]
4	20	PICU[0]	phub_termout0[4]	udb_intr[4]
5	21	PICU[1]	phub_termout0[5]	udb_intr[5]
6	22	PICU[2]	phub_termout0[6]	udb_intr[6]
7	23	PICU[3]	phub_termout0[7]	udb_intr[7]
8	24	PICU[4]	phub_termout0[8]	udb_intr[8]
9	25	PICU[5]	phub_termout0[9]	udb_intr[9]
10	26	PICU[6]	phub_termout0[10]	udb_intr[10]
11	27	PICU[12]	phub_termout0[11]	udb_intr[11]
12	28	PICU[15]	phub_termout0[12]	udb_intr[12]
13	29	Comparators Combined	phub_termout0[13]	udb_intr[13]
14	30	Switched Caps Combined	phub_termout0[14]	udb_intr[14]
15	31	I^2C	phub_termout0[15]	udb_intr[15]
16	32	CAN	phub_termout1[0]	udb_intr[16]
17	33	Timer/Counter0	phub_termout1[1]	udb_intr[17]
18	34	Timer/Counter1	phub_termout1[2]	udb_intr[18]
19	35	Timer/Counter2	phub_termout1[3]	udb_intr[19]
20	36	Timer/Counter3	phub_termout1[4]	udb_intr[20]
21	37	USB SOF Int	phub_termout1[5]	udb_intr[21]
22	38	USB Arb Int	phub_termout1[6]	udb_intr[22]
23	39	USB Bus Int	phub_termout1[7]	udb_intr[23]
24	40	USB Endpoint[0]	phub_termout1[8]	udb_intr[24]
25	41	USB Endpoint Data	phub_termout1[9]	udb_intr[25]
26	42	Reserved	phub_termout1[10]	udb_intr[26]
27	43	LCD	phub_termout1[11]	udb_intr[27]
28	44	DFB Int	phub_termout1[12]	udb_intr[28]
29	45	Decimator Int	phub_termout1[13]	udb_intr[29]
30	46	phub_err_int	phub_termout1[14]	udb_intr[30]
31	47	eeprom_fault_int	phub_termout1[15]	udb_intr[31]

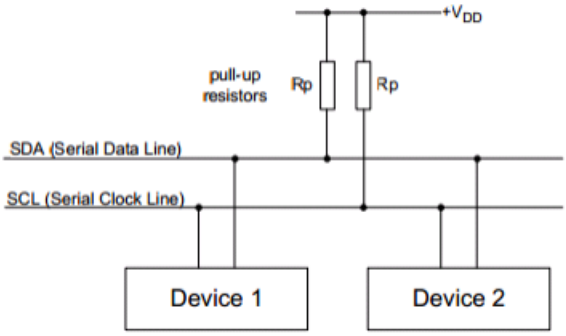
Figure 7-18. I²C Complete Transfer Timing



7.8.1 External Electrical Connections

As Figure 7-19 shows, the I²C bus requires external pull-up resistors (R_P). These resistors are primarily determined by the supply voltage, bus speed, and bus capacitance. For detailed information on how to calculate the optimum pull-up resistor value for your design, we recommend using the UM10204 I2C-bus specification and user manual Rev 6, or newer, available from the NXP website at www.nxp.com.

Figure 7-19. Connection of Devices to the I²C Bus



For most designs, the default values in Table 7-2 will provide excellent performance without any calculations. The default values were chosen to use standard resistor values between the minimum and maximum limits. The values in Table 7-2 work for designs with 1.8 V to 5.0V V_{DD}, less than 200-pF bus capacitance (C_B), up to 25 µA of total input leakage (I_{IL}), up to 0.4 V output voltage level (V_{OL}), and a max V_{IH} of 0.7 * V_{DD}. Standard Mode and Fast Mode can use either GPIO or SIO PSoC pins. Fast Mode Plus requires use of SIO pins to meet the V_{OL} spec at 20 mA. Calculation of custom pull-up resistor values is required; if your design does not meet the default assumptions, you use series resistors (RS) to limit injected noise, or you need to maximize the resistor value for low power consumption.

Table 7-2. Recommended default Pull-up Resistor Values

	R_P	Units
Standard Mode – 100 kbps	4.7 k, 5%	Ω
Fast Mode – 400 kbps	1.74 k, 1%	Ω
Fast Mode Plus – 1 Mbps	620, 5%	Ω

Calculation of the ideal pull-up resistor value involves finding a value between the limits set by three equations detailed in the NXP I²C specification. These equations are:

Equation 1:

$$R_{PMIN} = (V_{DD}(max) - V_{OL}(max))/(I_{OL}(min))$$

Equation 2:

$$R_{PMAX} = T_R(max)/0.8473 \times C_B(max)$$

Equation 3:

$$R_{PMAX} = V_{DD}(min) - V_{IH}(min) + V_{NH}(min)/I_{IH}(max)$$

Equation parameters:

V_{DD} = Nominal supply voltage for I²C bus

V_{OL} = Maximum output low voltage of bus devices.

I_{OL}= Low-level output current from I²C specification

T_R = Rise Time of bus from I²C specification

C_B = Capacitance of each bus line including pins and PCB traces

V_{IH} = Minimum high-level input voltage of all bus devices

V_{NH} = Minimum high-level input noise margin from I²C specification

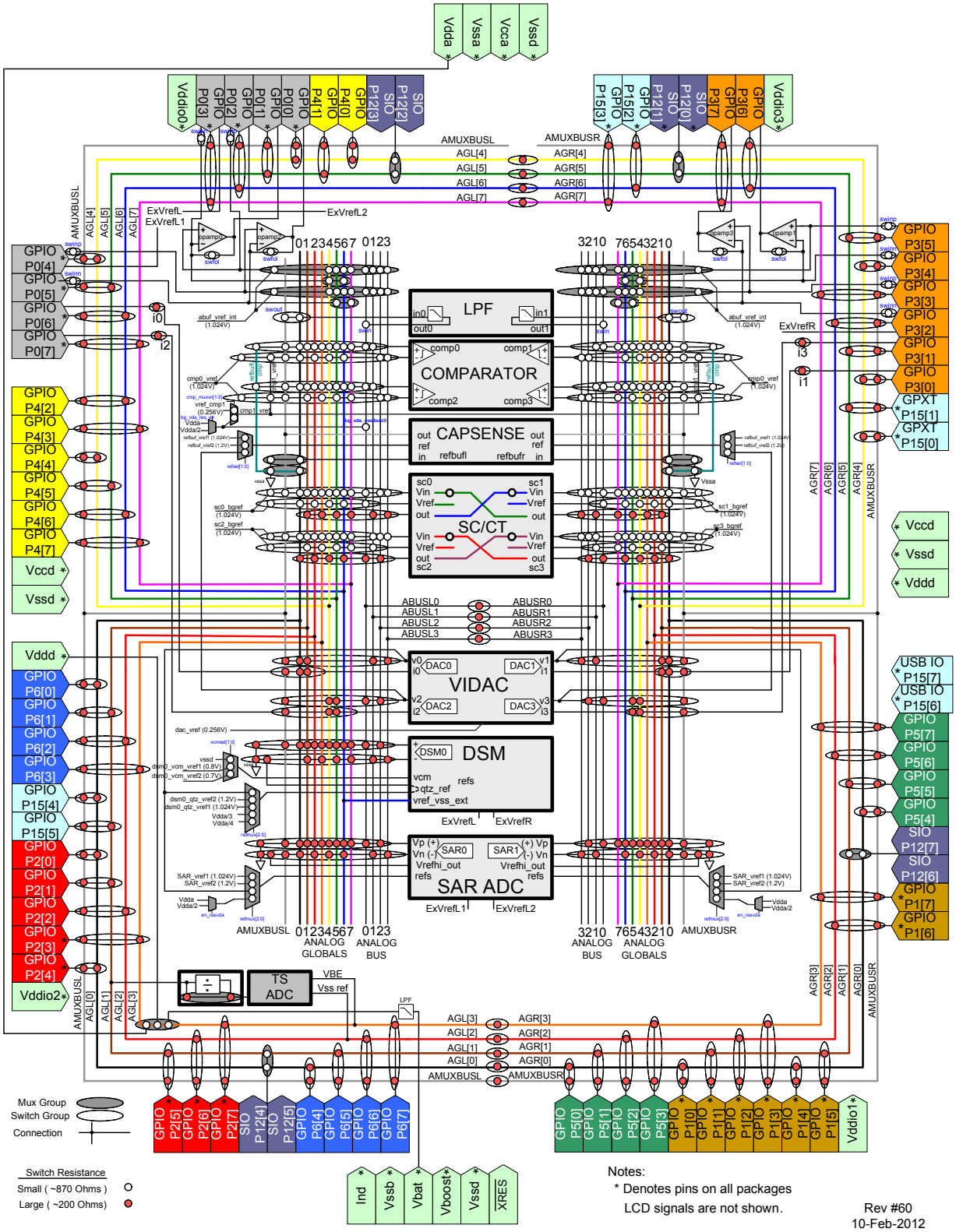
I_{IH} = Total input leakage current of all devices on the bus

The supply voltage (V_{DD}) limits the minimum pull-up resistor value due to bus devices maximum low output voltage (V_{OL}) specifications. Lower pull-up resistance increases current though the pins and can, therefore, exceed the spec conditions of V_{OH}. Equation 1 is derived using Ohm's law to determine the minimum resistance that will still meet the V_{OL} specification at 3 mA for standard and fast modes, and 20 mA for fast mode plus at the given V_{DD}.

Equation 2 determines the maximum pull-up resistance due to bus capacitance. Total bus capacitance is comprised of all pin, wire, and trace capacitance on the bus. The higher the bus capacitance, the lower the pull-up resistance required to meet the specified bus speeds rise time due to RC delays. Choosing a pull-up resistance higher than allowed can result in failing timing requirements resulting in communication errors. Most designs with five or less I²C devices and up to 20 centimeters of bus trace length have less than 100 pF of bus capacitance.

A secondary effect that limits the maximum pull-up resistor value is total bus leakage calculated in Equation 3. The primary source of leakage is I/O pins connected to the bus. If leakage is too high, the pull-ups will have difficulty maintaining an acceptable V_{IH} level causing communication errors. Most designs with five or less I²C devices on the bus have less than 10 µA of total leakage current.

Figure 8-2. CY8C58LP Analog Interconnect



To preserve detail of this figure, this figure is best viewed with a PDF display program or printed on a 11” × 17” paper.

8.7.1 LCD Segment Pin Driver

Each GPIO pin contains an LCD driver circuit. The LCD driver buffers the appropriate output of the LCD DAC to directly drive the glass of the LCD. A register setting determines whether the pin is a common or segment. The pin's LCD driver then selects one of the six bias voltages to drive the I/O pin, as appropriate for the display data.

8.7.2 Display Data Flow

The LCD segment driver system reads display data and generates the proper output voltages to the LCD glass to produce the desired image. Display data resides in a memory buffer in the system SRAM. Each time you need to change the common and segment driver voltages, the next set of pixel data moves from the memory buffer into the Port Data Registers via DMA.

8.7.3 UDB and LCD Segment Control

A UDB is configured to generate the global LCD control signals and clocking. This set of signals is routed to each LCD pin driver through a set of dedicated LCD global routing channels. In addition to generating the global LCD control signals, the UDB also produces a DMA request to initiate the transfer of the next frame of LCD data.

8.7.4 LCD DAC

The LCD DAC generates the contrast control and bias voltage for the LCD system. The LCD DAC produces up to five LCD drive voltages plus ground, based on the selected bias ratio. The bias voltages are driven out to GPIO pins on a dedicated LCD bias bus, as required.

8.8 CapSense

The CapSense system provides a versatile and efficient means for measuring capacitance in applications such as touch sense buttons, sliders, proximity detection, etc. The CapSense system uses a configuration of system resources, including a few hardware functions primarily targeted for CapSense. Specific resource usage is detailed in the CapSense component in PSoC Creator.

A capacitive sensing method using a Delta-Sigma Modulator (CSD) is used. It provides capacitance sensing using a switched capacitor technique with a delta-sigma modulator to convert the sensing current to a digital code.

8.9 Temp Sensor

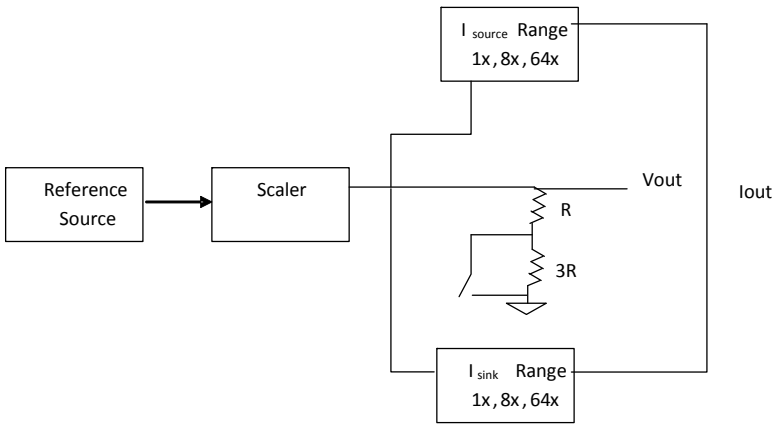
Die temperature is used to establish programming parameters for writing flash. Die temperature is measured using a dedicated sensor based on a forward biased transistor. The temperature sensor has its own auxiliary ADC.

8.10 DAC

The CY8C58LP parts contain four Digital to Analog Convertors (DACs). Each DAC is 8-bit and can be configured for either voltage or current output. The DACs support CapSense, power supply regulation, and waveform generation. Each DAC has the following features.

- Adjustable voltage or current output in 255 steps
- Programmable step size (range selection)
- Eight bits of calibration to correct ± 25% of gain error
- Source and sink option for current output
- 8 Msps conversion rate for current output
- 1 Msps conversion rate for voltage output
- Monotonic in nature
- Data and strobe inputs can be provided by the CPU or DMA, or routed directly from the DSI
- Dedicated low-resistance output pin for high-current mode

Figure 8-12. DAC Block Diagram



8.10.1 Current DAC

The current DAC (IDAC) can be configured for the ranges 0 to 31.875 µA, 0 to 255 µA, and 0 to 2.04 mA. The IDAC can be configured to source or sink current.

8.10.2 Voltage DAC

For the voltage DAC (VDAC), the current DAC output is routed through resistors. The two ranges available for the VDAC are 0 to 1.02 V and 0 to 4.08 V. In voltage mode any load connected to the output of a DAC should be purely capacitive (the output of the VDAC is not buffered).

Table 11-2. DC Specifications (continued)

Parameter	Description	Conditions		Min	Typ	Max	Units
I_{DD}[26]	**Hibernate Mode**						
	Hibernate mode current All regulators and oscillators off. SRAM retention GPIO interrupts are active Boost = OFF SIO pins in single ended input, unregulated output mode	V_{DD} = V_{DDIO} = 4.5–5.5 V	T = –40 °C	–	0.2	2	µA
			T = 25 °C	–	0.24	2	
			T = 85 °C	–	2.6	15	
			T = 105 °C	–	2.6	15	
		V_{DD} = V_{DDIO} = 2.7–3.6 V	T = –40 °C	–	0.11	2	
			T = 25 °C	–	0.3	2	
			T = 85 °C	–	2	15	
			T = 105 °C	–	2	15	
		V_{DD} = V_{DDIO} = 1.71–1.95 V	T = –40 °C	–	0.9	2	
			T = 25 °C	–	0.11	2	
			T = 85 °C	–	1.8	15	
			T = 105 °C	–	1.8	15	
I_{DDAR}[27]	Analog current consumption while device is reset	$V_{DDA} \le 3.6$ V		–	0.3	0.6	mA
		$V_{DDA} > 3.6$ V		–	1.4	3.3	mA
I_{DDDR}[27]	Digital current consumption while device is reset	$V_{DDD} \le 3.6$ V		–	1.1	3.1	mA
		$V_{DDD} > 3.6$ V		–	0.7	3.1	mA
I_{DD_PROG}[27]	Current consumption while device programming. Sum of digital, analog, and I/Os: IDDD + IDDA + IDDIOX.			–	15	21	mA

Figure 11-1. Active Mode Current vs F_{CPU}, V_{DD} = 3.3 V, Temperature = 25 °C

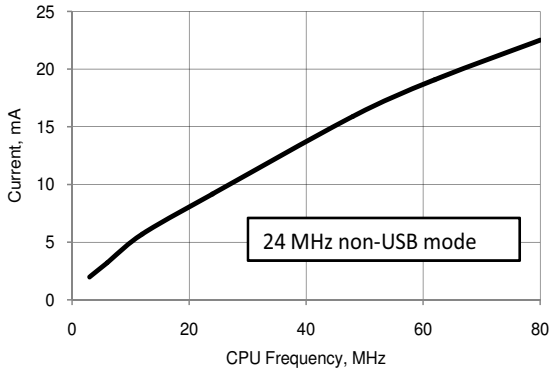


Figure 11-2. I_{DD} vs Frequency at 25 °C

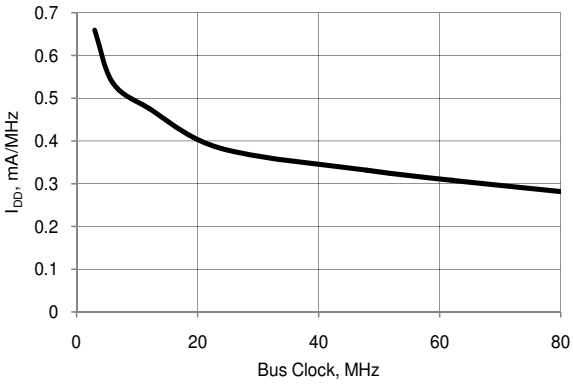


Figure 11-3. Active Mode Current vs Temperature and F_{CPU}, V_{DD} = 3.3 V

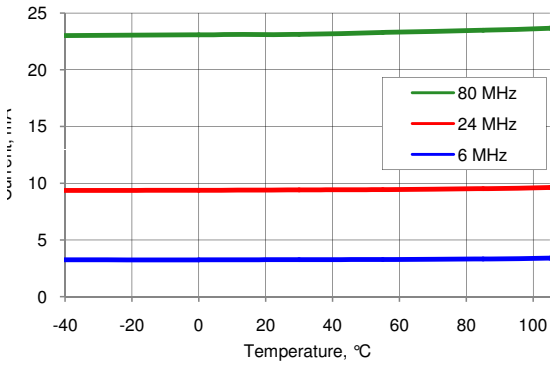
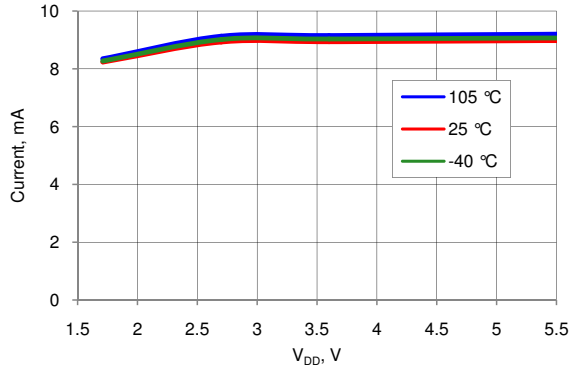


Figure 11-4. Active Mode Current vs V_{DD} and Temperature, F_{CPU} = 24 MHz



Notes

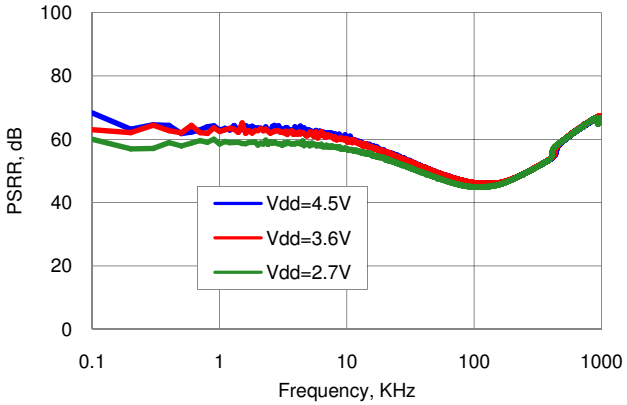
26. The current consumption of additional peripherals that are implemented only in programmed logic blocks can be found in their respective datasheets, available in PSoC Creator, the integrated design environment. To estimate total current, find CPU current at frequency of interest and add peripheral currents for your particular system from the device datasheet and component datasheets.
27. Based on device characterization (Not production tested).

11.3.2 Analog Core Regulator

Table 11-5. Analog Core Regulator DC *Specifications*

Parameter	Description	Conditions	Min	Typ	Max	Units
V_{DDA}	Input voltage		1.8	–	5.5	V
V_{CCA}	Output voltage		–	1.80	–	V
	Regulator output capacitor	±10%, X5R ceramic or better	0.9	1	1.1	µF

Figure 11-7. Analog Regulator PSRR vs Frequency and V_{DD}



11.3.3 Inductive Boost Regulator

Unless otherwise specified, operating conditions are: V_{BAT} = 0.5 V–3.6 V, V_{OUT} = 1.8 V–5.0 V, I_{OUT} = 0 mA–50 mA, L_{BOOST} = 4.7 µH–22 µH, C_{BOOST} = 22 µF || 3 × 1.0 µF || 3 × 0.1 µF, C_{BAT} = 22 µF, I_F = 1.0 A, excludes 99-pin CSP package. For information on using boost with 99-pin CSP package, contact Cypress support. Unless otherwise specified, all charts and graphs show typical values.

Table 11-6. Inductive Boost Regulator DC Specifications

Parameter	Description	Conditions		Min	Typ	Max	Units
V_{OUT}	Boost output voltage[29]	vsel = 1.8 V in register BOOST_CR0		1.71	1.8	1.89	V
		vsel = 1.9 V in register BOOST_CR0		1.81	1.90	2.00	V
		vsel = 2.0 V in register BOOST_CR0		1.90	2.00	2.10	V
		vsel = 2.4 V in register BOOST_CR0		2.16	2.40	2.64	V
		vsel = 2.7 V in register BOOST_CR0		2.43	2.70	2.97	V
		vsel = 3.0 V in register BOOST_CR0		2.70	3.00	3.30	V
		vsel = 3.3 V in register BOOST_CR0		2.97	3.30	3.63	V
		vsel = 3.6 V in register BOOST_CR0		3.24	3.60	3.96	V
		vsel = 5.0 V in register BOOST_CR0		4.50	5.00	5.50	V
V_{BAT}	Input voltage to boost[30]	I_{OUT} = 0 mA–5 mA	vsel = 1.8 V–2.0 V, T_A = 0 °C–70 °C	0.5	–	0.8	V
		I_{OUT} = 0 mA–15 mA	vsel = 1.8 V–5.0 V[31], T_A = –10 °C–85 °C	1.6	–	3.6	V
		I_{OUT} = 0 mA–25 mA	vsel = 1.8 V–2.7 V, T_A = –10 °C–85 °C	0.8	–	1.6	V
		I_{OUT} = 0 mA–50 mA	vsel = 1.8 V–3.3 V[31], T_A = –40 °C–85 °C	1.8	–	2.5	V
			vsel = 1.8 V–3.3 V[31], T_A = –10 °C–85 °C	1.3	–	2.5	V
			vsel = 2.5 V–5.0 V[31], T_A = –10 °C–85 °C	2.5	–	3.6	V

11.5 Analog Peripherals

Specifications are valid for –40 °C ≤ T_A ≤ 105 °C and T_J ≤ 120 °C, except where noted. Specifications are valid for 1.71 V to 5.5 V, except where noted.

11.5.1 Opamp

Table 11-18. Opamp DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
V_I	Input voltage range		V_{SSA}	–	V_{DDA}	V
Vos	Input offset voltage		–	–	2.5	mV
		Operating temperature –40 °C to 70 °C	–	–	2	mV
TCVos	Input offset voltage drift with temperature	Power mode = high	–	–	±30	µV / °C
Ge1	Gain error, unity gain buffer mode	Rload = 1 kΩ	–	–	±0.1	%
Cin	Input capacitance	Routing from pin	–	–	18	pF
Vo	Output voltage range	1 mA, source or sink, power mode = high	V_{SSA} + 0.05	–	V_{DDA} – 0.05	V
Iout	Output current capability, source or sink	V_{SSA} + 500 mV ≤ V_{OUT} ≤ V_{DDA} –500 mV, V_{DDA} > 2.7 V	25	–	–	mA
		V_{SSA} + 500 mV ≤ V_{OUT} ≤ V_{DDA} –500 mV, 1.7 V = V_{DDA} ≤ 2.7 V	16	–	–	mA
Idd	Quiescent current[43]	Power mode = min	–	250	400	uA
		Power mode = low	–	250	400	uA
		Power mode = med	–	330	950	uA
		Power mode = high	–	1000	2500	uA
CMRR	Common mode rejection ratio[43]		80	–	–	dB
PSRR	Power supply rejection ratio[43]	V_{DDA} ≥ 2.7 V	85	–	–	dB
		V_{DDA} < 2.7 V	70	–	–	dB
I_{IB}	Input bias current[43]	25 °C	–	10	–	pA

Figure 11-25. Opamp Vos Histogram, 7020 samples/1755 parts, 30 °C, VDDA = 3.3 V

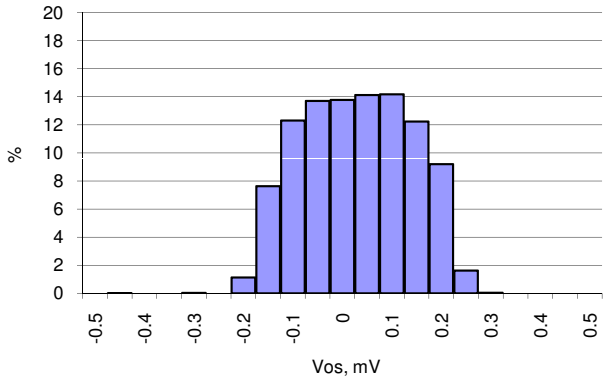
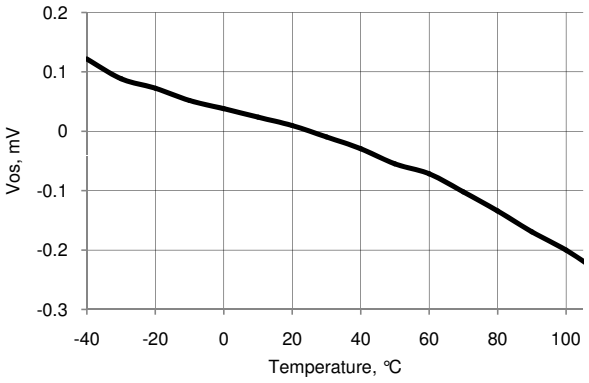


Figure 11-26. Opamp Vos vs Temperature, V_{DDA} = 5 V



Note
43. Based on device characterization (Not production tested).

Table 11-26. Delta-sigma ADC RMS Noise in Counts vs. Input Range and Sample Rate, 20-bit, External Reference, Differential[49]

Sample Rate, SPS	Input Voltage Range				
	± VREF	± VREF/2	± VREF/4	± VREF/8	± VREF/16
8	1.01	1.03	1.31	1.78	3.57
12	0.99	1.21	1.45	1.80	3.61
23	0.94	1.26	1.69	2.91	3.92
45	1.06	1.35	1.70	2.07	3.83
61	1.08	1.35	0.95	2.20	3.96
170	1.02	1.36			
187	0.96				

Figure 11-37. Delta-sigma ADC DNL vs Output Code, 16-bit, 48 ksps, 25 °C V_{DDA} = 3.3 V

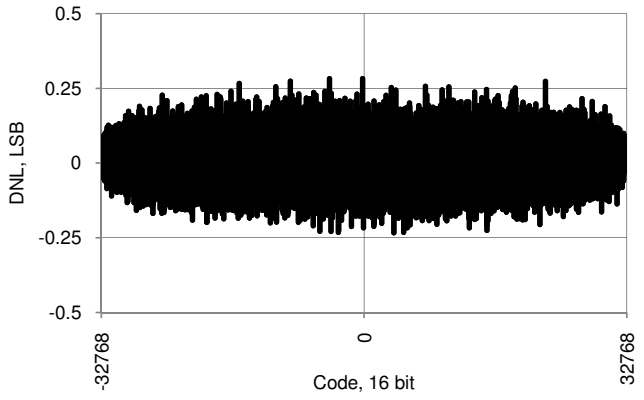
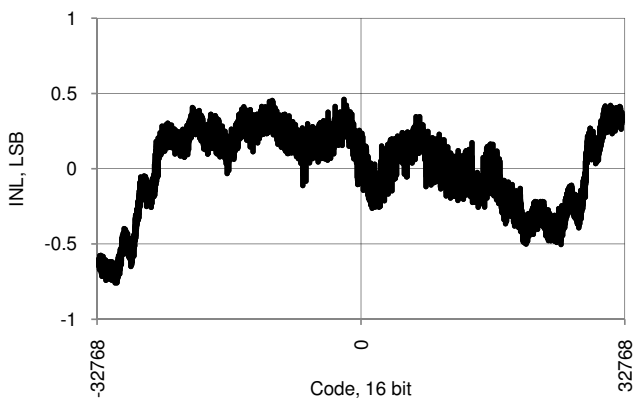


Figure 11-38. Delta-sigma ADC INL vs Output Code, 16-bit, 48 ksps, 25 °C V_{DDA} = 3.3 V



Note
49. The RMS noise (in volts) is the range (in volts) times noise in counts divided by 2^number of bits. RMS Noise = (Range × Counts) / 2^bits

11.6.2 Counter

The following specifications apply to the Timer/Counter/PWM peripheral, in counter mode. Counters can also be implemented in UDBs; for more information, see the Counter component datasheet in PSoC Creator.

Table 11-49. Counter DC Specifications[72]

Parameter	Description	Conditions	Min	Typ	Max	Units
	Block current consumption	16-bit counter, at listed input clock frequency	–	–	–	µA
	3 MHz		–	15	–	µA
	12 MHz		–	60	–	µA
	48 MHz		–	260	–	µA
	80 MHz		–	360	–	µA

Table 11-50. Counter AC Specifications[72]

Parameter	Description	Conditions	Min	Typ	Max	Units
	Operating frequency		DC	–	80.01	MHz
	Capture pulse[73]		15	–	–	ns
	Resolution[73]		15	–	–	ns
	Pulse width[73]		15	–	–	ns
	Pulse width (external)		30			ns
	Enable pulse width[73]		15	–	–	ns
	Enable pulse width (external)		30	–	–	ns
	Reset pulse width[73]		15	–	–	ns
	Reset pulse width (external)		30	–	–	ns

Notes
72. Based on device characterization (Not production tested).
73. For correct operation, the minimum Timer/Counter/PWM input pulse width is the period of bus clock.

11.7 Memory

Specifications are valid for –40 °C ≤ T_A ≤ 105 °C and T_J ≤ 120 °C, except where noted. Specifications are valid for 1.71 V to 5.5 V, except where noted.

11.7.1 Flash

Table 11-61. Flash DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Erase and program voltage	V_{DDD} pin	1.71	–	5.5	V

Table 11-62. Flash AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
T_{WRITE}	Row write time (erase + program)		–	15	20	ms
T_{ERASE}	Row erase time		–	10	13	ms
	Row program time		–	5	7	ms
T_{BULK}	Bulk erase time (256 KB)		–	–	140	ms
	Sector erase time (16 KB)		–	–	15	ms
T_{PROG}	Total device programming time	No overhead[80]	–	5	7.5	seconds
	Flash data retention time, retention period measured from last erase cycle	Ambient temp. T_A ≤ 55 °C, 100 K erase/program cycles	20	–	–	years
		Ambient temp. T_A ≤ 85 °C, 10 K erase/program cycles	10	–	–	
		Ambient temp. T_A ≤ 105 °C, 10 K erase/program cycles, ≤ one year at T_A ≥ 75 °C [81]	10	–	–	

11.7.2 EEPROM

Table 11-63. EEPROM DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Erase and program voltage		1.71	–	5.5	V

Table 11-64. EEPROM AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
T_{WRITE}	Single row erase/write cycle time		–	10	20	ms
	EEPROM data retention time, retention period measured from last erase cycle	Ambient temp, T_A ≤ 25 °C, 1M erase/program cycles	20	–	–	years
		Ambient temp, T_A ≤ 55 °C, 100K erase/program cycles	20	–	–	
		Ambient temp. T_A ≤ 85 °C, 10K erase/program cycles	10	–	–	
		Ambient temp. T_A ≤ 105 °C, 10K erase/program cycles, ≤ one year at T_A ≥75 °C [81]	10	–	–	

Notes
80. See PSoC 5 Device Programming Specifications for a description of a low-overhead method of programming PSoC 5 flash.
81. Cypress provides a retention calculator to calculate the retention lifetime based on customers' individual temperature profiles for operation over the –40 °C to +105 °C ambient temperature range. Contact customercare@cypress.com.

11.7.3 Nonvolatile Latches (NVL)

Table 11-65. NVL DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Erase and program voltage	V_{DDD} pin	1.71	–	5.5	V

Table 11-66. NVL AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	NVL endurance	Programmed at 25 °C	1K	–	–	program/ erase cycles
		Programmed at 0 °C to 70 °C	100	–	–	program/ erase cycles
	NVL data retention time	Ambient temp. $T_A \le 55$ °C	20	–	–	years
		Ambient temp. $T_A \le 85$ °C	10	–	–	
		Ambient temp. $T_A \le 105$ °C, ≤ one year at $T_A \ge 75$ °C [82]	10	–	–	

11.7.4 SRAM

Table 11-67. SRAM DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
V_{SRAM}	SRAM retention voltage[83]		1.2	–	–	V

Table 11-68. SRAM AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
F_{SRAM}	SRAM operating frequency		DC	–	80.01	MHz

Notes
82. Cypress provides a retention calculator to calculate the retention lifetime based on customers' individual temperature profiles for operation over the –40 °C to +105 °C ambient temperature range. Contact customercare@cypress.com.
83. Based on device characterization (Not production tested).

11.8 PSoC System Resources

Specifications are valid for –40 °C ≤ T_A ≤ 105 °C and T_J ≤ 120 °C, except where noted. Specifications are valid for 1.71 V to 5.5 V, except where noted.

11.8.1 POR with Brown Out

For brown out detect in regulated mode, V_{DDD} and V_{DDA} must be ≥ 2.0 V. Brown out detect is not available in externally regulated mode.

Table 11-71. Precise Low-Voltage Reset (PRES) with Brown Out DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
PRESR	Rising trip voltage	Factory trim	1.64	–	1.68	V
PRESF	Falling trip voltage		1.62	–	1.66	V

Table 11-72. Power-On-Reset (POR) with Brown Out AC Specifications[90]

Parameter	Description	Conditions	Min	Typ	Max	Units
PRES_TR[91]	Response time		–	–	0.5	µs
	V_{DDD}/V_{DDA} droop rate	Sleep mode	–	5	–	V/sec

11.8.2 Voltage Monitors

Table 11-73. Voltage Monitors DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
LVI	Trip voltage					
	LVI_A/D_SEL[3:0] = 0000b		1.68	1.73	1.77	V
	LVI_A/D_SEL[3:0] = 0001b		1.89	1.95	2.01	V
	LVI_A/D_SEL[3:0] = 0010b		2.14	2.20	2.27	V
	LVI_A/D_SEL[3:0] = 0011b		2.38	2.45	2.53	V
	LVI_A/D_SEL[3:0] = 0100b		2.62	2.71	2.79	V
	LVI_A/D_SEL[3:0] = 0101b		2.87	2.95	3.04	V
	LVI_A/D_SEL[3:0] = 0110b		3.11	3.21	3.31	V
	LVI_A/D_SEL[3:0] = 0111b		3.35	3.46	3.56	V
	LVI_A/D_SEL[3:0] = 1000b		3.59	3.70	3.81	V
	LVI_A/D_SEL[3:0] = 1001b		3.84	3.95	4.07	V
	LVI_A/D_SEL[3:0] = 1010b		4.08	4.20	4.33	V
	LVI_A/D_SEL[3:0] = 1011b		4.32	4.45	4.59	V
	LVI_A/D_SEL[3:0] = 1100b		4.56	4.70	4.84	V
	LVI_A/D_SEL[3:0] = 1101b		4.83	4.98	5.13	V
	LVI_A/D_SEL[3:0] = 1110b		5.05	5.21	5.37	V
	LVI_A/D_SEL[3:0] = 1111b		5.30	5.47	5.63	V
HVI	Trip voltage		5.57	5.75	5.92	V

Table 11-74. Voltage Monitors AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
LVI_tr[91]	Response time		–	–	1	µs

Notes
90. Based on device characterization (Not production tested).
91. This value is calculated, not measured.

11.8.3 Interrupt Controller

Table 11-75. Interrupt Controller AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Delay from interrupt signal input to ISR code execution from main line code[92]		–	–	12	Tcy CPU
	Delay from interrupt signal input to ISR code execution from ISR code (tail-chaining)[92]		–	–	6	Tcy CPU

11.8.4 JTAG Interface

Figure 11-79. JTAG Interface Timing

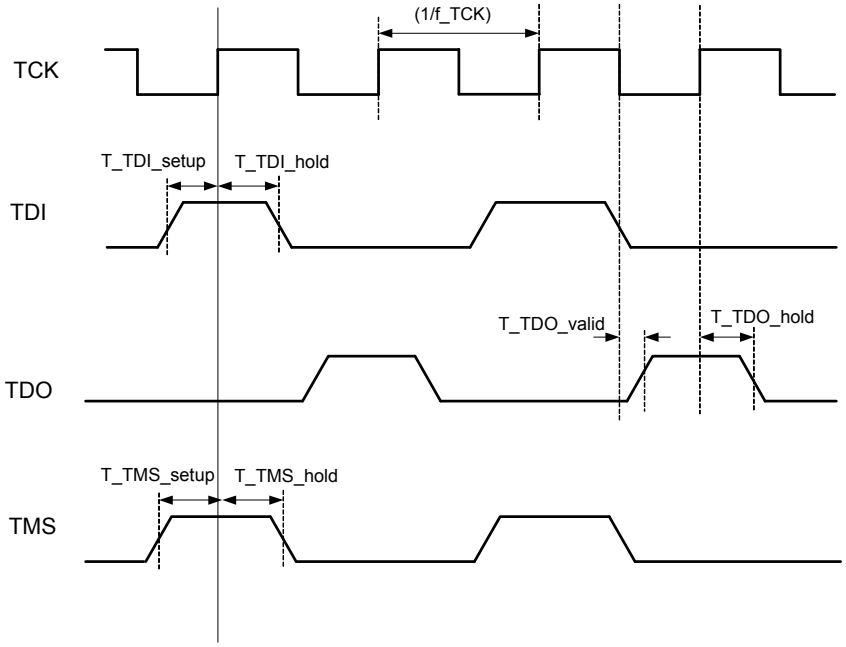


Table 11-76. JTAG Interface AC Specifications[93]

Parameter	Description	Conditions	Min	Typ	Max	Units
f_TCK	TCK frequency	3.3 V ≤ V_{DDD} ≤ 5 V	–	–	12[94]	MHz
		1.71 V ≤ V_{DDD} < 3.3 V	–	–	7[94]	MHz
T_TDI_setup	TDI setup before TCK high		(T/10) – 5	–	–	ns
T_TMS_setup	TMS setup before TCK high		T/4	–	–	
T_TDI_hold	TDI, TMS hold after TCK high	T = 1/f_TCK max	T/4	–	–	
T_TDO_valid	TCK low to TDO valid	T = 1/f_TCK max	–	–	2T/5	
T_TDO_hold	TDO hold after TCK high	T = 1/f_TCK max	T/4	–	–	
T_nTRST	Minimum nTRST pulse width	f_TCK = 2 MHz	8	–	–	ns

Notes
92. ARM Cortex-M3 NVIC spec. Visit www.arm.com for detailed documentation about the Cortex-M3 CPU.
93. Based on device characterization (Not production tested).
94. f_TCK must also be no more than 1/3 CPU clock frequency.

Table 11-80. IMO AC Specifications (continued)

Parameter	Description	Conditions	Min	Typ	Max	Units
Tstart_imo	Startup time[100]	From enable (during normal system operation)	–	–	13	µs
Jp-p	Jitter (peak to peak)[100]					
	F = 24 MHz		–	0.9	–	ns
	F = 3 MHz		–	1.6	–	ns
Jperiod	Jitter (long term)[101]					
	F = 24 MHz		–	0.9	–	ns
	F = 3 MHz		–	12	–	ns

Figure 11-82. IMO Frequency Variation vs. Temperature

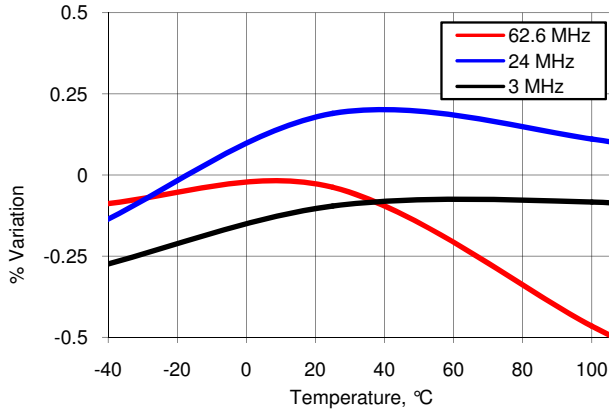
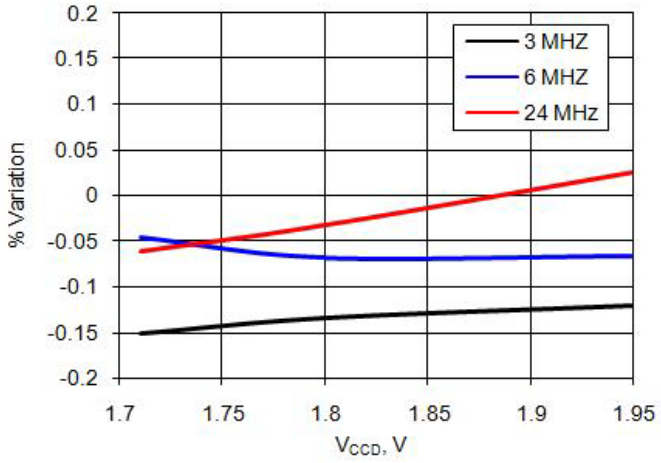


Figure 11-83. IMO Frequency Variation vs. V_{CC}



Notes
99. F_{IMO} is measured after packaging, and thus accounts for substrate and die attach stresses.
100. Based on device characterization (Not production tested).
101. Based on device characterization (Not production tested). USBIO pins tied to ground (VSSD).

11.9.3 MHz External Crystal Oscillator

For more information on crystal or ceramic resonator selection for the MHzECO, refer to application note AN54439: PSoC 3 and PSoC 5 External Oscillators.

Table 11-83. MHzECO DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
I_{CC}	Operating current[104]	13.56 MHz crystal	–	3.8	–	mA

Table 11-84. MHzECO AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
F	Crystal frequency range		4	–	25	MHz

11.9.4 kHz External Crystal Oscillator

Table 11-85. kHzECO DC Specifications[104]

Parameter	Description	Conditions	Min	Typ	Max	Units
I_{CC}	Operating current	Low power mode; CL = 6 pF	–	0.25	1.0	µA
DL	Drive level		–	–	1	µW

Table 11-86. kHzECO AC Specifications[104]

Parameter	Description	Conditions	Min	Typ	Max	Units
F	Frequency		–	32.768	–	kHz
T_{ON}	Startup time	High power mode	–	1	–	s

11.9.5 External Clock Reference

Table 11-87. External Clock Reference AC Specifications[104]

Parameter	Description	Conditions	Min	Typ	Max	Units
	External frequency range		0	–	33	MHz
	Input duty cycle range	Measured at $V_{DDIO}/2$	30	50	70	%
	Input edge rate	V_{IL} to V_{IH}	0.5	–	–	V/ns

11.9.6 Phase-Locked Loop

Table 11-88. PLL DC Specifications

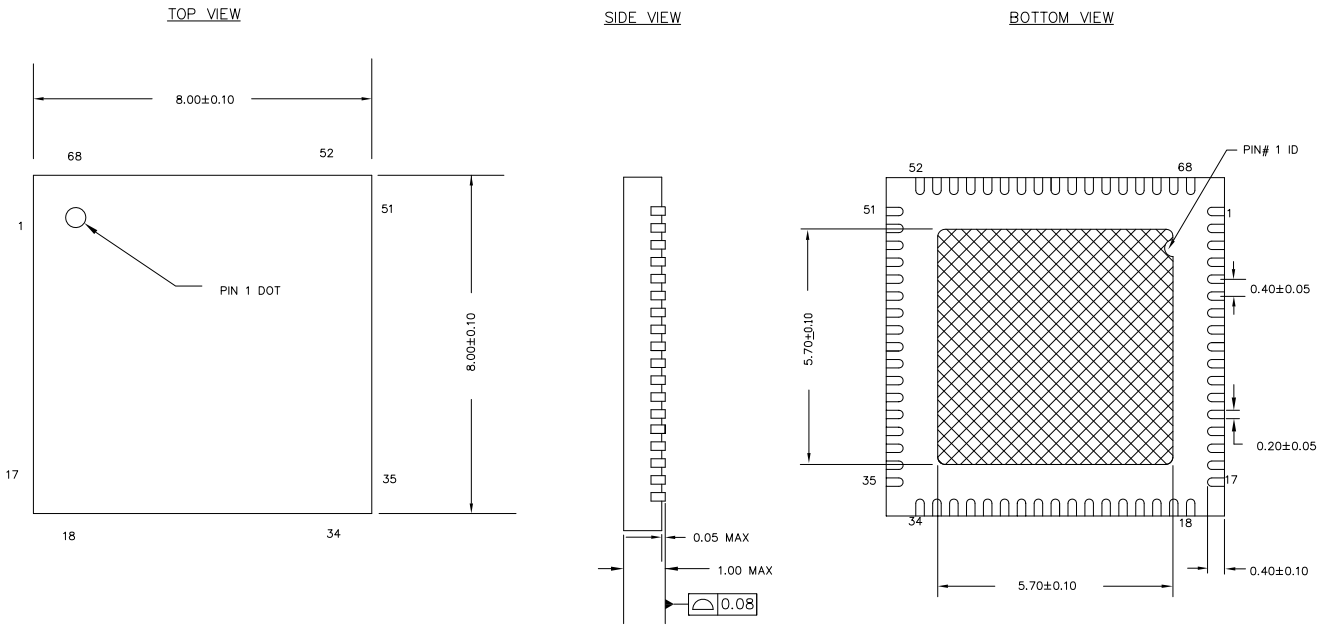
Parameter	Description	Conditions	Min	Typ	Max	Units
I_{DD}	PLL operating current	In = 3 MHz, Out = 80 MHz	–	650	–	µA
		In = 3 MHz, Out = 67 MHz	–	400	–	µA
		In = 3 MHz, Out = 24 MHz	–	200	–	µA

Table 11-89. PLL AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
Fpllin	PLL input frequency[105]		1	–	48	MHz
	PLL intermediate frequency[106]	Output of prescaler	1	–	3	MHz
Fpllout	PLL output frequency[105]		24	–	80	MHz
	Lock time at startup		–	–	250	µs
Jperiod-rms	Jitter (rms)[104]		–	–	250	ps

Notes
104.Based on device characterization (Not production tested).
105.This specification is guaranteed by testing the PLL across the specified range using the IMO as the source for the PLL.
106.PLL input divider, Q, must be set so that the input frequency is divided down to the intermediate frequency range. Value for Q ranges from 1 to 16.

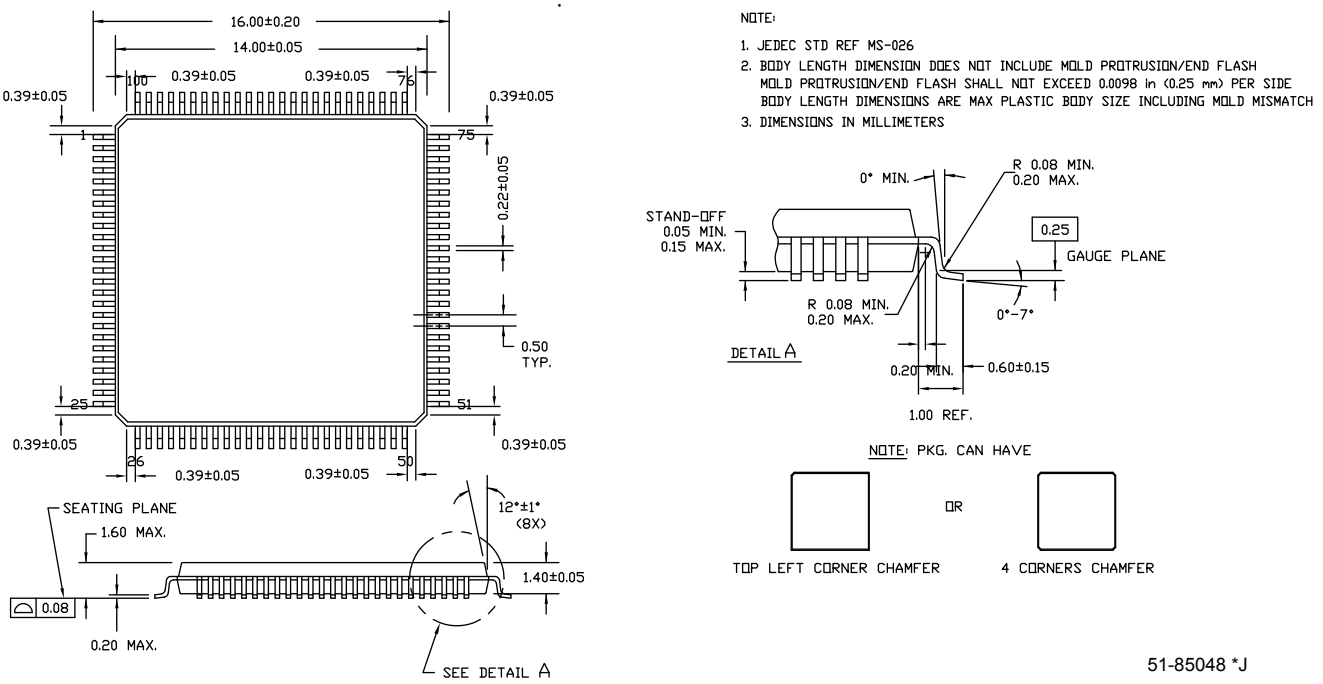
Figure 13-1. 68-pin QFN 8x8 with 0.4 mm Pitch Package Outline (Sawn Version)



NOTES:
1. HATCH AREA IS SOLDERABLE EXPOSED METAL.
2. REFERENCE JEDEC#: MO-220
3. PACKAGE WEIGHT: 17 ± 2mg
4. ALL DIMENSIONS ARE IN MILLIMETERS

001-09618 *E

Figure 13-2. 100-pin TQFP (14 x 14 x 1.4 mm) Package Outline



51-85048 *J

14. Acronyms

Table 14-1. Acronyms Used in this Document

Acronym	Description
abus	analog local bus
ADC	analog-to-digital converter
AG	analog global
AHB	AMBA (advanced microcontroller bus architecture) high-performance bus, an ARM data transfer bus
ALU	arithmetic logic unit
AMUXBUS	analog multiplexer bus
API	application programming interface
APSR	application program status register
ARM®	advanced RISC machine, a CPU architecture
ATM	automatic thump mode
BW	bandwidth
CAN	Controller Area Network, a communications protocol
CMRR	common-mode rejection ratio
CPU	central processing unit
CRC	cyclic redundancy check, an error-checking protocol
DAC	digital-to-analog converter, see also IDAC, VDAC
DFB	digital filter block
DIO	digital input/output, GPIO with only digital capabilities, no analog. See GPIO.
DMA	direct memory access, see also TD
DNL	differential nonlinearity, see also INL
DNU	do not use
DR	port write data registers
DSI	digital system interconnect
DWT	data watchpoint and trace
ECC	error correcting code
ECO	external crystal oscillator
EEPROM	electrically erasable programmable read-only memory
EMI	electromagnetic interference
EMIF	external memory interface
EOC	end of conversion
EOF	end of frame
EPSR	execution program status register
ESD	electrostatic discharge
ETM	embedded trace macrocell

Table 14-1. Acronyms Used in this Document (continued)

Acronym	Description
FIR	finite impulse response, see also IIR
FPB	flash patch and breakpoint
FS	full-speed
GPIO	general-purpose input/output, applies to a PSoC pin
HVI	high-voltage interrupt, see also LVI, LVD
IC	integrated circuit
IDAC	current DAC, see also DAC, VDAC
IDE	integrated development environment
I^2C, or IIC	Inter-Integrated Circuit, a communications protocol
IIR	infinite impulse response, see also FIR
ILO	internal low-speed oscillator, see also IMO
IMO	internal main oscillator, see also ILO
INL	integral nonlinearity, see also DNL
I/O	input/output, see also GPIO, DIO, SIO, USBIO
IPOR	initial power-on reset
IPSR	interrupt program status register
IRQ	interrupt request
ITM	instrumentation trace macrocell
LCD	liquid crystal display
LIN	Local Interconnect Network, a communications protocol.
LR	link register
LUT	lookup table
LVD	low-voltage detect, see also LVI
LVI	low-voltage interrupt, see also HVI
LVTTL	low-voltage transistor-transistor logic
MAC	multiply-accumulate
MCU	microcontroller unit
MISO	master-in slave-out
NC	no connect
NMI	nonmaskable interrupt
NRZ	non-return-to-zero
NVIC	nested vectored interrupt controller
NVL	nonvolatile latch, see also WOL
opamp	operational amplifier
PAL	programmable array logic, see also PLD
PC	program counter
PCB	printed circuit board
PGA	programmable gain amplifier