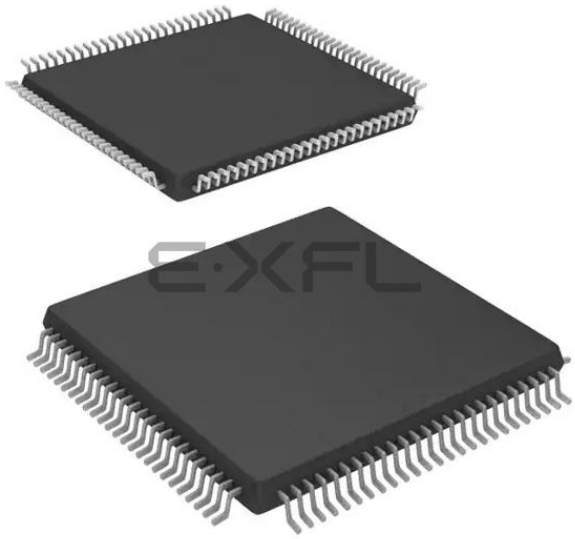

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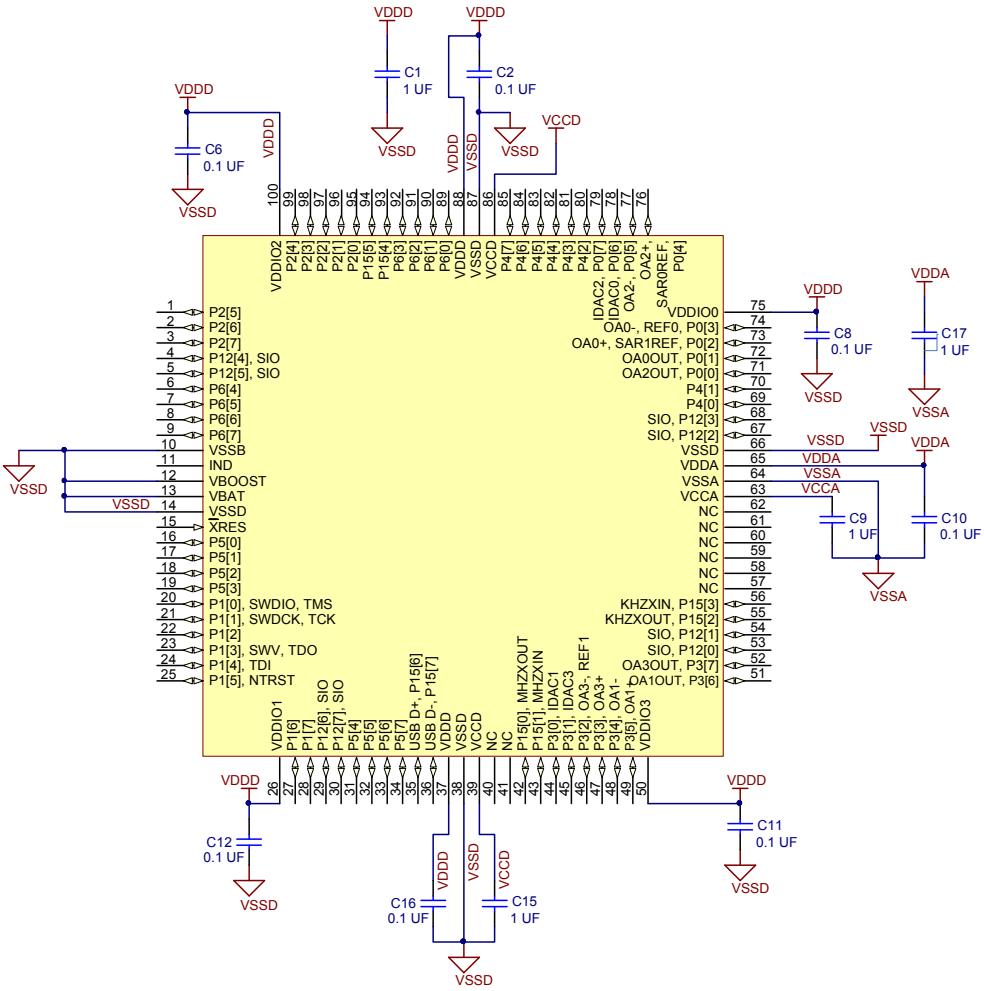
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, I²C, LINbus, SPI, UART/USART, USB
Peripherals	CapSense, DMA, LCD, POR, PWM, WDT
Number of I/O	62
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 5.5V
Data Converters	A/D 1x20b, 2x12b; D/A 4x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c5888axi-lp096

Contents

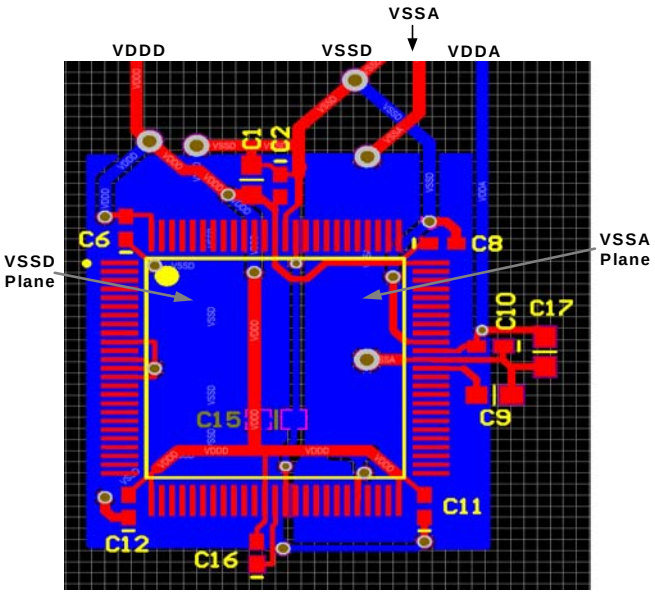
Figure 2-5. Example Schematic for 100-pin TQFP Part with Power Connections



Note The two V_{CCD} pins must be connected together with as short a trace as possible. A trace under the device is recommended, as shown in Figure 2-6.

For more information on pad layout, refer to http://www.cypress.com/cad-resources/psoc-5lp-cad-libraries.

Figure 2-6. Example PCB Layout for 100-pin TQFP Part for Optimal Analog Performance

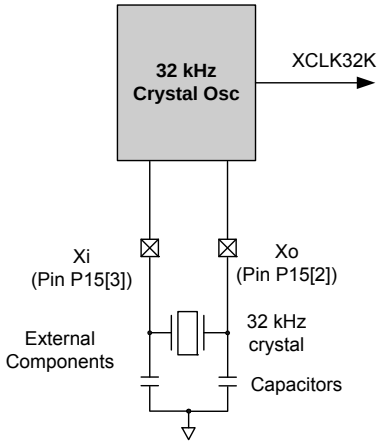


6.1.2.2 32.768 kHz ECO

The 32.768-kHz external crystal oscillator (32kHzECO) provides precision timing with minimal power consumption using an external 32.768-kHz watch crystal (see Figure 6-3). The 32kHzECO also connects directly to the sleep timer and provides the source for the RTC. The RTC uses a 1 second interrupt to implement the RTC functionality in firmware.

The oscillator works in two distinct power modes. This allows users to trade off power consumption with noise immunity from neighboring circuits. The GPIO pins connected to the external crystal and capacitors are fixed.

Figure 6-3. 32kHzECO Block Diagram



It is recommended that the external 32.768-kHz watch crystal have a load capacitance (CL) of 6 pF or 12.5 pF. Check the crystal manufacturer's datasheet. The two external capacitors, CL1 and CL2, are typically of the same value, and their total capacitance, CL1CL2 / (CL1 + CL2), including pin and trace capacitance, should equal the crystal CL value. For more information, refer to application note AN54439: PSoC 3 and PSoC 5 External Oscillators. See also pin capacitance specifications in the "GPIO" section on page 76.

6.1.2.3 Digital System Interconnect

The DSI provides routing for clocks taken from external clock oscillators connected to I/O. The oscillators can also be generated within the device in the digital system and UDBs.

While the primary DSI clock input provides access to all clocking resources, up to eight other DSI clocks (internally or externally generated) may be routed directly to the eight digital clock dividers. This is only possible if there are multiple precision clock sources.

6.1.3 Clock Distribution

All seven clock sources are inputs to the central clock distribution system. The distribution system is designed to create multiple high precision clocks. These clocks are customized for the design's requirements and eliminate the common problems found with limited resolution prescalers attached to peripherals. The clock distribution system generates several types of clock trees.

- The system clock is used to select and supply the fastest clock in the system for general system clock requirements and clock synchronization of the PSoC device.
- Bus clock 16-bit divider uses the system clock to generate the system's bus clock used for data transfers and the CPU. The CPU clock is directly derived from the bus clock.
- Eight fully programmable 16-bit clock dividers generate digital system clocks for general use in the digital system, as configured by the design's requirements. Digital system clocks can generate custom clocks derived from any of the seven clock sources for any purpose. Examples include baud rate generators, accurate PWM periods, and timer clocks, and many others. If more than eight digital clock dividers are required, the UDBs and fixed function timer/counter/PWMs can also generate clocks.
- Four 16-bit clock dividers generate clocks for the analog system components that require clocking, such as ADCs and mixers. The analog clock dividers include skew control to ensure that critical analog events do not occur simultaneously with digital switching events. This is done to reduce analog system noise.

Each clock divider consists of an 8-input multiplexer, a 16-bit clock divider (divide by 2 and higher) that generates ~50% duty cycle clocks, system clock resynchronization logic, and deglitch logic. The outputs from each digital clock tree can be routed into the digital system interconnect and then brought back into the clock system as an input, allowing clock chaining of up to 32 bits.

6.1.4 USB Clock Domain

The USB clock domain is unique in that it operates largely asynchronously from the main clock network. The USB logic contains a synchronous bus interface to the chip, while running on an asynchronous clock to process USB data. The USB logic requires a 48-MHz frequency. This frequency can be generated from different sources, including DSI clock at 48 MHz or doubled value of 24 MHz from internal oscillator, DSI signal, or crystal oscillator.

6.2 Power System

The power system consists of separate analog, digital, and I/O supply pins, labeled VDDA, VDDD, and VDDIOX, respectively. It also includes two internal 1.8 V regulators that provide the digital (VCCD) and analog (VCCA) supplies for the internal core logic. The output pins of the regulators (VCCD and VCCA) and the VDDIO pins must have capacitors connected as shown in Figure 6-4. The two V_{CCD} pins must be shorted together, with as short a trace as possible, and connected to a 1 µF ±10% X5R capacitor. The power system also contains a sleep regulator, an I^2C regulator, and a hibernate regulator.

6.2.1 Power Modes

PSoC 5LP devices have four different power modes, as shown in Table 6-2 and Table 6-3. The power modes allow a design to easily provide required functionality and processing power while simultaneously minimizing power consumption and maximizing battery life in low power and portable devices.

PSoC 5LP power modes, in order of decreasing power consumption are:

- Active
- Alternate active
- Sleep
- Hibernate

Active is the main processing mode. Its functionality is configurable. Each power controllable subsystem is enabled or disabled by using separate power configuration template registers. In alternate active mode, fewer subsystems are enabled, reducing power. In sleep mode most resources are disabled regardless of the template settings. Sleep mode is optimized to provide timed sleep intervals and RTC functionality. The lowest power mode is hibernate, which retains register and SRAM state, but no clocks, and allows wakeup only from I/O pins. Figure 6-5 illustrates the allowable transitions between power modes. Sleep and hibernate modes should not be entered until all VDDIO supplies are at valid voltage levels.

Table 6-2. Power Modes

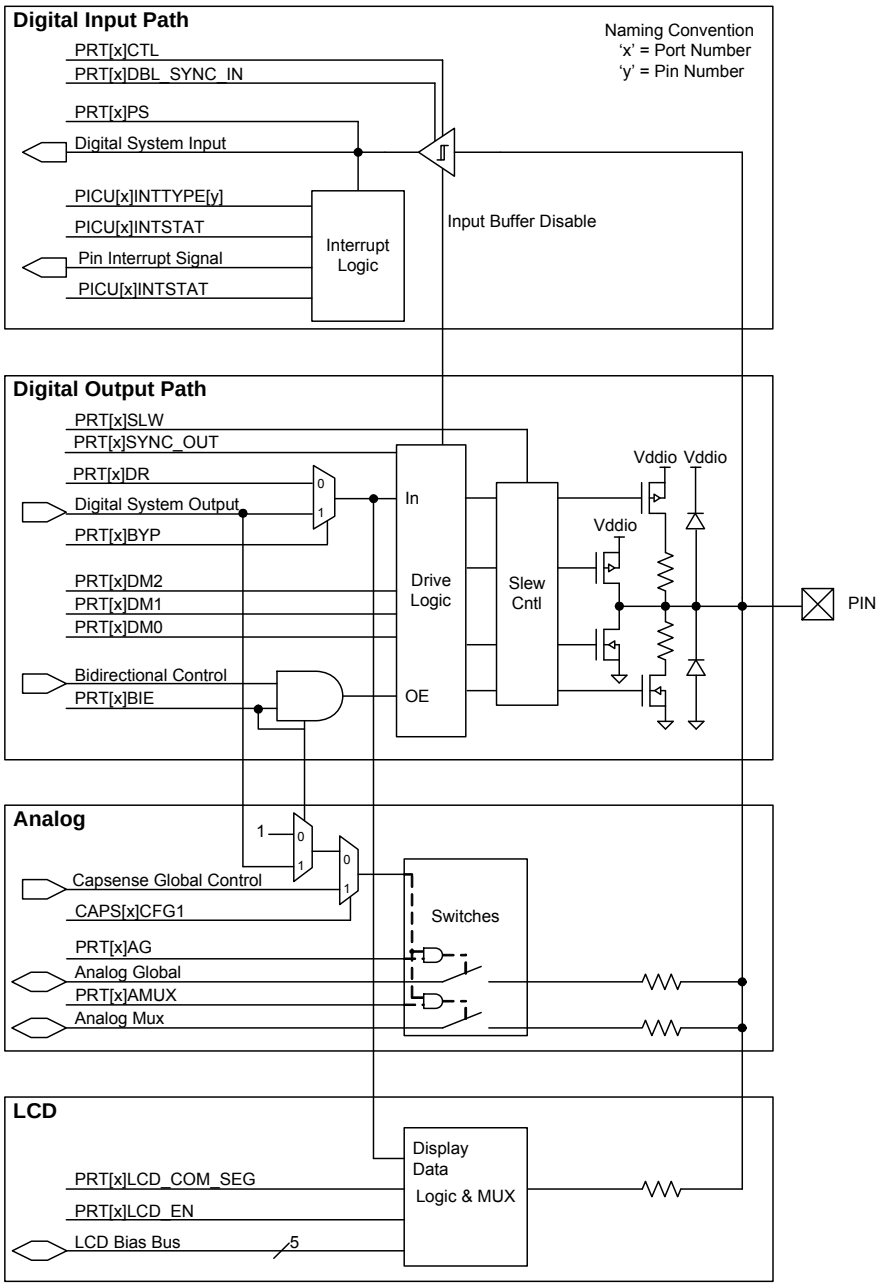
Power Modes	Description	Entry Condition	Wakeup Source	Active Clocks	Regulator
Active	Primary mode of operation, all peripherals available (program-mable)	Wakeup, reset, manual register entry	Any interrupt	Any (program-mable)	All regulators available. Digital and analog regulators can be disabled if external regulation used.
Alternate Active	Similar to Active mode, and is typically configured to have fewer peripherals active to reduce power. One possible configuration is to use the UDBs for processing, with the CPU turned off	Manual register entry	Any interrupt	Any (program-mable)	All regulators available. Digital and analog regulators can be disabled if external regulation used.
Sleep	All subsystems automatically disabled	Manual register entry	Comparator, PICU, I^2C, RTC, CTW, LVD	ILO/kHzECO	Both digital and analog regulators buzzed. Digital and analog regulators can be disabled if external regulation used.
Hibernate	All subsystems automatically disabled Lowest power consuming mode with all peripherals and internal regulators disabled, except hibernate regulator is enabled Configuration and memory contents retained	Manual register entry	PICU		Only hibernate regulator active.

Table 6-3. Power Modes Wakeup Time and Power Consumption

Sleep Modes	Wakeup Time	Current (Typ)	Code Execution	Digital Resources	Analog Resources	Clock Sources Available	Wakeup Sources	Reset Sources
Active	–	3.1 mA[8]	Yes	All	All	All	–	All
Alternate Active	–	–	User defined	All	All	All	–	All
Sleep	<25 µs	2 µA	No	I^2C	Comparator	ILO/kHzECO	Comparator, PICU, I^2C, RTC, CTW, LVD	XRES, LVD, WDR
Hibernate	<200 µs	300 nA	No	None	None	None	PICU	XRES

Note
8. Bus clock off. Execute from CPU instruction buffer at 6 MHz. See Table 11-2 on page 68.

Figure 6-8. GPIO Block Diagram



6.4.13 SIO as Comparator

This section applies only to SIO pins. The adjustable input level feature of the SIOs as explained in the Adjustable Input Level on page 38 can be used to construct a comparator. The threshold for the comparator is provided by the SIO's reference generator. The reference generator has the option to set the analog signal routed through the analog global line as threshold for the comparator. Note that a pair of SIO pins share the same threshold.

The digital input path in Figure 6-9 on page 35 illustrates this functionality. In the figure, 'Reference level' is the analog signal routed through the analog global. The hysteresis feature can also be enabled for the input buffer of the SIO, which increases noise immunity for the comparator.

6.4.14 Hot Swap

This section applies only to SIO pins. SIO pins support 'hot swap' capability to plug into an application without loading the signals that are connected to the SIO pins even when no power is applied to the PSoC device. This allows the unpowered PSoC to maintain a high impedance load to the external device while also preventing the PSoC from being powered through a SIO pin's protection diode.

Powering the device up or down while connected to an operational I2C bus may cause transient states on the SIO pins. The overall I2C bus design should take this into account.

6.4.15 Overvoltage Tolerance

All I/O pins provide an overvoltage tolerance feature at any operating VDD.

- There are no current limitations for the SIO pins as they present a high impedance load to the external circuit.
- The GPIO pins must be limited to 100 µA using a current limiting resistor. GPIO pins clamp the pin voltage to approximately one diode above the VDDIO supply.
- In case of a GPIO pin configured for analog input/output, the analog voltage on the pin must not exceed the VDDIO supply voltage to which the GPIO belongs.

A common application for this feature is connection to a bus such as I^2C where different devices are running from different supply voltages. In the I^2C case, the PSoC chip is configured into the Open Drain, Drives Low mode for the SIO pin. This allows an external pull-up to pull the I^2C bus voltage above the PSoC pin supply. For example, the PSoC chip could operate at 1.8 V, and an external device could run from 5 V. Note that the SIO pin's VIH and VIL levels are determined by the associated VDDIO supply pin.

The SIO pin must be in one of the following modes: 0 (high impedance analog), 1 (high impedance digital), or 4 (open drain drives low). See Figure 6-11 for details. Absolute maximum ratings for the device must be observed for all I/O pins.

6.4.16 Reset Configuration

While reset is active all I/Os are reset to and held in the High Impedance Analog state. After reset is released, the state can be reprogrammed on a port-by-port basis to pull-down or pull-up. To ensure correct reset operation, the port reset configuration data is stored in special nonvolatile registers. The stored reset data is automatically transferred to the port reset configuration registers at reset release.

6.4.17 Low Power Functionality

In all low power modes the I/O pins retain their state until the part is awakened and changed or reset. To awaken the part, use a pin interrupt, because the port interrupt logic continues to function in all low power modes.

6.4.18 Special Pin Functionality

Some pins on the device include additional special functionality in addition to their GPIO or SIO functionality. The specific special function pins are listed in "Pinouts" on page 6. The special features are:

- Digital
  - 4- to 25-MHz crystal oscillator
  - 32.768-kHz crystal oscillator
  - Wake from sleep on I^2C address match. Any pin can be used for I^2C if wake from sleep is not required.
  - JTAG interface pins
  - SWD interface pins
  - SWV interface pins
  - TRACEPORT interface pins
  - External reset
- Analog
  - Opamp inputs and outputs
  - High current IDAC outputs
  - External reference inputs

6.4.19 JTAG Boundary Scan

The device supports standard JTAG boundary scan chains on all pins for board level test.

7.7 Timers, Counters, and PWMs

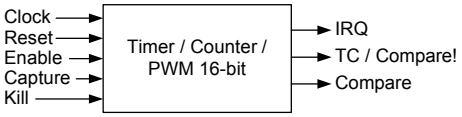
The Timer/Counter/PWM peripheral is a 16-bit dedicated peripheral providing three of the most common embedded peripheral features. As almost all embedded systems use some combination of timers, counters, and PWMs. Four of them have been included on this PSoC device family. Additional and more advanced functionality timers, counters, and PWMs can also be instantiated in Universal Digital Blocks (UDBs) as required. PSoC Creator allows you to choose the timer, counter, and PWM features that you need. The tool set utilizes the most optimal resources available.

The Timer/Counter/PWM peripheral can select from multiple clock sources, with input and output signals connected through the DSI routing. DSI routing allows input and output connections to any device pin and any internal digital signal accessible through the DSI. Each of the four instances has a compare output, terminal count output (optional complementary compare output), and programmable interrupt request line. The Timer/Counter/PWMs are configurable as free running, one shot, or Enable input controlled. The peripheral has timer reset and capture inputs, and a kill input for control of the comparator outputs. The peripheral supports full 16-bit capture.

Timer/Counter/PWM features include:

- 16-bit timer/counter/PWM (down count only)
- Selectable clock source
- PWM comparator (configurable for LT, LTE, EQ, GTE, GT)
- Period reload on start, reset, and terminal count
- Interrupt on terminal count, compare true, or capture
- Dynamic counter reads
- Timer capture mode
- Count while enable signal is asserted mode
- Free run mode
- One-shot mode (stop at end of period)
- Complementary PWM outputs with deadband
- PWM output kill

Figure 7-17. Timer/Counter/PWM



7.8 I²C

PSoC includes a single fixed-function I²C peripheral. Additional I²C interfaces can be instantiated using Universal Digital Blocks (UDBs) in PSoC Creator, as required.

The I²C peripheral provides a synchronous two-wire interface designed to interface the PSoC device with a two-wire I²C serial communication bus. It is compatible[13] with I²C Standard-mode, Fast-mode, and Fast-mode Plus devices as defined in the NXP I²C-bus specification and user manual (UM10204). The I²C bus I/O may be implemented with GPIO or SIO in open-drain modes.

To eliminate the need for excessive CPU intervention and overhead, I²C specific support is provided for status detection and generation of framing bits. I²C operates as a slave, a master, or multimaster (Slave and Master)[13]. In slave mode, the unit always listens for a start condition to begin sending or receiving data. Master mode supplies the ability to generate the Start and Stop conditions and initiate transactions. Multimaster mode provides clock synchronization and arbitration to allow multiple masters on the same bus. If Master mode is enabled and Slave mode is not enabled, the block does not generate interrupts on externally generated Start conditions. I²C interfaces through the DSI routing and allows direct connections to any GPIO or SIO pins.

I²C provides hardware address detect of a 7-bit address without CPU intervention. Additionally the device can wake from low power modes on a 7-bit hardware address match. If wakeup functionality is required, I²C pin connections are limited to one of two specific pairs of SIO pins. See descriptions of SCL and SDA pins in Pin Descriptions on page 12.

I²C features include:

- Slave and master, transmitter, and receiver operation
- Byte processing for low CPU overhead
- Interrupt or polling CPU interface
- Support for bus speeds up to 1 Mbps
- 7 or 10-bit addressing (10-bit addressing requires firmware support)
- SMBus operation (through firmware support - SMBus supported in hardware in UDBs)
- 7-bit hardware address compare
- Wake from low power modes on address match
- Glitch filtering (active and alternate-active modes only)

Data transfers follow the format shown in Figure 7-18. After the START condition (S), a slave address is sent. This address is 7 bits long followed by an eighth bit which is a data direction bit (R/W) - a 'zero' indicates a transmission (WRITE), a 'one' indicates a request for data (READ). A data transfer is always terminated by a STOP condition (P) generated by the master.

Notes
12. The I²C peripheral is non-compliant with the NXP I²C specification in the following areas: analog glitch filter, I/O V_{OL}/I_{OL}, I/O hysteresis. The I²C Block has a digital glitch filter (not available in sleep mode). The Fast-mode minimum fall-time specification can be met by setting the I/Os to slow speed mode. See the I/O Electrical Specifications in Inputs and Outputs on page 76 for details.
13. Fixed-block I²C does not support undefined bus conditions, nor does it support Repeated Start in Slave mode. These conditions should be avoided, or the UDB-based I²C component should be used instead.

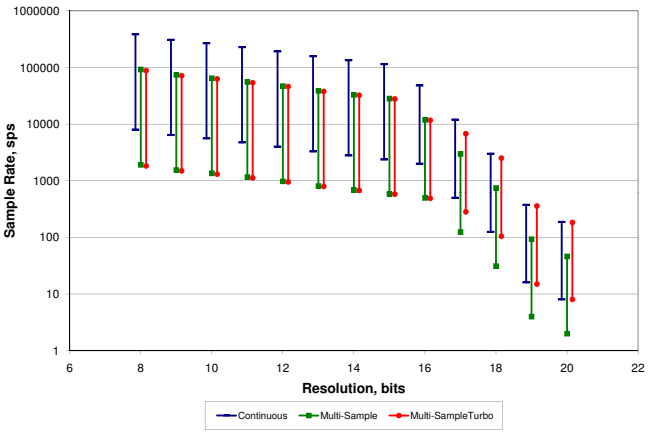
8.2 Delta-sigma ADC

The CY8C58LP device contains one delta-sigma ADC. This ADC offers differential input, high resolution and excellent linearity, making it a good ADC choice for both audio signal processing and measurement applications. The converter's nominal operation is 16 bits at 48 ksps. The ADC can be configured to output 20-bit resolution at data rates of up to 187 sps. At a fixed clock rate, resolution can be traded for faster data rates as shown in Table 8-1 and Figure 8-3.

Table 8-1. Delta-sigma ADC Performance

Bits	Maximum Sample Rate (sps)	SINAD (dB)
20	187	–
16	48 k	84
12	192 k	66
8	384 k	43

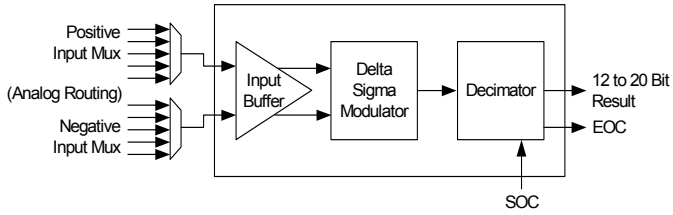
Figure 8-3. Delta-sigma ADC Sample Rates, Range = ±1.024 V



8.2.1 Functional Description

The ADC connects and configures three basic components, input buffer, delta-sigma modulator, and decimator. The basic block diagram is shown in Figure 8-4. The signal from the input muxes is delivered to the delta-sigma modulator either directly or through the input buffer. The delta-sigma modulator performs the actual analog to digital conversion. The modulator over-samples the input and generates a serial data stream output. This high speed data stream is not useful for most applications without some type of post processing, and so is passed to the decimator through the Analog Interface block. The decimator converts the high speed serial data stream into parallel ADC results. The modulator/decimator frequency response is $[(\sin x)/x]^4$.

Figure 8-4. Delta-sigma ADC Block Diagram



Resolution and sample rate are controlled by the Decimator. Data is pipelined in the decimator; the output is a function of the last four samples. When the input multiplexer is switched, the output data is not valid until after the fourth sample after the switch.

8.2.2 Operational Modes

The ADC can be configured by the user to operate in one of four modes: Single Sample, Multi Sample, Continuous, or Multi Sample (Turbo). All four modes are started by either a write to the start bit in a control register or an assertion of the Start of Conversion (SoC) signal. When the conversion is complete, a status bit is set and the output signal End of Conversion (EoC) asserts high and remains high until the value is read by either the DMA controller or the CPU.

8.2.2.1 Single Sample

In Single Sample mode, the ADC performs one sample conversion on a trigger. In this mode, the ADC stays in standby state waiting for the SoC signal to be asserted. When SoC is signaled the ADC performs four successive conversions. The first three conversions prime the decimator. The ADC result is valid and available after the fourth conversion, at which time the EoC signal is generated. To detect the end of conversion, the system may poll a control register for status or configure the external EoC signal to generate an interrupt or invoke a DMA request. When the transfer is done the ADC reenters the standby state where it stays until another SoC event.

8.2.2.2 Continuous

Continuous sample mode is used to take multiple successive samples of a single input signal. Multiplexing multiple inputs should not be done with this mode. There is a latency of three conversion times before the first conversion result is available. This is the time required to prime the decimator. After the first result, successive conversions are available at the selected sample rate.

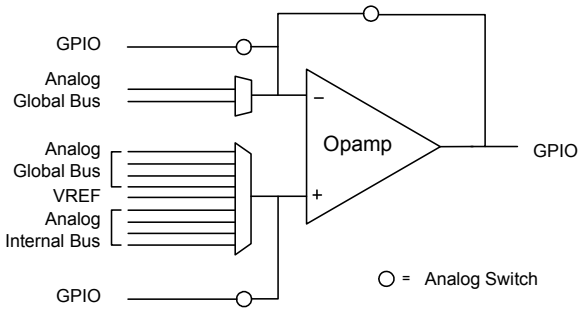
8.2.2.3 Multi Sample

Multi sample mode is similar to continuous mode except that the ADC is reset between samples. This mode is useful when the input is switched between multiple signals. The decimator is re-primed between each sample so that previous samples do not affect the current conversion. Upon completion of a sample, the next sample is automatically initiated. The results can be transferred using either firmware polling, interrupt, or DMA.

8.5 Opamps

The CY8C58LP family of devices contain four general purpose opamps.

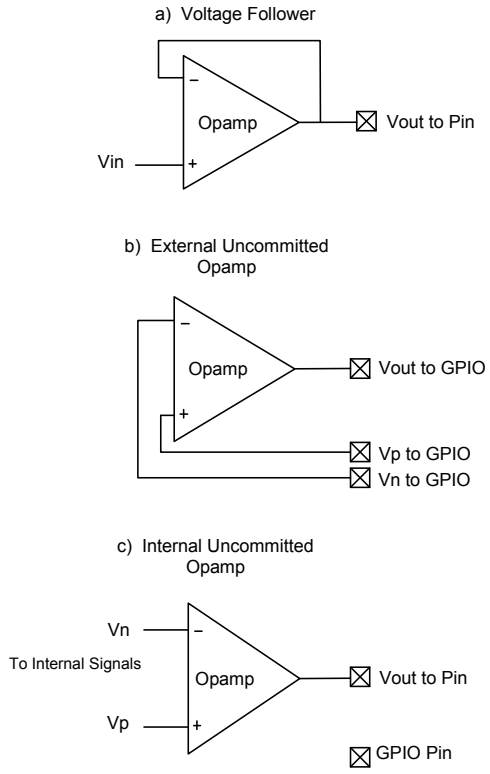
Figure 8-7. Opamp



The opamp is uncommitted and can be configured as a gain stage or voltage follower on external or internal signals.

See Figure 8-8. In any configuration, the input and output signals can all be connected to the internal global signals and monitored with an ADC, or comparator. The configurations are implemented with switches between the signals and GPIO pins.

Figure 8-8. Opamp Configurations



The opamp has three speed modes, slow, medium, and fast. The slow mode consumes the least amount of quiescent power and the fast mode consumes the most power. The inputs are able to swing rail-to-rail. The output swing is capable of rail-to-rail operation at low current output, within 50 mV of the rails. When driving high current loads (about 25 mA) the output voltage may only get within 500 mV of the rails.

8.6 Programmable SC/CT Blocks

The CY8C58LP family of devices contains four switched capacitor/continuous time (SC/CT) blocks. Each switched capacitor/continuous time block is built around a single rail-to-rail high bandwidth opamp.

Switched capacitor is a circuit design technique that uses capacitors plus switches instead of resistors to create analog functions. These circuits work by moving charge between capacitors by opening and closing different switches. Nonoverlapping in phase clock signals control the switches, so that not all switches are ON simultaneously.

The PSoC Creator tool offers a user friendly interface, which allows you to easily program the SC/CT blocks. Switch control and clock phase control configuration is done by PSoC Creator so users only need to determine the application use parameters such as gain, amplifier polarity, V_{REF} connection, and so on.

The same opamps and block interfaces are also connectable to an array of resistors which allows the construction of a variety of continuous time functions.

The opamp and resistor array is programmable to perform various analog functions including

- Naked Operational Amplifier - Continuous Mode
- Unity-Gain Buffer - Continuous Mode
- Programmable Gain Amplifier (PGA) - Continuous Mode
- Transimpedance Amplifier (TIA) - Continuous Mode
- Up/Down Mixer - Continuous Mode
- Sample and Hold Mixer (NRZ S/H) - Switched Cap Mode
- First Order Analog to Digital Modulator - Switched Cap Mode

8.6.1 Naked Opamp

The Naked Opamp presents both inputs and the output for connection to internal or external signals. The opamp has a unity gain bandwidth greater than 6.0 MHz and output drive current up to 650 µA. This is sufficient for buffering internal signals (such as DAC outputs) and driving external loads greater than 7.5 kohms.

8.6.2 Unity Gain

The Unity Gain buffer is a Naked Opamp with the output directly connected to the inverting input for a gain of 1.00. It has a -3 dB bandwidth greater than 6.0 MHz.

8.6.3 PGA

The PGA amplifies an external or internal signal. The PGA can be configured to operate in inverting mode or noninverting mode. The PGA function may be configured for both positive and negative gains as high as 50 and 49 respectively. The gain is adjusted by changing the values of R1 and R2 as illustrated in Figure 8-9. The schematic in Figure 8-9 shows the configuration and possible resistor settings for the PGA. The gain is switched from inverting and non inverting by changing the shared select value of the both the input muxes. The bandwidth for each gain case is listed in Table 8-3.

9.2 SWD Interface

The SWD interface is the preferred alternative to the JTAG interface. It requires only two pins instead of the four or five needed by JTAG. SWD provides all of the programming and debugging features of JTAG at the same speed. SWD does not provide access to scan chains or device chaining. The SWD clock frequency can be up to 1/3 of the CPU clock frequency.

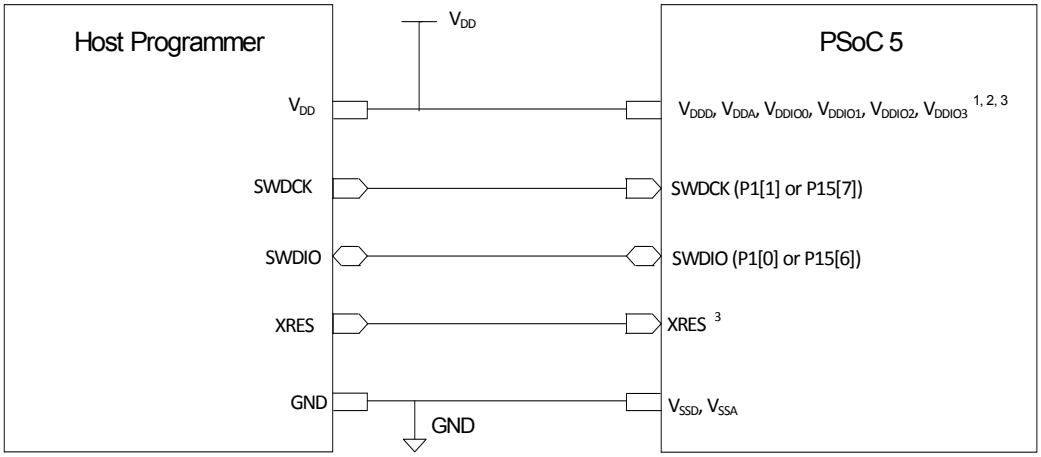
SWD uses two pins, either two of the JTAG pins (TMS and TCK) or the USBIO D+ and D- pins. The USBIO pins are useful for in system programming of USB solutions that would otherwise require a separate programming connector. One pin is used for the data clock and the other is used for data input and output.

SWD can be enabled on only one of the pin pairs at a time. This only happens if, within 8 µs (key window) after reset, that pin pair (JTAG or USB) receives a predetermined acquire sequence of 1s and 0s. If the NVL latches are set for SWD (see *Section 5.5*), this sequence need not be applied to the JTAG pin pair. The acquire sequence must always be applied to the USB pin pair.

SWD is used for debugging or for programming the flash memory.

The SWD interface can be enabled from the JTAG interface or disabled, allowing its pins to be used as GPIO. Unlike JTAG, the SWD interface can always be reacquired on any device during the key window. It can then be used to reenable the JTAG interface, if desired. When using SWD or JTAG pins as standard GPIO, make sure that the GPIO functionality and PCB circuits do not interfere with SWD or JTAG use.

Figure 9-2. SWD Interface Connections between PSoC 5LP and Programmer



[1] The voltage levels of the Host Programmer and the PSoC 5 voltage domains involved in programming should be the same. The XRES pin is powered by V_{DDIO1}. The USB SWD pins are powered by V_{DDD}. So for Programming using the USB SWD pins with XRES pin, the V_{DDD}, V_{DDIO1} of PSoC 5 should be at the same voltage level as Host V_{DD}. Rest of PSoC 5 voltage domains (V_{DDA}, V_{DDIO0}, V_{DDIO2}, V_{DDIO3}) need not be at the same voltage level as host Programmer. The Port 1 SWD pins are powered by V_{DDIO1}. So V_{DDIO1} of PSoC 5 should be at same voltage level as host V_{DD} for Port 1 SWD programming. Rest of PSoC 5 voltage domains (V_{DDD}, V_{DDA}, V_{DDIO0}, V_{DDIO2}, V_{DDIO3}) need not be at the same voltage level as host Programmer.

[2] Vdda must be greater than or equal to all other power supplies (Vddd, Vddio's) in PSoC 5.

[3] For Power cycle mode Programming, XRES pin is not required. But the Host programmer must have the capability to toggle power (Vddd, Vdda, All Vddio's) to PSoC 5. This may typically require external interface circuitry to toggle power which will depend on the programming setup. The power supplies can be brought up in any sequence, however, once stable, VDDA must be greater than or equal to all other supplies.

11.2 Device Level Specifications

Specifications are valid for –40 °C ≤ T_A ≤ 105 °C and T_J ≤ 120 °C, except where noted. Specifications are valid for 1.71 V to 5.5 V, except where noted. Unless otherwise specified, all charts and graphs show typical values.

Table 11-2. DC Specifications

Parameter	Description	Conditions		Min	Typ	Max	Units
V_{DDA}	Analog supply voltage and input to analog core regulator	Analog core regulator enabled		1.8	–	5.5	V
V_{DDA}	Analog supply voltage, analog regulator bypassed	Analog core regulator disabled		1.71	1.8	1.89	V
V_{DDD}	Digital supply voltage relative to V_{SSD}	Digital core regulator enabled		1.8	–	V_{DDA}[17]	V
				–	–	V_{DDA} + 0.1[19]	
V_{DDD}	Digital supply voltage, digital regulator bypassed	Digital core regulator disabled		1.71	1.8	1.89	V
V_{DDIO}[18]	I/O supply voltage relative to V_{SSIO}			1.71	–	V_{DDA}[17]	V
				–	–	V_{DDA} + 0.1[19]	
V_{CCA}	Direct analog core voltage input (Analog regulator bypass)	Analog core regulator disabled		1.71	1.8	1.89	V
V_{CCD}	Direct digital core voltage input (Digital regulator bypass)	Digital core regulator disabled		1.71	1.8	1.89	V
I_{DD}[20]	**Active Mode**						
	Sum of digital and analog IDDD + IDDA. IDDIOX for I/Os not included. IMO enabled, bus clock and CPU clock enabled. CPU executing complex program from flash.	V_{DDX} = 2.7 V to 5.5 V; F_{CPU} = 3 MHz[21]	T = –40 °C	–	1.9	3.8	mA
			T = 25 °C	–	1.9	3.8	
			T = 85 °C	–	2	3.8	
			T = 105 °C	–	2	3.8	
		V_{DDX} = 2.7 V to 5.5 V; F_{CPU} = 6 MHz	T = –40 °C	–	3.1	5	
			T = 25 °C	–	3.1	5	
			T = 85 °C	–	3.2	5	
			T = 105 °C	–	3.2	5	
		V_{DDX} = 2.7 V to 5.5 V; F_{CPU} = 12 MHz[21]	T = –40 °C	–	5.4	7	
			T = 25 °C	–	5.4	7	
			T = 85 °C	–	5.6	7	
			T = 105 °C	–	5.6	7	
		V_{DDX} = 2.7 V to 5.5 V; F_{CPU} = 24 MHz[21]	T = –40 °C	–	8.9	10.5	
			T = 25 °C	–	8.9	10.5	
			T = 85 °C	–	9.1	10.5	
			T = 105 °C	–	9.1	10.5	
		V_{DDX} = 2.7 V to 5.5 V; F_{CPU} = 48 MHz[21]	T = –40 °C	–	15.5	17	
			T = 25 °C	–	15.4	17	
			T = 85 °C	–	15.7	17	
			T = 105 °C	–	15.7	17.25	
		V_{DDX} = 2.7 V to 5.5 V; F_{CPU} = 62 MHz	T = –40 °C	–	18	19.5	
			T = 25 °C	–	18	19.5	
			T = 85 °C	–	18.5	19.5	
			T = 105 °C	–	19	21	
		V_{DDX} = 2.7 V to 5.5 V; F_{CPU} = 74 MHz	T = –40 °C	–	26.5	30	
			T = 25 °C	–	26.5	30	
			T = 85 °C	–	27	30	
			T = 105 °C	–	27	30	
		V_{DDX} = 2.7 V to 5.5 V; F_{CPU} = 80 MHz, IMO = 3 MHz with PLL	T = –40 °C	–	22	25.5	
			T = 25 °C	–	22	25.5	
			T = 85 °C	–	22.5	25.5	
			T = 105 °C	–	22.5	25.5	

Notes

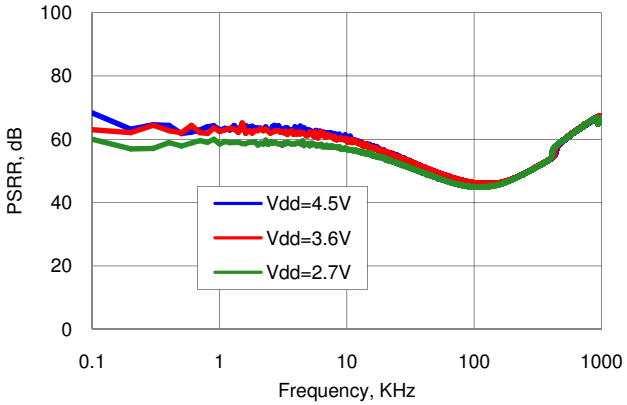
17. The power supplies can be brought up in any sequence. However, once stable, V_{DDA} must be greater than or equal to all other supplies.
18. The V_{DDIO} supply voltage must be greater than the maximum voltage on the associated GPIO pins. Maximum voltage on GPIO pin ≤ V_{DDIO} ≤ V_{DDA}.
19. Guaranteed by design, not production tested.
20. The current consumption of additional peripherals that are implemented only in programmed logic blocks can be found in their respective datasheets, available in PSoC Creator, the integrated design environment. To estimate total current, find CPU current at frequency of interest and add peripheral currents for your particular system from the device datasheet and component datasheets.
21. Based on device characterization (Not production tested).

11.3.2 Analog Core Regulator

Table 11-5. Analog Core Regulator DC *Specifications*

Parameter	Description	Conditions	Min	Typ	Max	Units
V_{DDA}	Input voltage		1.8	–	5.5	V
V_{CCA}	Output voltage		–	1.80	–	V
	Regulator output capacitor	±10%, X5R ceramic or better	0.9	1	1.1	µF

Figure 11-7. Analog Regulator PSRR vs Frequency and V_{DD}



11.3.3 Inductive Boost Regulator

Unless otherwise specified, operating conditions are: V_{BAT} = 0.5 V–3.6 V, V_{OUT} = 1.8 V–5.0 V, I_{OUT} = 0 mA–50 mA, L_{BOOST} = 4.7 µH–22 µH, C_{BOOST} = 22 µF || 3 × 1.0 µF || 3 × 0.1 µF, C_{BAT} = 22 µF, I_F = 1.0 A, excludes 99-pin CSP package. For information on using boost with 99-pin CSP package, contact Cypress support. Unless otherwise specified, all charts and graphs show typical values.

Table 11-6. Inductive Boost Regulator DC Specifications

Parameter	Description	Conditions		Min	Typ	Max	Units
V_{OUT}	Boost output voltage[29]	vsel = 1.8 V in register BOOST_CR0		1.71	1.8	1.89	V
		vsel = 1.9 V in register BOOST_CR0		1.81	1.90	2.00	V
		vsel = 2.0 V in register BOOST_CR0		1.90	2.00	2.10	V
		vsel = 2.4 V in register BOOST_CR0		2.16	2.40	2.64	V
		vsel = 2.7 V in register BOOST_CR0		2.43	2.70	2.97	V
		vsel = 3.0 V in register BOOST_CR0		2.70	3.00	3.30	V
		vsel = 3.3 V in register BOOST_CR0		2.97	3.30	3.63	V
		vsel = 3.6 V in register BOOST_CR0		3.24	3.60	3.96	V
		vsel = 5.0 V in register BOOST_CR0		4.50	5.00	5.50	V
V_{BAT}	Input voltage to boost[30]	I_{OUT} = 0 mA–5 mA	vsel = 1.8 V–2.0 V, T_A = 0 °C–70 °C	0.5	–	0.8	V
		I_{OUT} = 0 mA–15 mA	vsel = 1.8 V–5.0 V[31], T_A = –10 °C–85 °C	1.6	–	3.6	V
		I_{OUT} = 0 mA–25 mA	vsel = 1.8 V–2.7 V, T_A = –10 °C–85 °C	0.8	–	1.6	V
		I_{OUT} = 0 mA–50 mA	vsel = 1.8 V–3.3 V[31], T_A = –40 °C–85 °C	1.8	–	2.5	V
			vsel = 1.8 V–3.3 V[31], T_A = –10 °C–85 °C	1.3	–	2.5	V
			vsel = 2.5 V–5.0 V[31], T_A = –10 °C–85 °C	2.5	–	3.6	V

Table 11-20. 20-bit Delta-sigma ADC DC Specifications (continued)

Parameter	Description	Conditions	Min	Typ	Max	Units
Rin_Buff	ADC input resistance	Input buffer used	10	–	–	MΩ
Rin_ADC16	ADC input resistance	Input buffer bypassed, 16-bit, Range = ±1.024 V	–	74[46]	–	kΩ
Rin_ADC12	ADC input resistance	Input buffer bypassed, 12 bit, Range = ±1.024 V	–	148[46]	–	kΩ
Rin_ExtRef	ADC external reference input resistance		–	70[46, 47]	–	kΩ
Vextref	ADC external reference input voltage, see also internal reference in Voltage Reference on page 93	Pins P0[3], P3[2]	0.9	–	1.3	V
Current Consumption						
I_{DD_20}	I_{DDA} + I_{DDD} Current consumption, 20 bit[48]	187 sps, unbuffered	–	–	1.5	mA
I_{DD_16}	I_{DDA} + I_{DDD} Current consumption, 16 bit[48]	48 ksps, unbuffered	–	–	1.5	mA
I_{DD_12}	I_{DDA} + I_{DDD} Current consumption, 12 bit[48]	192 ksps, unbuffered	–	–	1.95	mA
I_{DD_8}	I_{DDA} + I_{DDD} Current consumption, 8 bit[48]	384 ksps, unbuffered	–	–	1.95	mA
I_{BUFF}	Buffer current consumption[48]		–	–	2.5	mA

Table 11-21. Delta-sigma ADC AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Startup time		–	–	4	Samples
THD	Total harmonic distortion[48]	Buffer gain = 1, 16 bit, Range = ±1.024 V	–	–	0.0032	%
20-Bit Resolution Mode						
SR20	Sample rate[48]	Range = ±1.024 V, unbuffered	7.8	–	187	sps
BW20	Input bandwidth at max sample rate[48]	Range = ±1.024 V, unbuffered	–	40	–	Hz
16-Bit Resolution Mode						
SR16	Sample rate[48]	Range = ±1.024 V, unbuffered	2	–	48	ksps
BW16	Input bandwidth at max sample rate[48]	Range = ±1.024 V, unbuffered	–	11	–	kHz
SINAD16int	Signal to noise ratio, 16-bit, internal reference[48]	Range = ±1.024V, unbuffered	81	–	–	dB
		T_A ≤ 105 °C	77	–	–	
SINAD16ext	Signal to noise ratio, 16-bit, external reference[48]	Range = ±1.024 V, unbuffered	84	–	–	dB
12-Bit Resolution Mode						
SR12	Sample rate, continuous, high power[48]	Range = ±1.024 V, unbuffered	4	–	192	ksps
BW12	Input bandwidth at max sample rate[48]	Range = ±1.024 V, unbuffered	–	44	–	kHz
SINAD12int	Signal to noise ratio, 12-bit, internal reference[48]	Range = ±1.024 V, unbuffered	66	–	–	dB
8-Bit Resolution Mode						
SR8	Sample rate, continuous, high power[48]	Range = ±1.024 V, unbuffered	8	–	384	ksps
BW8	Input bandwidth at max sample rate[48]	Range = ±1.024 V, unbuffered	–	88	–	kHz
SINAD8int	Signal to noise ratio, 8-bit, internal reference[48]	Range = ±1.024 V, unbuffered	43	–	–	dB

Notes
46. By using switched capacitors at the ADC input an effective input resistance is created. Holding the gain and number of bits constant, the resistance is proportional to the inverse of the clock frequency. This value is calculated, not measured. For more information see the Technical Reference Manual.
47. Recommend an external reference device with an output impedance <100 Ω, for example, the LM185/285/385 family. A 1 µF capacitor is recommended. For more information, see AN61290 - PSoC® 3 and PSoC 5LP Hardware Design Considerations.
48. Based on device characterization (not production tested).

11.5.4 SAR ADC

Table 11-28. SAR ADC DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Resolution		–	–	12	bits
	Number of channels – single-ended		–	–	No of GPIO	
	Number of channels – differential	Differential pair is formed using a pair of neighboring GPIO.	–	–	No of GPIO/2	
	Monotonicity[52]		Yes	–	–	
Ge	Gain error[53]	External reference	–	–	±0.1	%
V_{OS}	Input offset voltage		–	–	±2	mV
I_{DD}	Current consumption[52]		–	–	1	mA
	Input voltage range – single-ended[52]		V_{SSA}	–	V_{DDA}	V
	Input voltage range – differential[52]		V_{SSA}	–	V_{DDA}	V
PSRR	Power supply rejection ratio[52]		70	–	–	dB
CMRR	Common mode rejection ratio		70	–	–	dB
INL	Integral non linearity[52]	V_{DDA} 1.71 to 5.5 V, 1 Msps, V_{REF} 1 to 5.5 V, bypassed at ExtRef pin	–	–	+2/–1.5	LSB
		V_{DDA} 2.0 to 3.6 V, 1 Msps, V_{REF} 2 to V_{DDA}, bypassed at ExtRef pin	–	–	±1.2	LSB
		V_{DDA} 1.71 to 5.5 V, 500 ksps, V_{REF} 1 to 5.5 V, bypassed at ExtRef pin	–	–	±1.3	LSB
DNL	Differential non linearity[52]	V_{DDA} 1.71 to 5.5 V, 1 Msps, V_{REF} 1 to 5.5 V, bypassed at ExtRef pin	–	–	+2/–1	LSB
		V_{DDA} 2.0 to 3.6 V, 1 Msps, V_{REF} 2 to V_{DDA}, bypassed at ExtRef pin No missing codes	–	–	1.7/–0.99	LSB
		V_{DDA} 1.71 to 5.5 V, 500 ksps, V_{REF} 1 to 5.5 V, bypassed at ExtRef pin No missing codes	–	–	+2/–0.99	LSB
R_{IN}	Input resistance[52]		–	180	–	kΩ

Notes
52. Based on device characterization (Not production tested).
53. For total analog system Idd < 5 mA, depending on package used. With higher total analog system currents it is recommended that the SAR ADC be used in differential mode.

Table 11-34. IDAC DC Specifications (continued)

Parameter	Description	Conditions	Min	Typ	Max	Units
DNL	Differential nonlinearity	Sink mode, range = 255 µA, Rload = 2.4 kΩ, Cload = 15 pF	–	±0.3	±1	LSB
		Source mode, range = 255 µA, Rload = 2.4 kΩ, Cload = 15 pF	–	±0.3	±1	LSB
		Source mode, range = 31.875 µA, Rload = 20 kΩ, Cload = 15 pF[61]	–	±0.2	±1	LSB
		Sink mode, range = 31.875 µA, Rload = 20 kΩ, Cload = 15 pF[61]	–	±0.2	±1	LSB
		Source mode, range = 2.0 4 mA, Rload = 600 Ω, Cload = 15 pF[61]	–	±0.2	±1	LSB
		Sink mode, range = 2.0 4 mA, Rload = 600 Ω, Cload = 15 pF[61]	–	±0.2	±1	LSB
Vcompliance	Dropout voltage, source or sink mode	Voltage headroom at max current, Rload to V_{DDA} or Rload to V_{SSA}, V_{DIFF} from V_{DDA}	1	–	–	V
I_{DD}	Operating current, code = 0	Slow mode, source mode, range = 31.875 µA	–	44	100	µA
		Slow mode, source mode, range = 255 µA,	–	33	100	µA
		Slow mode, source mode, range = 2.04 mA	–	33	100	µA
		Slow mode, sink mode, range = 31.875 µA	–	36	100	µA
		Slow mode, sink mode, range = 255 µA	–	33	100	µA
		Slow mode, sink mode, range = 2.04 mA	–	33	100	µA
		Fast mode, source mode, range = 31.875 µA	–	310	500	µA
		Fast mode, source mode, range = 255 µA	–	305	500	µA
		Fast mode, source mode, range = 2.04 mA	–	305	500	µA
		Fast mode, sink mode, range = 31.875 µA	–	310	500	µA
		Fast mode, sink mode, range = 255 µA	–	300	500	µA
		Fast mode, sink mode, range = 2.04 mA	–	300	500	µA

Note
61. Based on device characterization (Not production tested).

13. Packaging

Table 13-1. Package Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Units
T_A	Operating ambient temperature		–40	25	105	°C
T_J	Operating junction temperature		–40	–	120	°C
T_{JA}	Package θ_{JA} (68-pin QFN)		–	15	–	°C/Watt
T_{JA}	Package θ_{JA} (100-pin TQFP)		–	34	–	°C/Watt
T_{JC}	Package θ_{JC} (68-pin QFN)		–	13	–	°C/Watt
T_{JC}	Package θ_{JC} (100-pin TQFP)		–	10	–	°C/Watt
T_A	Operating ambient temperature	For CSP parts	–40	25	85	°C
T_J	Operating junction temperature	For CSP parts	–40	–	100	°C
T_{JA}	Package θ_{JA} (99-ball CSP)			16.5		°C/Watt
T_{Jc}	Package θ_{JC} (99-ball CSP)		–	0.1	–	°C/Watt

Table 13-2. Solder Reflow Peak Temperature

Package	Maximum Peak Temperature	Maximum Time at Peak Temperature
68-pin QFN	260 °C	30 seconds
100-pin TQFP	260 °C	30 seconds
99-ball WLCSP	255 °C	30 seconds

Table 13-3. Package Moisture Sensitivity Level (MSL), IPC/JEDEC J-STD-2

Package	MSL
68-pin QFN	MSL 3
100-pin TQFP	MSL 3
99-ball WLCSP	MSL1

14. Acronyms

Table 14-1. Acronyms Used in this Document

Acronym	Description
abus	analog local bus
ADC	analog-to-digital converter
AG	analog global
AHB	AMBA (advanced microcontroller bus architecture) high-performance bus, an ARM data transfer bus
ALU	arithmetic logic unit
AMUXBUS	analog multiplexer bus
API	application programming interface
APSR	application program status register
ARM®	advanced RISC machine, a CPU architecture
ATM	automatic thump mode
BW	bandwidth
CAN	Controller Area Network, a communications protocol
CMRR	common-mode rejection ratio
CPU	central processing unit
CRC	cyclic redundancy check, an error-checking protocol
DAC	digital-to-analog converter, see also IDAC, VDAC
DFB	digital filter block
DIO	digital input/output, GPIO with only digital capabilities, no analog. See GPIO.
DMA	direct memory access, see also TD
DNL	differential nonlinearity, see also INL
DNU	do not use
DR	port write data registers
DSI	digital system interconnect
DWT	data watchpoint and trace
ECC	error correcting code
ECO	external crystal oscillator
EEPROM	electrically erasable programmable read-only memory
EMI	electromagnetic interference
EMIF	external memory interface
EOC	end of conversion
EOF	end of frame
EPSR	execution program status register
ESD	electrostatic discharge
ETM	embedded trace macrocell

Table 14-1. Acronyms Used in this Document (continued)

Acronym	Description
FIR	finite impulse response, see also IIR
FPB	flash patch and breakpoint
FS	full-speed
GPIO	general-purpose input/output, applies to a PSoC pin
HVI	high-voltage interrupt, see also LVI, LVD
IC	integrated circuit
IDAC	current DAC, see also DAC, VDAC
IDE	integrated development environment
I^2C, or IIC	Inter-Integrated Circuit, a communications protocol
IIR	infinite impulse response, see also FIR
ILO	internal low-speed oscillator, see also IMO
IMO	internal main oscillator, see also ILO
INL	integral nonlinearity, see also DNL
I/O	input/output, see also GPIO, DIO, SIO, USBIO
IPOR	initial power-on reset
IPSR	interrupt program status register
IRQ	interrupt request
ITM	instrumentation trace macrocell
LCD	liquid crystal display
LIN	Local Interconnect Network, a communications protocol.
LR	link register
LUT	lookup table
LVD	low-voltage detect, see also LVI
LVI	low-voltage interrupt, see also HVI
LVTTL	low-voltage transistor-transistor logic
MAC	multiply-accumulate
MCU	microcontroller unit
MISO	master-in slave-out
NC	no connect
NMI	nonmaskable interrupt
NRZ	non-return-to-zero
NVIC	nested vectored interrupt controller
NVL	nonvolatile latch, see also WOL
opamp	operational amplifier
PAL	programmable array logic, see also PLD
PC	program counter
PCB	printed circuit board
PGA	programmable gain amplifier

Document History Page (continued)

Description Title: PSoC® 5LP: CY8C58LP Family Datasheet Programmable System-on-Chip (PSoC®) Document Number: 001-84932				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
*J	5030641	MKEA	11/30/2015	Added Table 2-1. Removed the configurable XRES information. Updated *Section 5.6* Updated *Section 6.3.1.1*. Updated values for DSI Fmax, Fgpioin max, and Fsioin max. Corrected the web link for the PSoC 5 Device Programming Specifications in *Section 9.* Updated CSP Package Bootloader section. Added MHzECO DC Specifications. Updated 99-WLCSP and 100-pin TQFP package drawings. Added a footnote reference for the "CY8C5287AXI-LP095" part in Table 12-1 clarifying that it has 256 KB flash. Added the CY8C5667AXQ-LP040 part in Table 12-1.
*K	5478402	MKEA	10/25/2016	Updated More Information. Add Links to CAD Libraries in *Section 2.* Corrected typos in External Electrical Connections.
*L	5703770	GNKK	04/20/2017	Updated the Cypress logo and copyright information.

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