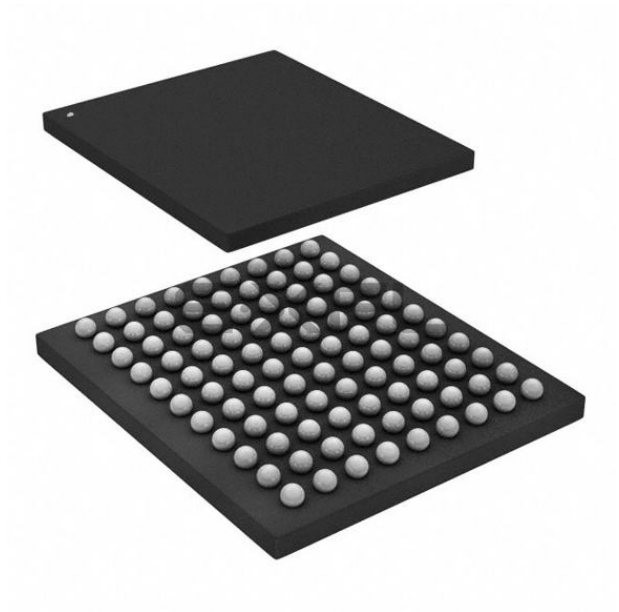
Infineon Technologies - CY8C5888FNI-LP214T Datasheet



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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	I²C, LINbus, SPI, UART/USART, USB
Peripherals	CapSense, DMA, LCD, POR, PWM, WDT
Number of I/O	62
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 5.5V
Data Converters	A/D 1x20b, 2x12b; D/A 4x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	99-UFBGA, WLCSP
Supplier Device Package	99-WLCSP (5.19x5.94)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c5888fni-lp214t

More Information

Cypress provides a wealth of data at www.cypress.com to help you to select the right PSoC device for your design, and to help you to quickly and effectively integrate the device into your design. For a comprehensive list of resources, see the knowledge base article KBA86521, How to Design with PSoC 3, PSoC 4, and PSoC 5LP. Following is an abbreviated list for PSoC 5LP:

- Overview: PSoC Portfolio, PSoC Roadmap
- Product Selectors: PSoC 1, PSoC 3, PSoC 4, PSoC 5LP
  In addition, PSoC Creator includes a device selection tool.
- Application notes: Cypress offers a large number of PSoC application notes and code examples covering a broad range of topics, from basic to advanced level. Recommended application notes for getting started with PSoC 5LP are:
  - AN77759: Getting Started With PSoC 5LP
  - AN77835: PSoC 3 to PSoC 5LP Migration Guide
  - AN61290: Hardware Design Considerations
  - AN57821: Mixed Signal Circuit Board Layout
  - AN58304: Pin Selection for Analog Designs
  - AN81623: Digital Design Best Practices
  - AN73854: Introduction To Bootloaders
- Development Kits:
  - CY8CKIT-059 is a low-cost platform for prototyping, with a unique snap-away programmer and debugger on the USB connector.
  - CY8CKIT-050 is designed for analog performance, for developing high-precision analog, low-power, and low-voltage applications.
  - CY8CKIT-001 provides a common development platform for any one of the PSoC 1, PSoC 3, PSoC 4, or PSoC 5LP families of devices.
  - The MiniProg3 device provides an interface for flash programming and debug.
- Technical Reference Manuals (TRM)
  - Architecture TRM
  - Registers TRM
- Programming Specification

PSoC Creator

PSoC Creator is a free Windows-based Integrated Design Environment (IDE). It enables concurrent hardware and firmware design of PSoC 3, PSoC 4, and PSoC 5LP based systems. Create designs using classic, familiar schematic capture supported by over 100 pre-verified, production-ready PSoC Components; see the list of component datasheets. With PSoC Creator, you can:

1. Drag and drop component icons to build your hardware system design in the main design workspace
2. Codesign your application firmware with the PSoC hardware, using the PSoC Creator IDE C compiler
3. Configure components using the configuration tools
4. Explore the library of 100+ components
5. Review component datasheets

Figure 1. Multiple-Sensor Example Project in PSoC Creator

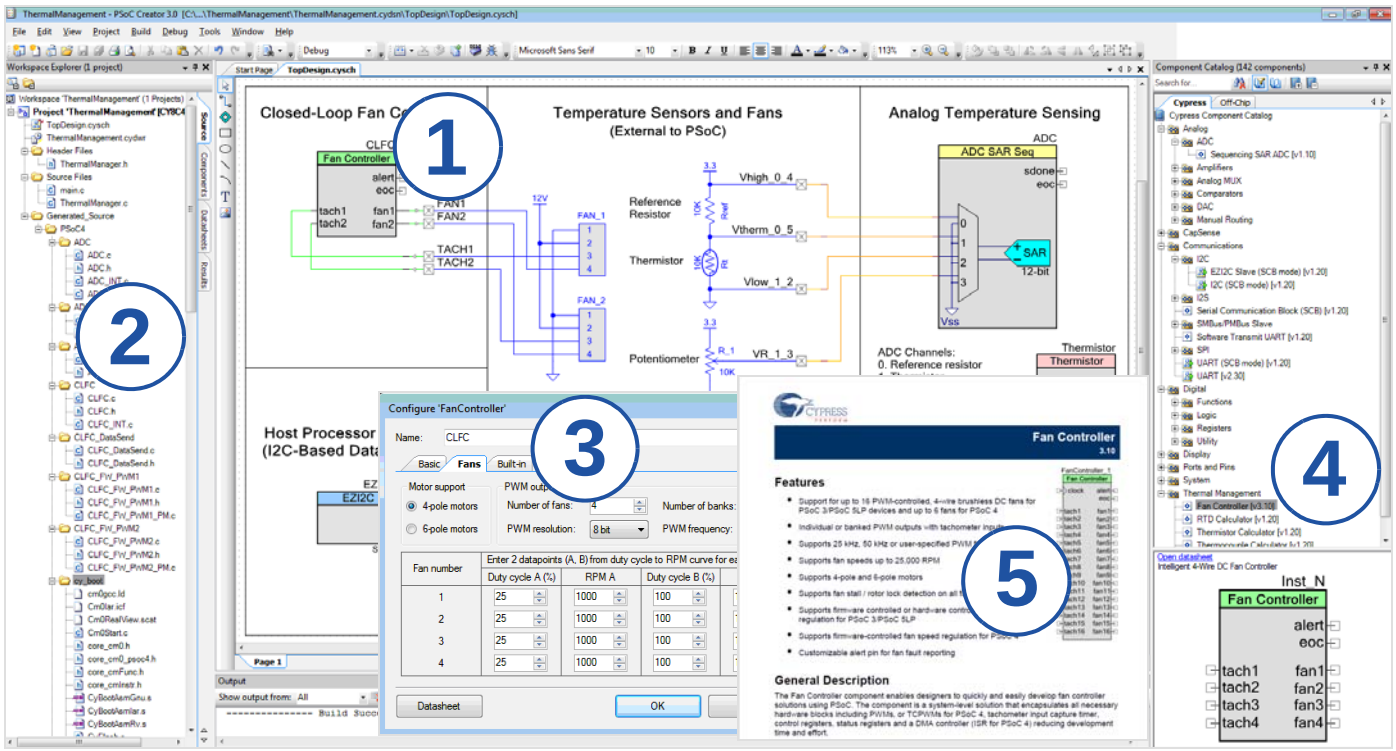
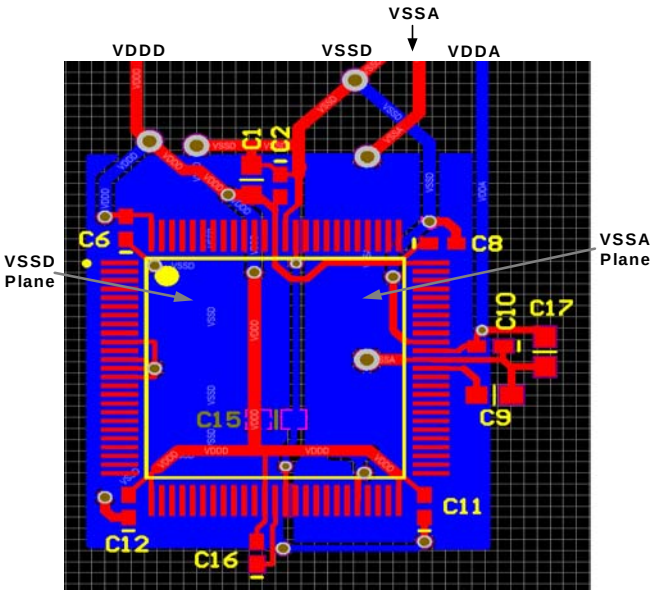


Figure 2-6. Example PCB Layout for 100-pin TQFP Part for Optimal Analog Performance

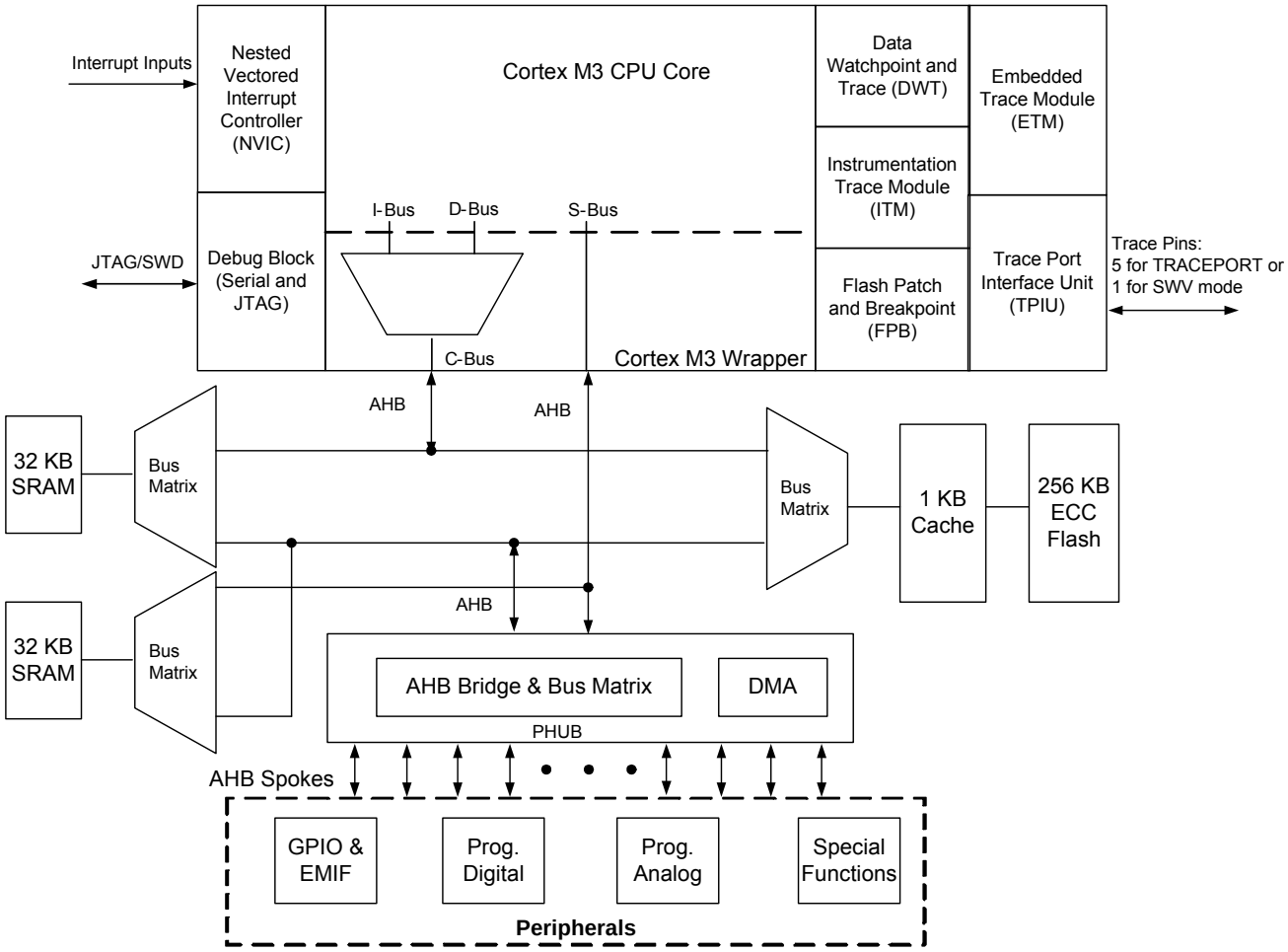


4. CPU

4.1 ARM Cortex-M3 CPU

The CY8C58LP family of devices has an ARM Cortex-M3 CPU core. The Cortex-M3 is a low-power 32-bit three-stage pipelined Harvard-architecture CPU that delivers 1.25 DMIPS/MHz. It is intended for deeply embedded applications that require fast interrupt handling features.

Figure 4-1. ARM Cortex-M3 Block Diagram



The Cortex-M3 CPU subsystem includes these features:

- ARM Cortex-M3 CPU
- Programmable nested vectored interrupt controller (NVIC), tightly integrated with the CPU core
- Full featured debug and trace modules, tightly integrated with the CPU core
- Up to 256 KB of flash memory, 2 KB of EEPROM, and 64 KB of SRAM
- Cache controller
- Peripheral HUB (PHUB)
- DMA controller
- External memory interface (EMIF)

4.1.1 Cortex-M3 Features

The Cortex-M3 CPU features include:

- 4 GB address space. Predefined address regions for code, data, and peripherals. Multiple buses for efficient and simultaneous accesses of instructions, data, and peripherals.
- The Thumb®-2 instruction set, which offers ARM-level performance at Thumb-level code density. This includes 16-bit and 32-bit instructions. Advanced instructions include:
  - Bit-field control
  - Hardware multiply and divide
  - Saturation
  - If-Then
  - Wait for events and interrupts
  - Exclusive access and barrier
  - Special register access

5.6 External Memory Interface

CY8C58LP provides an external memory interface (EMIF) for connecting to external memory devices. The connection allows read and write accesses to external memories. The EMIF operates in conjunction with UDBs, I/O ports, and other hardware to generate external memory address and control signals. At 33 MHz, each memory access cycle takes four bus clock cycles.

Figure 5-1 is the EMIF block diagram. The EMIF supports synchronous and asynchronous memories. The CY8C58LP only supports one type of external memory device at a time.

External memory is located in the Cortex-M3 external RAM space; it can use up to 24 address bits. See Memory Map on page 22. The memory can be 8 or 16 bits wide.

Cortex-M3 instructions can be fetched from external memory if it is 16-bit. Other limitations apply; for details, see application note AN89610, PSoC® 4 and PSoC 5LP ARM Cortex Code Optimization. There is no provision for code security in external memory. If code must be kept secure, then it should be placed in internal flash. See Flash Security on page 19 and Device Security on page 64.

Figure 5-1. EMIF Block Diagram

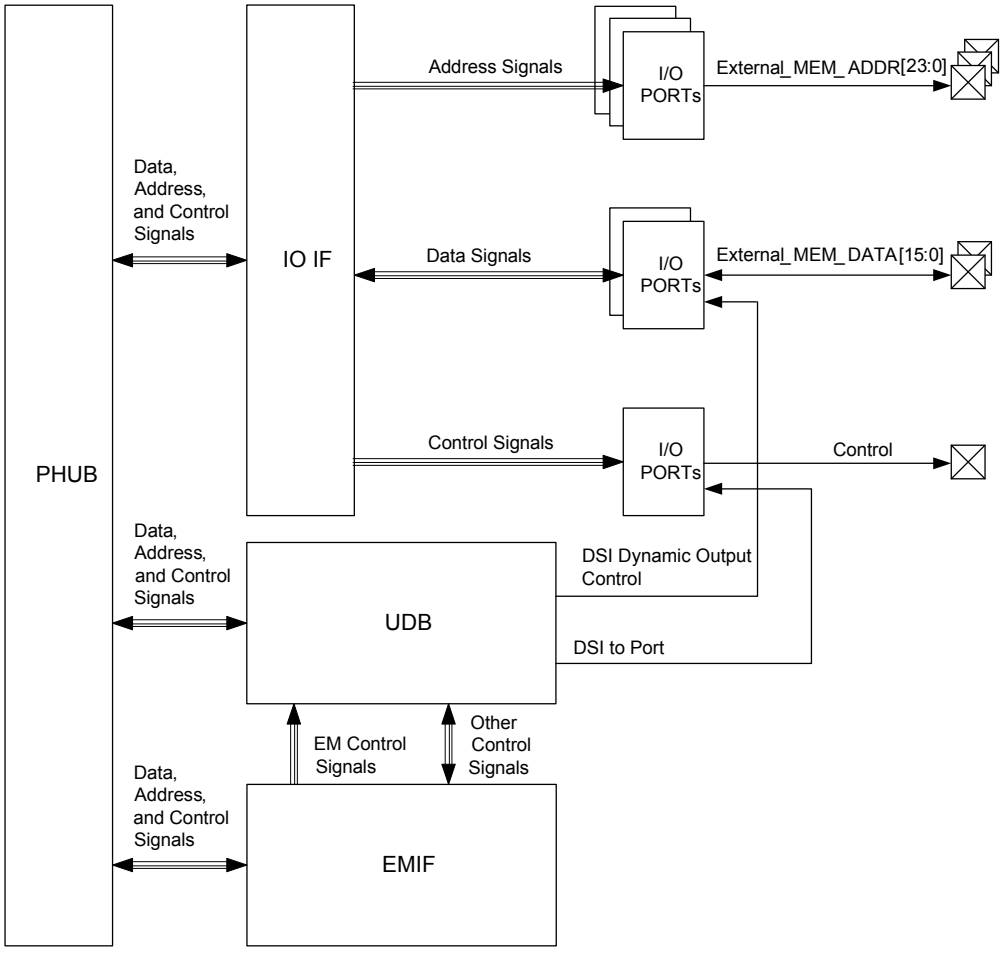
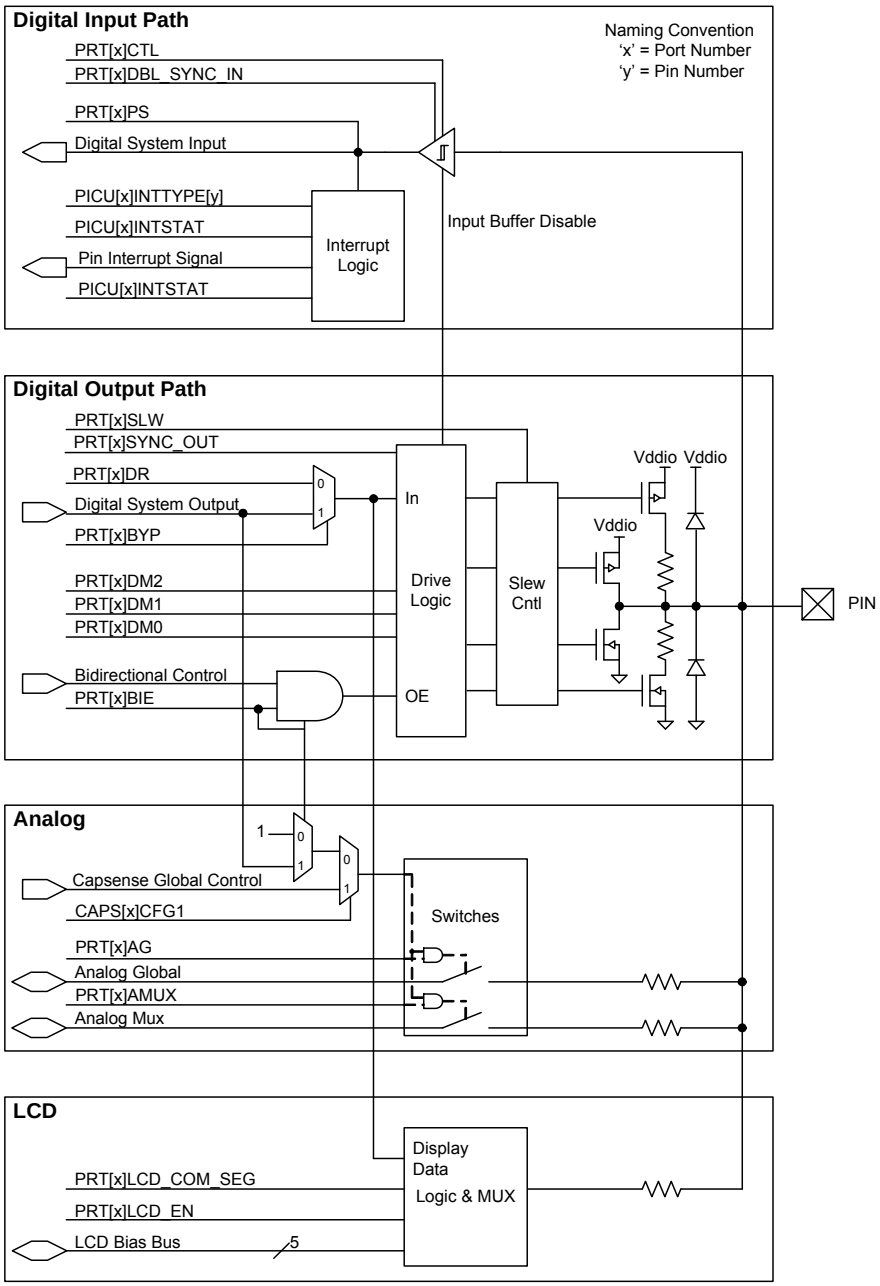


Figure 6-8. GPIO Block Diagram

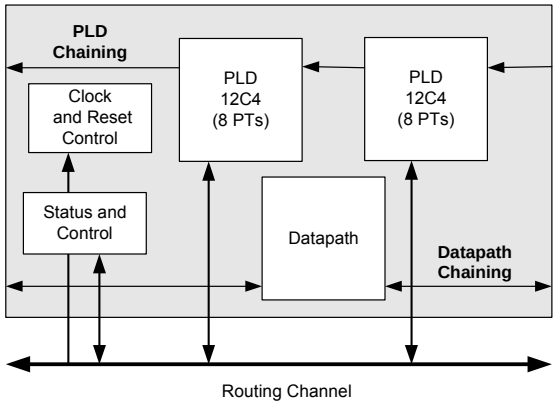


7.2 Universal Digital Block

The Universal Digital Block (UDB) represents an evolutionary step to the next generation of PSoC embedded digital peripheral functionality. The architecture in first generation PSoC digital blocks provides coarse programmability in which a few fixed functions with a small number of options are available. The new UDB architecture is the optimal balance between configuration granularity and efficient implementation. A cornerstone of this approach is to provide the ability to customize the devices digital operation to match application requirements.

To achieve this, UDBs consist of a combination of uncommitted logic (PLD), structured logic (Datapath), and a flexible routing scheme to provide interconnect between these elements, I/O connections, and other peripherals. UDB functionality ranges from simple self contained functions that are implemented in one UDB, or even a portion of a UDB (unused resources are available for other functions), to more complex functions that require multiple UDBs. Examples of basic functions are timers, counters, CRC generators, PWMs, dead band generators, and communications functions, such as UARTs, SPI, and I^2C. Also, the PLD blocks and connectivity provide full featured general purpose programmable logic within the limits of the available resources.

Figure 7-2. UDB Block Diagram



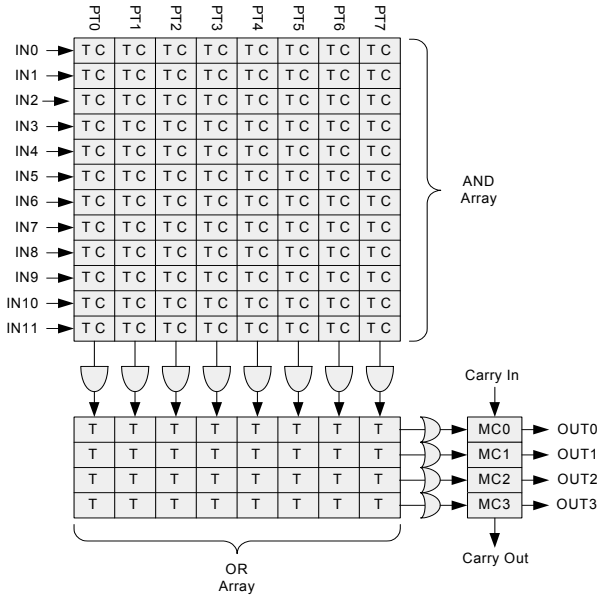
The main component blocks of the UDB are:

- PLD blocks - There are two small PLDs per UDB. These blocks take inputs from the routing array and form registered or combinational sum-of-products logic. PLDs are used to implement state machines, state bits, and combinational logic equations. PLD configuration is automatically generated from graphical primitives.
- Datapath Module - This 8-bit wide datapath contains structured logic to implement a dynamically configurable ALU, a variety of compare configurations and condition generation. This block also contains input/output FIFOs, which are the primary parallel data interface between the CPU/DMA system and the UDB.
- Status and Control Module - The primary role of this block is to provide a way for CPU firmware to interact and synchronize with UDB operation.
- Clock and Reset Module - This block provides the UDB clocks and reset selection and control.

7.2.1 PLD Module

The primary purpose of the PLD blocks is to implement logic expressions, state machines, sequencers, look up tables, and decoders. In the simplest use model, consider the PLD blocks as a standalone resource onto which general purpose RTL is synthesized and mapped. The more common and efficient use model is to create digital functions from a combination of PLD and datapath blocks, where the PLD implements only the random logic and state portion of the function while the datapath (ALU) implements the more structured elements.

Figure 7-3. PLD 12C4 Structure

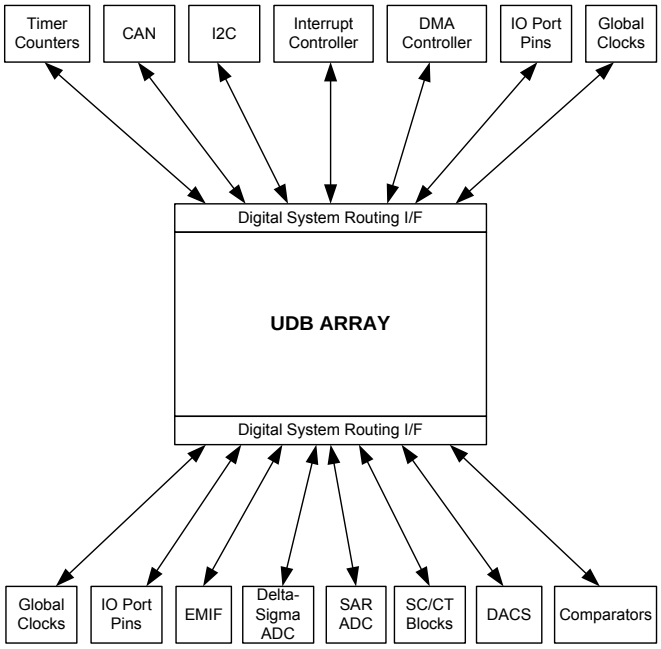


One 12C4 PLD block is shown in Figure 7-3. This PLD has 12 inputs, which feed across eight product terms. Each product term (AND function) can be from 1 to 12 inputs wide, and in a given product term, the true (T) or complement (C) of each input can be selected. The product terms are summed (OR function) to create the PLD outputs. A sum can be from 1 to 8 product terms wide. The 'C' in 12C4 indicates that the width of the OR gate (in this case 8) is constant across all outputs (rather than variable as in a 22V10 device). This PLA like structure gives maximum flexibility and insures that all inputs and outputs are permutable for ease of allocation by the software tools. There are two 12C4 PLDs in each UDB.

7.2.2 Datapath Module

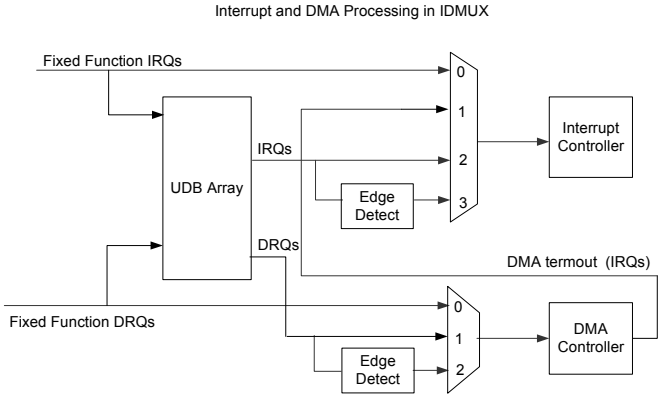
The datapath contains an 8-bit single cycle ALU, with associated compare and condition generation logic. This datapath block is optimized to implement embedded functions, such as timers, counters, integrators, PWMs, PRS, CRC, shifters and dead band generators, and many others.

Figure 7-9. Digital System Interconnect



Interrupt and DMA routing is very flexible in the CY8C58LP programmable architecture. In addition to the numerous fixed function peripherals that can generate interrupt requests, any data signal in the UDB array routing can also be used to generate a request. A single peripheral may generate multiple independent interrupt requests simplifying system and firmware design. Figure 7-10 shows the structure of the IDMUX (Interrupt/DMA Multiplexer).

Figure 7-10. Interrupt and DMA Processing in the IDMUX



7.4.1 I/O Port Routing

There are a total of 20 DSI routes to a typical 8-bit I/O port, 16 for data and four for drive strength control.

When an I/O pin is connected to the routing, there are two primary connections available, an input and an output. In conjunction with drive strength control, this can implement a bidirectional I/O pin. A data output signal has the option to be single synchronized (pipelined) and a data input signal has the option to be double synchronized. The synchronization clock is the system clock (see Figure 6-1). Normally all inputs from pins are synchronized as this is required if the CPU interacts with the signal or any signal derived from it. Asynchronous inputs have rare uses. An example of this is a feed through of combinational PLD logic from input pins to output pins.

Figure 7-11. I/O Pin Synchronization Routing

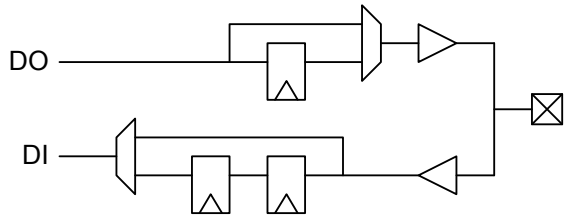
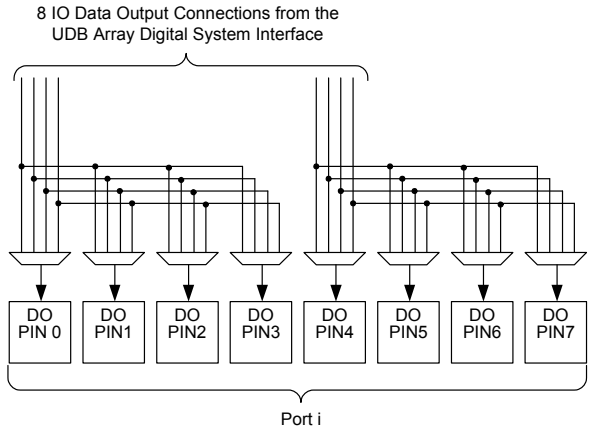


Figure 7-12. I/O Pin Output Connectivity



There are four more DSI connections to a given I/O port to implement dynamic output enable control of pins. This connectivity gives a range of options, from fully ganged 8-bits controlled by one signal, to up to four individually controlled pins. The output enable signal is useful for creating tri-state bidirectional pins and buses.

Figure 7-13. I/O Pin Output Enable Connectivity

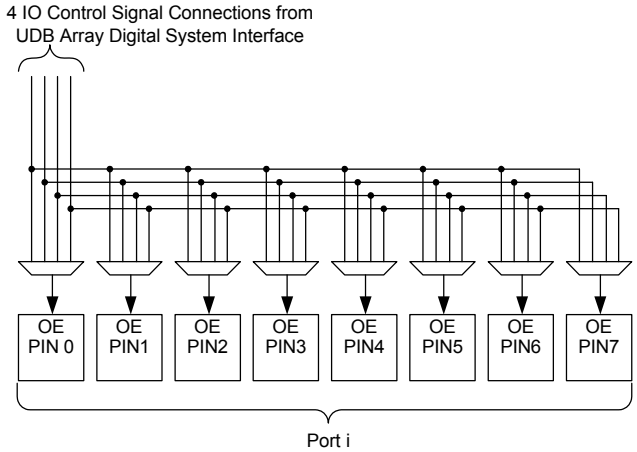
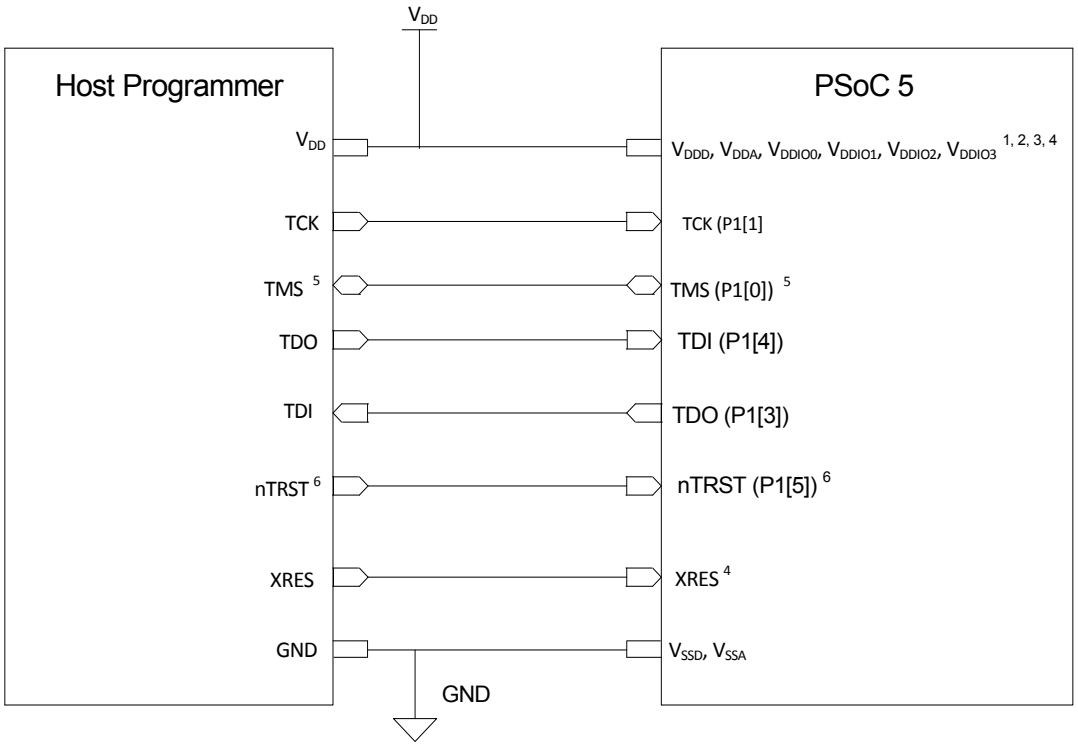


Figure 9-1. JTAG Interface Connections between PSoC 5LP and Programmer



[1] The voltage levels of Host Programmer and the PSoC 5 voltage domains involved in Programming should be same. The Port 1 JTAG pins and XRES pin are powered by V_{DDIO1}. So, V_{DDIO1} of PSoC 5 should be at same voltage level as host V_{DD}. Rest of PSoC 5 voltage domains (V_{DDD}, V_{DDA}, V_{DDIO0}, V_{DDIO2}, V_{DDIO3}) need not be at the same voltage level as host Programmer.

[2] Vdda must be greater than or equal to all other power supplies (Vddd, Vddio's) in PSoC 5.

[3] For Power cycle mode Programming, XRES pin is not required. But the Host programmer must have the capability to toggle power (Vddd, Vdda, All Vddio's) to PSoC 5. This may typically require external interface circuitry to toggle power which will depend on the programming setup. The power supplies can be brought up in any sequence, however, once stable, VDDA must be greater than or equal to all other supplies.

[4] For JTAG Programming, Device reset can also be done without connecting to the XRES pin or Power cycle mode by using the TMS,TCK,TDI, TDO pins of PSoC 5, and writing to a specific register. But this requires that the DPS setting in NVL is not equal to "Debug Ports Disabled".

[5] By default, PSoC 5 is configured for 4-wire JTAG mode unless user changes the DPS setting. So the TMS pin is unidirectional. But if the DPS setting is changed to non-JTAG mode, the TMS pin in JTAG is bi-directional as the SWD Protocol has to be used for acquiring the PSoC 5 device initially. After switching from SWD to JTAG mode, the TMS pin will be uni-directional. In such a case, unidirectional buffer should not be used on TMS line.

[6] nTRST JTAG pin (P1[5]) cannot be used to reset the JTAG TAP controlller during first time programming of PSoC 5 as the default setting is 4-wire JTAG (nTRST disabled). Use the TMS, TCK pins to do a reset of JTAG TAP controller.

10. Development Support

The CY8C58LP family has a rich set of documentation, development tools, and online resources to assist you during your development process. Visit psoc.cypress.com/getting-started to find out more.

10.1 Documentation

A suite of documentation, to ensure that you can find answers to your questions quickly, supports the CY8C58LP family. This section contains a list of some of the key documents.

Software User Guide: A step-by-step guide for using PSoC Creator. The software user guide shows you how the PSoC Creator build process works in detail, how to use source control with PSoC Creator, and much more.

Component Datasheets: The flexibility of PSoC allows the creation of new peripherals (components) long after the device has gone into production. Component datasheets provide all of the information needed to select and use a particular component, including a functional description, API documentation, example code, and AC/DC specifications.

Application Notes: PSoC application notes discuss a particular application of PSoC in depth; examples include brushless DC motor control and on-chip filtering. Application notes often include example projects in addition to the application note document.

Technical Reference Manual: PSoC Creator makes designing with PSoC as easy as dragging a peripheral onto a schematic, but, when low level details of the PSoC device are required, use the technical reference manual (TRM) as your guide.

Note Visit www.arm.com for detailed documentation about the Cortex-M3 CPU.

10.2 Online

In addition to print documentation, the Cypress PSoC forums connect you with fellow PSoC users and experts in PSoC from around the world, 24 hours a day, 7 days a week.

10.3 Tools

With industry standard cores, programming, and debugging interfaces, the CY8C58LP family is part of a development tool ecosystem. Visit us at www.cypress.com/go/psoccreator for the latest information on the revolutionary, easy to use PSoC Creator IDE, supported third party compilers, programmers, debuggers, and development kits.

11. Electrical Specifications

Specifications are valid for –40 °C ≤ T_A ≤ 105 °C and T_J ≤ 120 °C, except where noted. Specifications are valid for 1.71 V to 5.5 V, except where noted. The unique flexibility of the PSoC UDBs and analog blocks enable many functions to be implemented in PSoC Creator components, see the component datasheets for full AC/DC specifications of individual functions. See the Example Peripherals on page 40 for further explanation of PSoC Creator components.

11.1 Absolute Maximum Ratings

Table 11-1. Absolute Maximum Ratings DC Specifications[14]

Parameter	Description	Conditions	Min	Typ	Max	Units
V_{DDA}	Analog supply voltage relative to V_{SSA}		–0.5	–	6	V
V_{DDD}	Digital supply voltage relative to V_{SSD}		–0.5	–	6	V
V_{DDIO}	I/O supply voltage relative to V_{SSD}		–0.5	–	6	V
V_{CCA}	Direct analog core voltage input		–0.5	–	1.95	V
V_{CCD}	Direct digital core voltage input		–0.5	–	1.95	V
V_{SSA}	Analog ground voltage		V_{SSD} – 0.5	–	V_{SSD} + 0.5	V
V_{GPIO}[15]	DC input voltage on GPIO	Includes signals sourced by V_{DDA} and routed internal to the pin.	V_{SSD} – 0.5	–	V_{DDIO} + 0.5	V
V_{SIO}	DC input voltage on SIO	Output disabled	V_{SSD} – 0.5	–	7	V
		Output enabled	V_{SSD} – 0.5	–	6	V
V_{IND}	Voltage at boost converter input		0.5	–	5.5	V
V_{BAT}	Boost converter supply		V_{SSD} – 0.5	–	5.5	V
I_{VDDIO}	Current per V_{DDIO} supply pin		–	–	100	mA
I_{GPIO}	GPIO current		–30	–	41	mA
I_{SIO}	SIO current		–49	–	28	mA
I_{USBIO}	USBIO current		–56	–	59	mA
V_{EXTREF}	ADC external reference inputs	Pins P0[3], P3[2]	–	–	2	V
LU	Latch up current[16]		–140	–	140	mA
ESD_{HBM}	Electrostatic discharge voltage	Human body model	2000	–	–	V
ESD_{CDM}	ESD voltage	Charge device model	500	–	–	V

Notes
14. Usage above the absolute maximum conditions listed in Table 11-1 may cause permanent damage to the device. Exposure to Absolute Maximum conditions for extended periods of time may affect device reliability. The Maximum Storage Temperature is 150 °C in compliance with JEDEC Standard JESD22-A103, High Temperature Storage Life. When used below Absolute Maximum conditions but above normal operating conditions, the device may not operate to specification.
15. The V_{DDIO} supply voltage must be greater than the maximum voltage on the associated GPIO pins. Maximum voltage on GPIO pin ≤ V_{DDIO} ≤ V_{DDA}.
16. Meets or exceeds JEDEC Spec EIA/JESD78 IC Latch-up Test.

Table 11-3. AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
F_{CPU}	CPU frequency	1.71 V ≤ V_{DDD} ≤ 5.5 V	DC	–	80.01	MHz
F_{BUSCLK}	Bus frequency	1.71 V ≤ V_{DDD} ≤ 5.5 V	DC	–	80.01	MHz
S_{VDD}[28]	V_{DD} ramp rate		–	–	0.066	V/µs
T_{IO_INIT}[28]	Time from V_{DDD}/V_{DDA}/V_{CCD}/V_{CCA} ≥ IPOR to I/O ports set to their reset states		–	–	10	µs
$T_{STARTUP}$[28]	Time from V_{DDD}/V_{DDA}/V_{CCD}/V_{CCA} ≥ PRES to CPU executing code at reset vector	V_{CCA}/V_{DDA} = regulated from V_{DDA}/V_{DDD}, no PLL used, fast IMO boot mode (48 MHz typ.)	–	–	33	µs
		V_{CCA}/V_{CCD} = regulated from V_{DDA}/V_{DDD}, no PLL used, slow IMO boot mode (12 MHz typ.)	–	–	66	µs
T_{SLEEP}[28]	Wakeup from sleep mode – Application of non-LVD interrupt to beginning of execution of next CPU instruction		–	–	25	µs
$T_{HIBERNATE}$[28]	Wakeup from hibernate mode – Application of external interrupt to beginning of execution of next CPU instruction		–	–	150	µs

11.3 Power Regulators

Specifications are valid for –40 °C ≤ T_A ≤ 105 °C and T_J ≤ 120 °C, except where noted. Specifications are valid for 1.71 V to 5.5 V, except where noted.

11.3.1 Digital Core Regulator

Table 11-4. Digital Core Regulator DC *Specifications*

Parameter	Description	Conditions	Min	Typ	Max	Units
V_{DDD}	Input voltage		1.8	–	5.5	V
V_{CCD}	Output voltage		–	1.80	–	V
	Regulator output capacitor	±10%, X5R ceramic or better. The two V_{CCD} pins must be shorted together, with as short a trace as possible, see "Power System" section on page 26	0.9	1	1.1	µF

Figure 11-5. Analog and Digital Regulators, V_{CC} vs V_{DD}, 10 mA Load

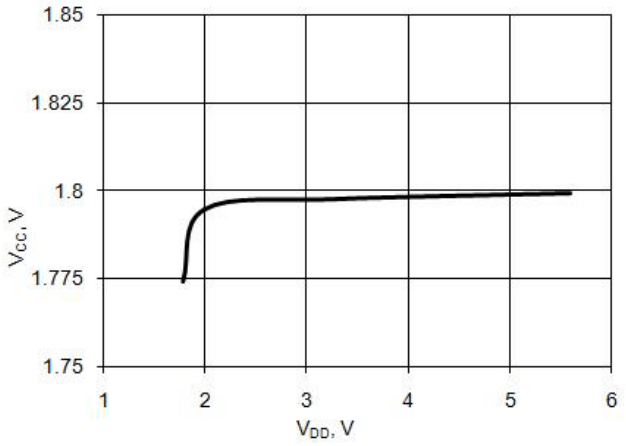
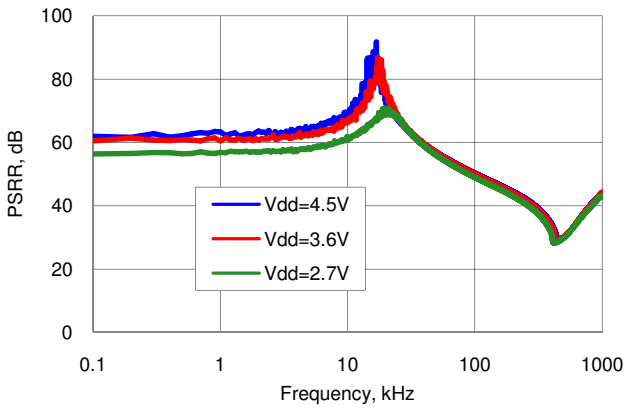


Figure 11-6. Digital Regulator PSRR vs Frequency and V_{DD}



Note
28. Based on device characterization (Not production tested).

Table 11-6. Inductive Boost Regulator DC Specifications (continued)

Parameter	Description	Conditions		Min	Typ	Max	Units
I_{OUT}	Output current	T_A = 0 °C–70 °C	V_{BAT} = 0.5 V–0.8 V	0	–	5	mA
		T_A = –10 °C–85 °C	V_{BAT} = 1.6 V–3.6 V	0	–	15	mA
			V_{BAT} = 0.8 V–1.6 V	0	–	25	mA
			V_{BAT} = 1.3 V–2.5 V	0	–	50	mA
			V_{BAT} = 2.5 V–3.6 V	0	–	50	mA
		T_A = –40 °C–85 °C	V_{BAT} = 1.8 V–2.5 V	0	–	50	mA
I_{LPK}	Inductor peak current			–	–	700	mA
I_Q	Quiescent current	Boost active mode		–	250	–	µA
		Boost sleep mode, I_{OUT} < 1 µA		–	25	–	µA
Reg_{LOAD}	Load regulation			–	–	10	%
Reg_{LINE}	Line regulation			–	–	10	%

Notes
29. Listed vsel options are characterized. Additional VSEL options are valid and guaranteed by design.
30. The boost will start at all valid V_{BAT} conditions including down to V_{BAT} = 0.5 V.
31. If V_{BAT} is greater than or equal to V_{OUT} boost setting, then V_{OUT} will be less than V_{BAT} due to resistive losses in the boost circuit.

Table 11-20. 20-bit Delta-sigma ADC DC Specifications (continued)

Parameter	Description	Conditions	Min	Typ	Max	Units
Rin_Buff	ADC input resistance	Input buffer used	10	–	–	MΩ
Rin_ADC16	ADC input resistance	Input buffer bypassed, 16-bit, Range = ±1.024 V	–	74[46]	–	kΩ
Rin_ADC12	ADC input resistance	Input buffer bypassed, 12 bit, Range = ±1.024 V	–	148[46]	–	kΩ
Rin_ExtRef	ADC external reference input resistance		–	70[46, 47]	–	kΩ
Vextref	ADC external reference input voltage, see also internal reference in Voltage Reference on page 93	Pins P0[3], P3[2]	0.9	–	1.3	V
Current Consumption						
I_{DD_20}	I_{DDA} + I_{DDD} Current consumption, 20 bit[48]	187 sps, unbuffered	–	–	1.5	mA
I_{DD_16}	I_{DDA} + I_{DDD} Current consumption, 16 bit[48]	48 ksps, unbuffered	–	–	1.5	mA
I_{DD_12}	I_{DDA} + I_{DDD} Current consumption, 12 bit[48]	192 ksps, unbuffered	–	–	1.95	mA
I_{DD_8}	I_{DDA} + I_{DDD} Current consumption, 8 bit[48]	384 ksps, unbuffered	–	–	1.95	mA
I_{BUFF}	Buffer current consumption[48]		–	–	2.5	mA

Table 11-21. Delta-sigma ADC AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Startup time		–	–	4	Samples
THD	Total harmonic distortion[48]	Buffer gain = 1, 16 bit, Range = ±1.024 V	–	–	0.0032	%
20-Bit Resolution Mode						
SR20	Sample rate[48]	Range = ±1.024 V, unbuffered	7.8	–	187	sps
BW20	Input bandwidth at max sample rate[48]	Range = ±1.024 V, unbuffered	–	40	–	Hz
16-Bit Resolution Mode						
SR16	Sample rate[48]	Range = ±1.024 V, unbuffered	2	–	48	ksps
BW16	Input bandwidth at max sample rate[48]	Range = ±1.024 V, unbuffered	–	11	–	kHz
SINAD16int	Signal to noise ratio, 16-bit, internal reference[48]	Range = ±1.024V, unbuffered	81	–	–	dB
		T_A ≤ 105 °C	77	–	–	
SINAD16ext	Signal to noise ratio, 16-bit, external reference[48]	Range = ±1.024 V, unbuffered	84	–	–	dB
12-Bit Resolution Mode						
SR12	Sample rate, continuous, high power[48]	Range = ±1.024 V, unbuffered	4	–	192	ksps
BW12	Input bandwidth at max sample rate[48]	Range = ±1.024 V, unbuffered	–	44	–	kHz
SINAD12int	Signal to noise ratio, 12-bit, internal reference[48]	Range = ±1.024 V, unbuffered	66	–	–	dB
8-Bit Resolution Mode						
SR8	Sample rate, continuous, high power[48]	Range = ±1.024 V, unbuffered	8	–	384	ksps
BW8	Input bandwidth at max sample rate[48]	Range = ±1.024 V, unbuffered	–	88	–	kHz
SINAD8int	Signal to noise ratio, 8-bit, internal reference[48]	Range = ±1.024 V, unbuffered	43	–	–	dB

Notes
46. By using switched capacitors at the ADC input an effective input resistance is created. Holding the gain and number of bits constant, the resistance is proportional to the inverse of the clock frequency. This value is calculated, not measured. For more information see the Technical Reference Manual.
47. Recommend an external reference device with an output impedance <100 Ω, for example, the LM185/285/385 family. A 1 µF capacitor is recommended. For more information, see AN61290 - PSoC® 3 and PSoC 5LP Hardware Design Considerations.
48. Based on device characterization (not production tested).

Table 11-22. Delta-sigma ADC Sample Rates, Range = ±1.024 V

Resolution, Bits	Continuous		Multi-Sample		Multi-Sample Turbo	
	Min	Max	Min	Max	Min	Max
8	8000	384000	1911	91701	1829	87771
9	6400	307200	1543	74024	1489	71441
10	5566	267130	1348	64673	1307	62693
11	4741	227555	1154	55351	1123	53894
12	4000	192000	978	46900	956	45850
13	3283	157538	806	38641	791	37925
14	2783	133565	685	32855	674	32336
15	2371	113777	585	28054	577	27675
16	2000	48000	495	11861	489	11725
17	500	12000	124	2965	282	6766
18	125	3000	31	741	105	2513
19	16	375	4	93	15	357
20	8	187.5	2	46	8	183

Figure 11-33. Delta-sigma ADC IDD vs sps, Range = ±1.024 V, Continuous Sample Mode, Input Buffer Bypassed

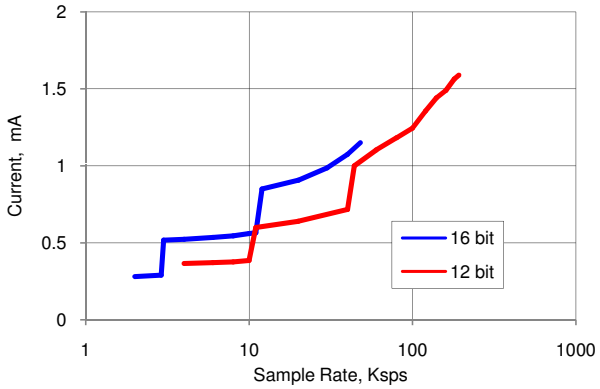


Figure 11-34. Delta-sigma ADC Noise Histogram, 1000 Samples, 20-Bit, 187 sps, Ext Ref, $V_{IN} = V_{REF}/2$, Range = ±1.024 V

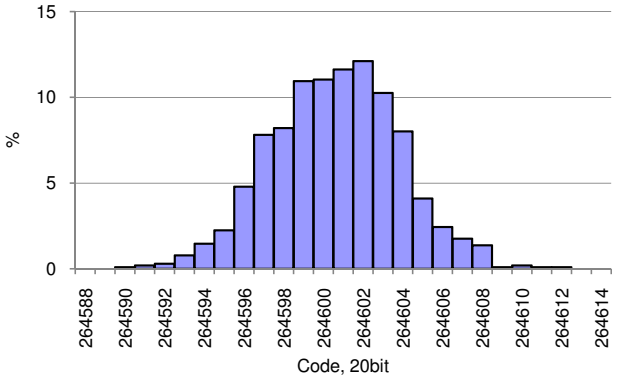


Figure 11-35. Delta-sigma ADC Noise Histogram, 1000 Samples, 16-bit, 48 ksps, Ext Ref, $V_{IN} = V_{REF}/2$, Range = ±1.024 V

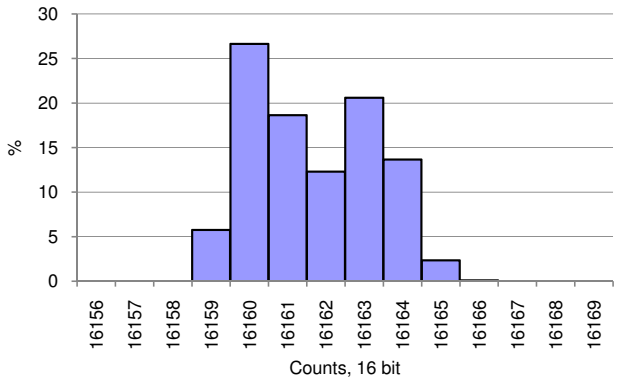
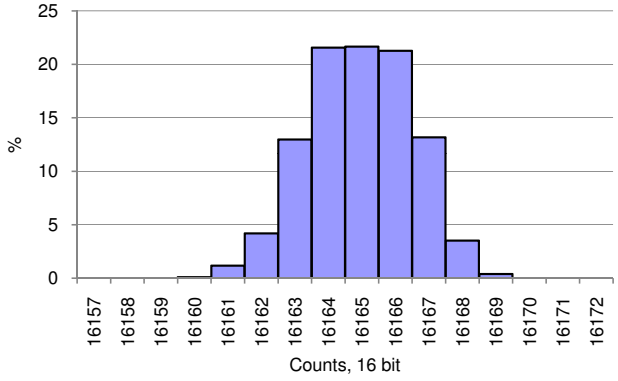


Figure 11-36. Delta-sigma ADC Noise Histogram, 1000 Samples, 16-bit, 48 ksps, Int Ref, $V_{IN} = V_{REF}/2$, Range = ±1.024 V



11.5.3 Voltage Reference

Table 11-27. Voltage Reference Specifications

See ADC external reference specifications in Delta-Sigma ADC on page 88.

Parameter	Description	Conditions		Min	Typ	Max	Units
V_{REF}[50]	Precision reference voltage	Initial trimming, 25 °C		1.023 (–0.1%)	1.024	1.025 (+0.1%)	V
	After typical PCB assembly, post reflow	Typical (non-optimized) board layout and 250 °C solder reflow. Device may be calibrated after assembly to improve performance.	–40 °C	–	±0.5	–	%
			25 °C	–	±0.2	–	%
			85 °C	–	±0.2	–	%
			105 °C	–	±0.3	–	%
	Temperature drift[51]			–	–	30	ppm/°C
	Long term drift[51]			–	100	–	ppm/Khr
	Thermal cycling drift (stability)[51]			–	100	–	ppm

Figure 11-39. Vref vs Temperature

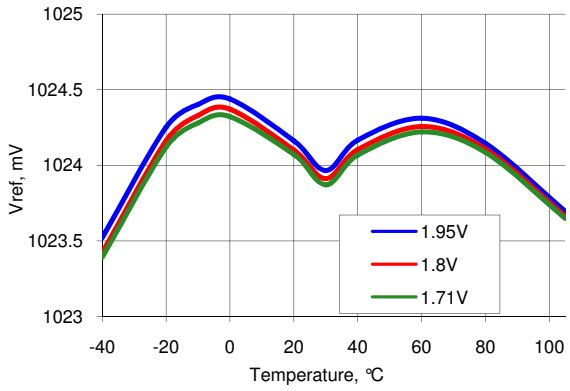
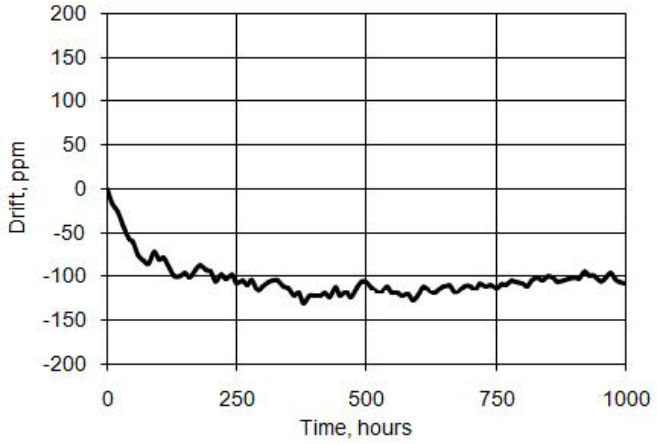


Figure 11-40. Vref Long-term Drift



Notes
50. V_{REF} is measured after packaging, and thus accounts for substrate and die attach stresses.
51. Based on device characterization (Not production tested).

11.5.4 SAR ADC

Table 11-28. SAR ADC DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Resolution		–	–	12	bits
	Number of channels – single-ended		–	–	No of GPIO	
	Number of channels – differential	Differential pair is formed using a pair of neighboring GPIO.	–	–	No of GPIO/2	
	Monotonicity[52]		Yes	–	–	
Ge	Gain error[53]	External reference	–	–	±0.1	%
V_{OS}	Input offset voltage		–	–	±2	mV
I_{DD}	Current consumption[52]		–	–	1	mA
	Input voltage range – single-ended[52]		V_{SSA}	–	V_{DDA}	V
	Input voltage range – differential[52]		V_{SSA}	–	V_{DDA}	V
PSRR	Power supply rejection ratio[52]		70	–	–	dB
CMRR	Common mode rejection ratio		70	–	–	dB
INL	Integral non linearity[52]	V_{DDA} 1.71 to 5.5 V, 1 Msps, V_{REF} 1 to 5.5 V, bypassed at ExtRef pin	–	–	+2/–1.5	LSB
		V_{DDA} 2.0 to 3.6 V, 1 Msps, V_{REF} 2 to V_{DDA}, bypassed at ExtRef pin	–	–	±1.2	LSB
		V_{DDA} 1.71 to 5.5 V, 500 ksps, V_{REF} 1 to 5.5 V, bypassed at ExtRef pin	–	–	±1.3	LSB
DNL	Differential non linearity[52]	V_{DDA} 1.71 to 5.5 V, 1 Msps, V_{REF} 1 to 5.5 V, bypassed at ExtRef pin	–	–	+2/–1	LSB
		V_{DDA} 2.0 to 3.6 V, 1 Msps, V_{REF} 2 to V_{DDA}, bypassed at ExtRef pin No missing codes	–	–	1.7/–0.99	LSB
		V_{DDA} 1.71 to 5.5 V, 500 ksps, V_{REF} 1 to 5.5 V, bypassed at ExtRef pin No missing codes	–	–	+2/–0.99	LSB
R_{IN}	Input resistance[52]		–	180	–	kΩ

Notes
52. Based on device characterization (Not production tested).
53. For total analog system Idd < 5 mA, depending on package used. With higher total analog system currents it is recommended that the SAR ADC be used in differential mode.

Figure 11-47. IDAC INL vs Input Code, Range = 255 µA, Source Mode

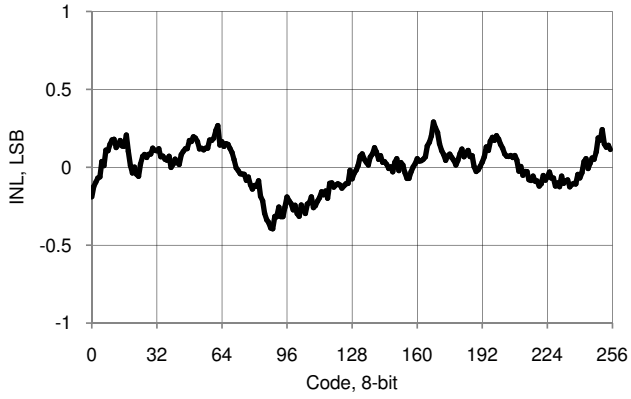


Figure 11-48. IDAC INL vs Input Code, Range = 255 µA, Sink Mode

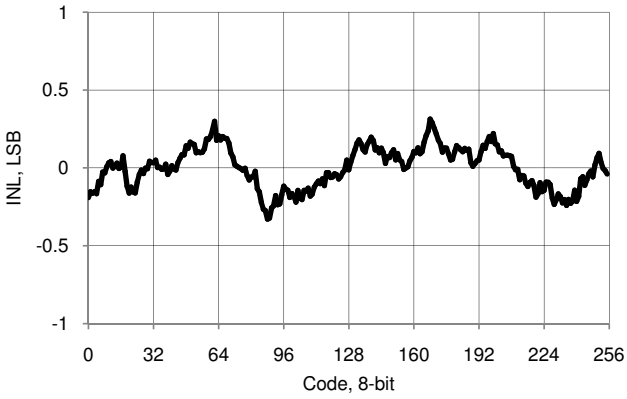


Figure 11-49. IDAC DNL vs Input Code, Range = 255 µA, Source Mode

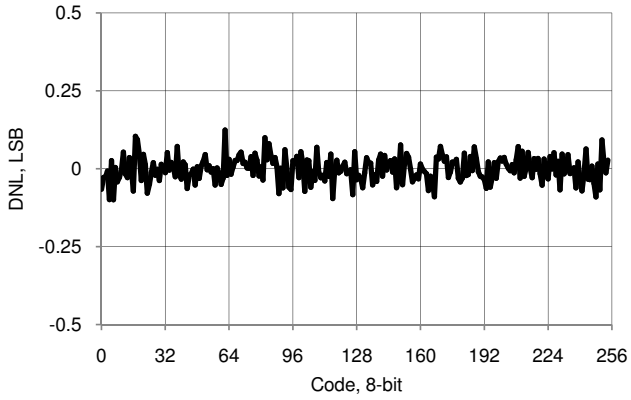


Figure 11-50. IDAC DNL vs Input Code, Range = 255 µA, Sink Mode

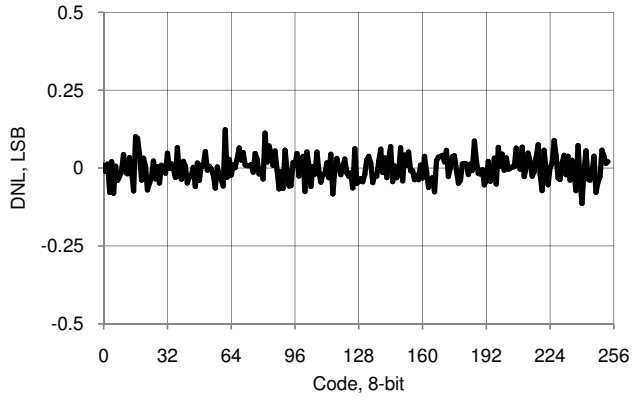


Figure 11-51. IDAC INL vs Temperature, Range = 255 µA, Fast Mode

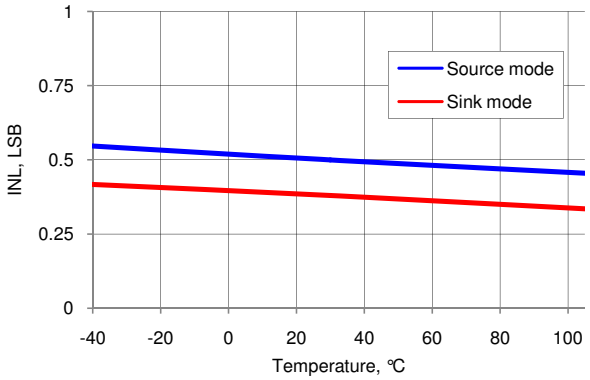
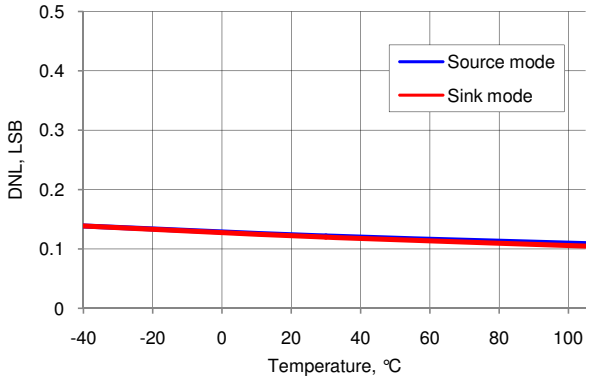


Figure 11-52. IDAC DNL vs Temperature, Range = 255 µA, Fast Mode



11.8.3 Interrupt Controller

Table 11-75. Interrupt Controller AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Delay from interrupt signal input to ISR code execution from main line code[92]		–	–	12	Tcy CPU
	Delay from interrupt signal input to ISR code execution from ISR code (tail-chaining)[92]		–	–	6	Tcy CPU

11.8.4 JTAG Interface

Figure 11-79. JTAG Interface Timing

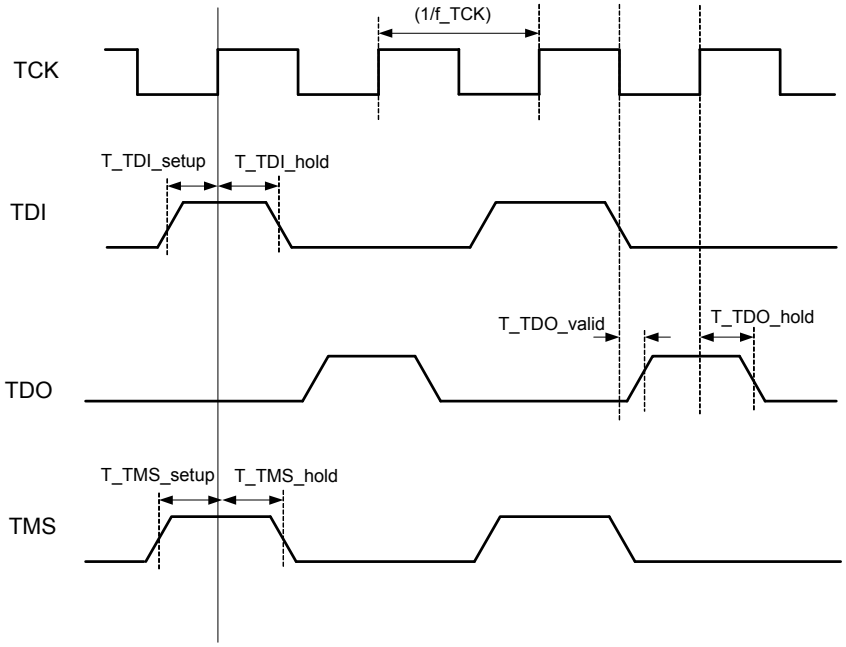


Table 11-76. JTAG Interface AC Specifications[93]

Parameter	Description	Conditions	Min	Typ	Max	Units
f_TCK	TCK frequency	3.3 V ≤ V_{DDD} ≤ 5 V	–	–	12[94]	MHz
		1.71 V ≤ V_{DDD} < 3.3 V	–	–	7[94]	MHz
T_TDI_setup	TDI setup before TCK high		(T/10) – 5	–	–	ns
T_TMS_setup	TMS setup before TCK high		T/4	–	–	
T_TDI_hold	TDI, TMS hold after TCK high	T = 1/f_TCK max	T/4	–	–	
T_TDO_valid	TCK low to TDO valid	T = 1/f_TCK max	–	–	2T/5	
T_TDO_hold	TDO hold after TCK high	T = 1/f_TCK max	T/4	–	–	
T_nTRST	Minimum nTRST pulse width	f_TCK = 2 MHz	8	–	–	ns

Notes
92. ARM Cortex-M3 NVIC spec. Visit www.arm.com for detailed documentation about the Cortex-M3 CPU.
93. Based on device characterization (Not production tested).
94. f_TCK must also be no more than 1/3 CPU clock frequency.

12. Ordering Information

In addition to the features listed in Table 12-1, every CY8C58LP device includes: up to 256 KB flash, 64 KB SRAM, 2 KB EEPROM, a precision on-chip voltage reference, precision oscillators, flash, ECC, DMA, a fixed function I^2C, JTAG/SWD programming and debug, external memory interface, boost, and more. In addition to these features, the flexible UDBs and analog subsection support a wide range of peripherals. To assist you in selecting the ideal part, PSoC Creator makes a part recommendation after you choose the components required by your application. All CY8C58LP derivatives incorporate device and flash security in user-selectable security levels; see the TRM for details.

Table 12-1. CY8C58LP Family with ARM Cortex-M3 CPU

Part Number	MCU Core				Analog								Digital				I/O[109]				Package	JTAG ID[110]
	CPU SPEED (MHZ)	FLASH (KB)	SRAM (KB)	EEPROM (KB)	LCD SEGMENT DRIVE	ADCS	DAC	COMPARATORS	SC/CT ANALOG BLOCKS[107]	OPAMPS	DFB	CAPSENSE	UDBS[108]	16-BIT TIMER/PWM	FS USB	CAN 2.0B	TOTAL I/O	GPIO	SIO	USBIO		
CY8C5868AXI-LP031	67	256	64	2	✔	1x20-bit Del-Sig 2x12-bit SAR	4	4	4	4	✔	✔	24	4	–	–	70	62	8	0	100-TQFP	0x2E11F069
CY8C5868AXI-LP032	67	256	64	2	✔	1x20-bit Del-Sig 2x12-bit SAR	4	4	4	4	✔	✔	24	4	✔	–	72	62	8	2	100-TQFP	0x2E120069
CY8C5868AXI-LP035	67	256	64	2	✔	1x20-bit Del-Sig 2x12-bit SAR	4	4	4	4	✔	✔	24	4	✔	✔	72	62	8	2	100-TQFP	0x2E123069
CY8C5868LTI-LP036	67	256	64	2	✔	1x20-bit Del-Sig 2x12-bit SAR	4	4	4	4	✔	✔	24	4	–	–	46	38	8	0	68-QFN	0x2E124069
CY8C5868LTI-LP038	67	256	64	2	✔	1x20-bit Del-Sig 2x12-bit SAR	4	4	4	4	✔	✔	24	4	✔	–	48	38	8	2	68-QFN	0x2E126069
CY8C5868LTI-LP039	67	256	64	2	✔	1x20-bit Del-Sig 2x12-bit SAR	4	4	4	4	✔	✔	24	4	✔	✔	48	38	8	2	68-QFN	0x2E127069
CY8C5867AXI-LP023	67	128	32	2	✔	1x20-bit Del-Sig 1x12-bit SAR	4	4	4	4	✔	✔	24	4	–	–	70	62	8	0	100-TQFP	0x2E117069
CY8C5867AXI-LP024	67	128	32	2	✔	1x20-bit Del-Sig 1x12-bit SAR	4	4	4	4	✔	✔	24	4	✔	–	72	62	8	2	100-TQFP	0x2E118069
CY8C5867LTI-LP025	67	128	32	2	✔	1x20-bit Del-Sig 1x12-bit SAR	4	4	4	4	✔	✔	24	4	–	–	46	38	8	0	68-QFN	0x2E119069
CY8C5867LTI-LP028	67	128	32	2	✔	1x20-bit Del-Sig 1x12-bit SAR	4	4	4	4	✔	✔	24	4	✔	–	48	38	8	2	68-QFN	0x2E11C069
CY8C5866AXI-LP020	67	64	16	2	✔	1x20-bit Del-Sig 1x12-bit SAR	4	4	4	4	✔	✔	20	4	✔	✔	72	62	8	2	100-TQFP	0x2E114069
CY8C5866AXI-LP021	67	64	16	2	✔	1x20-bit Del-Sig 1x12-bit SAR	4	4	4	4	✔	✔	20	4	✔	–	72	62	8	2	100-TQFP	0x2E115069
CY8C5866LTI-LP022	67	64	16	2	✔	1x20-bit Del-Sig 1x12-bit SAR	4	4	4	4	✔	✔	20	4	✔	–	48	38	8	2	68-QFN	0x2E116069
CY8C5888AXI-LP096	80	256	64	2	✔	1x20-bit Del-Sig 2x12-bit SAR	4	4	4	4	✔	✔	24	4	✔	✔	72	62	8	2	100-TQFP	0x2E160069
CY8C5888AXQ-LP096	80	256	64	2	✔	1x20-bit Del-Sig 2x12-bit SAR	4	4	4	4	✔	✔	24	4	✔	✔	72	62	8	2	100-TQFP	0x2E160069
CY8C5888LTI-LP097	80	256	64	2	✔	1x20-bit Del-Sig 2x12-bit SAR	4	4	4	4	✔	✔	24	4	✔	✔	48	38	8	2	68-QFN	0x2E161069
CY8C5888LTQ-LP097	80	256	64	2	✔	1x20-bit Del-Sig 2x12-bit SAR	4	4	4	4	✔	✔	24	4	✔	✔	48	38	8	2	68-QFN	0x2E161069
CY8C5888FNI-LP210	80	256	64	2	✔	1x20-bit Del-Sig 2x12-bit SAR	4	4	4	4	✔	✔	24	4	✔	✔	72	62	8	2	99-WLCSP	0x2E1D2069
CY8C5888FNI-LP214	80	256	64	2	✔	1x20-bit Del-Sig 2x12-bit SAR	4	4	4	4	✔	✔	24	4	✔	–	72	62	8	2	99-WLCSP	0x2E1D6069

Notes

107. Analog blocks support a wide variety of functionality including TIA, PGA, and mixers. See Example Peripherals on page 40 for more information on how analog blocks can be used.
108. UDBs support a wide variety of functionality including SPI, LIN, UART, timer, counter, PWM, PRS, and others. Individual functions may use a fraction of a UDB or multiple UDBs. Multiple functions can share a single UDB. See Example Peripherals on page 40 for more information on how UDBs can be used.
109. The I/O Count includes all types of digital I/O: GPIO, SIO, and the two USB I/O. See "I/O System and Routing" section on page 33 for details on the functionality of each of these types of I/O.
110. The JTAG ID has three major fields. The most significant nibble (left digit) is the version, followed by a 2 byte part number and a 3 nibble manufacturer ID.

Document History Page (continued)

Description Title: PSoC® 5LP: CY8C58LP Family Datasheet Programmable System-on-Chip (PSoC®) Document Number: 001-84932				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
*H (cont.)	4698847	AVER / MKEA / GJV	03/24/2015	Updated Electrical Specifications: Updated Memory: Updated Flash: Updated Table 11-62: Updated details in “Conditions” column corresponding to “Flash data retention time” parameter. Added Note 81 and referred the same note in last condition corresponding to “Flash data retention time” parameter. Updated EEPROM: Updated Table 11-64: Updated details in “Conditions” column corresponding to “EEPROM data retention time” parameter. Added Note 81 and referred the same note in last condition corresponding to “EEPROM data retention time” parameter. Updated Nonvolatile Latches (NVL): Updated Table 11-66: Updated details in “Conditions” column corresponding to “NVL data retention time” parameter. Added Note 82 and referred the same note in last condition corresponding to “NVL data retention time” parameter. Updated Clocking: Updated Internal Main Oscillator: Updated Table 11-80: Replaced 85 °C with 105 °C. Updated Figure 11-83. Updated Ordering Information: Updated Table 12-1: Updated part numbers. Updated Part Numbering Conventions: Added “Q: Extended” as sub bullet under “g: Temperature Range”. Updated Packaging: Updated Table 13-1: Changed maximum value of T_A parameter from 85 °C to 105 °C. Changed maximum value of T_J parameter from 100 °C to 120 °C. Updated : Updated : spec 001-88034 – Changed revision from ** to *A.
*I	4839323	MKEA	07/15/2015	Added reference to code examples in More Information. Updated typ value of T_{WRITE} from 2 to 10 in EEPROM AC specs table. Changed “Device supply for USB operation" to "Device supply (V_{DDD}) for USB operation" in USB DC Specifications. Clarified power supply sequencing and margin for V_{DDA} and V_{DDD}. Updated Serial Wire Debug Interface with limitations of debugging on Port 15. Updated Delta-sigma ADC DC Specifications