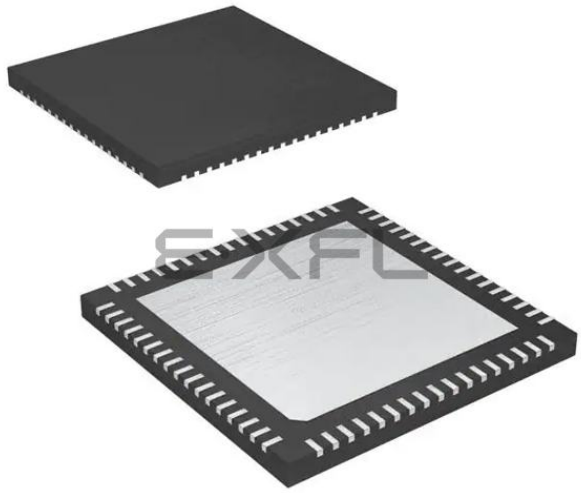


**Welcome to E-XFL.COM**

## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | ARM® Cortex®-M3 |
| Core Size | 32-Bit Single-Core |
| Speed | 80MHz |
| Connectivity | CANbus, I²C, LINbus, SPI, UART/USART, USB |
| Peripherals | CapSense, DMA, LCD, POR, PWM, WDT |
| Number of I/O | 38 |
| Program Memory Size | 256KB (256K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | 2K x 8 |
| RAM Size | 64K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.71V ~ 5.5V |
| Data Converters | A/D 1x20b, 2x12b; D/A 4x8b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 68-VFQFN Exposed Pad |
| Supplier Device Package | 68-QFN (8x8) |
| Purchase URL | https://www.e-xfl.com/product-detail/infineon-technologies/cy8c5888lti-lp097 |

In addition to the flexibility of the UDB array, PSoC also provides configurable digital blocks targeted at specific functions. For the CY8C58LP family, these blocks can include four 16-bit timers, counters, and PWM blocks; $I^2C$ slave, master, and multimaster; Full-Speed USB; and Full CAN 2.0.

For more details on the peripherals see the Example Peripherals on page 40 of this datasheet. For information on UDBs, DSI, and other digital blocks, see the Digital Subsystem on page 40 of this datasheet.

PSoC's analog subsystem is the second half of its unique configurability. All analog performance is based on a highly accurate absolute voltage reference with less than 0.1% error over temperature and voltage. The configurable analog subsystem includes:

- Analog muxes
- Comparators
- Analog mixers
- Voltage references
- ADCs
- DACs
- Digital filter block (DFB)

All GPIO pins can route analog signals into and out of the device using the internal analog bus. This allows the device to interface up to 62 discrete analog signals. One of the ADCs in the analog subsystem is a fast, accurate, configurable delta-sigma ADC with these features:

- Less than 100-µV offset
- A gain error of 0.2%
- Integral non linearity (INL) less than ±2 LSB
- Differential non linearity (DNL) less than ±1 LSB
- SINAD better than 84 dB in 16-bit mode

This converter addresses a wide variety of precision analog applications including some of the most demanding sensors.

The CY8C58LP family also offers up to two SAR ADCs. Featuring 12-bit conversions at up to 1 M samples per second, they also offer low nonlinearity and offset errors and SNR better than 70 dB. They are well-suited for a variety of higher speed analog applications.

The output of any of the ADCs can optionally feed the programmable DFB via DMA without CPU intervention. You can configure the DFB to perform IIR and FIR digital filters and several user defined custom functions. The DFB can implement filters with up to 64 taps. It can perform a 48-bit multiply-accumulate (MAC) operation in one clock cycle.

Four high-speed voltage or current DACs support 8-bit output signals at an update rate of up to 8 Msps. They can be routed out of any GPIO pin. You can create higher resolution voltage PWM DAC outputs using the UDB array. This can be used to create a pulse width modulated (PWM) DAC of up to 10 bits, at up to 48 kHz. The digital DACs in each UDB support PWM, PRS, or delta-sigma algorithms with programmable widths.

In addition to the ADCs, DACs, and DFB, the analog subsystem provides multiple:

- Comparators
- Uncommitted opamps
- Configurable switched capacitor/continuous time (SC/CT) blocks. These support:
  - Transimpedance amplifiers
  - Programmable gain amplifiers
  - Mixers
  - Other similar analog components

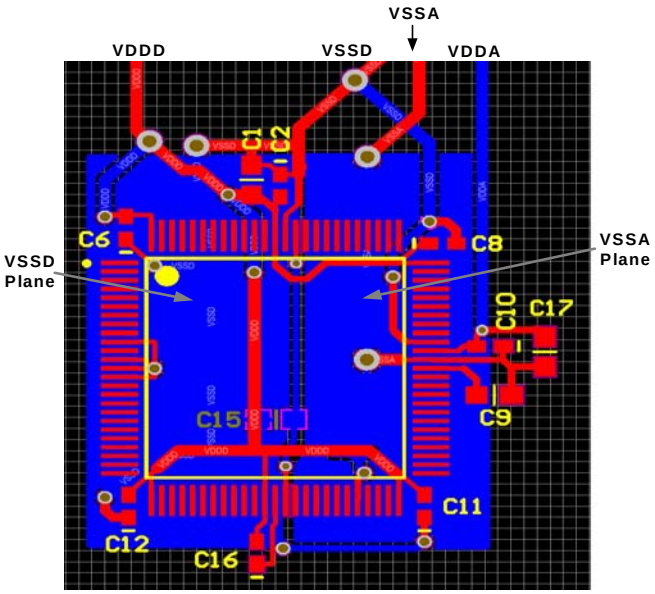
See the "Analog Subsystem" section on page 51 of this datasheet for more details.

PSoC's CPU subsystem is built around a 32-bit three-stage pipelined ARM Cortex-M3 processor running at up to 80 MHz. The Cortex-M3 includes a tightly integrated nested vectored interrupt controller (NVIC) and various debug and trace modules. The overall CPU subsystem includes a DMA controller, flash cache, and RAM. The NVIC provides low latency, nested interrupts, and tail-chaining of interrupts and other features to increase the efficiency of interrupt handling. The DMA controller enables peripherals to exchange data without CPU involvement. This allows the CPU to run slower (saving power) or use those CPU cycles to improve the performance of firmware algorithms. The flash cache also reduces system power consumption by allowing less frequent flash access.

PSoC's nonvolatile subsystem consists of flash, byte-writeable EEPROM, and nonvolatile configuration options. It provides up to 256 KB of on-chip flash. The CPU can reprogram individual blocks of flash, enabling boot loaders. You can enable an ECC for high reliability applications. A powerful and flexible protection model secures the user's sensitive information, allowing selective memory block locking for read and write protection. Two KB of byte-writable EEPROM is available on-chip to store application data. Additionally, selected configuration options such as boot speed and pin drive mode are stored in nonvolatile memory. This allows settings to activate immediately after POR.

The three types of PSoC I/O are extremely flexible. All I/Os have many drive modes that are set at POR. PSoC also provides up to four I/O voltage domains through the $V_{DDIO}$ pins. Every GPIO has analog I/O, LCD drive, CapSense, flexible interrupt generation, slew rate control, and digital I/O capability. The SIOs on PSoC allow $V_{OH}$ to be set independently of $V_{DDIO}$ when used as outputs. When SIOs are in input mode they are high impedance. This is true even when the device is not powered or when the pin voltage goes above the supply voltage. This makes the SIO ideally suited for use on an $I^2C$ bus where the PSoC may not be powered when other devices on the bus are. The SIO pins also have high current sink capability for applications such as LED drives. The programmable input threshold feature of the SIO can be used to make the SIO function as a general purpose analog comparator. For devices with FS USB, the USB physical interface is also provided (USBIO). When not using USB, these pins may also be used for limited digital functionality and device programming. All the features of the PSoC I/Os are covered in detail in the I/O System and Routing on page 33 of this datasheet.

**Figure 2-6. Example PCB Layout for 100-pin TQFP Part for Optimal Analog Performance**



# 5. Memory

## 5.1 Static RAM

CY8C58LP static RAM (SRAM) is used for temporary data storage. Code can be executed at full speed from the portion of SRAM that is located in the code space. This process is slower from SRAM above 0x20000000. The device provides up to 64 KB of SRAM. The CPU or the DMA controller can access all of SRAM. The SRAM can be accessed simultaneously by the Cortex-M3 CPU and the DMA controller if accessing different 32-KB blocks.

## 5.2 Flash Program Memory

Flash memory in PSoC devices provides nonvolatile storage for user firmware, user configuration data, bulk data storage, and optional ECC data. The main flash memory area contains up to 256 KB of user program space.

Up to an additional 32 KB of flash space is available for Error Correcting Codes (ECC). If ECC is not used this space can store device configuration data and bulk user data. User code may not be run out of the ECC flash memory section. ECC can correct one bit error and detect two bit errors per 8 bytes of firmware memory; an interrupt can be generated when an error is detected. The flash output is 9 bytes wide with 8 bytes of data and 1 byte of ECC data.

The CPU or DMA controller read both user code and bulk data located in flash through the cache controller. This provides higher CPU performance. If ECC is enabled, the cache controller also performs error checking and correction.

Flash programming is performed through a special interface and preempts code execution out of flash. Code execution may be done out of SRAM during flash programming.

The flash 24programming interface performs flash erasing, programming and setting code protection levels. Flash in-system serial programming (ISSP), typically used for production programming, is possible through both the SWD and JTAG interfaces. In-system programming, typically used for bootloaders, is also possible using serial interfaces such as $I^2C$, USB, UART, and SPI, or any communications protocol.

## 5.3 Flash Security

All PSoC devices include a flexible flash protection model that prevents access and visibility to on-chip flash memory. This prevents duplication or reverse engineering of proprietary code. Flash memory is organized in blocks, where each block contains 256 bytes of program or data and 32 bytes of ECC or configuration data.

The device offers the ability to assign one of four protection levels to each row of flash. Table 5-1 lists the protection modes available. Flash protection levels can only be changed by performing a complete flash erase. The Full Protection and Field Upgrade settings disable external access (through a debugging tool such as PSoC Creator, for example). If your application requires code update through a boot loader, then use the Field Upgrade setting. Use the Unprotected setting only when no security is needed in your application. The PSoC device also offers an advanced security feature called Device Security which permanently disables all test, programming, and debug ports, protecting your application from external access (see the "Device Security" section on page 64). For more information on how to take full advantage of the security features in PSoC, see the PSoC 5 TRM.

**Table 5-1. Flash Protection**

| Protection Setting | Allowed | Not Allowed |
|---|---|---|
| Unprotected | External read and write + internal read and write | – |
| Factory Upgrade | External write + internal read and write | External read |
| Field Upgrade | Internal read and write | External read and write |
| Full Protection | Internal read | External read and write + internal write |

**Disclaimer**

Note the following details of the flash code protection features on Cypress devices.

Cypress products meet the specifications contained in their particular Cypress datasheets. Cypress believes that its family of products is one of the most secure families of its kind on the market today, regardless of how they are used. There may be methods, unknown to Cypress, that can breach the code protection features. Any of these methods, to our knowledge, would be dishonest and possibly illegal. Neither Cypress nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Cypress is willing to work with the customer who is concerned about the integrity of their code. Code protection is constantly evolving. We at Cypress are committed to continuously improving the code protection features of our products.

## 5.4 EEPROM

PSoC EEPROM memory is a byte addressable nonvolatile memory. The CY8C58LP has 2 KB of EEPROM memory to store user data. Reads from EEPROM are random access at the byte level. Reads are done directly; writes are done by sending write commands to an EEPROM programming interface. CPU code execution can continue from flash during EEPROM writes. EEPROM is erasable and writeable at the row level. The EEPROM is divided into 128 rows of 16 bytes each. The factory default values of all EEPROM bytes are 0.

Because the EEPROM is mapped to the Cortex-M3 Peripheral region, the CPU cannot execute out of EEPROM. There is no ECC hardware associated with EEPROM. If ECC is required it must be handled in firmware.

It can take as much as 20 milliseconds to write to EEPROM or flash. During this time the device should not be reset, or unexpected changes may be made to portions of EEPROM or flash. Reset sources (see Reset Sources on page 32) include XRES pin, software reset, and watchdog; care should be taken to make sure that these are not inadvertently activated. In addition, the low voltage detect circuits should be configured to generate an interrupt instead of a reset.

**Figure 6-1. Clocking Subsystem**

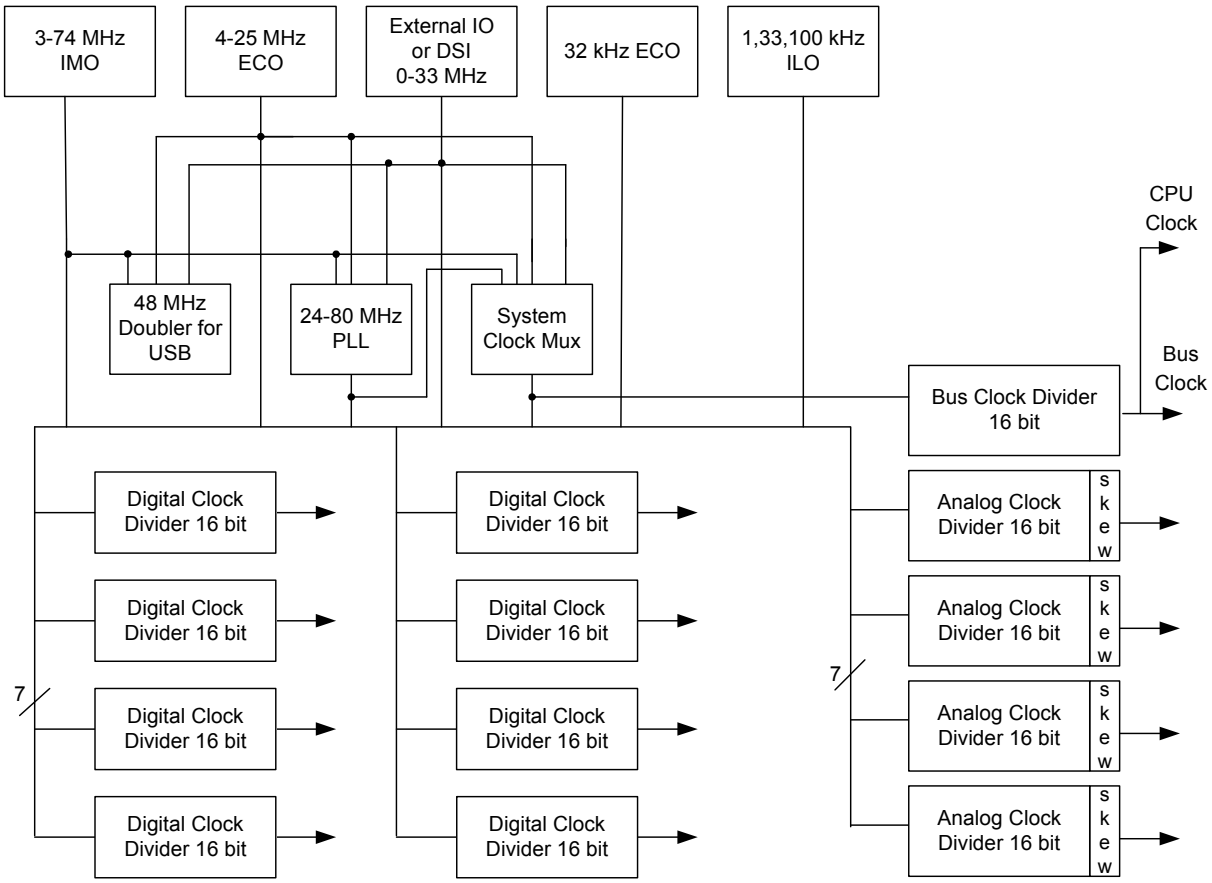
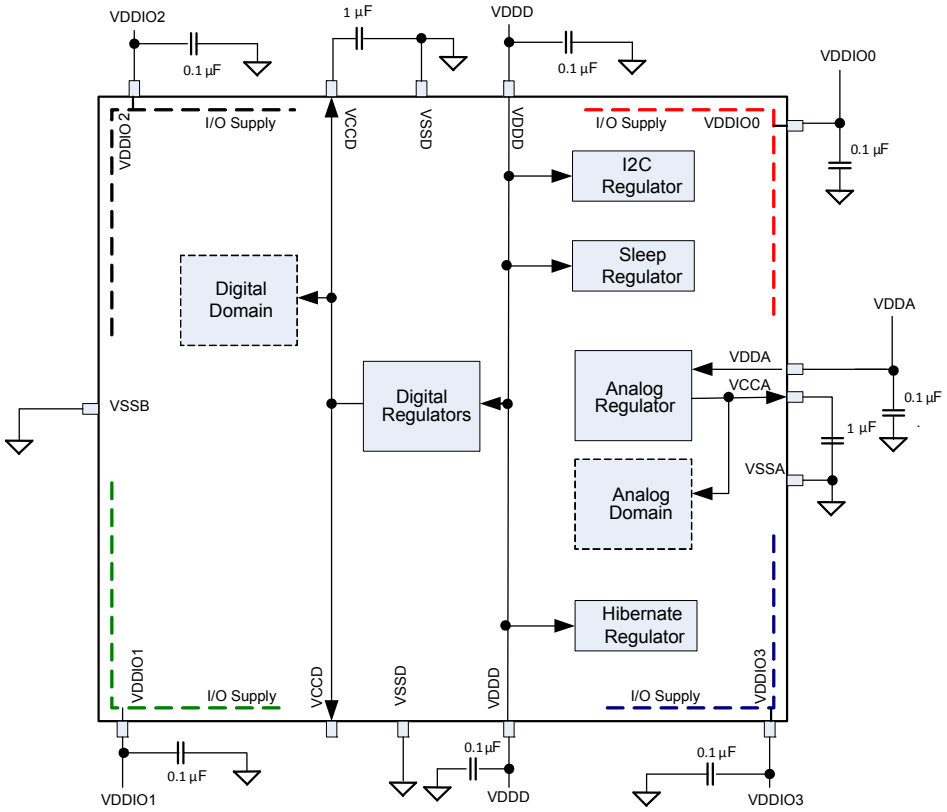


**Figure 6-4. PSoC Power System**




**Notes**

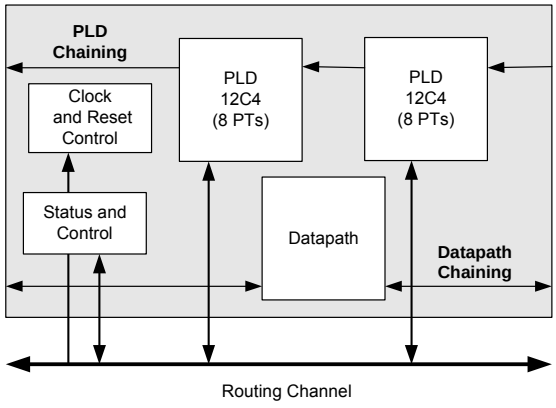
- The two $V_{CCD}$ pins must be connected together with as short a trace as possible. A trace under the device is recommended, as shown in Figure 2-6.
- You can power the device in internally regulated mode, where the voltage applied to the $V_{DDx}$ pins is as high as 5.5 V, and the internal regulators provide the core voltages. **In this mode, do not apply power to the $V_{CCx}$ pins, and do not tie the $V_{DDx}$ pins to the $V_{CCx}$ pins.**
- You can also power the device in externally regulated mode, that is, by directly powering the $V_{CCD}$ and $V_{CCA}$ pins. In this configuration, the $V_{DDD}$ pins should be shorted to the $V_{CCD}$ pins and the $V_{DDA}$ pin should be shorted to the $V_{CCA}$ pin. The allowed supply range in this configuration is 1.71 V to 1.89 V. After power up in this configuration, the internal regulators are on by default, and should be disabled to reduce power consumption.
- It is good practice to check the datasheets for your bypass capacitors, specifically the working voltage and the DC bias specifications. With some capacitors, the actual capacitance can decrease considerably when the DC bias ($V_{DDX}$ or $V_{CCX}$ in Figure 6-4) is a significant percentage of the rated working voltage.

## 7.2 Universal Digital Block

The Universal Digital Block (UDB) represents an evolutionary step to the next generation of PSoC embedded digital peripheral functionality. The architecture in first generation PSoC digital blocks provides coarse programmability in which a few fixed functions with a small number of options are available. The new UDB architecture is the optimal balance between configuration granularity and efficient implementation. A cornerstone of this approach is to provide the ability to customize the devices digital operation to match application requirements.

To achieve this, UDBs consist of a combination of uncommitted logic (PLD), structured logic (Datapath), and a flexible routing scheme to provide interconnect between these elements, I/O connections, and other peripherals. UDB functionality ranges from simple self contained functions that are implemented in one UDB, or even a portion of a UDB (unused resources are available for other functions), to more complex functions that require multiple UDBs. Examples of basic functions are timers, counters, CRC generators, PWMs, dead band generators, and communications functions, such as UARTs, SPI, and $I^2C$. Also, the PLD blocks and connectivity provide full featured general purpose programmable logic within the limits of the available resources.

**Figure 7-2. UDB Block Diagram**



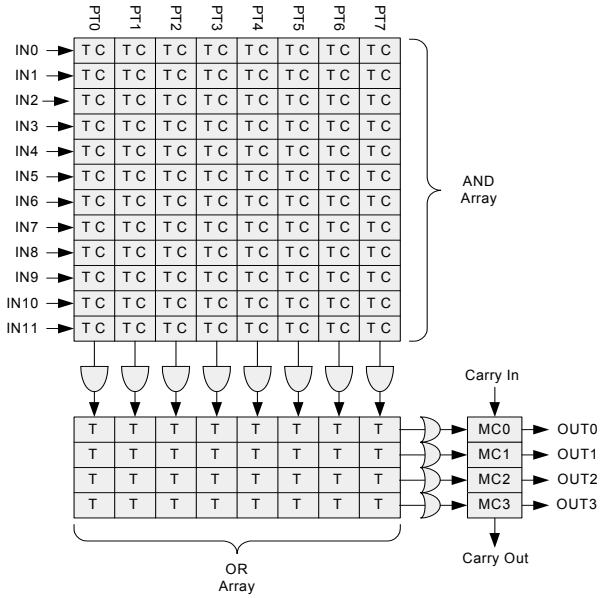

The main component blocks of the UDB are:

- PLD blocks - There are two small PLDs per UDB. These blocks take inputs from the routing array and form registered or combinational sum-of-products logic. PLDs are used to implement state machines, state bits, and combinational logic equations. PLD configuration is automatically generated from graphical primitives.
- Datapath Module - This 8-bit wide datapath contains structured logic to implement a dynamically configurable ALU, a variety of compare configurations and condition generation. This block also contains input/output FIFOs, which are the primary parallel data interface between the CPU/DMA system and the UDB.
- Status and Control Module - The primary role of this block is to provide a way for CPU firmware to interact and synchronize with UDB operation.
- Clock and Reset Module - This block provides the UDB clocks and reset selection and control.

### *7.2.1 PLD Module*

The primary purpose of the PLD blocks is to implement logic expressions, state machines, sequencers, look up tables, and decoders. In the simplest use model, consider the PLD blocks as a standalone resource onto which general purpose RTL is synthesized and mapped. The more common and efficient use model is to create digital functions from a combination of PLD and datapath blocks, where the PLD implements only the random logic and state portion of the function while the datapath (ALU) implements the more structured elements.

**Figure 7-3. PLD 12C4 Structure**




One 12C4 PLD block is shown in Figure 7-3. This PLD has 12 inputs, which feed across eight product terms. Each product term (AND function) can be from 1 to 12 inputs wide, and in a given product term, the true (T) or complement (C) of each input can be selected. The product terms are summed (OR function) to create the PLD outputs. A sum can be from 1 to 8 product terms wide. The 'C' in 12C4 indicates that the width of the OR gate (in this case 8) is constant across all outputs (rather than variable as in a 22V10 device). This PLA like structure gives maximum flexibility and insures that all inputs and outputs are permutable for ease of allocation by the software tools. There are two 12C4 PLDs in each UDB.

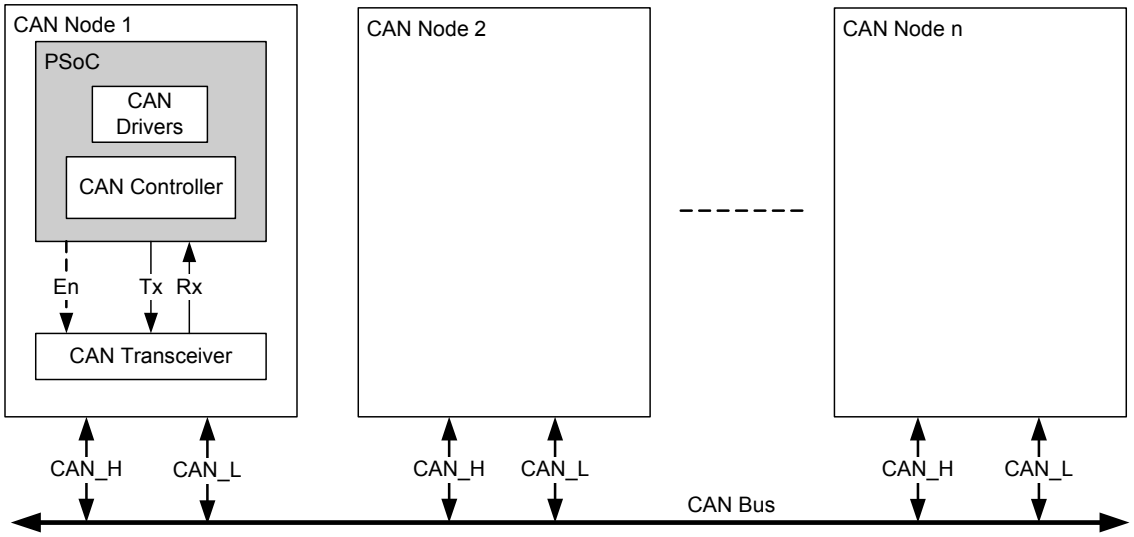
### *7.2.2 Datapath Module*

The datapath contains an 8-bit single cycle ALU, with associated compare and condition generation logic. This datapath block is optimized to implement embedded functions, such as timers, counters, integrators, PWMs, PRS, CRC, shifters and dead band generators, and many others.

## 7.5 CAN

The CAN peripheral is a fully functional Controller Area Network (CAN) supporting communication baud rates up to 1 Mbps. The CAN controller implements the CAN2.0A and CAN2.0B specifications as defined in the Bosch specification and conforms to the ISO-11898-1 standard. The CAN protocol was originally designed for automotive applications with a focus on a high level of fault detection. This ensures high communication reliability at a low cost. Because of its success in automotive applications, CAN is used as a standard communication protocol for motion oriented machine control networks (CANOpen) and factory automation applications (DeviceNet). The CAN controller features allow the efficient implementation of higher level protocols without affecting the performance of the microcontroller CPU. Full configuration support is provided in PSoC Creator.

**Figure 7-14. CAN Bus System Implementation**




### *7.5.1 CAN Features*

- CAN2.0A/B protocol implementation - ISO 11898 compliant
  - Standard and extended frames with up to 8 bytes of data per frame
  - Message filter capabilities
  - Remote Transmission Request (RTR) support
  - Programmable bit rate up to 1 Mbps
- Listen Only mode
- SW readable error counter and indicator
- Sleep mode: Wake the device from sleep with activity on the Rx pin
- Supports two or three wire interface to external transceiver (Tx, Rx, and Enable). The three-wire interface is compatible with the Philips PHY; the PHY is not included on-chip. The three wires can be routed to any I/O
- Enhanced interrupt controller
  - CAN receive and transmit buffers status
  - CAN controller error status including BusOff
- Receive path
  - 16 receive buffers each with its own message filter
  - Enhanced hardware message filter implementation that covers the ID, IDE and RTR
  - DeviceNet addressing support
  - Multiple receive buffers linkable to build a larger receive message array
  - Automatic transmission request (RTR) response handler
  - Lost received message notification
- Transmit path
  - Eight transmit buffers
  - Programmable transmit priority
  - Round robin
  - Fixed priority
  - Message transmissions abort capability

### *7.5.2 Software Tools Support*

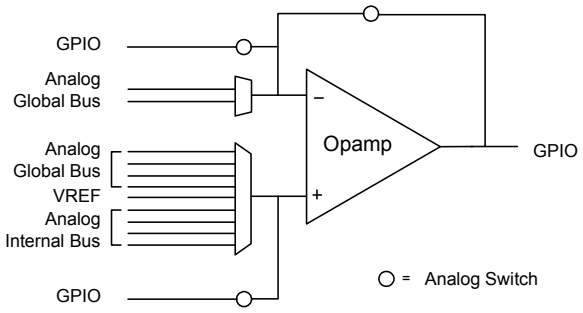
CAN Controller configuration integrated into PSoC Creator:

- CAN Configuration walkthrough with bit timing analyzer
- Receive filter setup

## 8.5 Opamps

The CY8C58LP family of devices contain four general purpose opamps.

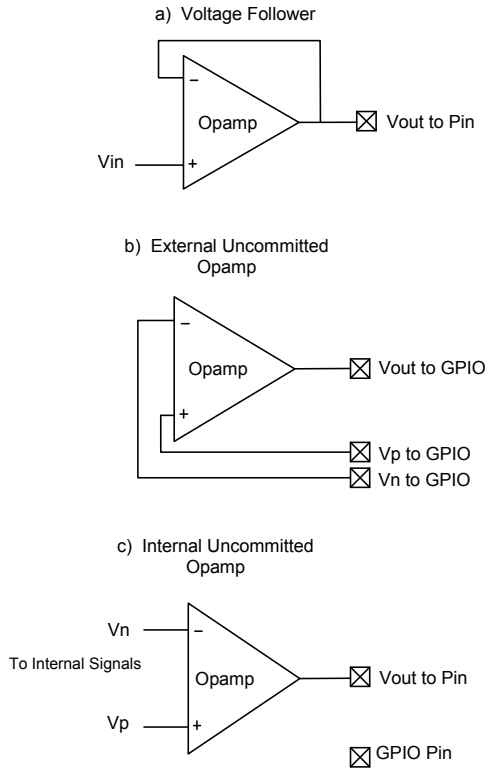
**Figure 8-7. Opamp**




The opamp is uncommitted and can be configured as a gain stage or voltage follower on external or internal signals.

See Figure 8-8. In any configuration, the input and output signals can all be connected to the internal global signals and monitored with an ADC, or comparator. The configurations are implemented with switches between the signals and GPIO pins.

**Figure 8-8. Opamp Configurations**




The opamp has three speed modes, slow, medium, and fast. The slow mode consumes the least amount of quiescent power and the fast mode consumes the most power. The inputs are able to swing rail-to-rail. The output swing is capable of rail-to-rail operation at low current output, within 50 mV of the rails. When driving high current loads (about 25 mA) the output voltage may only get within 500 mV of the rails.

## 8.6 Programmable SC/CT Blocks

The CY8C58LP family of devices contains four switched capacitor/continuous time (SC/CT) blocks. Each switched capacitor/continuous time block is built around a single rail-to-rail high bandwidth opamp.

Switched capacitor is a circuit design technique that uses capacitors plus switches instead of resistors to create analog functions. These circuits work by moving charge between capacitors by opening and closing different switches. Nonoverlapping in phase clock signals control the switches, so that not all switches are ON simultaneously.

The PSoC Creator tool offers a user friendly interface, which allows you to easily program the SC/CT blocks. Switch control and clock phase control configuration is done by PSoC Creator so users only need to determine the application use parameters such as gain, amplifier polarity, $V_{REF}$ connection, and so on.

The same opamps and block interfaces are also connectable to an array of resistors which allows the construction of a variety of continuous time functions.

The opamp and resistor array is programmable to perform various analog functions including

- Naked Operational Amplifier - Continuous Mode
- Unity-Gain Buffer - Continuous Mode
- Programmable Gain Amplifier (PGA) - Continuous Mode
- Transimpedance Amplifier (TIA) - Continuous Mode
- Up/Down Mixer - Continuous Mode
- Sample and Hold Mixer (NRZ S/H) - Switched Cap Mode
- First Order Analog to Digital Modulator - Switched Cap Mode

### *8.6.1 Naked Opamp*

The Naked Opamp presents both inputs and the output for connection to internal or external signals. The opamp has a unity gain bandwidth greater than 6.0 MHz and output drive current up to 650 µA. This is sufficient for buffering internal signals (such as DAC outputs) and driving external loads greater than 7.5 kohms.

### *8.6.2 Unity Gain*

The Unity Gain buffer is a Naked Opamp with the output directly connected to the inverting input for a gain of 1.00. It has a -3 dB bandwidth greater than 6.0 MHz.

### *8.6.3 PGA*

The PGA amplifies an external or internal signal. The PGA can be configured to operate in inverting mode or noninverting mode. The PGA function may be configured for both positive and negative gains as high as 50 and 49 respectively. The gain is adjusted by changing the values of R1 and R2 as illustrated in Figure 8-9. The schematic in Figure 8-9 shows the configuration and possible resistor settings for the PGA. The gain is switched from inverting and non inverting by changing the shared select value of the both the input muxes. The bandwidth for each gain case is listed in Table 8-3.

### 11.4.3 USBIO

For operation in GPIO mode, the standard range for $V_{DDD}$ applies, see Device Level Specifications on page 68.

**Table 11-13. USBIO DC Specifications**

| Parameter | Description | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| Rusbi | USB D+ pull-up resistance[40] | With idle bus | 0.900 | – | 1.575 | kΩ |
| Rusba | USB D+ pull-up resistance[40] | While receiving traffic | 1.425 | – | 3.090 | kΩ |
| Vohusb | Static output high[40] | 15 kΩ ±5% to Vss, internal pull-up enabled | 2.8 | – | 3.6 | V |
| Volusb | Static output low[40] | 15 kΩ ±5% to Vss, internal pull-up enabled | – | – | 0.3 | V |
| Vihgpio | Input voltage high, GPIO mode[40] | $V_{DDD}$ = 1.8 V | 1.5 | – | – | V |
| | | $V_{DDD}$ = 3.3 V | 2 | – | – | V |
| | | $V_{DDD}$ = 5.0 V | 2 | – | – | V |
| Vilgpio | Input voltage low, GPIO mode[40] | $V_{DDD}$ = 1.8 V | – | – | 0.8 | V |
| | | $V_{DDD}$ = 3.3 V | – | – | 0.8 | V |
| | | $V_{DDD}$ = 5.0 V | – | – | 0.8 | V |
| Vohgpio | Output voltage high, GPIO mode[40] | $I_{OH}$ = 4 mA, $V_{DDD}$ = 1.8 V | 1.6 | – | – | V |
| | | $I_{OH}$ = 4 mA, $V_{DDD}$ = 3.3 V | 3.1 | – | – | V |
| | | $I_{OH}$ = 4 mA, $V_{DDD}$ = 5.0 V | 4.2 | – | – | V |
| Volgpio | Output voltage low, GPIO mode[40] | $I_{OL}$ = 4 mA, $V_{DDD}$ = 1.8 V | – | – | 0.3 | V |
| | | $I_{OL}$ = 4 mA, $V_{DDD}$ = 3.3 V | – | – | 0.3 | V |
| | | $I_{OL}$ = 4 mA, $V_{DDD}$ = 5.0 V | – | – | 0.3 | V |
| Vdi | Differential input sensitivity | \|(D+)–(D–)\| | – | – | 0.2 | V |
| Vcm | Differential input common mode range | | 0.8 | – | 2.5 | V |
| Vse | Single ended receiver threshold | | 0.8 | – | 2 | V |
| Rps2 | PS/2 pull-up resistance[40] | In PS/2 mode, with PS/2 pull-up enabled | 3 | – | 7 | kΩ |
| Rext | External USB series resistor[40] | In series with each USB pin | 21.78 (–1%) | 22 | 22.22 (+1%) | Ω |
| Zo | USB driver output impedance[40] | Including Rext | 28 | – | 44 | Ω |
| $C_{IN}$ | USB transceiver input capacitance | | – | – | 20 | pF |
| $I_{IL}$[40] | Input leakage current (absolute value)[40] | 25 °C, $V_{DDD}$ = 3.0 V | – | – | 2 | nA |

**Note**
40. Based on device characterization (Not production tested).

**Figure 11-24. USBIO Output Low Voltage and Current, GPIO Mode**

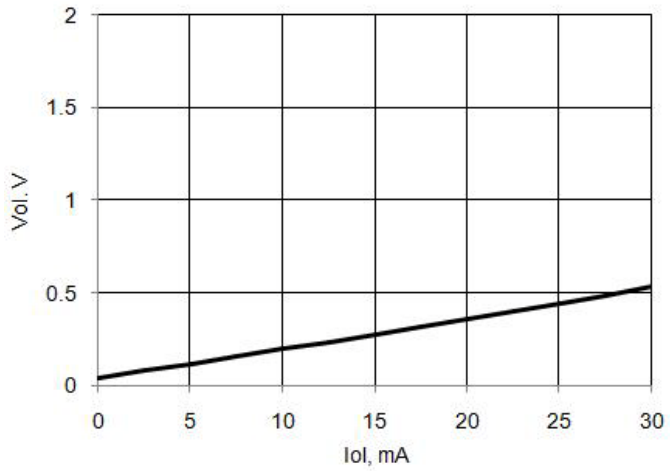



**Table 11-15. USB Driver AC Specifications**[42]

| Parameter | Description | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| Tr | Transition rise time | | – | – | 20 | ns |
| Tf | Transition fall time | | – | – | 20 | ns |
| TR | Rise/fall time matching | $V_{USB\_5}$, $V_{USB\_3.3}$, see USB DC Specifications on page 114 | 90% | – | 111% | |
| Vcrs | Output signal crossover voltage | | 1.3 | – | 2 | V |

*11.4.4 XRES*

**Table 11-16. XRES DC Specifications**

| Parameter | Description | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $V_{IH}$ | Input voltage high threshold | | $0.7 \times V_{DDIO}$ | – | – | V |
| $V_{IL}$ | Input voltage low threshold | | – | – | $0.3 \times V_{DDIO}$ | V |
| Rpullup | Pull-up resistor | | 3.5 | 5.6 | 8.5 | kΩ |
| $C_{IN}$ | Input capacitance[42] | | – | 3 | | pF |
| $V_H$ | Input voltage hysteresis (Schmitt-Trigger)[42] | | – | 100 | – | mV |
| Idiode | Current through protection diode to $V_{DDIO}$ and $V_{SSIO}$ | | – | – | 100 | µA |

**Table 11-17. XRES AC Specifications**[42]

| Parameter | Description | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $T_{RESET}$ | Reset pulse width | | 1 | – | – | µs |

**Note**
42. Based on device characterization (Not production tested).

### 11.5.3 Voltage Reference

**Table 11-27. Voltage Reference Specifications**

See ADC external reference specifications in Delta-Sigma ADC on page 88.

| Parameter | Description | Conditions | | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|
| $V_{REF}$[50] | Precision reference voltage | Initial trimming, 25 °C | | 1.023 (–0.1%) | 1.024 | 1.025 (+0.1%) | V |
| | After typical PCB assembly, post reflow | Typical (non-optimized) board layout and 250 °C solder reflow. Device may be calibrated after assembly to improve performance. | –40 °C | – | ±0.5 | – | % |
| | | | 25 °C | – | ±0.2 | – | % |
| | | | 85 °C | – | ±0.2 | – | % |
| | | | 105 °C | – | ±0.3 | – | % |
| | Temperature drift[51] | | | – | – | 30 | ppm/°C |
| | Long term drift[51] | | | – | 100 | – | ppm/Khr |
| | Thermal cycling drift (stability)[51] | | | – | 100 | – | ppm |

**Figure 11-39. Vref vs Temperature**

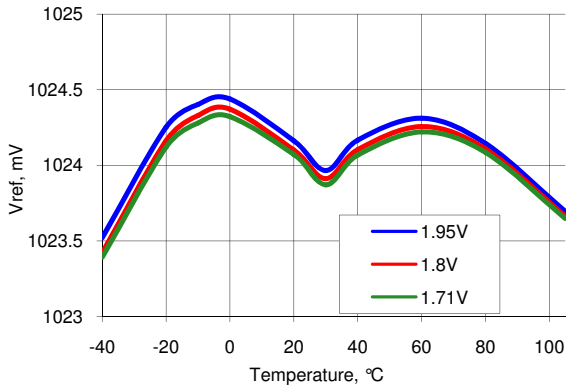
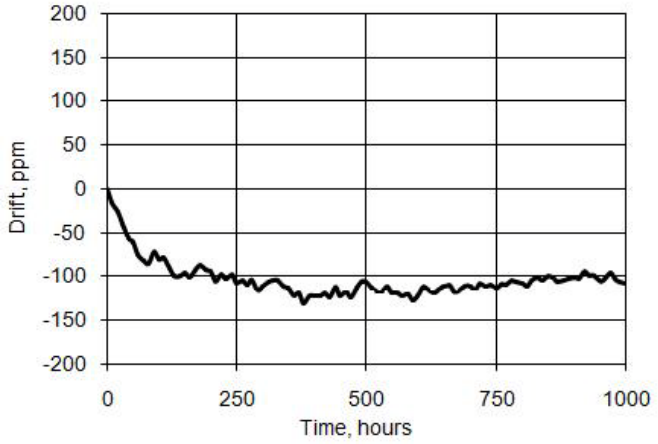



**Figure 11-40. Vref Long-term Drift**




**Notes**
50. $V_{REF}$ is measured after packaging, and thus accounts for substrate and die attach stresses.
51. Based on device characterization (Not production tested).

### 11.5.6 Comparator

**Table 11-32. Comparator DC Specifications**[58]

| Parameter | Description | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $V_{OS}$ | Input offset voltage in fast mode | Factory trim, Vdda > 2.7 V, Vin ≥ 0.5 V | – | | 10 | mV |
| | Input offset voltage in slow mode | Factory trim, Vin ≥ 0.5 V | – | | 9 | mV |
| $V_{OS}$ | Input offset voltage in fast mode[59] | Custom trim | – | – | 4 | mV |
| | Input offset voltage in slow mode[59] | Custom trim | – | – | 4 | mV |
| $V_{OS}$ | Input offset voltage in ultra low power mode | | – | ±12 | – | mV |
| TCVos | Temperature coefficient, input offset voltage | $V_{CM}$ = $V_{DDA}$ / 2, fast mode | – | 63 | 85 | µV/°C |
| | | $V_{CM}$ = $V_{DDA}$ / 2, slow mode | – | 15 | 20 | |
| $V_{HYST}$ | Hysteresis | Hysteresis enable mode | – | 10 | 32 | mV |
| $V_{ICM}$ | Input common mode voltage | High current / fast mode | $V_{SSA}$ | – | $V_{DDA}$ | V |
| | | Low current / slow mode | $V_{SSA}$ | – | $V_{DDA}$ | V |
| | | Ultra low power mode | $V_{SSA}$ | – | $V_{DDA}$ – 1.15 | V |
| CMRR | Common mode rejection ratio | | – | 50 | – | dB |
| $I_{CMP}$ | High current mode/fast mode | | – | – | 400 | µA |
| | Low current mode/slow mode | | – | – | 100 | µA |
| | Ultra low power mode | | – | 6 | – | µA |

**Table 11-33. Comparator AC Specifications**[58]

| Parameter | Description | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $T_{RESP}$ | Response time, high current mode[59] | 50 mV overdrive, measured pin-to-pin | – | 75 | 110 | ns |
| | Response time, low current mode[59] | 50 mV overdrive, measured pin-to-pin | – | 155 | 200 | ns |
| | Response time, ultra low power mode[59] | 50 mV overdrive, measured pin-to-pin | – | 55 | – | µs |

**Notes**
58. The recommended procedure for using a custom trim value for the on-chip comparators can be found in the TRM.
59. Based on device characterization (Not production tested).

**Figure 11-47. IDAC INL vs Input Code, Range = 255 µA, Source Mode**

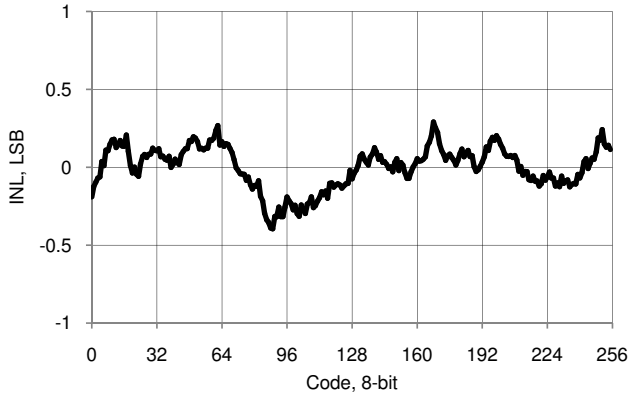



**Figure 11-48. IDAC INL vs Input Code, Range = 255 µA, Sink Mode**

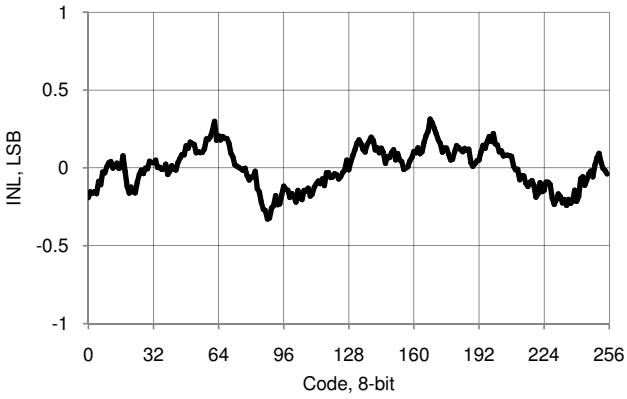



**Figure 11-49. IDAC DNL vs Input Code, Range = 255 µA, Source Mode**

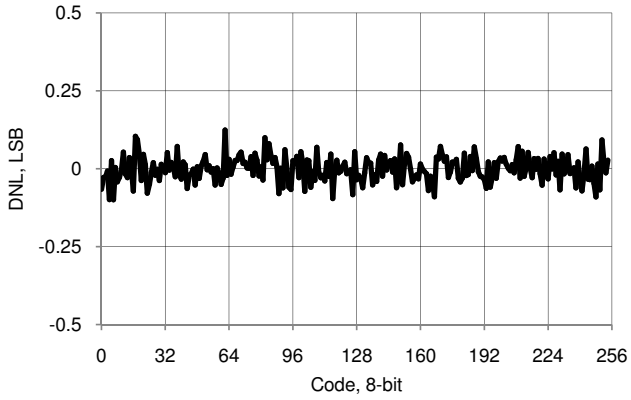



**Figure 11-50. IDAC DNL vs Input Code, Range = 255 µA, Sink Mode**

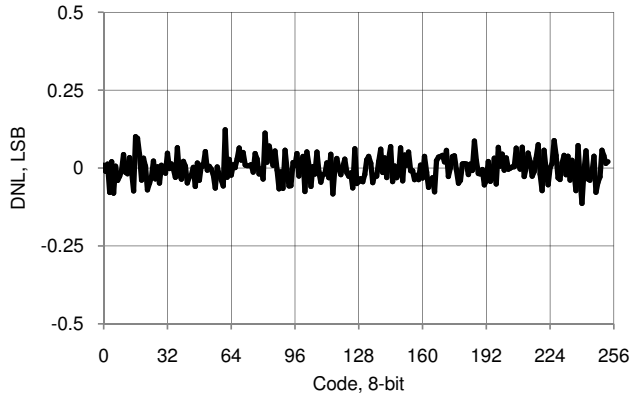



**Figure 11-51. IDAC INL vs Temperature, Range = 255 µA, Fast Mode**

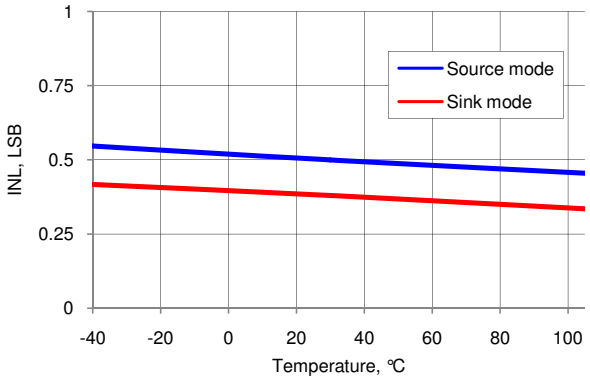



**Figure 11-52. IDAC DNL vs Temperature, Range = 255 µA, Fast Mode**

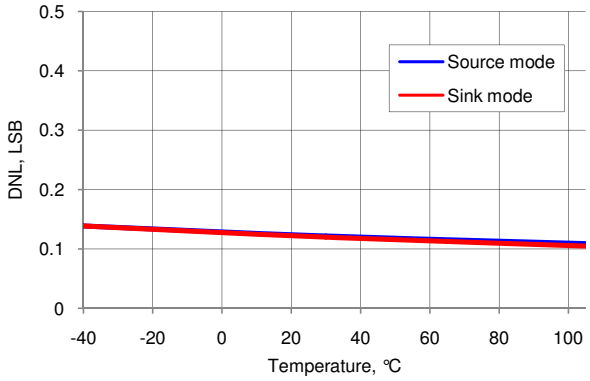


**Figure 11-53. IDAC Full Scale Error vs Temperature, Range = 255 µA, Source Mode**

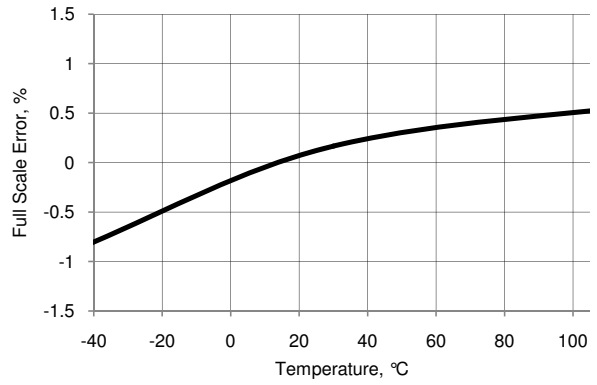



**Figure 11-54. IDAC Full Scale Error vs Temperature, Range = 255 µA, Sink Mode**

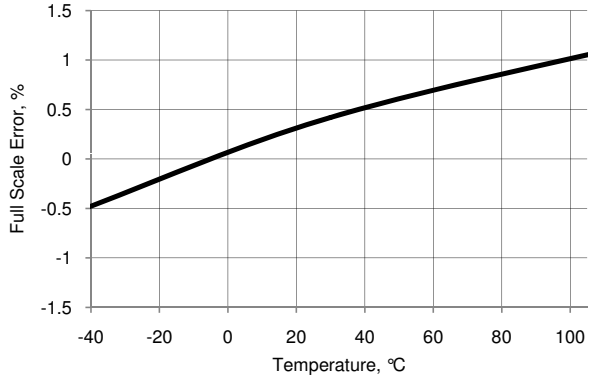



**Figure 11-55. IDAC Operating Current vs Temperature, Range = 255 µA, Code = 0, Source Mode**

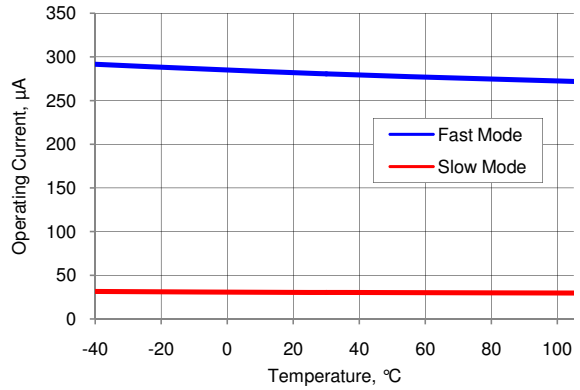
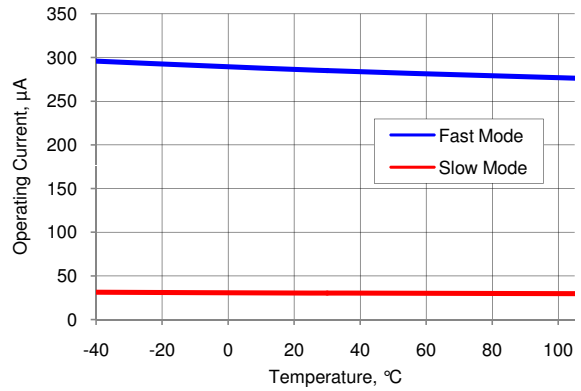



**Figure 11-56. IDAC Operating Current vs Temperature, Range = 255 µA, Code = 0, Sink Mode**



### *11.5.8 Voltage Digital to Analog Converter (VDAC)*

See the VDAC component datasheet in PSoC Creator for full electrical specifications and APIs.

Unless otherwise specified, all charts and graphs show typical values.

**Table 11-36. VDAC DC Specifications**

| Parameter | Description | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| | Resolution | | – | 8 | – | bits |
| INL1 | Integral nonlinearity | 1 V scale | – | ±2.1 | ±2.5 | LSB |
| INL4 | Integral nonlinearity[63] | 4 V scale | – | ±2.1 | ±2.5 | LSB |
| DNL1 | Differential nonlinearity | 1 V scale | – | ±0.3 | ±1 | LSB |
| DNL4 | Differential nonlinearity[63] | 4 V scale | – | ±0.3 | ±1 | LSB |
| Rout | Output resistance | 1 V scale | – | 4 | – | kΩ |
| | | 4 V scale | – | 16 | – | kΩ |
| $V_{OUT}$ | Output voltage range, code = 255 | 1 V scale | – | 1.02 | – | V |
| | | 4 V scale, Vdda = 5 V | – | 4.08 | – | V |
| | Monotonicity | | – | – | Yes | – |
| $V_{OS}$ | Zero scale error | | – | 0 | ±0.9 | LSB |
| Eg | Gain error | 1 V scale | – | – | ±2.5 | % |
| | | 4 V scale | – | – | ±2.5 | % |
| TC_Eg | Temperature coefficient, gain error | 1 V scale | – | – | 0.03 | %FSR / °C |
| | | 4 V scale | – | – | 0.03 | %FSR / °C |
| $I_{DD}$ | Operating current[63] | Slow mode | – | – | 100 | µA |
| | | Fast mode | – | – | 500 | µA |

**Figure 11-61. VDAC INL vs Input Code, 1 V Mode**

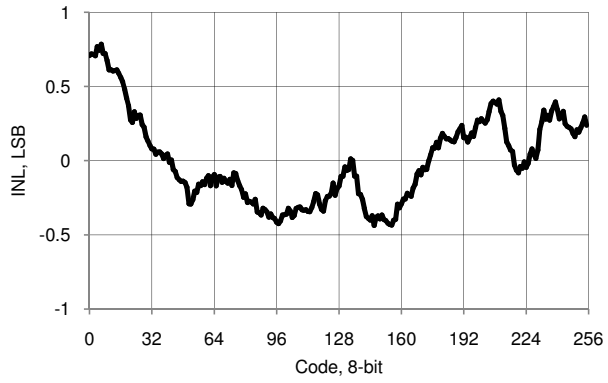
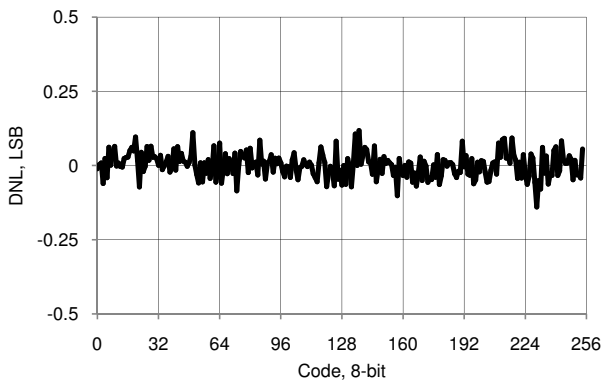



**Figure 11-62. VDAC DNL vs Input Code, 1 V Mode**




**Note**
63. Based on device characterization (Not production tested).

### 11.5.12 Temperature Sensor

**Table 11-44. Temperature Sensor Specifications**

| Parameter | Description | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| | Temp sensor accuracy | Range: –40 °C to +105 °C | – | ±5 | – | °C |

### 11.5.13 LCD Direct Drive

**Table 11-45. LCD Direct Drive DC Specifications[69]**

| Parameter | Description | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $I_{CC}$ | LCD Block (no glass) | Device sleep mode with wakeup at 400Hz rate to refresh LCD, bus, clock = 3MHz, Vddio = Vdda = 3V, 8 commons, 16 segments, 1/5 duty cycle, 40 Hz frame rate, no glass connected | – | 81 | – | µA |
| $I_{CC\_SEG}$ | Current per segment driver | Strong drive mode | – | 260 | – | µA |
| $V_{BIAS}$ | LCD bias range ($V_{BIAS}$ refers to the main output voltage(V0) of LCD DAC) | $V_{DDA} \geq 3$ V and $V_{DDA} \geq V_{BIAS}$ | 2 | – | 5 | V |
| | LCD bias step size | $V_{DDA} \geq 3$ V and $V_{DDA} \geq V_{BIAS}$ | – | 9.1 × $V_{DDA}$ | – | mV |
| | LCD capacitance per segment/ common driver | Drivers may be combined | – | 500 | 5000 | pF |
| | Maximum segment DC offset | $V_{DDA} \geq 3$ V and $V_{DDA} \geq V_{BIAS}$ | – | – | 20 | mV |
| $I_{OUT}$ | Output drive current per segment driver) | $V_{DDIO}$ = 5.5 V, strong drive mode | 355 | – | 710 | µA |

**Table 11-46. LCD Direct Drive AC Specifications[69]**

| Parameter | Description | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $f_{LCD}$ | LCD frame rate | | 10 | 50 | 150 | Hz |

**Note**
69. Based on device characterization (Not production tested).

## 11.6 Digital Peripherals

Specifications are valid for –40 °C ≤ $T_A$ ≤ 105 °C and $T_J$ ≤ 120 °C, except where noted. Specifications are valid for 1.71 V to 5.5 V, except where noted.

### *11.6.1 Timer*

The following specifications apply to the Timer/Counter/PWM peripheral in timer mode. Timers can also be implemented in UDBs; for more information, see the Timer component datasheet in PSoC Creator.

**Table 11-47. Timer DC Specifications**[70]

| Parameter | Description | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| | Block current consumption | 16-bit timer, at listed input clock frequency | – | – | – | µA |
| | 3 MHz | | – | 15 | – | µA |
| | 12 MHz | | – | 60 | – | µA |
| | 48 MHz | | – | 260 | – | µA |
| | 80 MHz | | – | 360 | – | µA |

**Table 11-48. Timer AC Specifications**[70]

| Parameter | Description | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| | Operating frequency | | DC | – | 80.01 | MHz |
| | Capture pulse width (Internal)[71] | | 15 | – | – | ns |
| | Capture pulse width (external) | | 30 | – | – | ns |
| | Timer resolution[71] | | 15 | – | – | ns |
| | Enable pulse width[71] | | 15 | – | – | ns |
| | Enable pulse width (external) | | 30 | – | – | ns |
| | Reset pulse width[71] | | 15 | – | – | ns |
| | Reset pulse width (external) | | 30 | – | – | ns |

**Notes**
70. Based on device characterization (Not production tested).
71. For correct operation, the minimum Timer/Counter/PWM input pulse width is the period of bus clock.

### 11.6.3 Pulse Width Modulation

The following specifications apply to the Timer/Counter/PWM peripheral, in PWM mode. PWM components can also be implemented in UDBs; for more information, see the PWM component datasheet in PSoC Creator.

**Table 11-51. PWM DC Specifications**[74]

| Parameter | Description | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| | Block current consumption | 16-bit PWM, at listed input clock frequency | – | – | – | µA |
| | 3 MHz | | – | 15 | – | µA |
| | 12 MHz | | – | 60 | – | µA |
| | 48 MHz | | – | 260 | – | µA |
| | 80 MHz | | – | 360 | – | µA |

**Table 11-52. PWM AC Specifications**[74]

| Parameter | Description | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| | Operating frequency | | DC | – | 80.01 | MHz |
| | Pulse width[75] | | 15 | – | – | ns |
| | Pulse width (external) | | 30 | – | – | ns |
| | Kill pulse width[75] | | 15 | – | – | ns |
| | Kill pulse width (external) | | 30 | – | – | ns |
| | Enable pulse width[75] | | 15 | – | – | ns |
| | Enable pulse width (external) | | 30 | – | – | ns |
| | Reset pulse width[75] | | 15 | – | – | ns |
| | Reset pulse width (external) | | 30 | – | – | ns |

### 11.6.4 $I^2C$

**Table 11-53. Fixed $I^2C$ DC Specifications**[74]

| Parameter | Description | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| | Block current consumption | Enabled, configured for 100 kbps | – | – | 250 | µA |
| | | Enabled, configured for 400 kbps | – | – | 260 | µA |

**Table 11-54. Fixed $I^2C$ AC Specifications**[76]

| Parameter | Description | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| | Bit rate | | – | – | 1 | Mbps |

### 11.6.5 Controller Area Network

**Table 11-55. CAN DC Specifications**[74, 77]

| Parameter | Description | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $I_{DD}$ | Block current consumption | | – | – | 200 | µA |

**Table 11-56. CAN AC Specifications**[74, 77]

| Parameter | Description | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| | Bit rate | Minimum 8 MHz clock | – | – | 1 | Mbit |

**Notes**
74. Based on device characterization (Not production tested).
75. For correct operation, the minimum Timer/Counter/PWM input pulse width is the period of bus clock.
76. Rise/fall time matching (TR) not guaranteed, see Table 11-15 on page 84.
77. Refer to ISO 11898 specification for details.

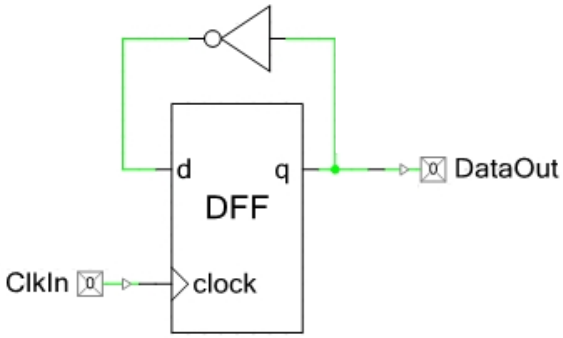
### *11.6.8 Universal Digital Blocks (UDBs)*

PSoC Creator provides a library of pre-built and tested standard digital peripherals (UART, SPI, LIN, PRS, CRC, timer, counter, PWM, AND, OR, and so on) that are mapped to the UDB array. See the component datasheets in PSoC Creator for full AC/DC specifications, APIs, and example code.

**Table 11-60. UDB AC Specifications**[79]

| Parameter | Description | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| Datapath Performance | | | | | | |
| $F_{MAX\_TIMER}$ | Maximum frequency of 16-bit timer in a UDB pair | | – | – | 67.01 | MHz |
| $F_{MAX\_ADDER}$ | Maximum frequency of 16-bit adder in a UDB pair | | – | – | 67.01 | MHz |
| $F_{MAX\_CRC}$ | Maximum frequency of 16-bit CRC/PRS in a UDB pair | | – | – | 67.01 | MHz |
| PLD Performance | | | | | | |
| $F_{MAX\_PLD}$ | Maximum frequency of a two-pass PLD function in a UDB pair | | – | – | 67.01 | MHz |
| Clock to Output Performance | | | | | | |
| $t_{CLK\_OUT}$ | Propagation delay for clock in to data out, see Figure 11-76. | 25 °C, $V_{DDD} \geq 2.7$ V | – | 20 | 25 | ns |
| $t_{CLK\_OUT}$ | Propagation delay for clock in to data out, see Figure 11-76. | Worst-case placement, routing, and pin selection | – | – | 55 | ns |

**Figure 11-76. Clock to Output Performance**




**Note**
79. Based on device characterization (Not production tested).

### 11.8.5 SWD Interface

**Figure 11-80. SWD Interface Timing**

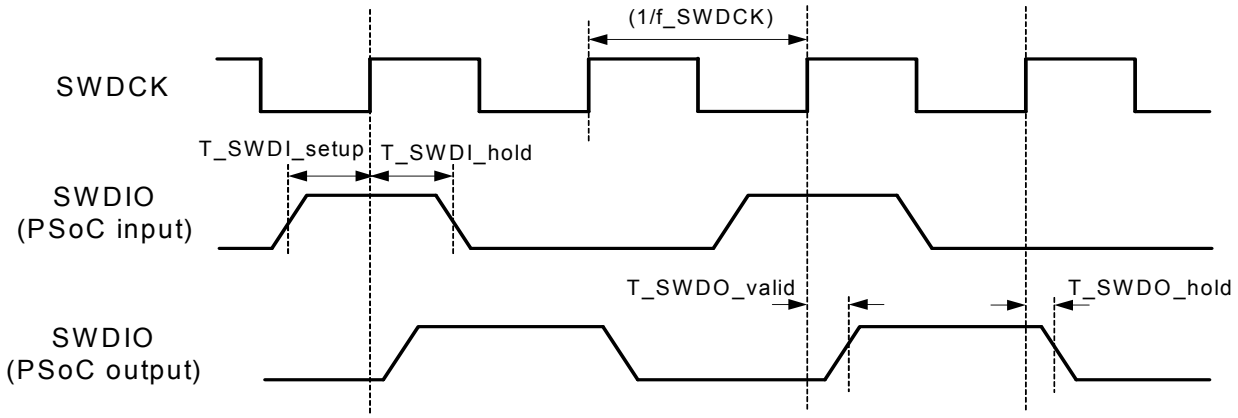



**Table 11-77. SWD Interface AC Specifications**[95]

| Parameter | Description | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| f_SWDCK | SWDCLK frequency | 3.3 V ≤ $V_{DDD}$ ≤ 5 V | – | – | 12[96] | MHz |
| | | 1.71 V ≤ $V_{DDD}$ < 3.3 V | – | – | 7[96] | MHz |
| | | 1.71 V ≤ $V_{DDD}$ < 3.3 V, SWD over USBIO pins | – | – | 5.5[96] | MHz |
| T_SWDI_setup | SWDIO input setup before SWDCK high | T = 1/f_SWDCK max | T/4 | – | – | |
| T_SWDI_hold | SWDIO input hold after SWDCK high | T = 1/f_SWDCK max | T/4 | – | – | |
| T_SWDO_valid | SWDCK high to SWDIO output | T = 1/f_SWDCK max | – | – | T/2 | |
| T_SWDO_hold | SWDIO output hold after SWDCK high | T = 1/f_SWDCK max | 1 | – | – | ns |

### 11.8.6 TPIU Interface

**Table 11-78. TPIU Interface AC Specifications**[95]

| Parameter | Description | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| | TRACEPORT (TRACECLK) frequency | | – | – | 33[97] | MHz |
| | SWV bit rate | | – | – | 33[97] | Mbit |

**Notes**
95. Based on device characterization (Not production tested).
96. f_SWDCK must also be no more than 1/3 CPU clock frequency.
97. TRACEPORT signal frequency and bit rate are limited by GPIO output frequency, see Table 11-9 on page 77.