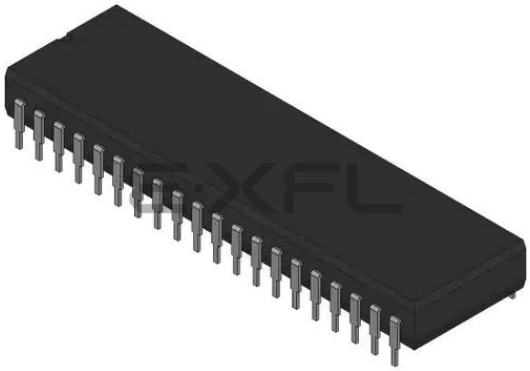

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RAM Size	-
Voltage - Supply (Vcc/Vdd)	-
Data Converters	-
Oscillator Type	-
Operating Temperature	-
Mounting Type	-
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Supplier Device Package	-
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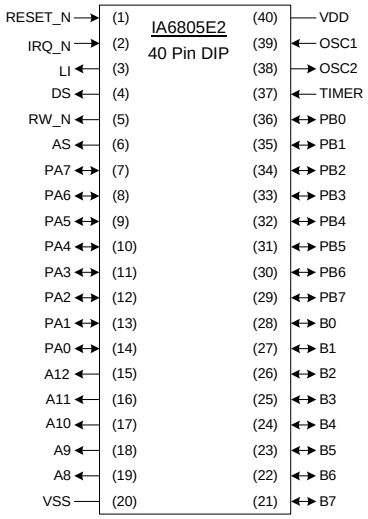
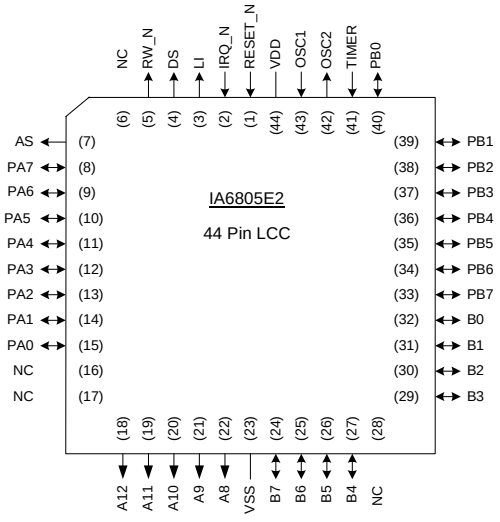
FEATURES

- **Form, Fit, and Function Compatible with the Harris© CDP6805E2CE and Motorola© MC146805E2**
- **Internal 8-bit Timer with 7-Bit Programmable Prescaler**
- **On-chip Clock**
- **Memory Mapped I/O**
- **Versatile Interrupt Handling**
- **True Bit Manipulation**
- **Bit Test and Branch Instruction**
- **Vectored Interrupts**
- **Power-saving STOP and WAIT Modes**
- **Fully Static Operation**
- **112 Bytes of RAM**
- **Packaging options available: 40 Pin Plastic DIP or, 44 Pin Plastic Leaded Chip Carrier, Standard or RoHS packages available**

The IA6805E2 is a "plug-and-play" drop-in replacement for the original IC. Innovasic produces replacement ICs using its MILES™, or Managed IC Lifetime Extension System, cloning technology. This technology produces replacement ICs far more complex than "emulation" while ensuring they are compatible with the original IC. MILES™ captures the design of a clone so it can be produced even as silicon technology advances. MILES™ also verifies the clone against the original IC so that even the "undocumented features" are duplicated. This data sheet documents all necessary engineering information about the IA6805E2 including functional and I/O descriptions, electrical characteristics, and applicable timing.

Package Pinout





I/O Signal Description

The table below describes the I/O characteristics for each signal on the IC. The signal names correspond to the signal names on the pinout diagrams provided.

SIGNAL NAME	I/O	DESCRIPTION
V_{DD} and V_{SS} (Power and Ground)	N/A	**Source:** These two pins provide power to the chip. V_{DD} provides +5 volts (±0.5) power and V_{SS} is ground.
RESET_n (Reset)	I	**TTL:** Input pin that can be used to reset the MPU's internal state by pulling the reset_n pin low.
IRQ_n (Interrupt Request)	I	**TTL:** Input pin that is level and edge sensitive. Can be used to request an interrupt sequence.
LI (Load Instruction)	O	**TTL with slew rate control:** Output pin used to indicate that a next opcode fetch is in progress. Used only for certain debugging and test systems. Not connected in normal operation. Overlaps Data Strobe (DS) signal. This output is capable of driving one standard TTL load and 50pF.
DS (Data Strobe)	O	**TTL with slew rate control:** Output pin used to transfer data to or from a peripheral or memory. DS occurs anytime the MPU does a data read or write and during data transfer to or from internal memory. DS is available at f_{OSC} ,5 when the MPU is not in the WAIT or STOP mode. This output is capable of driving one standard TTL load and 130pF.
RW_n (Read/Write)	O	**TTL with slew rate control:** Output pin used to indicate the direction of data transfer from internal memory, I/O registers, and external peripheral devices and memories. Indicates to a selected peripheral whether the MPU is to read (RW_n high) or write (RW_n low) data on the next data strobe. This output is capable of driving one standard TTL load and 130pF.
AS (Address Strobe)	O	**TTL with slew rate control:** Output strobe used to indicate the presence of an address on the 8-bit multiplexed bus. The AS line is used to demultiplex the eight least significant address bits from the data bus. AS is available at f_{OSC} , 5 when the MPU is not in the WAIT or STOP modes. This output is capable of driving one standard TTL load and 130pF.
PA0-PA7/PB0-PB7 (Input/Output Lines)	I/O	**TTL with slew rate control:** These 16 lines constitute Input/Output ports A and B. Each line is individually programmed to be either an input or output under software control of the Data Direction Register (DDR) as shown below in **Table 1** and **Figure 2**. The port I/O is programmed by writing the corresponding bit in the DDR to a "1" for output and a "0" for input. In the output mode the bits are latched and appear on the corresponding output pins. All the DDR's are initialized to a "0" on reset. The output port registers are not initialized on reset. Each output is capable of driving one standard TTL load and 50pF.
A8-A12 (High Order Address Lines)	O	**TTL with slew rate control:** These five outputs constitute the higher order non-multiplexed address lines. Each output is capable of driving one standard TTL load and 130pF.
B0-B7 (Address/Data Bus)	I/O	**TTL with slew rate control:** These bi-directional lines constitute the lower order addresses and data. These lines are multiplexed with address present at address strobe time and data present at data strobe time. When in the data mode, these lines are bi-directional, transferring data to and from memory and peripheral devices as indicated by the RW_n pin. As outputs, these lines are capable of driving one standard TTL load and 130pF.
Timer	I	**TTL:** Input used to control the internal timer/counter circuitry.
OSC1, OSC2 (System Clock)	I/O	**TTL Oscillator input/output:** These pins provide control input for the on-chip clock oscillator circuits. Either a crystal or external clock is connected to these pins to provide a system clock. The crystal connection is shown in **Figure 3**. The OSC1 to bus transitions for system designs using oscillators slower than 5MHz is shown in **Figure 4**.
Crystal		The circuit shown in **Figure 3** is recommended when using a crystal. An external CMOS oscillator is recommended when using crystals outside the specified ranges. To minimize output distortion and start-up stabilization time, the crystal and components should be mounted as close to the input pins as possible.
External Clock		When an external clock is used, it should be applied to the OSC1 input with the OSC2 input not connected, as shown in **Figure 3**.

Table 1

I/O Pin Functions

R/W-n	DDR	I/O Pin Functions
0	0	The I/O pin is in input mode. Data is written into the output data latch.
0	1	Data is written into the output data latch and output to the I/O pin.
1	0	The state of the I/O pin is read.
1	1	the I/O pin is in an output mode. The output data latch is read.

I/O Port Circuitry and Register Configuration:

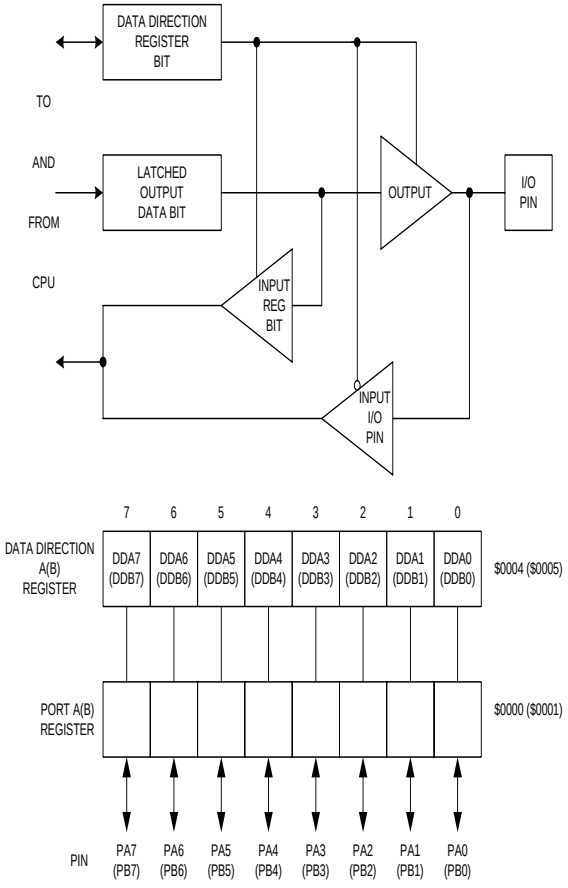


Figure 2. PA0-PA7/PB0-PB7 (Input/Output Lines)

I(Interrupt Mask Bit)

The interrupt mask bit indicates that both the external interrupt and the timer interrupt are disabled (masked). If an interrupt occurs while this bit is set, the interrupt is latched and is processed as soon as the interrupt bit is cleared.

H(Half Carry Bit)

The half carry bit indicates that a carry occurred between bits 3 and 4 of the ALU during an ADD or ADC operation.

Resets:

The MPU can be reset by initial power up or by the external reset pin (reset_n).

POR(Power On Reset)

Power on reset occurs on initial power up. It is strictly for power initialization conditions and should not be used to detect drops in the power supply voltage. There is a 1920 t_{CYC} time out delay from the time the oscillator is detected. If the reset_n pin is still low at the end of the delay, the MPU will remain in the reset state until the external pin goes high.

Reset_n

The reset_n pin is used to reset the MPU. The reset pin must stay low for a minimum of t_{cyc} to guarantee a reset. The reset_n pin is provided with a Schmitt Trigger to improve noise immunity capability.

Interrupts:

The MPU can be interrupted with the external interrupt pin (irq_n), the internal timer interrupt request, or the software interrupt instruction. When any of these interrupts occur, normal processing is suspended at the end of the current instruction execution. The processor registers are saved on the stack (stacking order shown in Figure 7) and the interrupt mask (I) is set to prevent additional interrupts. Normal processing resumes after the RTI instruction causes the register contents to be recovered from the stack. When the current instruction is completed, the processor checks all pending hardware interrupts and if unmasked (I bit clear) proceeds with interrupt processing. Otherwise, the next instruction is fetched and executed. Masked interrupts are latched for later interrupt service. External interrupts hold higher priority than timer interrupts. At the end of an instruction execution, if both an external interrupt and timer interrupt are pending, the external interrupt is serviced first. The SWI gets executed with the same priority as any other instruction if the hardware interrupts are masked (I bit set). Figure 8 shows the Reset and Interrupt processing flowchart.

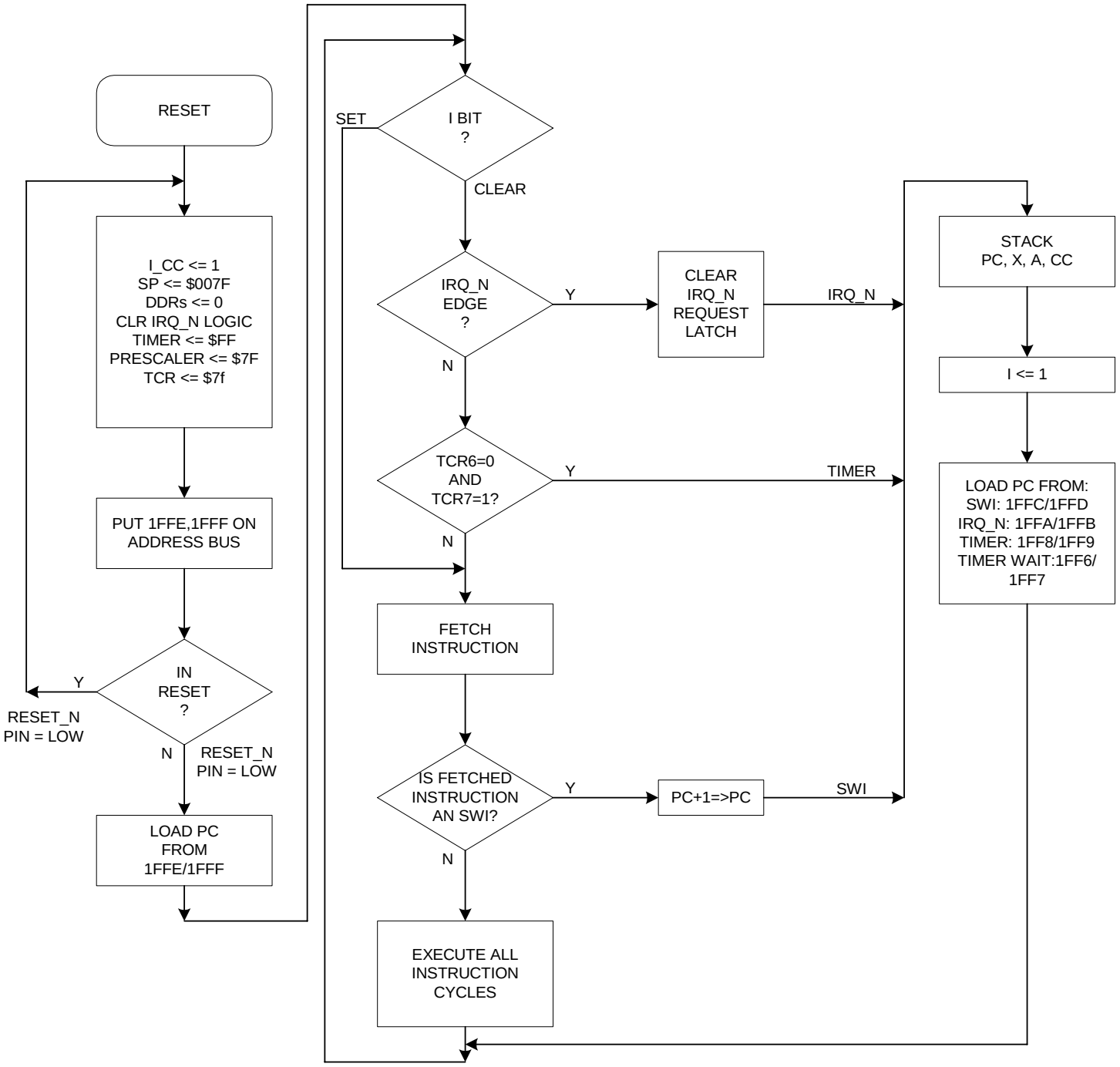


Figure 8. Reset and Interrupt Processing Flowchart

External Interrupt:

If the external interrupt pin irq_n is "low" and the interrupt mask bit of the condition code register is cleared, the external interrupt occurs. When the interrupt is recognized, the current state of the machine is pushed onto the stack and the condition code register I-bit gets set masking further interrupts until the present one is serviced. The program counter is then loaded with the contents of the interrupt vector, which contains the location of the interrupt service routine. The contents of $1FFA and $1FFB specify the address for this service routine. A functional diagram of the external interrupt is shown in Figure 9 and a mode diagram of the external interrupt is shown in Figure 10. The timing diagram shows two different treatments of the interrupt line (irq_n) to the processor. The first shows several interrupt lines "wire ORed" to form the interrupts at the processor. If the interrupt line (irq_n) remains low after servicing an interrupt, the next interrupt is recognized. The second shows single pulses on the interrupt line spaced far enough apart to be serviced. The minimum time between pulses is a function of the length of the interrupt service. After a pulse occurs, the next pulse should not occur until an RTI has occurred. The time between pulses (t_{ILIL}) is obtained by adding 20 instruction cycles to the total number of cycles it takes to complete the service routine including the RTI instruction.

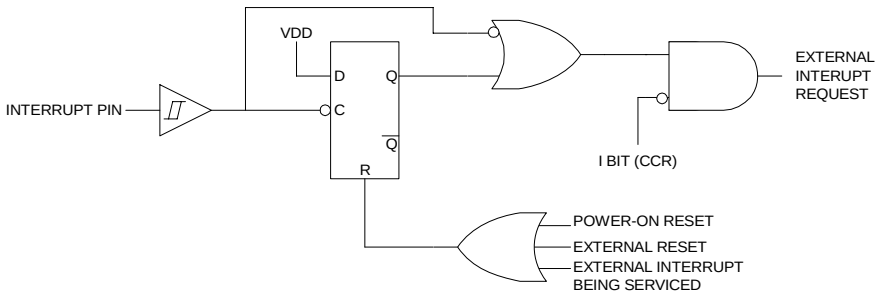


Figure 9. Interrupt Functional Diagram

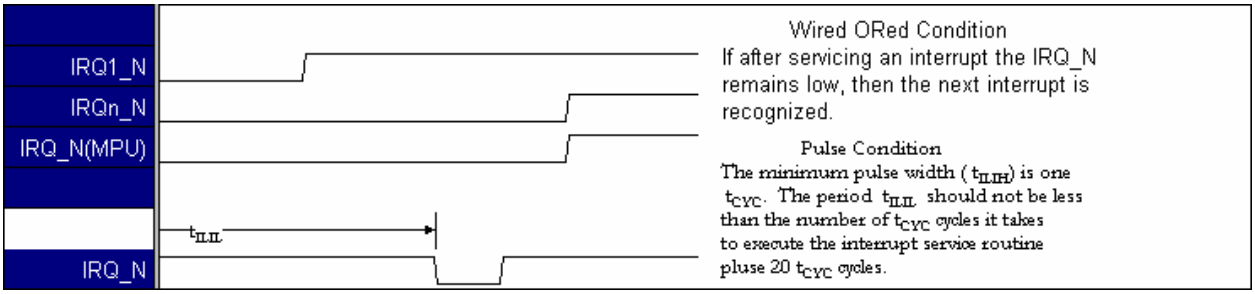


Figure 10. Interrupt Mode Diagram

Timer Interrupt:

If the timer mask bit (TCR6) and the interrupt mask bit (I) of the condition code register are cleared, each time the timer decrements to zero ($01 to $00 transition) an interrupt request is generated. When the interrupt is recognized, the current state of the machine is pushed onto the stack and the condition code register I-bit gets set masking further interrupts until the present one is serviced. The program counter is then loaded with the contents of the timer interrupt vector, which contains the location of the timer interrupt service routine. The contents of $1FF8 and $1FF9 specify the address for this service routine. If the MPU is in the wait mode and a timer interrupt occurs, then the contents of $1FF6 and $1FF7 specify the service routine. When the timer interrupt service routine is complete, the software executes an RTI instruction to restore the machine state and starts executing the interrupt program.

Software Interrupt:

Software interrupt is an executable instruction regardless of the state of the interrupt mask bit (I) in the condition code register. SWI is similar to hardware interrupts. It executes after the other interrupts if the interrupt mask bit is zero. The contents of $1FFC and $1FFD specify the address for this service routine.

Low Power Modes:

The low power modes consist of the stop instruction and the wait instruction. The following paragraphs explain these modes of operation.

Wait Mode:

The wait instruction places the MPU in low power consumption mode. The wait instruction disables clocking of most internal registers. The DS and AS output lines go "low" and the RW_n line goes "high". The multiplexed address/data bus goes to the data input state. The high order address lines remain at the address of the next instruction. External interrupts are enabled by clearing the I bit in the condition code register. All other registers, memory, and I/O remain unaltered. Only an external interrupt, timer interrupt, or reset will bring the MPU out of the wait mode. The timer may be enabled to allow a periodic exit from the wait mode. If an external and a timer interrupt occur at the same time, the external interrupt is serviced first. Then, if the timer interrupt request is not cleared in the external interrupt routine, the normal timer interrupt (not the timer wait interrupt) is serviced since the MPU is no longer in the wait mode. Figure 12 shows a flowchart of the wait function.

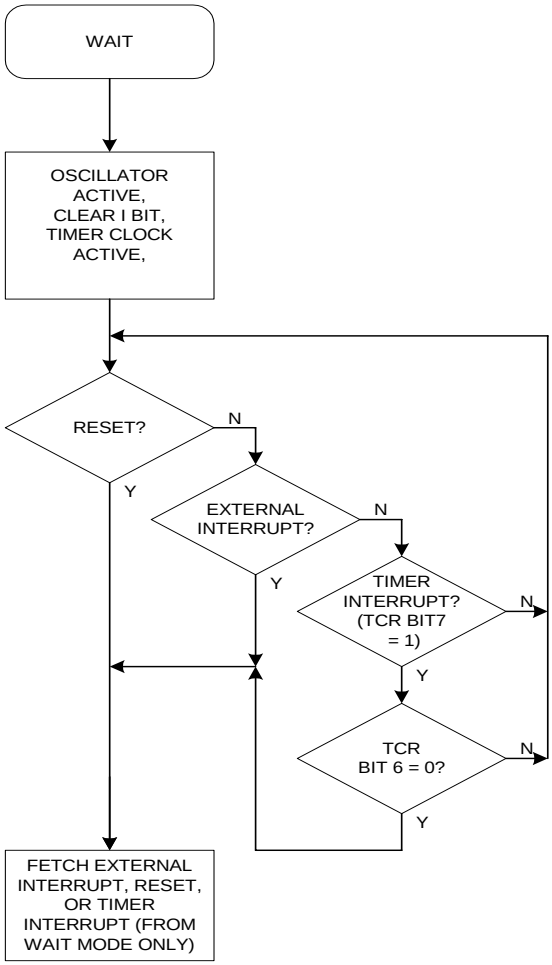


Figure 12. WAIT Function Flowchart

Timer:

The MPU contains a single 8-bit software programmable counter driven by a 7-bit software programmable prescaler. The counter may be loaded under program control and decrements to zero. When the counter decrements to zero, the timer interrupt request bit in the timer control register (TCR7) is set. Figure 13 shows a block diagram of the timer. If the timer mask bit (TCR6) and the interrupt mask bit (I) of the condition code register are cleared, an interrupt request is generated. After completion of the current instruction, the current state of the machine is pushed onto the stack. The timer interrupt vector address is then fetched from locations $1FF8 and $1FF9 and the interrupt routine is executed, unless the MPU was in the WAIT mode in which case the interrupt vector address in locations $1FF6 and $1FF7 is fetched. Power-On-Reset causes the counter to set to $FF.

NOTE: 1. Prescaler and counter are clocked on the falling edge of the internal clock (AS) or external input.

2. Counter is written to during Data Strobe (DS) and counts down continuously.

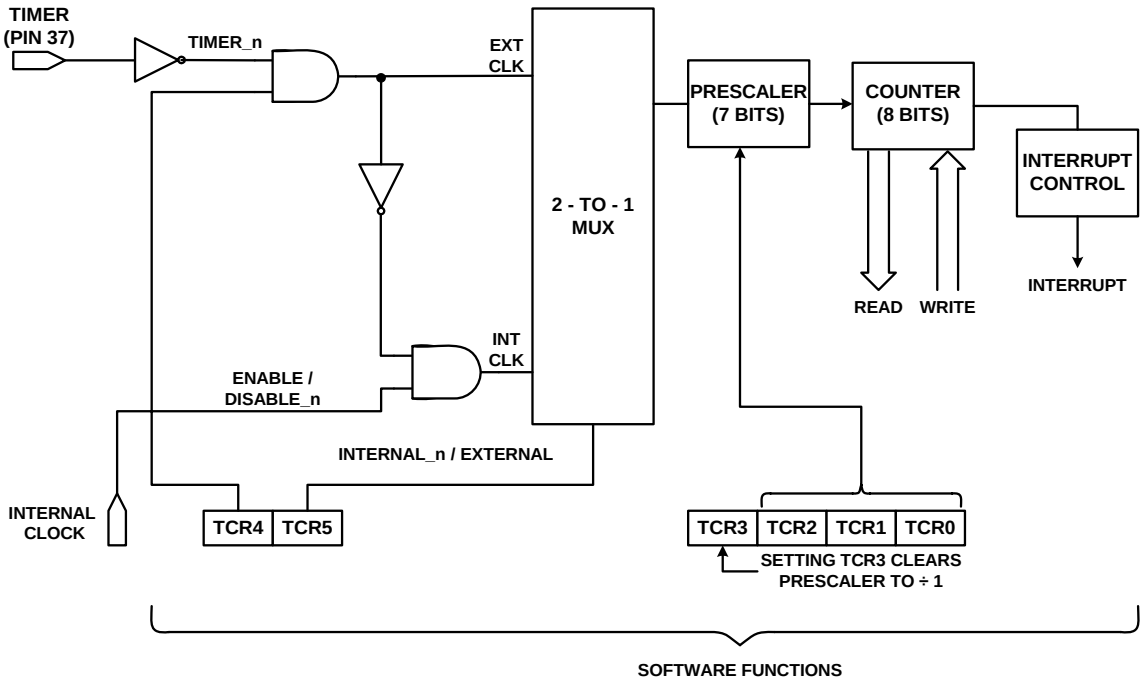


Figure 13. Timer Block Diagram

TCR (Timer Control Register ($0009)):

An 8-bit register that controls functions such as configuring operation mode, setting ratio of the prescaler, and generating timer interrupt request signals. All bits except bit 3 are read/write. Bits TCR5 - TCR0 are unaffected by reset_n.

7	6	5	4	3	2	1	0
TCR7	TCR6	TCR5	TCR4	TCR3	TCR2	TCR1	TCR0
Reset:							
0	1	0	0	0	0	0	0

TCR7 – Timer Interrupt Request

Used to indicate the timer interrupt when it is logic one.

1 – Set when the counter decrements to zero or under program control.

0 – Cleared on external reset, POR, STOP instruction, or program control.

TCR6 – Timer Interrupt Mask

Used to inhibit the timer interrupt.

1 – Interrupt inhibited. Set on external reset, POR, STOP instruction, or program control.

0 – Interrupt enabled.

TCR5 – External or Internal

Selects input clock source. Unaffected by reset.

1 – External clock selected.

0 – Internal clock selected (AS) ($f_{OSC}/5$).

TCR4 – Timer External Enable

Used to enable external timer pin or to enable the internal clock. Unaffected by reset.

1 – Enables external timer pin.

0 – Disables external timer pin.

TCR3 – Prescaler Clear

Write only bit. Writing a "1" to this bit resets the prescaler to zero. A read of this location always indicates a zero. Unaffected by reset.

TCR2, **TCR1**, **TCR0** – Prescaler select bits

Decoded to select one of eight outputs of the prescaler. Unaffected by reset.

Prescaler

TRC2	TRC1	TRC0	RESET
0	0	0	÷1
0	0	1	÷2
0	1	0	÷4
0	1	1	÷8
1	0	0	÷16
1	0	1	÷32
1	1	0	÷64
1	1	1	÷128

Opcode Map Summary:

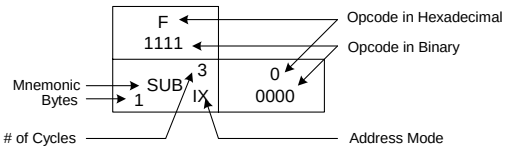
The following table is an opcode map for the instructions used on the MPU. The legend following the table shows how to use the table.

	Bit Manipulation		Branch	Read-Modify-Write					Control		Register/Memory						
	BTB	BSC	REL	DIR	INH	INH	IX1	IX	INH	INH	IMM	DIR	EXT	IX2	IX1	IX	
Hi	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	Hi
Low	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111	Low
0 0000	5 BRSET0 3 BTB	5 BSET0 2 BSC	3 BRA 2 REL	5 NEG 2 DIR	3 NEGA 1 INH	3 NEGX 1 INH	6 NEG 2 IX1	5 NEG 1 IX	9 RTI 1 INH		2 SUB 2 IMM	3 SUB 2 DIR	4 SUB 3 EXT	5 SUB 3 IX2	4 SUB 2 IX1	3 SUB 1 IX	0 0000
1 0001	5 BRCLR0 3 BTB	5 BCLR0 2 BSC	3 BRN 2 REL						6 RTS 1 INH		2 CMP 2 IMM	3 CMP 2 DIR	4 CMP 3 EXT	5 CMP 3 IX2	4 CMP 2 IX1	3 CMP 1 IX	1 0001
2 0010	5 BRSET1 3 BTB	5 BSET1 2 BSC	3 BHI 2 REL								2 SBC 2 IMM	3 SBC 2 DIR	4 SBC 3 EXT	5 SBC 3 IX2	4 SBC 2 IX1	3 SBC 1 IX	2 0010
3 0011	5 BRCLR1 3 BTB	5 BCLR1 2 BSC	3 BLS 2 REL	5 COM 2 DIR	3 COMA 1 INH	3 COMX 1 INH	6 COM 2 IX1	5 COM 1 IX	10 SWI 1 INH		2 CPX 2 IMM	3 CPX 2 DIR	4 CPX 3 EXT	5 CPX 3 IX2	4 CPX 2 IX1	3 CPX 1 IX	3 0011
4 0100	5 BRSET2 3 BTB	5 BSET2 2 BSC	3 BCC 2 REL	5 LSR 2 DIR	3 LSRA 1 INH	3 LSRX 1 INH	6 LSR 2 IX1	5 LSR 1 IX			2 AND 2 IMM	3 AND 2 DIR	4 AND 3 EXT	5 AND 3 IX2	4 AND 2 IX1	3 AND 1 IX	4 0100
5 0101	5 BRCLR2 3 BTB	5 BCLR2 2 BSC	3 BCS 2 REL								2 BIT 2 IMM	3 BIT 2 DIR	4 BIT 3 EXT	5 BIT 3 IX2	4 BIT 2 IX1	3 BIT 1 IX	5 0101
6 0110	5 BRSET3 3 BTB	5 BSET3 2 BSC	3 BNE 2 REL	5 ROR 2 DIR	3 RORA 1 INH	3 RORX 1 INH	6 ROR 2 IX1	5 ROR 1 IX			2 LDA 2 IMM	3 LDA 2 DIR	4 LDA 3 EXT	5 LDA 3 IX2	4 LDA 2 IX1	3 LDA 1 IX	6 0110
7 0111	5 BRCLR3 3 BTB	5 BCLR3 2 BSC	3 BEQ 2 REL	5 ASR 2 DIR	3 ASRA 1 INH	3 ASRX 1 INH	6 ASR 2 IX1	5 ASR 1 IX		2 TAX 1 INH		4 STA 2 DIR	5 STA 3 EXT	6 STA 3 IX2	5 STA 2 IX1	4 STA 1 IX	7 0111
8 1000	5 BRSET4 3 BTB	5 BSET4 2 BSC	3 BHCC 2 REL	5 LSL 2 DIR	3 LSLA 1 INH	3 LSLX 1 INH	6 LSL 2 IX1	5 LSL 1 IX		2 CLC 1 INH	2 EOR 2 IMM	3 EOR 2 DIR	4 EOR 3 EXT	5 EOR 3 IX2	4 EOR 2 IX1	3 EOR 1 IX	8 1000
9 1001	5 BRCLR4 3 BTB	5 BCLR4 2 BSC	3 BHCS 2 REL	5 ROL 2 DIR	3 ROLA 1 INH	3 ROLX 1 INH	6 ROL 2 IX1	5 ROL 1 IX		2 SEC 1 INH	2 ADC 2 IMM	3 ADC 2 DIR	4 ADC 3 EXT	5 ADC 3 IX2	4 ADC 2 IX1	3 ADC 1 IX	9 1001
A 1010	5 BRSET5 3 BTB	5 BSET5 2 BSC	3 BPL 2 REL	5 DEC 2 DIR	3 DECA 1 INH	3 DECX 1 INH	6 DEC 2 IX1	5 DEC 1 IX		2 CLI 1 INH	2 ORA 2 IMM	3 ORA 2 DIR	4 ORA 3 EXT	5 ORA 3 IX2	4 ORA 2 IX1	3 ORA 1 IX	A 1010
B 1011	5 BRCLR5 3 BTB	5 BCLR5 2 BSC	3 BMI 2 REL							2 SEI 1 INH	2 ADD 2 IMM	3 ADD 2 DIR	4 ADD 3 EXT	5 ADD 3 IX2	4 ADD 2 IX1	3 ADD 1 IX	B 1011
C 1100	5 BRSET6 3 BTB	5 BSET6 2 BSC	3 BMC 2 REL	5 INC 2 DIR	3 INCA 1 INH	3 INCX 1 INH	6 INC 2 IX1	5 INC 1 IX		2 RSP 1 INH		2 JMP 2 DIR	3 JMP 3 EXT	4 JMP 3 IX2	3 JMP 2 IX1	2 JMP 1 IX	C 1100
D 1101	5 BRCLR6 3 BTB	5 BCLR6 2 BSC	3 BMS 2 REL	4 TST 2 DIR	3 TSTA 1 INH	3 TSTX 1 INH	6 TST 2 IX1	4 TST 1 IX		2 NOP 1 INH	6 BSR 2 IMM	5 JSR 2 DIR	6 JSR 3 EXT	7 JSR 3 IX2	6 JSR 2 IX1	5 JSR 1 IX	D 1101
E 1110	5 BRSET7 3 BTB	5 BSET7 2 BSC	3 BIL 2 REL						2 STOP 1 INH		2 LDX 2 IMM	3 LDX 2 DIR	4 LDX 3 EXT	5 LDX 3 IX2	4 LDX 2 IX1	3 LDX 1 IX	E 1110
F 1111	5 BRCLR7 3 BTB	5 BCLR7 2 BSC	3 BIH 2 REL	5 CLR 2 DIR	3 CLRA 1 INH	3 CLRX 1 INH	6 CLR 2 IX1	5 CLR 1 IX	2 WAIT 1 INH	2 TXA 1 INH		4 STX 2 DIR	5 STX 3 EXT	6 STX 3 IX2	5 STX 2 IX1	4 STX 1 IX	F 1111

Abbreviations for Address Modes:

INH	Inherent
A	Accumulator
X	Index Register
IMM	Immediate
DIR	Direct
EXT	Extended
REL	Relative
BSC	Bit set/clear
BTB	Bit test and branch
IX	Indexed, no offset
IX1	Indexed, 1 byte offset
IX2	Indexed, 2 byte offset

Legend:



AC/DC Parameters

Absolute maximum ratings:
Supply Voltage (V_{DD}).....-0.3V to 6V
Input Pin Voltage (V_{IN}).....-0.3 to V_{DD}+0.3V
Operating Temperature.....-40°C to 85°C
Storage temperature Range (Tstg).....- 55°C to 150°C
ESD Protection (HBM).....5000V

Note: The specifications indicate levels where permanent damage to the device may occur. Functional operation is not guaranteed under these conditions. Operation at absolute maximum conditions for extended periods may adversely affect the long-term reliability of the device.

DC Characteristics

(V_{DD}=4.5 to 5.5 Vdc, V_{SS}=0, T_A=T_L to T_H), unless otherwise specified

DC CHARACTERISTICS

Symbol	Parameter	Min	Max	Unit
V_{DD}	Supply Voltage	4.5	5.5	V
V_{OL}	Output Voltage, $I_{LOAD} \leq 2mA$	-	0.4	V
V_{OH}		3.5	-	V
I_{OL}	Output Current	-	2	mA
I_{OH}		-	-2	mA
V_{IH}	High Level input Voltage	2	-	V
V_{IL}	Low Level input Voltage	-	0.8	V
I_{IH}	High Level input Current	-	1	µA
I_{IL}	Low Level input Current	-	-1	µA
Vt-	Schmitt Negative Threshold	1.1	-	V
Vt+	Schmitt Positive Threshold	-	1.87	V
	Frequency of Operation			
f_{OSC}	Crystal	-	5	MHz
f_{OSC}	External Clock	DC	5	MHz

Control Timing

V_{SS}=0V, T_A=T_L to T_H

Parameters	Sym	V_{DD} = 5.0V ±10% f_{OSC} = 5MHz			Unit
		Min	Typ	Max	
I/O Port Timing – Input Setup Time (Figure 14)	t_{PVASL}	196	-	-	ns
Input Hold Time (Figure 14)	t_{ASLPX}	0	-	-	ns
Output Delay Time (Figure 14)	t_{ASLPV}	-	-	0	ns
Interrupt Setup Time (Figure 15)	T_{ILASL}	0.4	-	-	µs
Crystal Oscillator Startup Time (Figure 16)	t_{OXOV}	-	5	100	ms
Wait Recovery Startup Time (Figure 17)	t_{IVASH}	-	-	2	µs
Stop Recovery Startup Time (Figure 18)	t_{ILASH}	-	-	2	µs
Required Interrupt Release (Figure 15)	t_{DSLIH}	-	-	1.0	µs
Timer Pulse Width (Figure 17)	t_{TH}, t_{TL}	0.5	-	-	t_{CYC}
Reset Pulse Width (Figure 16)	t_{RL}	1.05	-	-	µs
Timer Period (Figure 17)	t_{TLTL}	1.0	-	-	t_{CYC}
Interrupt Pulse Width Low (Figure10)	t_{ILIH}	1.0	-	-	t_{CYC}
Interrupt Pulse Period (Figure 10)	t_{ILIL}	*	-	-	t_{CYC}
Oscillator Cycle Period (1/5 of t_{CYC}) (Figure 3)	t_{OLOL}	200	-	-	ns
OSC1 Pulse Width High (Figure 3)	t_{OH}	75	-	-	ns
OSC1 Pulse Width Low (Figure 3)	t_{OL}	75	-	-	ns

*The minimum period of t_{ILIL} should not be less than the number of t_{CYC} cycles it takes to execute the interrupt service routine plus 20 t_{CYC} cycles.

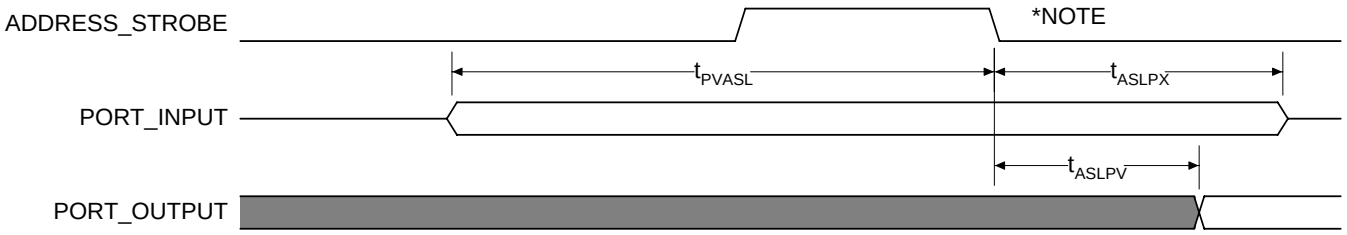
Bus Timing

V_{SS}=0V, T_A=T_L to T_H (Figure 19)

Num	Parameters	V_{DD} = 5.0V ±10% f_{OSC} = 5MHz 1 TTL, 100pF Load		Unit
		Min	Max	
1	Cycle Time	1000	DC	ns
2	Pulse Width, DS Low	587	-	ns
3	Pulse Width, DS High	403	-	ns
4	Clock Transition	-	4	ns
8	RW_n	9	-	ns
9	Non-Muxed Address Hold	97	-	ns
11	RW_n Delay From DS Fall	-	40	ns
16	Non-Muxed Address Delay From AS Rise	-	11	ns
17	MPU Read Data Setup	18	-	ns
18	Read Data Hold	0		ns
19	MPU Data Delay, Write	-	0	ns
21	Write Data Hold	204	-	ns
23	Muxed Address Delay From AS Rise	-	26	ns
24	Muxed Address Valid to AS Fall	185	-	ns
25	Muxed Address Hold	103	-	ns
26	Delay DS Fall to AS Rise	190	-	ns
27	Pulse Width, AS High	203	-	ns
28	Delay, AS Fall to DS Rise	185	-	ns

V_{LOW} = 0.8V, V_{HIGH} = V_{DD} – 2.0V, V_{DD} = 5.0V ±10%

T_A = T_L to T_H, C_L on Port = 50pF, f_{OSC} = 5MHz



*Note: The address strobe of the first cycle of the next instruction.

Figure 14. I/O Port Timing

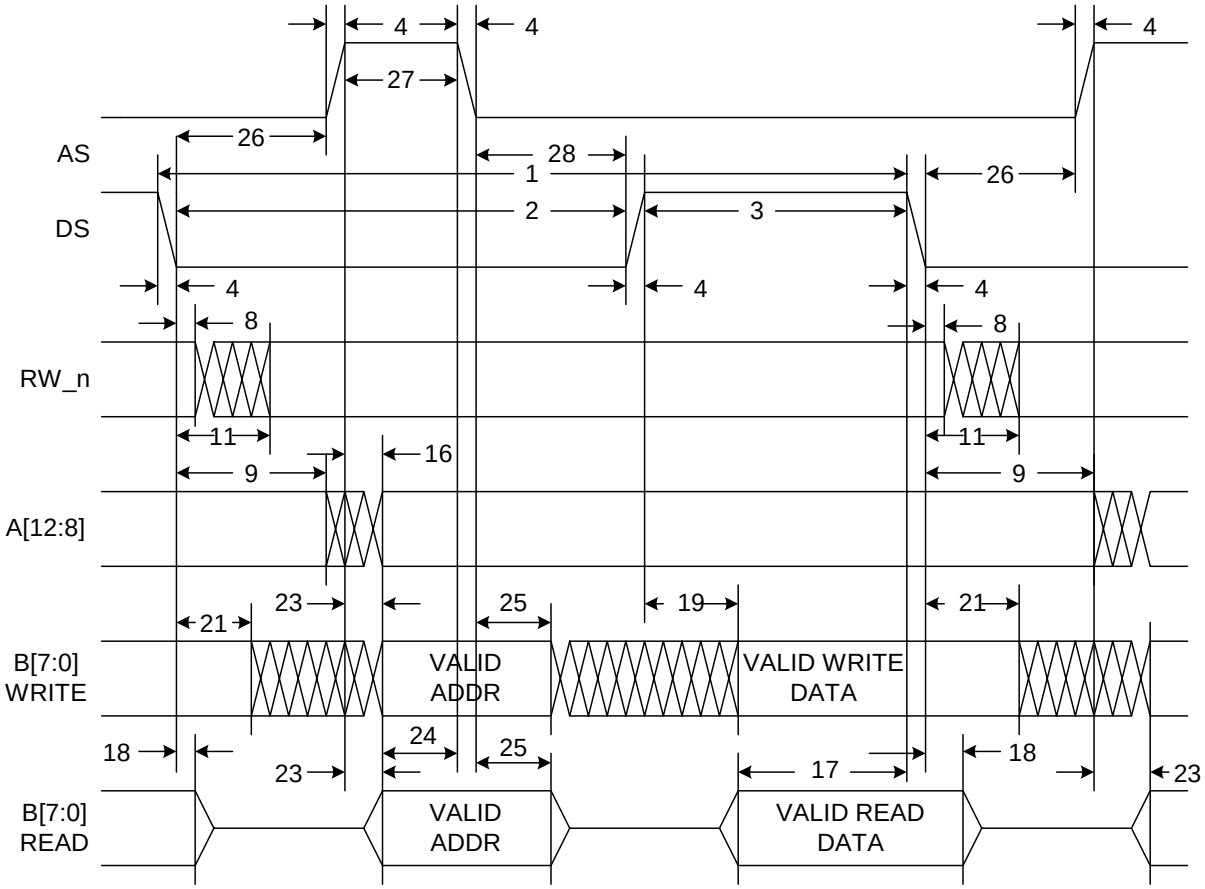
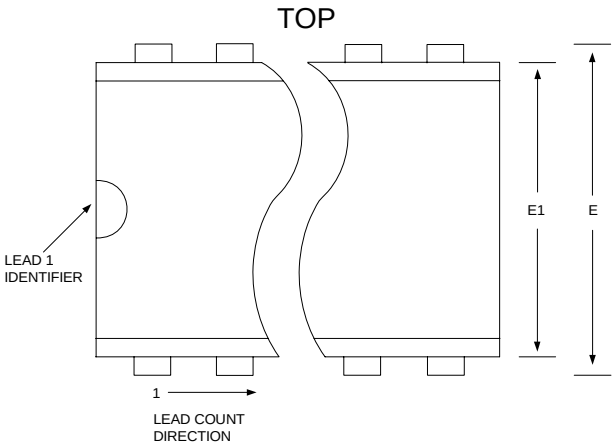
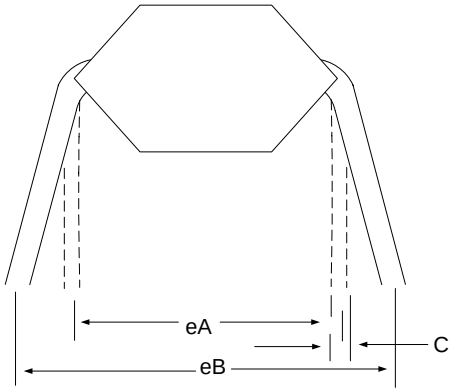


Figure 19. Bus Timing

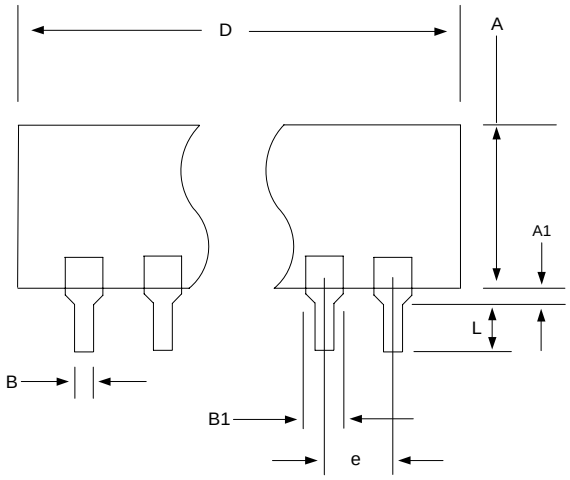
Packaging Information

PDIP Packaging





SIDE VIEW (WIDTH)

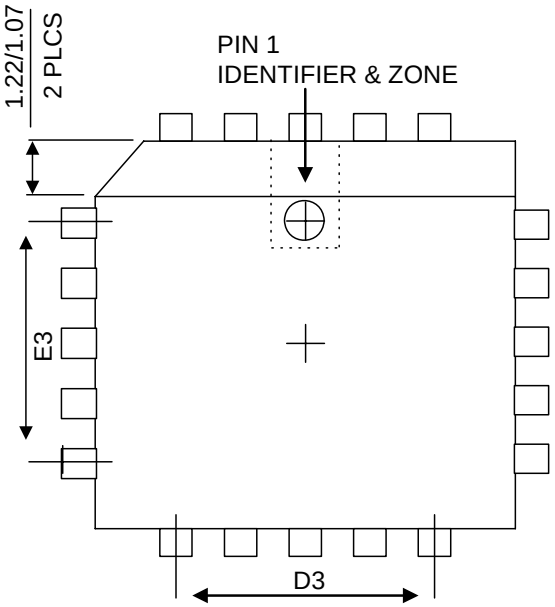


SIDE VIEW (LENGTH)

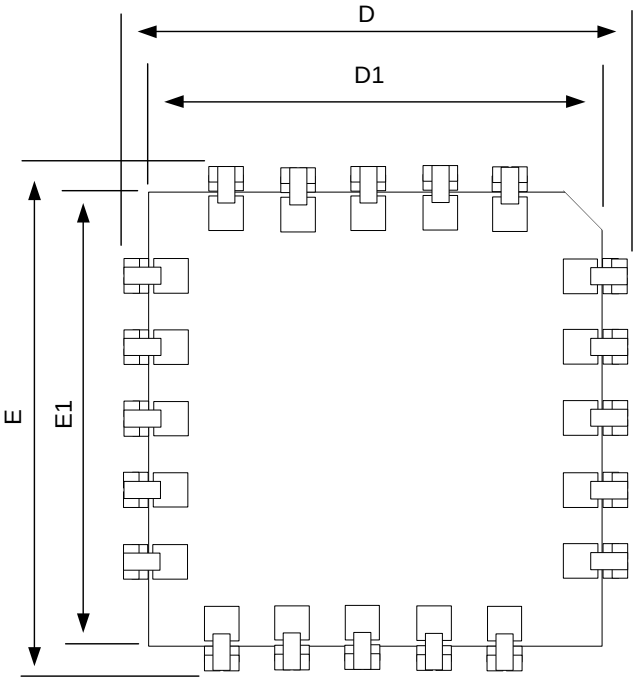
Lead Count

Symbol	40 (in Inches)	
	MIN	MAX
A	-	.200
A1	.015	-
B	.015	.020
B1	.040	.060
C	.008	.012
D	1.980	2.065
E	.580	.610
E1	.520	.560
e	.100 TYP	
eA	.580	-
eB	-	.686
L	.100 MIN	

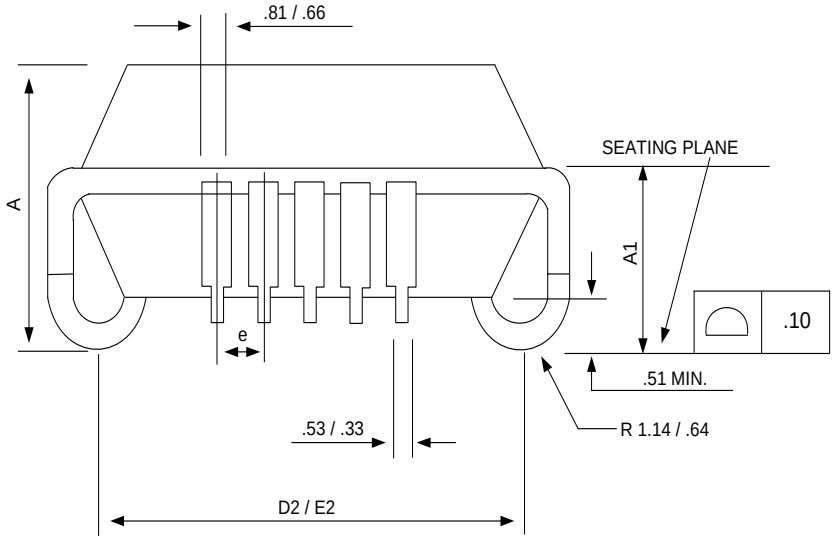
PLCC Packaging



TOP VIEW



BOTTOM VIEW



SIDE VIEW

LEAD COUNT

Symbol	44 (in Millimeters)	
	MIN	MAX
A	4.20	4.57
A1	2.29	3.04
D1	16.51	16.66
D2	14.99	16.00
D3	12.70 BSC	
E1	16.51	16.66
E2	14.99	16.00
E3	12.70 BSC	
e	1.27 BSC	
D	17.40	17.67
E	17.40	17.65

Ordering Information

The IA6805E2 is available in two package styles, both standard and RoHS compliant, listed in the table below. Other packages and temperature grades may be available for additional cost and lead time.

Order Number	Temperature Grade	Package Type
IA6805E2-PDW40I-00	Industrial	40 Lead Plastic DIP, 600 mil wide
IA6805E2-PDW40I-R-00 (RoHS compliant)	Industrial	40 Lead Plastic DIP, 600 mil wide
IA6805E2-PLC44I-00	Industrial	44 Lead Plastic Leaded Chip Carrier
IA6805E2-PLC44I-R-00 (RoHS compliant)	Industrial	44 Lead Plastic Leaded Chip Carrier

Cross Reference to Original Manufacturers

Innovasic Part Number	Motorola® Part Number	Harris® Part Number
IA6805E2-PDW40I	❑ MC146805E2CP	❑ CDP6805E2CE
	❑ MC146805E2P	❑ CDP6805E2E
IA6805E2-PLC44I	❑ MC146805E2CFN	❑ CDP6805E2CQ
	❑ MC146805E2FN	❑ CDP6805E2Q

Errata

Production Version 00

1. ***Functional differences between IA6805E2 and Harris and Motorola Versions:***

   A. Stop mode on IA6805E2 will not halt oscillator. Recovery from stop will be quicker.

   B. There is a functional difference between the IA6805E2 and the original device instruction sets regarding instructions for BSET and BCLR. **Analysis:** The instructions, BSET and BCLR (bit set and bit clear), are not supposed to affect the carry flag in the condition code register but in the IA6805E2 they do. Any situations where the BSET or BCLR commands are executed between a decision type instruction (branches) based on the carry flag and the instruction that was to update the carry flag should be considered suspect. **Workaround:** The workaround selected by the particular user is code dependent. Software will need to be revised to address the instruction set issues noted above.

   C. There is a functional difference between the IA6805E2 and the original device regarding the external timer input. **Analysis:** The original device is edge sensitive on this input (negative edge). The IA6805E has a synchronizing register on this input. If the stimulus to this input is a negative pulse less than a clock cycle wide, it is possible that this event will be missed by the timer circuit. **Workaround:** The workaround selected by the particular user is situation dependent. The input pulse either needs to be a minimum of 1 clock cycle wide or the pulse needs to be centered on the falling edge of the input clock.

2. ***Observations:***

   A. Original data sheets for Motorola and Harris are inconsistent when describing timer input mode 2. Original parts and Innovasic will AND together the timer input with the inverse of the internal clock (AS).

   B. Original Harris part would unpredictably "pre-increment" timer counter when writing to timer registers. IA6805E2 will not.

   C. Original Harris part displays incorrect address on external pins during intermediate cycles (not a functional problem) of multi-cycle instructions when accessing memory at page boundaries. IA6805E2 will not.

   D. Execution of illegal op-codes on the IA6805E2 will force a system reset. On the original Harris and Motorola parts, execution of illegal op-codes would produce unpredictable results.