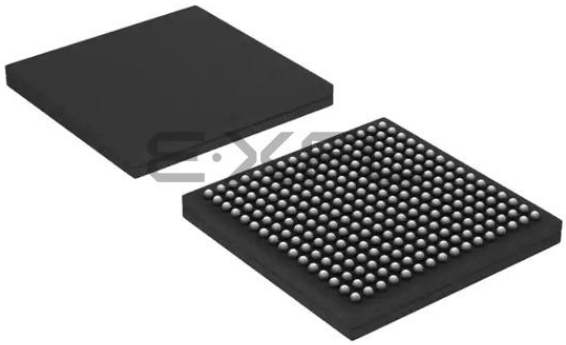

Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	Coldfire V4
Core Size	32-Bit Single-Core
Speed	250MHz
Connectivity	1-Wire®, CANbus, EBI/EMI, Ethernet, I²C, SmartCard, SPI, SSI, UART/USART, USB, USB OTG
Peripherals	DMA, PWM, WDT
Number of I/O	87
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	1.14V ~ 1.32V
Data Converters	A/D 8x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	256-LBGA
Supplier Device Package	256-MAPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcf54415cmj250

Table 1. MCF5441*x* family configurations (continued)

Module	MCF54410	MCF54415	MCF54416	MCF54417	MCF54418
NAND flash controller	•	•	•	•	•
1-Wire® interface	•	•	•	•	•
Serial boot facility	•	•	•	•	•
Watchdog timer	•	•	•	•	•
Interrupt controllers (INTC)	3	3	3	3	3
Edge port module (EPORT)	3 IRQs	5 IRQs	5 IRQs	5 IRQs	5 IRQs
Rapid GPIO pins	9	16	16	16	16
General-purpose I/O (GPIO) pins	48	87	87	87	87
JTAG - IEEE® 1149.1 Test Access Port	•	•	•	•	•
Package	196 MAPBGA	256 MAPBGA			

1.1 Ordering information

Table 2. Orderable part numbers

Freescale Part Number	Description	Package	Speed	Temperature
MCF54410CMF250	MCF54410 Microprocessor	196 MAPBGA	250 MHz	–40 to +85°C
MCF54415CMJ250	MCF54415 Microprocessor	256 MAPBGA		
MCF54416CMJ250	MCF54416 Microprocessor			
MCF54417CMJ250	MCF54417 Microprocessor			
MCF54418CMJ250	MCF54418 Microprocessor			

2 Hardware design considerations

2.1 Power filtering

To further enhance noise isolation, an external filter is strongly recommended for the analog V_{DD} pins (VDDA_PLL and VDDA_DAC_ADC). The filter shown in Figure 1 should be connected between the board 3.3 V (nominal) supply and the analog pins. The resistor and capacitors should be placed as close to the dedicated analog V_{DD} pin as possible. The 10 Ω resistor in the given filter is required.

Table 5. MCF5441*x* Signal information and muxing (continued)

Signal name	GPIO	Alternate 1	Alternate 2	Pullup (U)[1] Pulldown (D)	Direction[2]	Voltage domain	Pad type[3]	196 MAPBGA	256 MAPBGA
FlexCAN 1									
CAN1_TX	PB0	UART9_TXD	I2C1_SCL	—	I/O	EVDD	ssr	—	D14
CAN1_RX	PC7	UART9_RXD	I2C1_SDA	—	I/O	EVDD	ssr	—	D15
SDRAM controller									
SD_A14	—	—	—	—	O	SDVDD	st_dec ap	—	P6
SD_A[13:0]	—	—	—	—	O	SDVDD	st_dec ap	P3, M1, M3, L2, L1, N4, M2, P2, L3, L4, N1, N2, K1, N3	R4, R1, R3, N4, P3, T4, R2, T2, N3, P5, P4, N5, P2, T3
SD_BA[2:0]	—	—	—	—	O	SDVDD	st_dec ap	M6, J4, P4	P7, N6, R5
$\overline{\text{SD\_CAS}}$	—	—	—	—	O	SDVDD	st_dec ap	K4	N8
SD_CKE	—	—	—	—	O	SDVDD	st_dec ap	N6	R7
SD_CLK	—	—	—	—	O	SDVDD	st_ck	P6	T5
$\overline{\text{SD\_CLK}}$	—	—	—	—	O	SDVDD	st_ck	P7	T6
$\overline{\text{SD\_CS}}$	—	—	—	—	O	SDVDD	st_dec ap	M5	N7
SD_D[7:0]	—	—	—	—	I/O	SDVDD	st_odt	P11, M10, N10, M9, P10, M8, N8, M7	T12, R11, T11, R10, N9, T10, P9, R9
SD_DM	—	—	—	—	O	SDVDD	st_odt	N7	T7
SD_DQS	—	—	—	—	I/O	SDVDD	st_dqs	P8	T8
$\overline{\text{SD\_DQS}}$	—	—	—	—	I/O	SDVDD	st_dqs	P9	T9
SD_ODT	—	—	—	—	O	SDVDD	st_dec ap	P5	P8
$\overline{\text{SD\_RAS}}$	—	—	—	—	O	SDVDD	st_dec ap	M4	R6
$\overline{\text{SD\_WE}}$	—	—	—	—	O	SDVDD	st_dec ap	N5	R8
SD_VREF	—	—	—	—	—	SDVDD	st_vref	N9	P10
SD_VTT	—	—	—	—	—	SDVDD	st_vtt	L8	N10

Table 5. MCF5441*x* Signal information and muxing (continued)

Signal name	GPIO	Alternate 1	Alternate 2	Pullup (U)[1] Pulldown (D)	Direction[2]	Voltage domain	Pad type[3]	196 MAPBGA	256 MAPBGA
DSPI0_PCS0/$\overline{SS}$	PD7	I2C3_SDA	SDHC_DAT3	—	I/O	EVDD	msr	J1	K2
DSPI0_SCK/ SBF_CK	PD6	I2C3_SCL	SDHC_CLK	—	I/O	EVDD	msr	J3	L2
DSPI0_SIN/ SBF_DI	PD5	UART3_RXD	SDHC_CMD	U[14]	I	EVDD	msr	K2	L3
DSPI0_SOUT/ SBF_DO	PD4	UART3_TXD	SDHC_DAT0	—	O	EVDD	msr	J2	K1
One wire									
OW_DAT	RGPIO0/PD3	$\overline{DACK0}$	—	—	I/O	EVDD	ssr	M11	N11
DMA timers									
T3IN/PWM_EXTA3	RGPIO1/PD2	T3OUT	USBO_VBUS_EN/ ULPI_DIR[15]	—	I	EVDD	msr	G13	G13
T2IN/PWM_EXTA2	RGPIO2/PD1	T2OUT	SDHC_DAT2	—	I	EVDD	msr	J12	H14
T1IN/PWM_EXTA1	RGPIO3/PD0	T1OUT	SDHC_DAT1	—	I	EVDD	msr	H13	H13
T0IN/PWM_EXTA0	RGPIO4/PE7	T0OUT	USBO_VBUS_OC/ ULPI_NXT[16]	—[17]	I	EVDD	msr	J13	H15
UART 2									
$\overline{UART2\_CTS}$	RGPIO14/PE6	UART6_TXD	SSI1_BCLK	—	I	EVDD	msr	—	M4
$\overline{UART2\_RTS}$	RGPIO15/PE5	UART6_RXD	SSI1_FS	—	O	EVDD	msr	—	M3
UART2_RXD	PE4	PWM_A3	SSI1_RXD	—	I	EVDD	msr	—	P1
UART2_TXD	PE3	PWM_B3	SSI1_TXD	—	I/O[18]	EVDD	msr	—	N2
UART 1									
$\overline{UART1\_CTS}$	RGPIO7/PE2	UART5_TXD	DSPI3_SCK	—	I	EVDD	msr	D12	C10
$\overline{UART1\_RTS}$	RGPIO8/PE1	UART5_RXD	DSPI3_PCS0	—	O	EVDD	msr	D11	D10
UART1_RXD	PE0	I2C5_SDA	DSPI3_SIN	—	I	EVDD	msr	B10	C9
UART1_TXD	PF7	I2C5_SCL	DSPI3_SOUT	—	I/O[18]	EVDD	msr	C10	D9
UART 0									
$\overline{UART0\_CTS}$	RGPIO5/PF6	UART4_TXD	DSPI2_SCK	—	I	EVDD	msr	E12	E13
$\overline{UART0\_RTS}$	RGPIO6/PF5	UART4_RXD	DSPI2_PCS0	—	O	EVDD	msr	C12	B11
UART0_RXD	PF4	I2C4_SDA	DSPI2_SIN	—	I	EVDD	msr	C11	B10
UART0_TXD	PF3	I2C4_SCL	DSPI2_SOUT	—	I/O[18]	EVDD	msr	B11	D11

Table 5. MCF5441*x* Signal information and muxing (continued)

Signal name	GPIO	Alternate 1	Alternate 2	Pullup (U)[1] Pulldown (D)	Direction[2]	Voltage domain	Pad type[3]	196 MAPBGA	256 MAPBGA
Enhanced secure digital host controller									
SDHC_DAT3	PF2	PWM_A1	DSPI1_PCS0	—	I/O	EVDD	msr	—	B13
SDHC_DAT2	PF1	PWM_B1	DSPI1_PCS2	—	I/O	EVDD	msr	—	E14
SDHC_DAT1	PF0	PWM_A2	DSPI1_PCS1	—	I/O	EVDD	msr	—	D12
SDHC_DAT0	PG7	PWM_B2	DSPI1_SOUT	—	I/O	EVDD	msr	—	B12
SDHC_CMD	PG6	PWM_B0	DSPI1_SIN	—	I/O	EVDD	msr	—	C11
SDHC_CLK	PG5	PWM_A0	DSPI1_SCK	—	O	EVDD	msr	—	A10
Smart card interface 0									
SIM0_DATA	RGPIO13/PG4	PWM_FAULT2	SDHC_DAT7	—	I/O	EVDD	msr	—	E12
SIM0_VEN	RGPIO12/PG3	PWM_FAULT0	—	—	O	EVDD	msr	—	D13
SIM0_RST	RGPIO11/PG2	PWM_FORCE	SDHC_DAT6	—	O	EVDD	msr	—	C15
SIM0_PD	RGPIO10/PG1	PWM_SYNC	SDHC_DAT5	—	I	EVDD	msr	—	C14
SIM0_CLK	RGPIO9/PG0	PWM_FAULT1	SDHC_DAT4	—	O	EVDD	msr	—	A11
Synchronous serial interface 0[19]									
SSI0_RXD	PH7	I2C2_SDA	SIM1_VEN	—	I	EVDD	msr	B12	C12
SSI0_TXD	PH6	I2C2_SCL	SIM1_DATA	—	O	EVDD	msr	A11	C13
SSI0_FS	PH5	UART7_TXD	SIM1_RST	—	I/O	EVDD	msr	C13	E15
SSI0_MCLK	PH4	SSI_CLKIN	SIM1_CLK	—	O	EVDD	msr	A12	A12
SSI0_BCLK	PH3	UART7_RXD	SIM1_PD	—	I/O	EVDD	msr	D13	A13
Ethernet subsystem									
MII0_MDC	PI1	RMII0_MDC[20]	—	—	O	EVDD	fsr	N14	P16
MII0_MDIO	PI0	RMII0_MDIO[20]	—	—	I/O	EVDD	fsr	M14	N16
MII0_RXDV	PJ7	RMII0_CRS_DV[20]	—	—	I	EVDD	fsr	M13	P14
MII0_RXD[1:0]	PJ[6:5]	RMII0_RXD[1:0][20]	—	—	I	EVDD	fsr	P13, N13	R15, T15
MII0_RXER	PJ4	RMII0_RXER[20]	—	—	I	EVDD	fsr	M12	N14
MII0_TXD[1:0]	PJ[3:2]	RMII0_TXD[1:0][20]	—	—	O	EVDD	fsr	L12, L11	R13, P13
MII0_TXEN	PJ1	RMII0_TXEN[20]	—	D[21]	O	EVDD	fsr	N12	P12
MII0_COL	PJ0	RMII1_MDC	ULPI_STP	—	I	EVDD	fsr	—	R12
MII0_TXER	PK7	RMII1_MDIO	ULPI_DATA4	—	O	EVDD	fsr	—	R14
MII0_CRS	PK6	RMII1_CRS_DV	ULPI_DATA5	—	I	EVDD	fsr	—	P11
MII0_RXD[3:2]	PK[5:4]	RMII1_RXD[1:0]	ULPI_DATA[1:0]	—	I	EVDD	fsr	—	P15, N13

Table 5. MCF5441*x* Signal information and muxing (continued)

Signal name	GPIO	Alternate 1	Alternate 2	Pullup (U)[1] Pulldown (D)	Direction[2]	Voltage domain	Pad type[3]	196 MAPBGA	256 MAPBGA
VSSA_ADC	—	—	—	—	—	—	vssint	—	H5
VDDA_DAC_ADC	—	—	—	—	—	—	vddint	—	J4
VSSA_DAC_ADC	—	—	—	—	—	—	vssint	—	J5
VSTBY[24]	—	—	—	—	—	—	vddint	E14	E16
VSS	—	—	—	—	—	—	—	A1, A14, D8, D14, E8, F8, G4, G8, G9, G11, H4, H8–11, J7–11, J14, K5, K6, K11, P1, P14	A1, A16, D16, E8, F7, F8, G6–G11, H6, H7, H9–H11, J6, J11, J12, K12, L4, L7–L12, M5, M6, T1, T16

1 All pins available with GPIO contain a configurable pull-up/down. This column indicates the pull devices that are enabled automatically at reset. Pull-ups are generally only enabled on pins with their primary function, except as noted.

2 Refers to pin's primary function.

3 For details on the available slew rates of the various pad types see section "Output Pad Loading and Slew Rate" of the *MCF5441x Data Sheet* or section "Slew Rate Control Registers (SRCR_x)" in chapter "Pin-Multiplexing and Control" of the *MCF5441x Reference Manual.*

4 Enabled as input only in oscillator bypass mode (internal crystal oscillator is disabled).

5 These pins are time-division multiplexed between the FlexBus and NFC. An arbitration mechanism determines which module drives these pins at any point in time.

6 An internal pulldown circuit is enabled during system reset for FB_AD[10].

7 An internal pullup circuit is enabled when the system is in reset state.

8 Configurable pull that is enabled and pulled up after reset.

9 When configured for FB_A1, this pin is time-division multiplexed between the FlexBus and NFC. An arbitration mechanism determines which module drives the pin at any point in time. When not configured as FB_A1, NFC_ALE cannot be used.

10 When configured for FB_A0, this pin is time-division multiplexed between the FlexBus and NFC. An arbitration mechanism determines which module drives the pin at any point in time. When not configured as FB_A0, NFC_CLE cannot be used.

11 Since USB_CLKIN is a clock signal, it must be dedicated to the USB system. Do not implement this pin as dual-use.

12 When Alternate 2 is selected, then internal pullup/pulldown control will come from the MISCCR[3] register of CIM.

13 When booting from serial boot flash, the SBF function is enabled automatically. After the SBF function completes its reset sequence, the signals are returned to GPIO functionality.

14 Automatic pull-up when SBF controls the pin during reset only. Configurable pull when UART, DSPI, or SDHC control the pin.

15 If ULPI is enabled, ULPI_DIR is available as the Alternate 2 function. If ULPI is disabled, USBO_VBUS_EN is available.

16 If ULPI is enabled, ULPI_NXT is available as the Alternate 2 function. If ULPI is disabled, USBO_VBUS_OC is available.

17 When Alternate 2 is selected, then internal pullup/pulldown control will come from the MISCCR[2] register of CIM.

18 UART*x*_TXD pad can act as RXD(input) pad when UART One Wire mode is enabled.

19 The SIM1 signals are available with 256 MAPBGA but are not available with 196 MAPBGA.

20 These RMII functions are selected by the mode chosen by the MAC-NET, not by the pin-multiplexing and control (GPIO) module.

4.2 Thermal characteristics

Table 7. Thermal characteristics

Characteristic		Symbol	196 MAPBGA	256 MAPBGA	Unit
Junction to ambient, natural convection[1]	Single layer board (1s)[2]	θ_{JA}	58	—	
	Four layer board (2s2p)[2,3]	θ_{JA}	35	32	°C/W
Junction to ambient (@200 ft/min)[1, 3]	Single layer board (1s)	θ_{JMA}	48	—	
	Four layer board (2s2p)	θ_{JMA}	32	29	°C/W
Junction to board[4]		θ_{JB}	22	22	°C/W
Junction to case[5]		θ_{JC}	14	12	°C/W
Junction to top of package, natural convection[1, 6]		Ψ_{jt}	3	2	°C/W
Maximum operating junction temperature		T_j	105	105	°C

1 θ_{JA} and Ψ_{jt} parameters are simulated in conformance with EIA/JESD Standard 51-2 for natural convection. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.

2 Per JEDEC JESD51-2 with the single layer board horizontal. Board meets JESD51-9 specification.

3 Per JEDEC JESD51-6 with the board horizontal.

4 Thermal resistance between the die and the printed circuit board in conformance with JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

5 Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).

6 Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written in conformance with Psi-JT.

The average chip-junction temperature (T_J) in °C can be obtained from:

$$T_J = T_A + (P_D \times \Theta_{JMA}) \quad \textit{Eqn. 1}$$

Where:

T_A = Ambient Temperature, °C
Q_{JMA} = Package Thermal Resistance, Junction-to-Ambient, °C/W
P_D = $P_{INT} + P_{I/O}$
P_{INT} = $I_{DD} \times IV_{DD}$, Watts - Chip Internal Power
$P_{I/O}$ = Power Dissipation on Input and Output Pins — User Determined

For most applications $P_{I/O} < P_{INT}$ and can be ignored. An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$$P_D = \frac{K}{(T_J + 273°C)} \quad \textit{Eqn. 2}$$

Solving equations 1 and 2 for K gives:

$$K = P_D \times (T_A \times 273°C) + Q_{JMA} \times P_D^2 \quad \textit{Eqn. 3}$$

where K is a constant pertaining to the particular part. K can be determined from Equation 3 by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving Equation 1 and Equation 2 iteratively for any value of T_A.

4.3 ESD protection

Table 8. ESD protection characteristics[1, 2]

Characteristics	Symbol	Value	Units
ESD Target for Human Body Model	HBM	2000	V

1 All ESD testing is in conformity with JESD22 Stress Test Qualification.

2 A device is defined as a failure if after exposure to ESD pulses the device no longer meets the device specification requirements. Complete DC parametric and functional testing is performed per applicable specification at room temperature followed by hot temperature, unless specified otherwise in the device specifications provided in this document.

4.4 Static latch-up (LU)

Two complementary static tests are required on six parts to assess the latch-up performance:

- A supply over voltage is applied to each power supply pin.
- A current injection is applied to each input, output, and configurable I/O pin.

These tests are compliant with the EIA/JESD 78 IC latch-up standard.

Table 9. Latch-up results

No.	Symbol		Parameter	Conditions	Class
1	LU	CC	Static latch-up class	T_A = 125 °C conforming to JESD 78	II level A

4.5 DC electrical specifications

Table 10. Power supply specifications

Characteristic	Symbol	Pin Name	Min	Max	Units
Internal logic supply voltage, nominal 1.2 V	IV_{DD}	IVDD	1.14	1.32	V
FlexBus supply voltage Nominal 1.8–3.3 V	FBV_{DD}	FB_VDD	1.71	3.63	V
SDRAM supply voltage DDR2 @ 1.8 V	SDV_{DD}	SD_VDD	1.71	1.98	V
SDRAM input reference voltage	SDV_{REF}	SD_VREF	0.49 x SDV_{DD}	0.51 x SDV_{DD}	V
SDRAM termination supply voltage	SDV_{TT}	SD_VTT	SDV_{REF} – 0.04	SDV_{REF} + 0.04	V
PLL analog operation voltage range, nominal 3.3 V	PV_{DD}	VDD_OSC_A_PLL	3.135	3.63	V

Table 11. I/O electrical specifications (continued)

Characteristic	Symbol	Min	Max	Units
Weak internal pull-up/pull-down device current[1]	I_{APU}	10	315	µA
Selectable weak internal pull-up/pull-down device current[1]	I_{APU}	25	150	µA
Input capacitance [2] All input-only pins All input/output (three-state) pins	C_{in}	 — —	 7 7	pF
Output loading for CMOS pads (EV_{DD} and FBV_{DD} domains) Low drive High drive	C_L		 50 200	pF
Output loading for SDRAMC pads (SDV_{DD} domain) Low drive High drive	C_L		 5 50	pF

1 Refer to the signals section for pins having weak internal pull-up devices.
2 This parameter is characterized before qualification rather than 100% tested.

4.6 Output pad loading and slew rate

The output pins on the MCF5441x devices have programmable slew rates. Table 12 lists the rise/fall time for pins based on the type of pad used for the signal, the value programmed into the appropriate field of the slew rate control registers, and capacitive loading. Refer to Table 5 for a list of the external signals to pad connections.

NOTE

To allow the I/O interfaces to run at their maximum frequency, set their respective slew rate select values to 11.

Table 12. Output pad slew rates

Pad type[1]	Slew rate select field value	Drive load (pF)	Rise/fall time (ns)
ssr	11	50	2.2
		200	6
	10	50	22
		200	28
	01	50	42
		200	50
	00	50	210
		200	220

Table 17. NFC timing specifications (continued)

Num	Characteristic	Symbol	Min	Max	Unit
NF7	NFC_ALE setup time	t_{ALS}	$1.5 \times t_{NFC}$	—	ns
NF8	NFC_ALE hold time	t_{ALH}	t_{NFC}	—	ns
NF9	Data setup time	t_{DS}	$0.5 \times t_{NFC} - 4$	—	ns
NF10	Data hold time	t_{DH}	$0.5 \times t_{NFC} - 10$	—	ns
NF11	Write cycle time	t_{WC}	t_{NFC}	—	ns
NF12	$\overline{\text{NFC\_WE}}$ high hold time	t_{WH}	$0.5 \times t_{NFC} - 1$	—	ns
NF13	Ready to $\overline{\text{NFC\_RE}}$ low	t_{RR}	$4.5 \times t_{NFC}$	—	ns
NF14	$\overline{\text{NFC\_RE}}$ pulse width	t_{RP}	$0.5 \times t_{NFC} - 0.5$	—	ns
NF15	Read cycle time	t_{RC}	t_{NFC}	—	ns
NF16	$\overline{\text{NFC\_RE}}$ high hold time	t_{REH}	$0.5 \times t_{NFC} - 1$	—	ns
NF17	Data in setup time	t_{DSU}	6	—	ns

[1] 50 MHz maximum frequency can only be used if the part is in EDO (enhanced data out) mode.

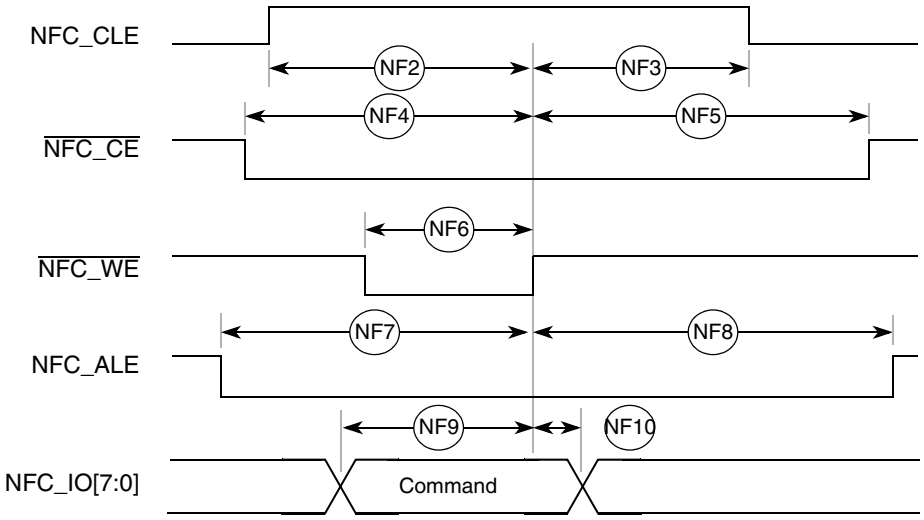

Figure 13. Command latch cycle timing

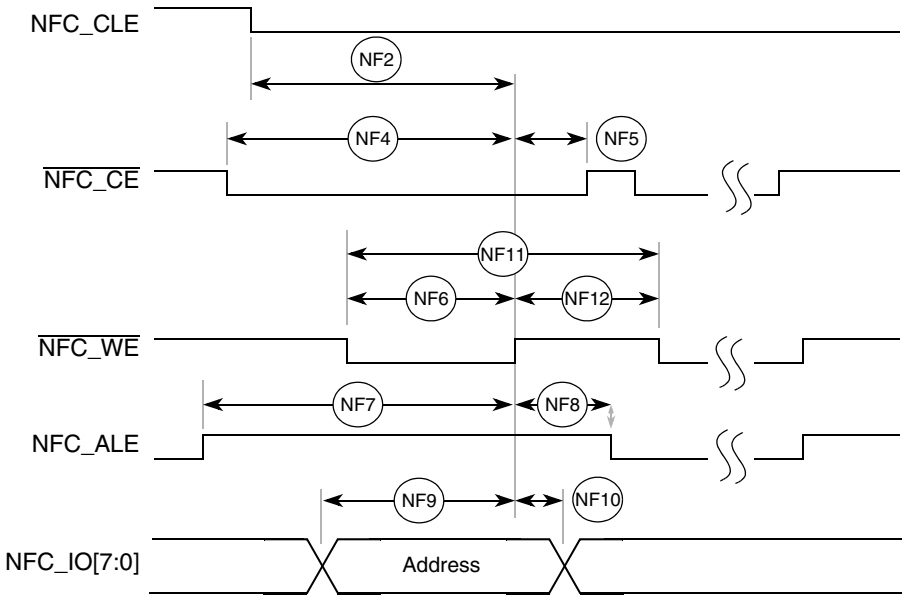

Figure 14. Address latch cycle timing

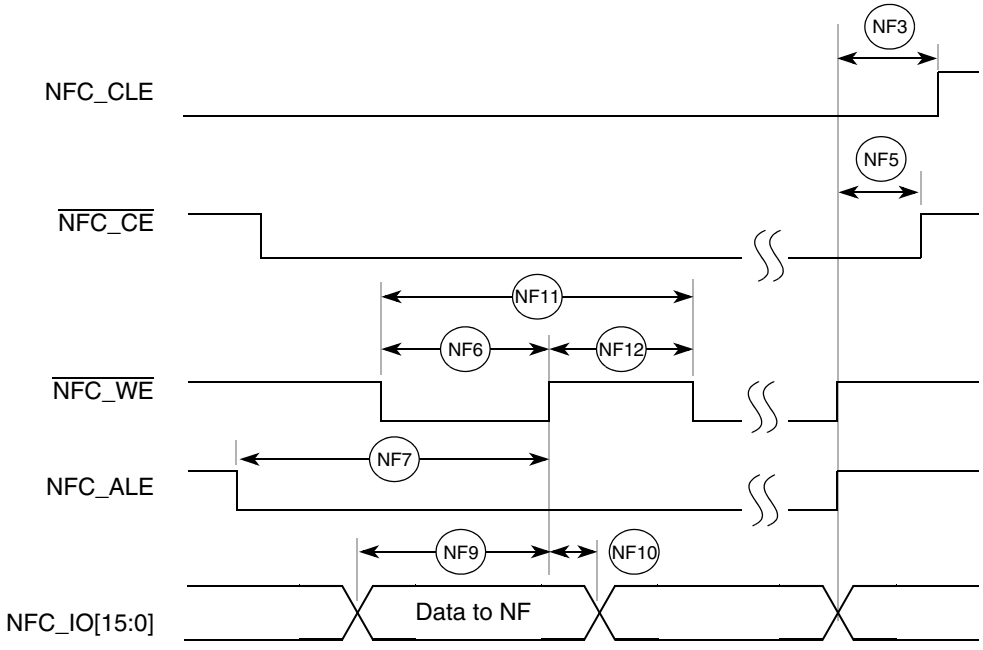

Figure 15. Write data latch timing

4.15.2 eSDHC electrical DC characteristics

Table 21 lists the eSDHC electrical DC characteristics.

Table 21. MMC/SD interface electrical specifications

Num	Parameter	Design value	Min	Max	Unit	Condition/remark
Bus signal line load						
7	Pull-up resistance	47	10	100	kΩ	Internal PU
8	Open drain resistance	NA	NA	NA	kΩ	For MMC cards only
Open drain signal level						For MMC cards only
9	Output high voltage		V_{DD} – 0.2		V	I_{OH} = –100 µA
10	Output low voltage			0.3	V	I_{OL} = 2 mA
Bus signal levels						
11	Output high voltage		0.75 x V_{DD}		V	I_{OH} = –100 µA @V_{DD} min
12	Output low voltage			0.125 x V_{DD}	V	I_{OL} = 100 µA @V_{DD} min
13	Input high voltage		0.625 x V_{DD}	V_{DD} + 3	V	
14	Input low voltage		V_{SS} – 0.3	0.25 x V_{DD}	V	

4.16 SIM timing specifications

Each SIM card interface consist of a total of 12 pins (two separate ports of six pins each. Mostly one port with 5 pins is used).

The interface is meant to be used with synchronous SIM cards. This means that the SIM module provides a clock for the SIM card to use. The frequency of this clock is normally 372 times the data rate on the TX/RX pins, however SIM module can work with CLK equal to 16 times the data rate on TX/RX pins.

There is no timing relationship between the clock and the data. The clock that the SIM module provides to the SIM card is used by the SIM card to recover the clock from the data, like a standard UART. All six (or five when a bidirectional TXRX is used) of the pins for each half of the SIM module are asynchronous to each other. There are no required timing relationships between the signals in normal mode. However, there are some in reset and power down sequences.

All SIM signals use pad type pad_msr. SIM timing is fairly relaxed compared to other interfaces and can be met at 50 pF loading with any slew rate setting other than 00.[1]

1.These timing parameters are specified assuming maximum operating frequency and the fastest pad slew rate setting (11). When operating this interface at lower frequencies, increase the slew rate by using the 10, 01, or 00 setting to increase edge rise and fall times, thus reducing EMI.

Table 23. Timing requirements for power-down sequence

Num	Description	Symbol	Min	Max	Unit
1	SIM reset to SIM clock stop	$S_{rst2clk}$	0.9 ÷ f_{CKIL}	0.8	µs
2	SIM reset to SIM TX data low	$S_{rst2dat}$	1.8 ÷ f_{CKIL}	1.2	µs
3	SIM reset to SIM voltage enable low	$S_{rst2ven}$	2.7 ÷ f_{CKIL}	1.8	µs
4	SIM presence detect to SIM reset low	S_{pd2rst}	0.9 ÷ f_{CKIL}	25	ns

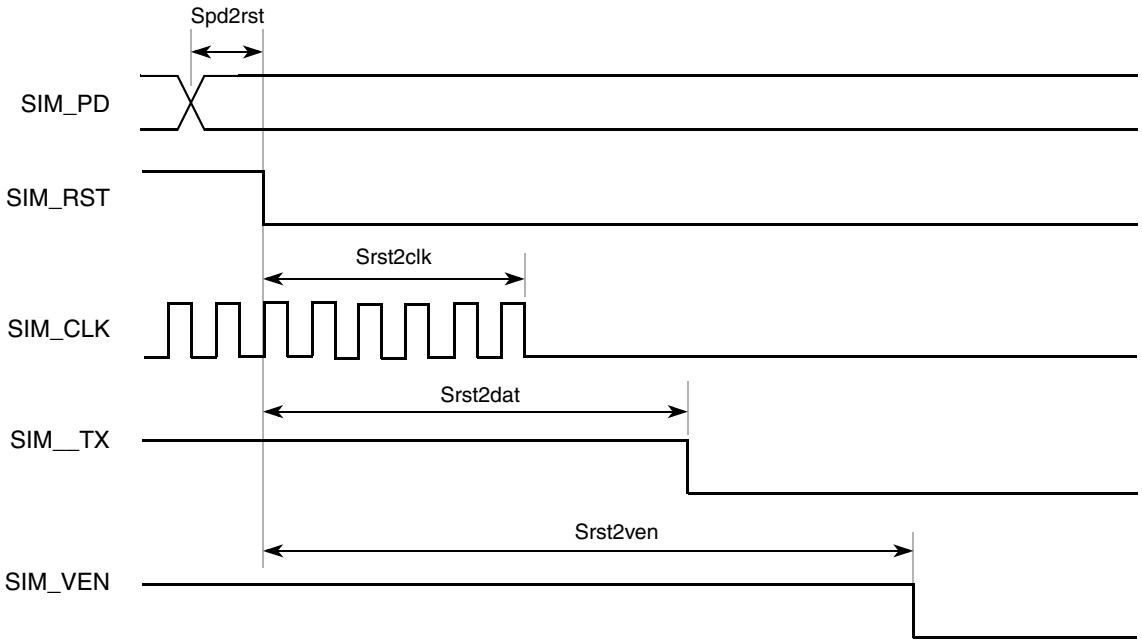

Figure 24. SmartCard interface power-down AC timing

4.17 SSI timing specifications

This section provides the AC timings for the SSI in master (clocks driven) and slave modes (clocks input). All timings are given for non-inverted serial clock polarity (SSI_TCR[TSCKP] = 0, SSI_RCR[RSCKP] = 0) and a non-inverted frame sync (SSI_TCR[TFSI] = 0, SSI_RCR[RFSI] = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timings remain valid by inverting the clock signal (SSI_BCLK) and/or the frame sync (SSI_FS) shown in the figures below.

All SSI signals use pad type pad_msr. The following timing specifications assume a pad slew rate setting of 11 and a load of 50 pF. When the SSI_MCLK output is not used, the maximum SSI bit clock (SSI_BCLK) frequency is such that timing can also be met at slew rate settings 10 and 01.[1]

1.These timing parameters are specified assuming maximum operating frequency and the fastest pad slew rate setting (11). When operating this interface at lower frequencies, increase the slew rate by using the 10, 01, or 00 setting to increase edge rise and fall times, thus reducing EMI.

Table 27. DAC parameters[1] (continued)

Characteristic	Name	Min	Typical	Max	Unit
Integral non-linearity (497 to 3599)	INL	—	—	±8.0	lsb
Differential non-linearity (497 to 3599)	DNL	—	—	±0.5	lsb
Gain error (497 to 3599)	E_{GAIN}	—	±0.26	—	%
Effective number of bits	ENOB	9	—	—	bits
DAC power-up time	t_{DAPU}	—	—	11	us
Output load resistance	R_L	3K	—	—	Ohm
Output load capacitance	C_L	—	400	—	pF
Power supply ripple rejection	PSRR	—	60	—	dB

[1] All measurements were made at V_{DD} = 3.3V, V_{REFH} = 3.3V, and V_{REFL} = ground

4.20 mcPWM timing specifications

Table 28. mcPWM timing

Num	Characteristic	Min	Max	Unit
G1	FB_CLK high to output valid	—	7	ns
G2	FB_CLK high to output invalid	1	—	ns
G3	Input valid to FB_CLK high	3	—	ns
G4	FB_CLK high to input invalid	1	—	ns

4.21 I^2C timing specifications

Table 29 lists specifications for the I^2C input timing parameters shown in Figure 27.

Table 29. I^2C input timing specifications between SCL and SDA

Num	Characteristic	Min	Max	Units
I1	Start condition hold time	2	—	$1/f_{SYS}$
I2	Clock low period	8	—	$1/f_{SYS}$
I3	I2C_SCL/I2C_SDA rise time (V_{IL} = 0.5 V to V_{IH} = 2.4 V)	—	1	ms
I4	Data hold time	0	—	ns
I5	I2C_SCL/I2C_SDA fall time (V_{IH} = 2.4 V to V_{IL} = 0.5 V)	—	1	ms
I6	Clock high time	4	—	$1/f_{SYS}$
I7	Data setup time	0	—	ns
I8	Start condition setup time (for repeated start condition only)	2	—	$1/f_{SYS}$
I9	Stop condition setup time	2	—	$1/f_{SYS}$

Table 30 lists specifications for the I^2C output timing parameters shown in Figure 27.

4.22.1 Receive signal timing specifications

The following timing specs meet the requirements for MII and RMII interfaces for a range of transceiver devices.

Table 31. Receive signal timing

Num	Characteristic	MII mode		RMII mode		Unit
		Min	Max	Min	Max	
—	RXCLK frequency	—	25	—	50	MHz
E1	RXD[n:0], RXDV, RXER to RXCLK setup[1]	5	—	4	—	ns
E2	RXCLK to RXD[n:0], RXDV, RXER hold[1]	5	—	2	—	ns
E3	RXCLK pulse width high	35%	65%	35%	65%	RXCLK period
E4	RXCLK pulse width low	35%	65%	35%	65%	RXCLK period

1 In MII mode, n = 3; In RMII mode, n = 1

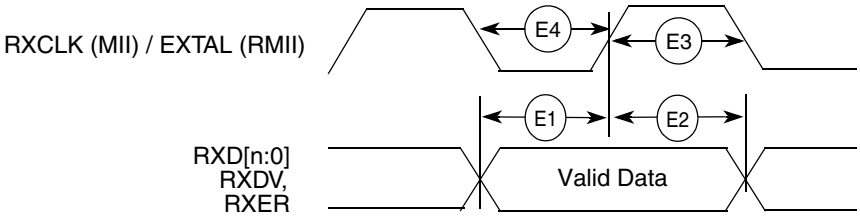

Figure 28. MII/RMII receive signal timing diagram

4.22.2 Transmit signal timing specifications

Table 32. Transmit signal timing

Num	Characteristic	MII mode		RMII mode		Unit
		Min	Max	Min	Max	
—	TXCLK frequency	—	25	—	50	MHz
E5	TXCLK to TXD[n:0], TXEN, TXER invalid[1]	4	—	5	—	ns
E6	TXCLK to TXD[n:0], TXEN, TXER valid[1]	—	25	—	14	ns
E7	TXCLK pulse width high	35%	65%	35%	65%	t_{TXCLK}
E8	TXCLK pulse width low	35%	65%	35%	65%	t_{TXCLK}

1 In MII mode, n = 3; In RMII mode, n = 1

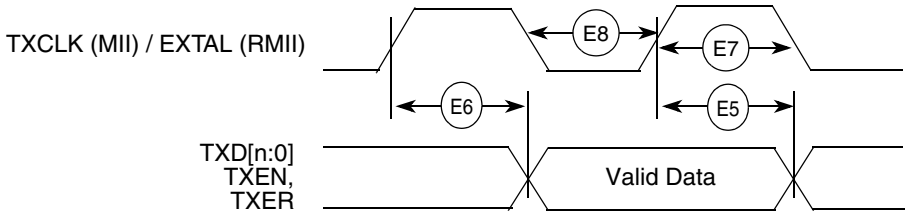

Figure 29. MII/RMII transmit signal timing diagram

4.22.3 Asynchronous input signal timing specifications

Table 33. MII/RMII transmit signal timing

Num	Characteristic	Min	Max	Unit
E9	CRS, COL minimum pulse width	1.5	—	TXCLK period

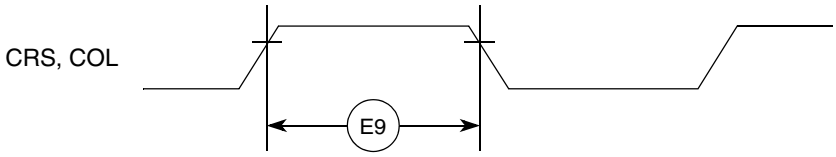

Figure 30. MII/RMII async inputs timing diagram

4.22.4 MDIO serial management timing specifications

Table 34. MDIO serial management channel signal timing

Num	Characteristic	Symbol	Min	Max	Unit
E10	MDC cycle time	t_{MDC}	400	—	ns
E11	MDC pulse width		40	60	% t_{MDC}
E12	MDC to MDIO output valid		—	375	ns
E13	MDC to MDIO output invalid		25	—	ns
E14	MDIO input to MDC setup		10	—	ns
E15	MDIO input to MDC hold		0	—	ns

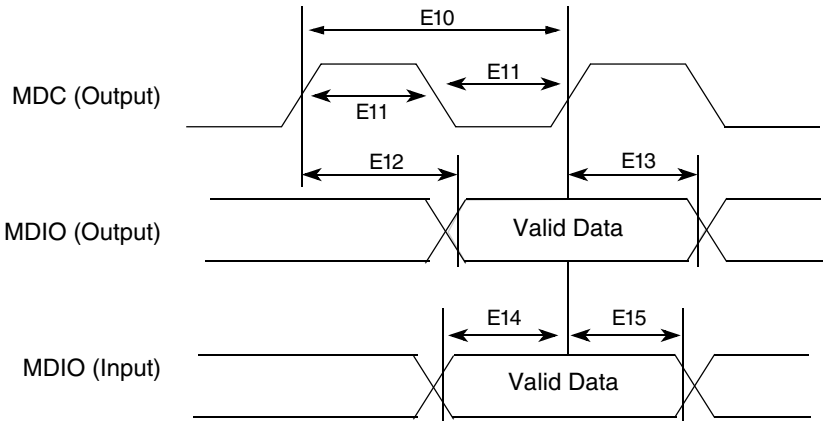

Figure 31. MDIO serial management channel timing diagram

4.23 32-bit timer module timing specifications

Table 35 lists timer module AC timings.

Table 35. Timer module AC timing specifications

Name	Characteristic	Min	Max	Unit
T1	DT*n*IN cycle time (*n* = 0:3)	3	—	$1/f_{SYS/2}$
T2	DT*n*IN pulse width (*n* = 0:3)	1	—	$1/f_{SYS/2}$

4.24 DSPI timing specifications

The DMA Serial Peripheral Interface (DSPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. Table 36 provides DSPI timing characteristics for classic SPI timing modes. Refer to the DSPI chapter of the *MCF54418 Reference Manual* for information on the modified transfer formats used for communicating with slower peripheral devices.

All DSPI signals use pad type pad_msr. The following timing specifications assume a pad slew rate setting of 11 and a load of 50 pF.[1]

Table 36. DSPI module AC timing specifications[1]

Name	Characteristic	Symbol	Min	Max	Unit	Notes
Master Mode						
—	DSPI_SCK frequency	f_{SCK}	—	50	MHz	
DS1	DSPI_SCK cycle time	t_{SCK}	20	—	ns	2
DS2	DSPI_SCK duty cycle	—	$(t_{sck} \div 2) - 2.0$	$(t_{sck} \div 2) + 2.0$	ns	3
DS3	DSPI_PCS*n* to DSPI_SCK delay	t_{CSC}	$(t_{sck} \div 2) - 2.0$	—	ns	4
DS4	DSPI_SCK to DSPI_PCS*n* delay	t_{ASC}	$(t_{sck} \div 2) - 3.0$	—	ns	5
DS5	DSPI_SCK to DSPI_SOUT valid	—	—	5	ns	

1.These timing parameters are specified assuming maximum operating frequency and the fastest pad slew rate setting (11). When operating this interface at lower frequencies, increase the slew rate by using the 10, 01, or 00 setting to increase edge rise and fall times, thus reducing EMI.

Table 36. DSPI module AC timing specifications[1] (continued)

Name	Characteristic	Symbol	Min	Max	Unit	Notes
DS6	DSPI_SCK to DSPI_SOUT invalid	—	–5	—	ns	
DS7	DSPI_SIN to DSPI_SCK input setup	—	6	—	ns	
DS8	DSPI_SCK to DSPI_SIN input hold	—	0	—	ns	
Slave Mode						
—	DSPI_SCK frequency	f_{SCK}	—	$f_{SYS} \div 8$	MHz	
DS9	DSPI_SCK cycle time	t_{SCK}	$8 \div f_{SYS}$	—	ns	
DS10	DSPI_SCK duty cycle	—	$(t_{sck} \div 2) - 2.0$	$(t_{sck} \div 2) + 2.0$	ns	
DS11	DSPI_SCK to DSPI_SOUT valid	—	—	12	ns	
DS12	DSPI_SCK to DSPI_SOUT invalid	—	0	—	ns	
DS13	DSPI_SIN to DSPI_SCK input setup	—	2	—	ns	
DS14	DSPI_SCK to DSPI_SIN input hold	—	7	—	ns	
DS15	$\overline{\text{DSPI\_SS}}$ active to DSPI_SOUT driven	—	—	10	ns	
DS16	$\overline{\text{DSPI\_SS}}$ inactive to DSPI_SOUT not driven	—	—	10	ns	

1 Timings shown are for DMCR[MTFE] = 0 (classic SPI) and DCTAR*n*[CPHA] = 0. Data is sampled on the DSPI_SIN pin on the odd-numbered DSPI_SCK edges and driven on the DSPI_SOUT pin on even-numbered DSPI edges.

2 When in master mode, the baud rate is programmable in DCTAR*n*[DBR], DCTAR*n*[PBR], and DCTAR*n*[BR].

3 This specification assumes a 50/50 duty cycle setting. The duty cycle is programmable in DCTAR*n*[DBR], DCTAR*n*[CPHA], and DCTAR*n*[PBR].

4 The DSPI_PCS*n* to DSPI_SCK delay is programmable in DCTAR*n*[PCSSCK] and DCTAR*n*[CSSCK].

5 The DSPI_SCK to DSPI_PCS*n* delay is programmable in DCTAR*n*[PASC] and DCTAR*n*[ASC].

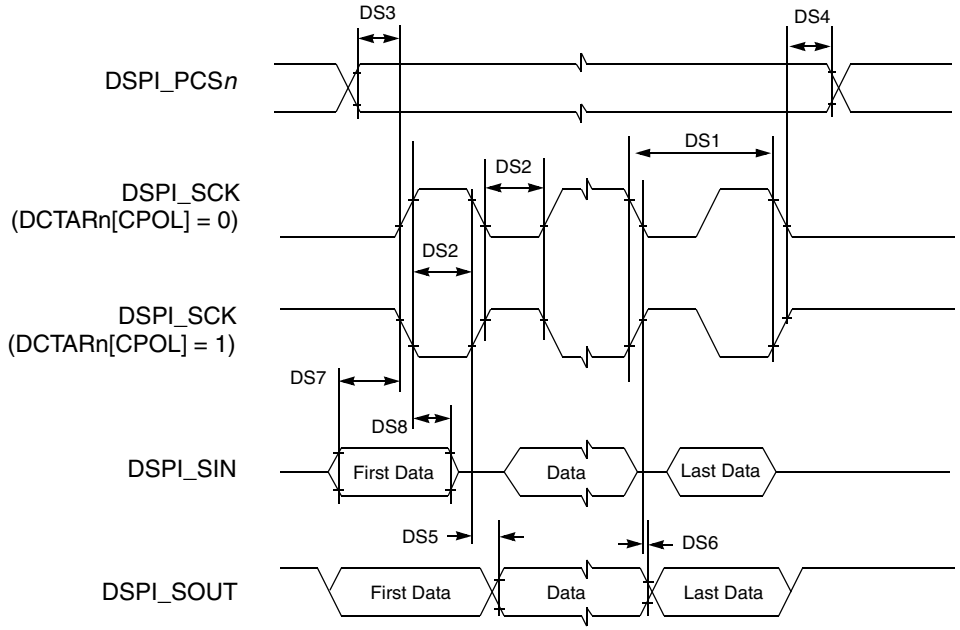

Figure 32. DSPI Classic SPI timing — master Mode

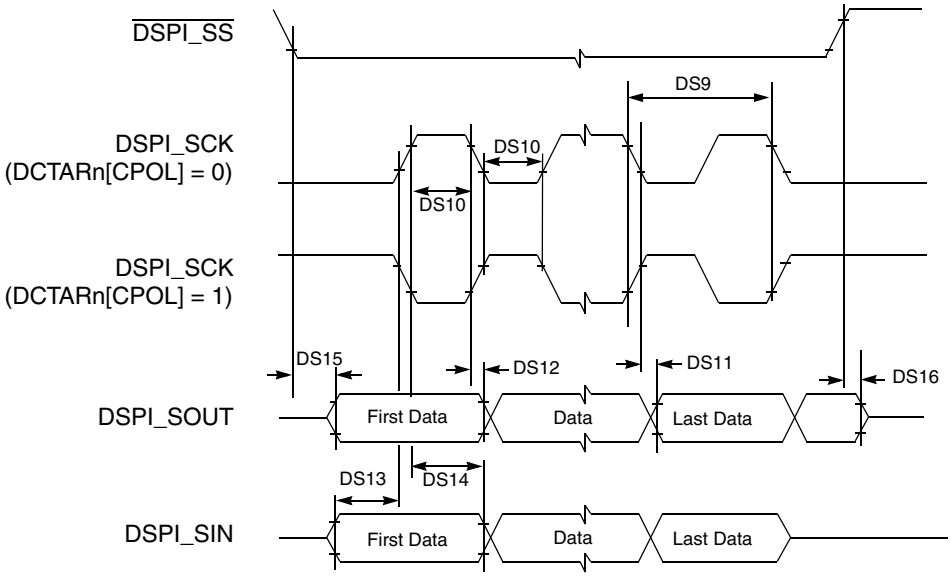

Figure 33. DSPI Classic SPI timing — slave mode

4.30 Debug AC timing specifications

Table 41 lists specifications for the debug AC timing parameters shown in Figure 41 and Table 42.

All debug signals use pad type pad_msr except for PSTCLK which use pad type pad_fsr. The following timing specifications assume a pad slew rate setting of 11 and a load of 50 pF.[1]

Table 41. Debug AC timing specification

Num	Characteristic	Min	Max	Units
D0	PSTCLK cycle time	0.5	0.5	$1/f_{SYS}$
D1	PSTCLK rising to PSTDDATA valid	—	3.0	ns
D2	PSTCLK rising to PSTDDATA invalid	0.5	—	ns
D3	DSI-to-DSCLK setup	1	—	PSTCLK
D4[1]	DSCLK-to-DSO hold	4	—	PSTCLK
D5	DSCLK cycle time	5	—	PSTCLK
D6	BKPT assertion time	1	—	PSTCLK

1 DSCLK and DSI are synchronized internally. D4 is measured from the synchronized DSCLK input relative to the rising edge of PSTCLK.

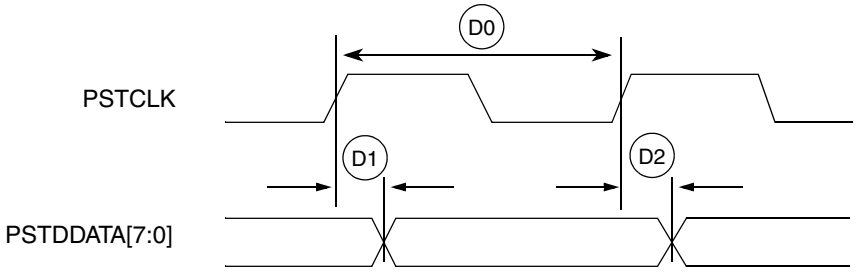

Figure 41. Real-time trace AC timing

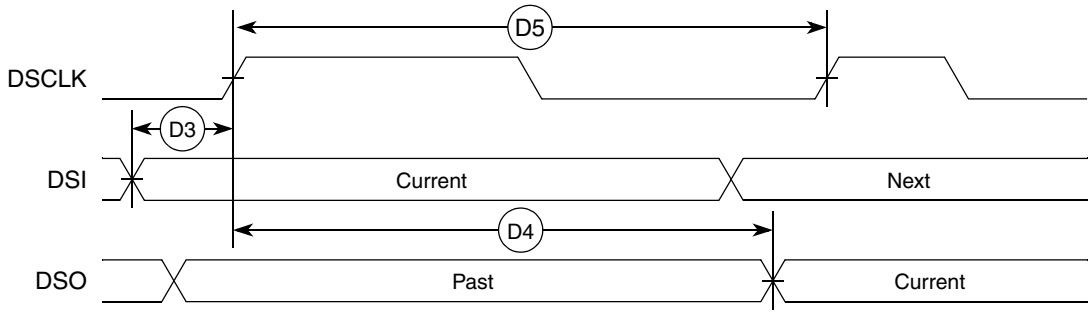

Figure 42. BDM serial port AC timing

1.These timing parameters are specified assuming maximum operating frequency and the fastest pad slew rate setting (11). When operating this interface at lower frequencies, increase the slew rate by using the 10, 01, or 00 setting to increase edge rise and fall times, thus reducing EMI.

7 Revision history

Table 43 summarizes revisions to this document.

Table 43. Revision history

Rev. No.	Date	Summary of changes
2	10 Jun 2009	In Section 2.2, "Supply voltage sequencing" added the following note: **NOTE** All I/O VDD pins must be powered on when the device is functioning, except when in standby mode. In standby mode, all I/O VDD pins, except VSTBY_RTC (battery), can be switched off. Added Section 3.2, "Pinout—169 MAPBGA" and Section 3.3, "Pinout—256 MAPBGA" and updated Table 5 with pin locations. In Section 4.1, "Absolute maximum ratings": • Added USB OTG, USB host, ADC, DAC/ADC, and RTC standby supply voltages In Section 4.5, "DC electrical specifications": • Added RTC standby supply voltage • Split out Power Supplies and I/O Characteristics to two separate tables In Section 4.10, "FlexBus timing specifications": • Changed maximum frequency to 100MHz and updated specs throughout the table • Changed FB2 maximum from 5 to 6 • Added notes to Figure 11 and Figure 12 In Section 4.12, "DDR SDRAM controller timing specifications": • Changed minimum frequency from 50 to 100 • Changed maximum DD1 from 20 to 10 • Changed DD5 from 2 to 0.5 x t_{SDCK} – 1 • Changed DD6 from 1.2 x t_{SDCK} to WL + 0.2 x t_{SDCK} • Changed DD7 from 1.5 to 0.7 • Changed DD8 from 1.0 to 0.7 • Changed DD9 from 1.0 to 0.5 • Changed DD10 from 0.25 x t_{SDCK} + 0.5 to 0.375 x t_{SDCK} In Section 4.17, "SSI timing specifications": • Changed S7, S9, S15, and S17 from 10 to 15 In Section 4.22.2, "Transmit signal timing specifications": • Changed E5 for MII from 5 to 4 In Section 4.20, "mcPWM timing specifications": • Changed G2 from 2 to 1 In Section 4.24, "DSPI timing specifications": • Changed DS3 from (2 x 1/fsys) – 2.0 to (t_{sck} ³ 2) – 2.0 • Changed DS4 from (2 x 1/fsys) – 3.0 to (t_{sck} ³ 2) – 3.0 • Changed DS7 from 7 to 6 • Changed DS11 from 4 to 12 In Section 4.25, "SBF timing specifications": • Changed SB5 maximum from 5 to 3 • Changed SB6 minimum from –5 to 5 In Section 4.26, "1-Wire timing specifications": • Added link to 1-wire specs In Section 4.27, "General purpose I/O timing specifications": • Changed G2 from 1.5 to 1 In Section 4.28, "Rapid general purpose I/O timing specifications": • Changed RG1 from 3 to 6 • Changed RG2 from 1.5 to 0.5 • Changed RG3 from 3 to 6 In Section 4.29, "JTAG and boundary scan timing specifications": • Changed J9-12 and J14 from TBD In Section 4.30, "Debug AC timing specifications": • Changed D2 from 1.5 to 0.5