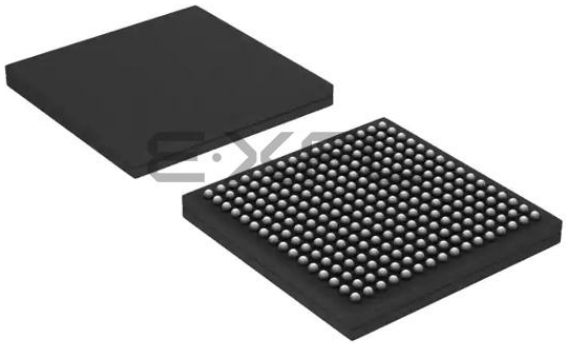

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	Coldfire V4
Core Size	32-Bit Single-Core
Speed	250MHz
Connectivity	1-Wire®, CANbus, EBI/EMI, Ethernet, I²C, SmartCard, SPI, SSI, UART/USART, USB, USB OTG
Peripherals	DMA, PWM, WDT
Number of I/O	87
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	1.14V ~ 1.32V
Data Converters	A/D 8x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	256-LBGA
Supplier Device Package	256-MAPBGA (17x17)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mcf54417cmj250

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1 MCF5441*x* family comparison

Table 1. MCF5441*x* family configurations

Module	MCF54410	MCF54415	MCF54416	MCF54417	MCF54418
Version 4 ColdFire core with EMAC (enhanced multiply-accumulate unit) and MMU (memory management unit)	•	•	•	•	•
Cryptography acceleration unit (CAU)	—	—	•	—	•
Core (system) and SDRAM clock	up to 250 MHz				
Peripheral clock (Core clock ÷ 2)	up to 125 MHz				
External bus (FlexBus) clock	up to 100 MHz				
Performance (Dhrystone 2.1 MIPS)	up to 385				
Static RAM (SRAM)	64 KB				
Independent data/instruction cache	8 KB each				
USB 2.0 Host controller	—	•	•	•	•
USB 2.0 Host/Device/On-the-Go controller	•	•	•	•	•
UTMI+ Low Pin Interface (ULPI) for external high-speed USB PHY	—	•	•	•	•
10/100 Mbps Ethernet controller with IEEE 1588 support	1	2	2	2	2
Level 2 IEEE 1588-compliant 3-port Ethernet switch	—	—	—	•	•
Enhanced Secure Digital host controller (eSDHC)	•	•	•	•	•
Smart card/Subscriber Identity Module (SIM)	—	2 ports	2 ports	2 ports	2 ports
UARTs	6	10	10	10	10
DSPI	3	4	4	4	4
CAN 2.0B controllers	1	2	2	2	2
I^2C	4	6	6	6	6
Synchronous serial interface (SSI)	1	2	2	2	2
12-bit ADC	—	•	•	•	•
12-bit DAC	—	2	2	2	2
32-bit DMA timers	4	4	4	4	4
Periodic interrupt timers (PIT)	4	4	4	4	4
Motor control PWM timer (mcPWM)	—	8 channel	8 channel	8 channel	8 channel
64-channel DMA controller	•	•	•	•	•
Real-time clock with 2 KB standby RAM and battery back-up input	•	•	•	•	•
DDR2 SDRAM controller	•	•	•	•	•
FlexBus external memory controller	•	•	•	•	•

Figure 5 shows an example for bypassing the FlexBus power supply for the MPU. This bypass should be applied to as many FB_VDD signals as routing allows. Each one should be placed as close to the ball as possible.

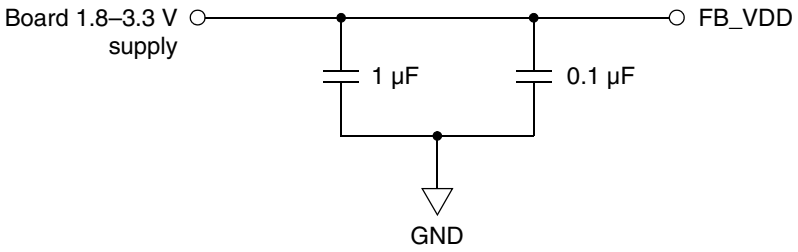
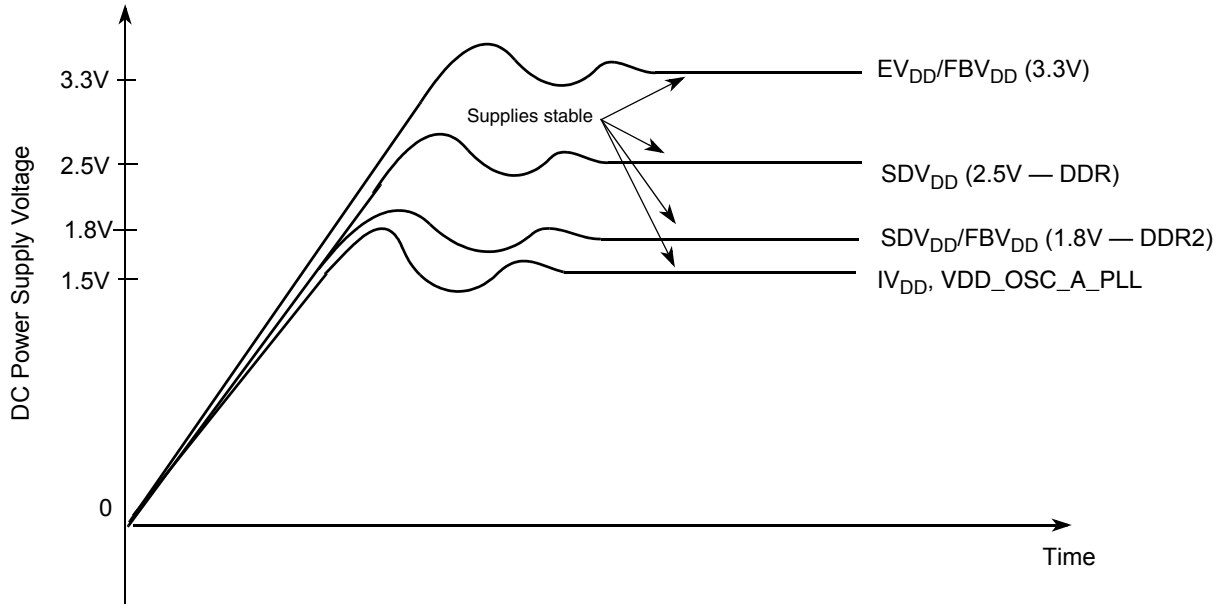


Figure 5. FB_VDD power filter

2.2 Supply voltage sequencing

Figure 6 shows requirements in the sequencing of the I/O V_{DD} (EV_{DD}), FlexBus V_{DD} (FBV_{DD}), SDRAM V_{DD} (SDV_{DD}), PLL V_{DD} (VDD_OSC_A_PLL), and internal logic/core V_{DD} (IV_{DD}).



Notes:
1 Input voltage must not be greater than the supply voltage (EV_{DD}, FBV_{DD}, SDV_{DD}, IV_{DD}, or PV_{DD}) by more than 0.5V at any time, including during power-up.
2 Use 25 V/millisecond or slower rise time for all supplies.

Figure 6. Supply voltage sequencing and separation cautions

The relationships between FBV_{DD}, SDV_{DD} and EV_{DD} are non-critical during power-up and power-down sequences. FBV_{DD} (1.8 – 3.3V), SDV_{DD} (2.5V or 1.8V) and EV_{DD} are specified relative to IV_{DD}.

NOTE

All I/O VDD pins must be powered on when the device is functioning, except when in standby mode.

In standby mode, all I/O VDD pins, except VSTBY_RTC (battery), can be switched off.

Table 4. Special-case default signal functionality

Pin	Default signal
FB_CLK, FB_OE, FB_R/W, FB_BE/BWE[1:0], FB_CS[5:4]	FB_CLK, FB_OE, FB_R/W, FB_BE/BWE[1:0], FB_CS[5:4]
FB_ALE	FB_ALE or FB_TS (depending on RCON[3])
FB_BE/BWE3	Boot from NFC, NF_ALE. Otherwise, FB_BE/BWE3.
FB_BE/BWE2	Boot from NFC, NF_CLE. Otherwise, FB_BE/BWE2.
FB_CS1	Boot from NFC, NFC_CE. Otherwise, GPIO.
FB_CS0	Boot from FlexBus, FB_CS0. Otherwise, GPIO.
FB_TA	Boot from NFC, NFC_R/B. Otherwise, FB_TA.
ALLPST, PST[3:0], DDATA[3:0]	ALLPST, PST[3:0], DDATA[3:0]

NOTE

While most modules and functionalities between the 196 and 256 MAPBGA package are the same, the following modules have been removed from 196 MAPBGA for pin space:

UART2, UART6, UART9, PWM, SSI1, SIM1, USB HOST, IRQ6, IRQ3, IRQ2, FLEXCAN1, I2C1, ADC, DAC.

Other modifications to the 196 MAPBGA package are:

- SDRAMC — One address line, SD_A14, is removed.
- SDHC — Number of data lines for eSDHC have been reduced to 4 instead of 8.
- MAC — Only MAC0_RMII mode is implemented.

Table 5. MCF5441*x* Signal information and muxing

Signal name	GPIO	Alternate 1	Alternate 2	Pullup (U)[1] Pulldown (D)	Direction[2]	Voltage domain	Pad type[3]	196 MAPBGA	256 MAPBGA
Reset									
RESET	—	—	—	U	I	EVDD	ssr	K14	K15
RSTOUT	—	—	—	—	O	EVDD	msr	P12	L16
Clock									
EXTAL/ RMII_REF_CLK	—	—	—	—	I[4]	EVDD	ae	G14	G16

[21] Configurable pull that is enabled and pulled down after reset.

[22] The ALLPST signal is available only on the 196 MAPBGA package and allows limited debug trace functionality compared to the 256 MAPBGA package.

[23] If JTAG_EN is asserted, these pins default to Alternate 1 (JTAG) functionality. The GPIO module is not responsible for assigning these pins.

[24] VSTBY is for optional standby lithium battery. If not used, connect to EVDD.

3.2 Pinout—196 MAPBGA

The pinout for the MCF54410 package is shown below.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	
A	GND	FB_AD10	FB_AD14	FB_AD16	FB_AD18	FB_AD19	FB_AD24	FB_AD27	FB_AD30	FB_AD31	SSI0_TXD	SSI0_MCLK	USB_DPLS	GND	A
B	FB_AD6	FB_AD9	FB_AD11	FB_AD13	FB_AD17	FB_AD20	FB_AD23	FB_AD26	FB_AD29	U1_RXD	U0_TXD	SSI0_RXD	USB_DMNS	RTC_EXTAL	B
C	FB_AD3	FB_AD5	FB_AD8	FB_AD12	FB_AD15	FB_AD21	FB_AD22	FB_AD25	FB_AD28	U1_TXD	U0_RXD	U0RTS_B	SSI0_FS	RTC_XTAL	C
D	FB_AD0	FB_AD2	FB_AD4	FB_AD7	FBVDD	FBVDD	FBVDD	GND	CVDD	CVDD	U1RTS_B	U1CTS_B	SSI0_BCLK	GND	D
E	FB_BE2_B	FB_ALE	FB_AD1	FBVDD	FBVDD	FBVDD	FBVDD	GND	CVDD	CVDD	IRQ4_B	U0CTS_B	IRQ1_B	VSTBY	E
F	FB_BE0_B	FB_BE1_B	FB_BE3_B	EVDD	EVDD	EVDD	EVDD	GND	CVDD	CVDD	VDD_USBO	CVDD	VSS_OSC_A_PLL	VDD_OSC_A_PLL	F
G	FB_CLK	FB_CS0_B	FB_CS1_B	GND	BOOTMOD1	EVDD	EVDD	GND	GND	IRQ7_B	GND	I2C0_SDA	T3IN	EXTAL	G
H	FB_OE_B	FB_RW_B	FB_TA_B	GND	BOOTMOD0	EVDD	EVDD	GND	GND	GND	GND	I2C0_SCL	T1IN	XTAL	H
J	DSPI0_PCS0	DSPI0_SOUT	DSPI0_SCK	SD_BA1	EVDD	EVDD	GND	GND	GND	GND	GND	T2IN	T0IN	GND	J
K	SD_A1	DSPI0_SIN	DSPI0_PCS1	SD_CAS_B	GND	GND	SDVDD	SDVDD	SDVDD	TEST	GND	ALLPST	TMS	RSTIN_B	K
L	SD_A9	SD_A10	SD_A5	SD_A4	SDVDD	SDVDD	SDVDD	SD_VTT	TRST_B	TDI	RM110_TXD0	RM110_TXD1	TDO	TCLK	L
M	SD_A12	SD_A7	SD_A11	SD_RAS_B	SD_CS_B	SD_BA2	SD_D0	SD_D2	SD_D4	SD_D6	OWIO	RMII0_RXER	RMII0_CRS_DV	RMII0_MDIO	M
N	SD_A3	SD_A2	SD_A0	SD_A8	SD_WE_B	SD_CKE	SD_DQM	SD_D1	SD_VREF	SD_D5	JTAG_EN	RMII0_TXEN	RMII0_RXD0	RMII0_MDC	N
P	GND	SD_A6	SD_A13	SD_BA0	SD_ODT	SD_CLK	SD_CLK_B	SD_DQS	SD_DQS_B	SD_D3	SD_D7	RSTOUT_B	RMII0_RXD1	GND	P
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	

Figure 7. MCF54410 Pinout (196 MAPBGA)

3.3 Pinout—256 MAPBGA

The pinout for the MCF54415, MCF54416, MCF54417, and MCF54418 packages are shown below.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	
A	VSS	FB_AD3	FB_AD13	FB_AD14	FB_AD16	FB_AD20	FB_AD22	FB_AD26	FB_AD29	SDHC_CLK	SIM0_CLK	SSI0_MCLK	SSI0_BCLK	USBO_DM	USBH_DM	VSS	A
B	FB_CS4	FB_AD2	FB_AD8	FB_AD11	FB_AD15	FB_AD19	FB_AD24	FB_AD28	FB_AD31	UART0_RXD	UART0_RTS	SDHC_DAT0	SDHC_DAT3	USBO_DP	USBH_DP	RTC_EXTAL	B
C	FB_BE/BWE3	FB_AD1	FB_AD7	FB_AD9	FB_AD10	FB_AD17	FB_AD23	FB_AD30	UART1_RXD	UART1_CTS	SDHC_CMD	SSI0_RXD	SSI0_TXD	SIM0_PD	SIM0_RST	RTC_XTAL	C
D	FB_BE/BWE1	FB_ALE	FB_AD5	FB_AD12	FB_AD18	FB_AD21	FB_AD25	FB_AD27	UART1_TXD	UART1_RTS	UART0_TXD	SDHC_DAT1	SIM0_VEN	CAN1_TX	CAN1_RX	VSS	D
E	FB_CS1	FB_BE/BWE2	FB_AD4	FB_AD6	FB_VDD	FB_VDD	FB_VDD	VSS	IVDD	IVDD	IVDD	SIM0_XMT	UART0_CTS	SDHC_DAT2	SSI0_FS	VSTBY_RTC	E
F	FB_OE	FB_CS5	FB_AD0	FB_BE/BWE0	FB_VDD	FB_VDD	VSS	VSS	IVDD	IVDD	IVDD	IRQ7	IRQ1	IRQ4	VDD_OSC_A_PLL	VSS_OSC_A_PLL	F
G	FB_CLK	FB_R/W	FB_CS0	ADC_IN4	FB_VDD	VSS	VSS	VSS	VSS	VSS	VSS	VDD_USBO	T3IN	I2C0_SDA	I2C0_SCL	EXTAL	G
H	ADC_IN0	ADC_IN6	FB_TA	AVDD_ADC	AVSS_ADC	VSS	VSS	EVDD	VSS	VSS	VSS	VDD_USBH	T1IN	T2IN	T0IN	XTAL	H
J	ADC_IN1	ADC_IN2	ADC_IN5	VDDA_DAC_ADC	VSSA_DAC_ADC	VSS	EVDD	EVDD	EVDD	EVDD	VSS	VSS	PST3	PST0	PST1	PST2	J
K	DSPI0_SOUT	DSPI0_PCS0	ADC_IN7	ADC_IN3	BOOT MOD1	EVDD	EVDD	EVDD	EVDD	EVDD	EVDD	VSS	TRST	TDO	RESET	TMS	K
L	DSPI0_PCS1	DSPI0_SCK	DSPI0_SIN	VSS	BOOT MOD0	EVDD	VSS	VSS	VSS	VSS	VSS	VSS	TDI	DDATA0	DDATA3	RST OUT	L
M	IRQ3	IRQ2	UART2_RTS	UART2_CTS	VSS	VSS	SD_VDD	SD_VDD	SD_VDD	SD_VDD	SD_VDD	SD_VDD	DDATA2	MII0_RXCLK	DDATA1	TCLK	M
N	IRQ6	UART2_TXD	SD_A5	SD_A10	SD_A2	SD_BA1	SD_CS	SD_CAS	SD_D3	SD_VTT	OW_IO	MII0_TXD2	MII0_RXD2	MII0_RXER	JTAG_EN	MII0_MDIO	N
P	UART2_RXD	SD_A1	SD_A9	SD_A3	SD_A4	SD_A14	SD_BA2	SD_ODT	SD_D1	SD_VREF	MII0_CRS	MII0_TXEN	MII0_TXD0	MII0_RXDV	MII0_RXD3	MII0_MDC	P
R	SD_A12	SD_A7	SD_A11	SD_A13	SD_BA0	SD_RAS	SD_CKE	SD_WE	SD_D0	SD_D4	SD_D6	MII0_COL	MII0_TXD1	MII0_TXER	MII0_RXD1	TEST	R
T	VSS	SD_A6	SD_A0	SD_A8	SD_CLK	SD_CLK	SD_DM	SD_DQS	SD_DQS	SD_D2	SD_D5	SD_D7	MII0_TXD3	MII0_TXCLK	MII0_RXD0	VSS	T
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	

Figure 8. MCF54415, MCF54416, MCF54417, and MCF54418 Pinout (256 MAPBGA)

4 Electrical characteristics

This document contains electrical specification tables and reference timing diagrams for the MCF5441*x* microprocessor. This section contains detailed information on AC/DC electrical characteristics and AC timing specifications.

NOTE

The specifications for this device in any other document are superseded by the specifications in this document.

4.1 Absolute maximum ratings

Table 6. Absolute maximum ratings[1, 2]

Rating	Symbol	Pin name	Value	Units
External I/O pad supply voltage	EV_{DD}	EVDD	–0.3 to +4.0	V
Internal logic supply voltage	IV_{DD}	IVDD	–0.5 to +2.0	V
FlexBus I/O pad supply voltage	FBV_{DD}	FB_VDD	–0.3 to +4.0	V
SDRAM I/O pad supply voltage	SDV_{DD}	SD_VDD	–0.3 to +4.0	V
PLL supply voltage	PV_{DD}	VDD_OSC_A_PLL	–0.3 to +4.0	V
USB OTG supply voltage	$USBV_{DD}$	VDD_USBO	–0.3 to +4.0	V
USB host supply voltage	$USBV_{DD}$	VDD_USBH	–0.3 to +4.0	V
ADC supply voltage	AV_{DD}	VDDA_ADC	–0.3 to +4.0	V
DAC and ADC supply voltage	—	VDDA_DAC_ADC	–0.3 to +4.0	V
RTC standby supply voltage	$RTCV_{STBY}$	VSTBY_RTC	–0.3 to +4.0	V
Digital input voltage[3]	V_{IN}	—	–0.3 to +3.6	V
Instantaneous maximum current Single pin limit (applies to all pins) [3, 4, 5]	I_{DD}	—	25	mA
Operating temperature range (packaged)	T_A $(T_L – T_H)$	—	–40 to +85	°C
Storage temperature range	T_{stg}	—	–55 to +150	°C

1 Functional operating conditions are given in Table 11. Absolute maximum ratings are stress ratings only, and functional operation at the maximum is not guaranteed. Continued operation at these levels may affect device reliability or cause permanent damage to the device.

2 This device contains circuitry protecting against damage due to high static voltage or electrical fields. However, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Immunity to static and electrical fields is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., V_{SS} or EV_{DD}).

3 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, and then use the larger of the two values.

4 All functional non-supply pins are internally clamped to V_{SS} and EV_{DD} .

5 Power supply must maintain regulation within operating EV_{DD}, FBV_{DD}, and SDV_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{in} > EV_{DD}$, FBV_{DD}, or SDV_{DD}) is greater than I_{DD}, the injection current may flow out of EV_{DD}, FBV_{DD}, or SDV_{DD} and could result in external power supply going out of regulation. Ensure the external EV_{DD}, FBV_{DD}, or SDV_{DD} load shunts current greater than maximum injection current. This is the greatest risk when the MPU is not consuming power (for example, no clock).

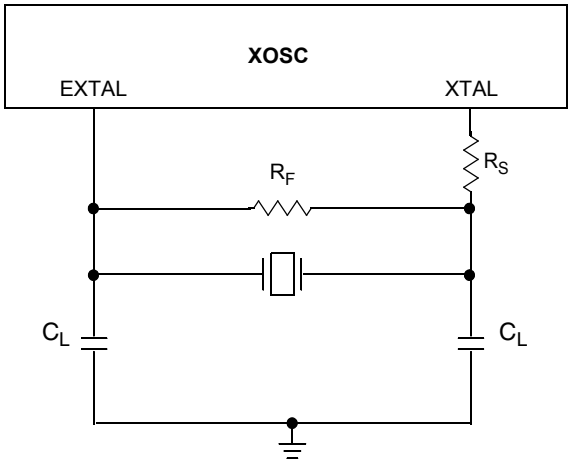


Figure 9. Typical crystal circuit

4.9 Reset timing specifications

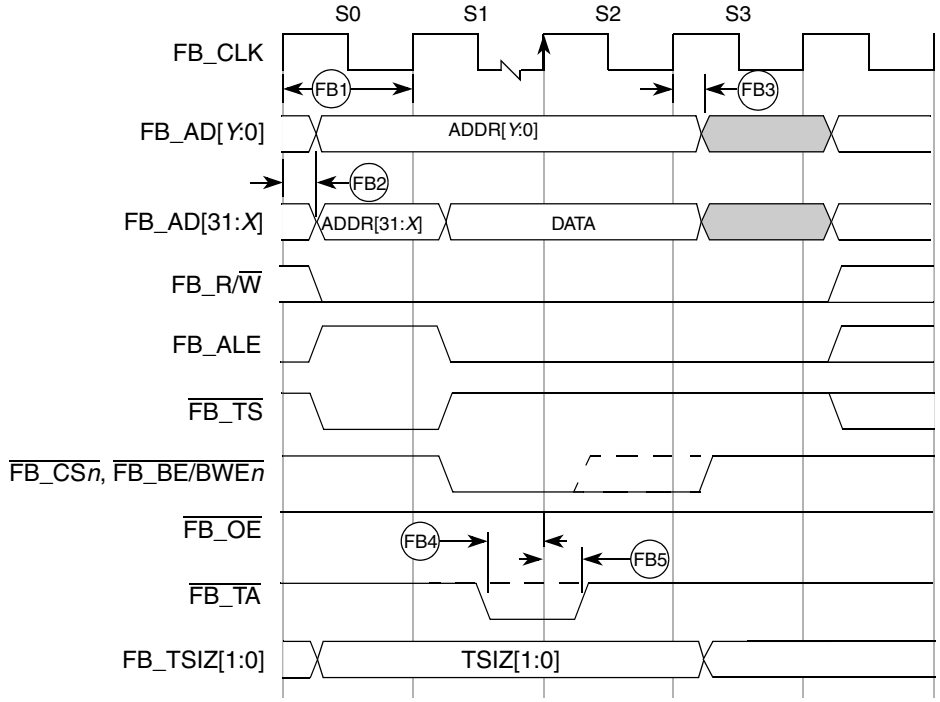
Table 15 lists specifications for the reset timing parameters shown in Figure 10.

Table 15. Reset and configuration override timing

Num	Characteristic	Min	Max	Unit
R1[1]	$\overline{\text{RESET}}$ valid to FB_CLK (setup)	9	—	ns
R2	FB_CLK to $\overline{\text{RESET}}$ invalid (hold)	1.5	—	ns
R3	$\overline{\text{RESET}}$ valid time[2]	5	—	FB_CLK cycles
R4	FB_CLK to $\overline{\text{RSTOUT}}$ valid	—	10	ns
R5	$\overline{\text{RSTOUT}}$ valid to Configuration Override inputs valid	0	—	ns
R6	Configuration Override inputs valid to $\overline{\text{RSTOUT}}$ invalid (setup)	20	—	FB_CLK cycles
R7	Configuration Override inputs invalid after $\overline{\text{RSTOUT}}$ invalid (hold)	0	—	ns
R8	$\overline{\text{RSTOUT}}$ invalid to Configuration Override inputs High Impedance	—	1	FB_CLK cycles
R9	Minimum RSTOUT pulse width	512	—	FB_CLK cycles

1 $\overline{\text{RESET}}$ and configuration override data lines are synchronized internally. Setup and hold times must be met only if recognition on a particular clock is required.

2 During low power STOP, the synchronizers for the $\overline{\text{RESET}}$ input are bypassed and $\overline{\text{RESET}}$ is asserted asynchronously to the system. Thus, $\overline{\text{RESET}}$ must be held a minimum of 100 ns.



Note:

1 FB2 and FB3 output specifications are valid for all FB_AD[31:0], FB_R/W, FB_ALE, FB_TS, FB_CS*n*, FB_OE, FB_BE/BWE*n*, and FB_TSIZ[1:0].

2 FB4 and FB5 input specifications are valid for all FB_AD[31:0] and FB_TA.

Figure 12. FlexBus write timing

4.11 NAND flash controller (NFC) timing specifications

The NAND flash controller (NFC) implements the interface to standard NAND flash memory devices. This section describes the timing parameters of the NFC.

All NFC signals use pad type pad_fsr. The following timing specifications assume a pad slew rate setting of 11 and a load of 50 pF.[1]

Table 17. NFC timing specifications

Num	Characteristic	Symbol	Min	Max	Unit
	Frequency of operation		—	40[1]	MHz
NF1	Clock period	t_{NFC}	25	—	ns
NF2	NFC_CLE setup time	t_{CLS}	$1.5 \times t_{NFC}$	—	ns
NF3	NFC_CLE hold time	t_{CLH}	t_{NFC}	—	ns
NF4	NFC_CE setup time	t_{CS}	$1.5 \times t_{NFC}$	—	ns
NF5	NFC_CE hold time	t_{CH}	t_{NFC}	—	ns
NF6	NFC_WE pulse width	t_{WP}	$0.5 \times t_{NFC} - 0.5$	—	ns

1.These timing parameters are specified assuming maximum operating frequency and the fastest pad slew rate setting (11). When operating this interface at lower frequencies, increase the slew rate by using the 10, 01, or 00 setting to increase edge rise and fall times, thus reducing EMI.

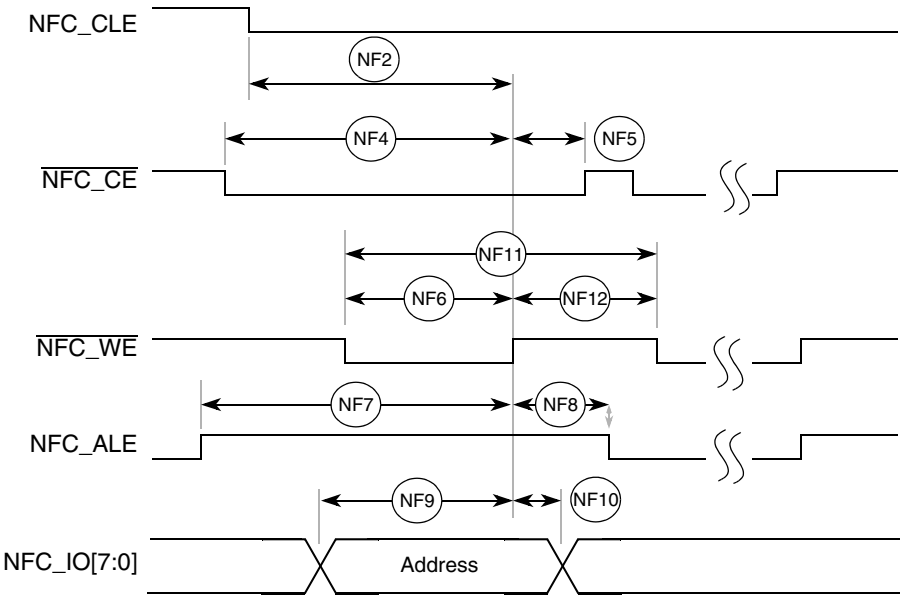


Figure 14. Address latch cycle timing

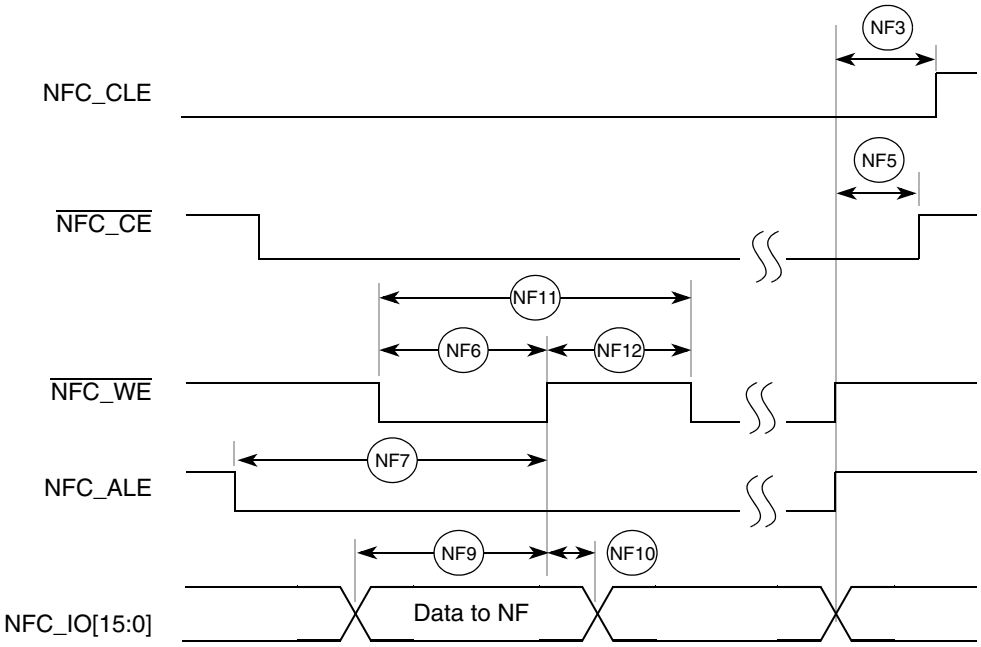


Figure 15. Write data latch timing

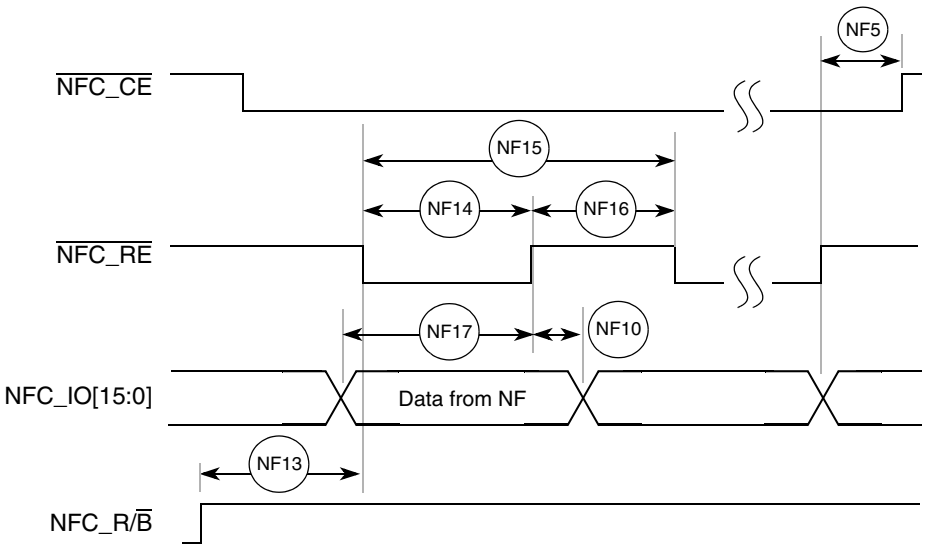


Figure 16. Read data latch timing

4.12 DDR SDRAM controller timing specifications

The following timing numbers must be followed to properly latch or drive data onto the SDRAM memory bus. All timing numbers are relative to the DQS byte lanes.

Table 18. SDRAM timing specifications

Num	Characteristic	Symbol	Min	Max	Unit	Notes
	Frequency of operation		100	250	MHz	
DD1	Clock period	t_{SDCK}	4.0	10.0	ns	
DD2	Pulse width high	t_{SDCKH}	0.45	0.55	t_{SDCK}	1
DD3	Pulse width low	t_{SDCKL}	0.45	0.55	t_{SDCK}	3
DD4	Address, SD_CKE, $\overline{\text{SD_CAS}}$, $\overline{\text{SD_RAS}}$, $\overline{\text{SD_WE}}$, $\overline{\text{SD_CS}}$[1:0] — output valid	t_{CMV}	—	$0.5 \times t_{SDCK} + 1$	ns	2
DD5	Address, SD_CKE, $\overline{\text{SD_CAS}}$, $\overline{\text{SD_RAS}}$, $\overline{\text{SD_WE}}$, $\overline{\text{SD_CS}}$[1:0] — output hold	t_{CMH}	$0.5 \times t_{SDCK} - 1$	—	ns	
DD6	Write command to first DQS latching transition	t_{DQSS}	—	$WL + 0.2 \times t_{SDCK}$	ns	
DD7	Data and data mask output setup (DQ→DQS) relative to DQS (DDR write mode)	t_{QS}	0.4	—	ns	3 4
DD8	Data and data mask output hold (DQS→DQ) relative to DQS (DDR write mode)	t_{QH}	0.4	—	ns	5
DD9	Input data skew relative to DQS (input setup)	t_{IS}	—	0.5	ns	6
DD10	Input data hold relative to DQS.	t_{IH}	$0.375 \times t_{SDCK}$	—	ns	7

1 Pulse width high plus pulse width low cannot exceed min and max clock period.

2 Command output valid should be 1/2 the memory bus clock (t_{SDCK}) plus some minor adjustments for process, temperature, and voltage variations.

4.15.2 eSDHC electrical DC characteristics

Table 21 lists the eSDHC electrical DC characteristics.

Table 21. MMC/SD interface electrical specifications

Num	Parameter	Design value	Min	Max	Unit	Condition/remark
Bus signal line load						
7	Pull-up resistance	47	10	100	kΩ	Internal PU
8	Open drain resistance	NA	NA	NA	kΩ	For MMC cards only
Open drain signal level						For MMC cards only
9	Output high voltage		V_{DD} – 0.2		V	I_{OH} = –100 µA
10	Output low voltage			0.3	V	I_{OL} = 2 mA
Bus signal levels						
11	Output high voltage		0.75 x V_{DD}		V	I_{OH} = –100 µA @V_{DD} min
12	Output low voltage			0.125 x V_{DD}	V	I_{OL} = 100 µA @V_{DD} min
13	Input high voltage		0.625 x V_{DD}	V_{DD} + 3	V	
14	Input low voltage		V_{SS} – 0.3	0.25 x V_{DD}	V	

4.16 SIM timing specifications

Each SIM card interface consist of a total of 12 pins (two separate ports of six pins each. Mostly one port with 5 pins is used).

The interface is meant to be used with synchronous SIM cards. This means that the SIM module provides a clock for the SIM card to use. The frequency of this clock is normally 372 times the data rate on the TX/RX pins, however SIM module can work with CLK equal to 16 times the data rate on TX/RX pins.

There is no timing relationship between the clock and the data. The clock that the SIM module provides to the SIM card is used by the SIM card to recover the clock from the data, like a standard UART. All six (or five when a bidirectional TXRX is used) of the pins for each half of the SIM module are asynchronous to each other. There are no required timing relationships between the signals in normal mode. However, there are some in reset and power down sequences.

All SIM signals use pad type pad_msr. SIM timing is fairly relaxed compared to other interfaces and can be met at 50 pF loading with any slew rate setting other than 00.[1]

1.These timing parameters are specified assuming maximum operating frequency and the fastest pad slew rate setting (11). When operating this interface at lower frequencies, increase the slew rate by using the 10, 01, or 00 setting to increase edge rise and fall times, thus reducing EMI.

4.16.1 General timing requirements

Figure 21 shows the timing of the SIM module, and Table 22 lists the timing parameters.

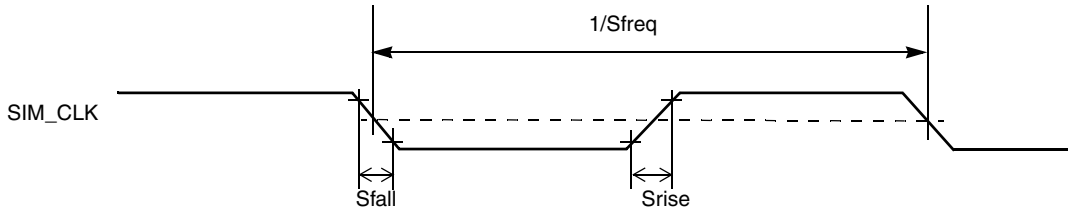


Figure 21. SIM clock timing diagram

Table 22. SIM timing specification—High Drive strength

Num	Description	Symbol	Min	Max	Unit
1	SIM clock frequency (SIM_CLK)[1]	S_{freq}	0.01	5 (Some new cards may reach 10)	MHz
2	SIM_CLK rise time [2]	S_{rise}	–	20	ns
3	SIM_CLK fall time [3]	S_{fall}	–	20	ns
4	SIM input transition time (RX, SIM_PD)	S_{trans}	–	25	ns

[1] 50% duty cycle clock
[2] With C = 50pF
[3] With C = 50pF

4.16.2 Reset sequence

4.16.2.1 Cards with internal reset

The reset sequence for this kind of SIM card is as follows (see Figure 22):

- After powerup, the clock signal is enabled on SIM_CLK (time T0)
- After 200 clock cycles, RX must be high.
- The card must send a response on RX acknowledging the reset between 400 and 40,000 clock cycles after T0.

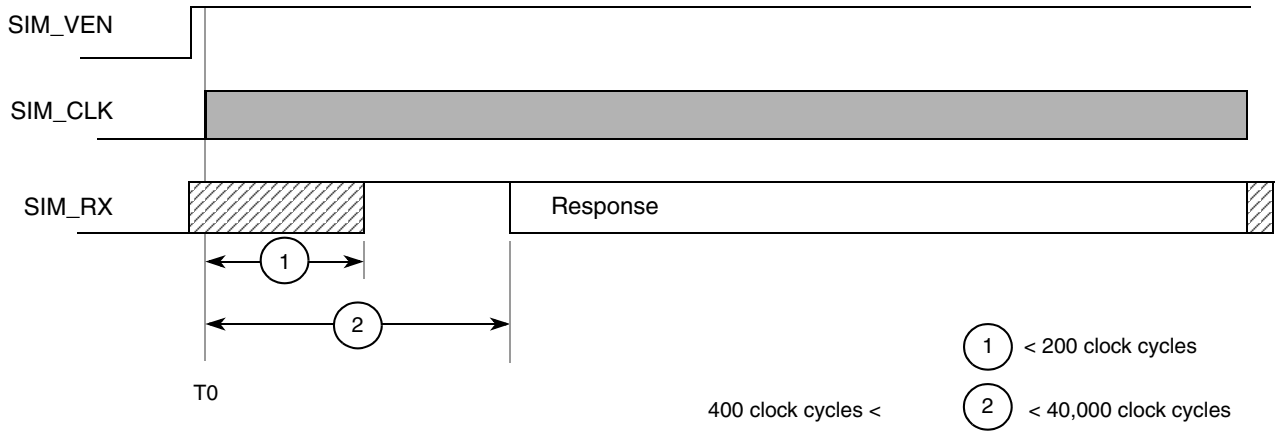


Figure 22. Internal-reset card reset sequence

Table 24. SSI timing — master modes[1]

Num	Description	Symbol	Min	Max	Units	Notes
S1	SSI_MCLK cycle time	t_{MCLK}	15.15	—	ns	[2]
S2	SSI_MCLK pulse width high / low		45%	55%	t_{MCLK}	
S3	SSI_BCLK cycle time	t_{BCLK}	80	—	ns	[3]
S4	SSI_BCLK pulse width		45%	55%	t_{BCLK}	
S5	SSI_BCLK to SSI_FS output valid		—	15	ns	
S6	SSI_BCLK to SSI_FS output invalid		0	—	ns	
S7	SSI_BCLK to SSI_TXD valid		—	15	ns	
S8	SSI_BCLK to SSI_TXD invalid / high impedance		0	—	ns	
S9	SSI_RXD / SSI_FS input setup before SSI_BCLK		15	—	ns	
S10	SSI_RXD / SSI_FS input hold after SSI_BCLK		0	—	ns	

1 All timings specified with a capacitive load of 25pF.
2 SSI_MCLK can be generated from SSI_CLKIN or a divided version of the internal system clock (f_{sys}).
3 SSI_BCLK can be derived from SSI_CLKIN or a divided version of the internal system clock (f_{sys}).

Table 25. SSI timing — slave modes[1]

Num	Description	Symbol	Min	Max	Units	Notes
S11	SSI_BCLK cycle time	t_{BCLK}	80	—	ns	
S12	SSI_BCLK pulse width high / low		45%	55%	t_{BCLK}	
S13	SSI_FS input setup before SSI_BCLK		10	—	ns	
S14	SSI_FS input hold after SSI_BCLK		2	—	ns	
S15	SSI_BCLK to SSI_TXD / SSI_FS output valid		—	15	ns	
S16	SSI_BCLK to SSI_TXD / SSI_FS output invalid / high impedance		0	—	ns	
S17	SSI_RXD setup before SSI_BCLK		15	—	ns	
S18	SSI_RXD hold after SSI_BCLK		2	—	ns	

1 All timings specified with a capacitive load of 25pF.

Table 27. DAC parameters[1] (continued)

Characteristic	Name	Min	Typical	Max	Unit
Integral non-linearity (497 to 3599)	INL	—	—	±8.0	lsb
Differential non-linearity (497 to 3599)	DNL	—	—	±0.5	lsb
Gain error (497 to 3599)	E_{GAIN}	—	±0.26	—	%
Effective number of bits	ENOB	9	—	—	bits
DAC power-up time	t_{DAPU}	—	—	11	us
Output load resistance	R_L	3K	—	—	Ohm
Output load capacitance	C_L	—	400	—	pF
Power supply ripple rejection	PSRR	—	60	—	dB

[1] All measurements were made at V_{DD} = 3.3V, V_{REFH} = 3.3V, and V_{REFL} = ground

4.20 mcPWM timing specifications

Table 28. mcPWM timing

Num	Characteristic	Min	Max	Unit
G1	FB_CLK high to output valid	—	7	ns
G2	FB_CLK high to output invalid	1	—	ns
G3	Input valid to FB_CLK high	3	—	ns
G4	FB_CLK high to input invalid	1	—	ns

4.21 I^2C timing specifications

Table 29 lists specifications for the I^2C input timing parameters shown in Figure 27.

Table 29. I^2C input timing specifications between SCL and SDA

Num	Characteristic	Min	Max	Units
I1	Start condition hold time	2	—	$1/f_{SYS}$
I2	Clock low period	8	—	$1/f_{SYS}$
I3	I2C_SCL/I2C_SDA rise time (V_{IL} = 0.5 V to V_{IH} = 2.4 V)	—	1	ms
I4	Data hold time	0	—	ns
I5	I2C_SCL/I2C_SDA fall time (V_{IH} = 2.4 V to V_{IL} = 0.5 V)	—	1	ms
I6	Clock high time	4	—	$1/f_{SYS}$
I7	Data setup time	0	—	ns
I8	Start condition setup time (for repeated start condition only)	2	—	$1/f_{SYS}$
I9	Stop condition setup time	2	—	$1/f_{SYS}$

Table 30 lists specifications for the I^2C output timing parameters shown in Figure 27.

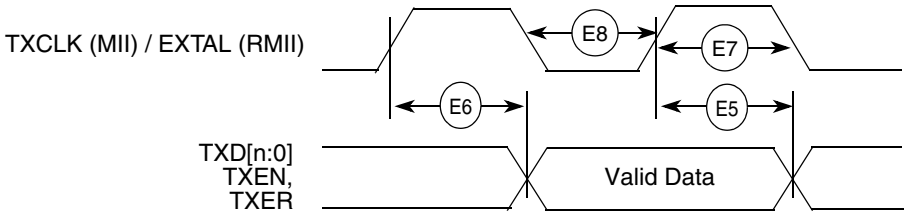


Figure 29. MII/RMII transmit signal timing diagram

4.22.3 Asynchronous input signal timing specifications

Table 33. MII/RMII transmit signal timing

Num	Characteristic	Min	Max	Unit
E9	CRS, COL minimum pulse width	1.5	—	TXCLK period

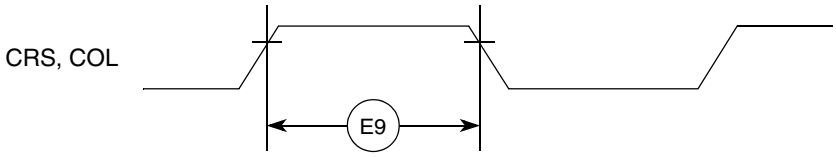


Figure 30. MII/RMII async inputs timing diagram

4.22.4 MDIO serial management timing specifications

Table 34. MDIO serial management channel signal timing

Num	Characteristic	Symbol	Min	Max	Unit
E10	MDC cycle time	t_{MDC}	400	—	ns
E11	MDC pulse width		40	60	% t_{MDC}
E12	MDC to MDIO output valid		—	375	ns
E13	MDC to MDIO output invalid		25	—	ns
E14	MDIO input to MDC setup		10	—	ns
E15	MDIO input to MDC hold		0	—	ns

4.26 1-Wire timing specifications

Specifications for the 1-Wire interface are provided by Maxim Integrated Products, Inc. Please refer to data sheet information for the appropriate device at www.maxim-ic.com.

4.27 General purpose I/O timing specifications

Table 38. GPIO timing[1]

Num	Characteristic	Min	Max	Unit
G1	FB_CLK high to GPIO output valid	—	9	ns
G2	FB_CLK high to GPIO output invalid	1	—	ns
G3	GPIO input valid to FB_CLK high	9	—	ns
G4	FB_CLK high to GPIO input invalid	1.5	—	ns

[1] These general purpose specifications apply to the following signals: $\overline{\text{IRQ}}n$, all UART signals, all timer signals, FlexCAN signals, $\overline{\text{DACK}}n$ and $\overline{\text{DREQ}}n$, and all signals configured as GPIO.

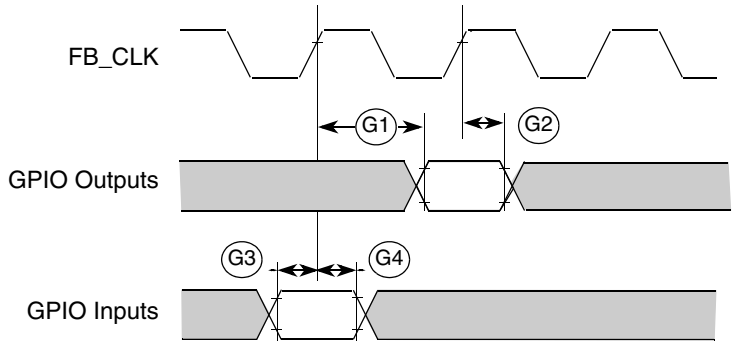


Figure 35. GPIO timing

4.28 Rapid general purpose I/O timing specifications

RGPIO signals use a mix of pad types: pad_fsr, pad_msr, and pad_ssr. The following timing specifications assume a pad slew rate setting of 11 and a load of 50 pF.

Table 39. RGPIO timing

Num	Characteristic	Min	Max	Unit
RG1	PST_CLK high to RGPIO output valid	—	6	ns
RG2	PST_CLK high to RGPIO output Invalid	0.5	—	ns
RG3	RGPIO input valid to PST_CLK high	6	—	ns
RG4	PST_CLK high to RGPIO input invalid	1.5	—	ns

4.30 Debug AC timing specifications

Table 41 lists specifications for the debug AC timing parameters shown in Figure 41 and Table 42.

All debug signals use pad type pad_msr except for PSTCLK which use pad type pad_fsr. The following timing specifications assume a pad slew rate setting of 11 and a load of 50 pF.[1]

Table 41. Debug AC timing specification

Num	Characteristic	Min	Max	Units
D0	PSTCLK cycle time	0.5	0.5	$1/f_{SYS}$
D1	PSTCLK rising to PSTDDATA valid	—	3.0	ns
D2	PSTCLK rising to PSTDDATA invalid	0.5	—	ns
D3	DSI-to-DSCLK setup	1	—	PSTCLK
D4[1]	DSCLK-to-DSO hold	4	—	PSTCLK
D5	DSCLK cycle time	5	—	PSTCLK
D6	BKPT assertion time	1	—	PSTCLK

[1] DSCLK and DSI are synchronized internally. D4 is measured from the synchronized DSCLK input relative to the rising edge of PSTCLK.

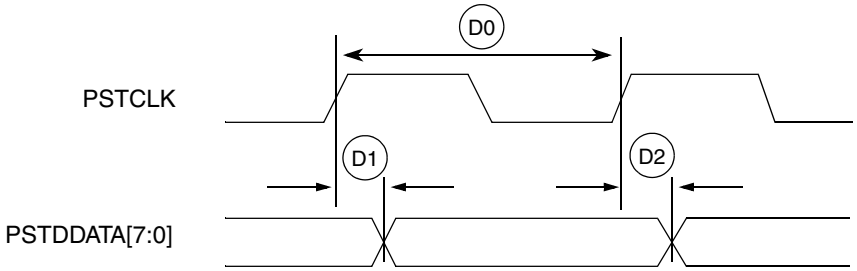


Figure 41. Real-time trace AC timing

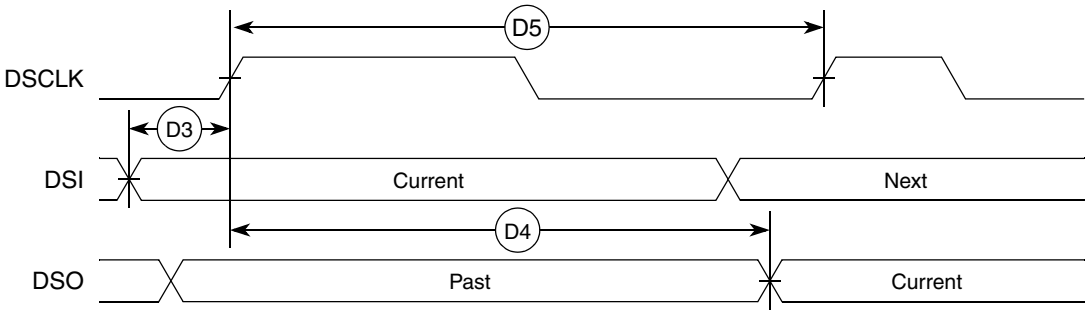


Figure 42. BDM serial port AC timing

1.These timing parameters are specified assuming maximum operating frequency and the fastest pad slew rate setting (11). When operating this interface at lower frequencies, increase the slew rate by using the 10, 01, or 00 setting to increase edge rise and fall times, thus reducing EMI.

5 Package information

The latest package outline drawings are available on the product summary pages on http://www.freescale.com/coldfire. Table 42 lists the case outline numbers per device. Use these numbers in the web page's keyword search engine to find the latest package outline drawings.

Table 42. Package information

Device	Package type	Case outline numbers
MCF54410	196 MAPBGA	98ASA00321D
MCF54415	256 MAPBGA	98ARH98219A
MCF54416		
MCF54417		
MCF54418		

6 Product documentation

Documentation is available from a local Freescale distributor, a Freescale sales office, the Freescale Literature Distribution Center, or through the Freescale world-wide web address at http://www.freescale.com/coldfire.