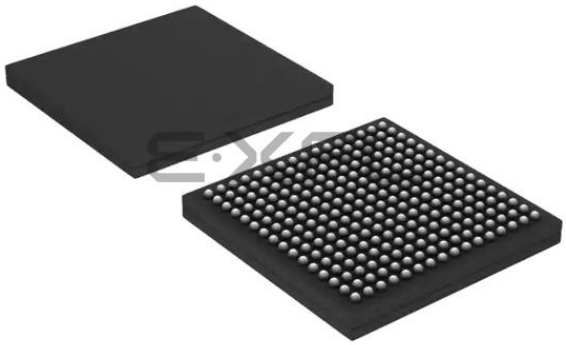

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	Coldfire V4
Core Size	32-Bit Single-Core
Speed	250MHz
Connectivity	1-Wire®, CANbus, EBI/EMI, Ethernet, I²C, SmartCard, SPI, SSI, UART/USART, USB, USB OTG
Peripherals	DMA, PWM, WDT
Number of I/O	87
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	1.14V ~ 1.32V
Data Converters	A/D 8x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	256-LBGA
Supplier Device Package	256-MAPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcf54418cmj250

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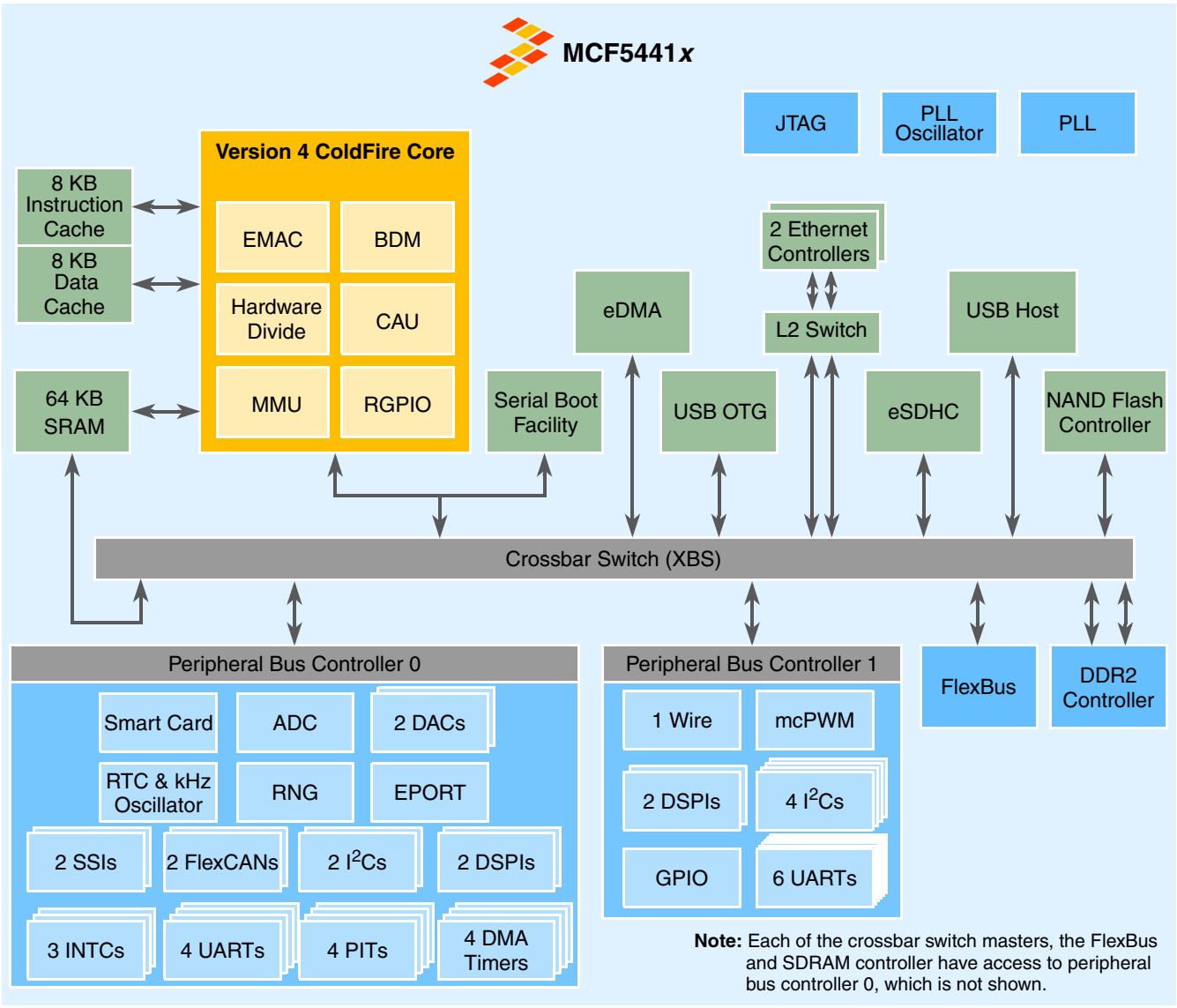


ADC – Analog-to-digital converter
BDM – Background debug module
CAU – Cryptography acceleration unit
DAC – Digital-to-analog
DSPI – DMA serial peripheral interface
eDMA – Enhanced direct memory access module
eSDHC – Enhanced Secure Digital host controller
EMAC – Enhanced multiply-accumulate unit
EPORT – Edge port module
GPIO – General purpose input/output module
I²C – Inter-Integrated Circuit
INTC – Interrupt controller
JTAG – Joint Test Action Group interface
mcPWM – Motor control pulse width modulator
PIT – Programmable interrupt timers
PLL – Phase locked loop module
RGPIO – Rapid GPIO
RNG – Random number generator
RTC – Real time clock
SSI – Synchronous serial interface
USB OTG – Universal Serial Bus On-the-Go controller

Table 1. MCF5441*x* family configurations (continued)

Module	MCF54410	MCF54415	MCF54416	MCF54417	MCF54418
NAND flash controller	•	•	•	•	•
1-Wire® interface	•	•	•	•	•
Serial boot facility	•	•	•	•	•
Watchdog timer	•	•	•	•	•
Interrupt controllers (INTC)	3	3	3	3	3
Edge port module (EPORT)	3 IRQs	5 IRQs	5 IRQs	5 IRQs	5 IRQs
Rapid GPIO pins	9	16	16	16	16
General-purpose I/O (GPIO) pins	48	87	87	87	87
JTAG - IEEE® 1149.1 Test Access Port	•	•	•	•	•
Package	196 MAPBGA	256 MAPBGA			

1.1 Ordering information

Table 2. Orderable part numbers

Freescale Part Number	Description	Package	Speed	Temperature
MCF54410CMF250	MCF54410 Microprocessor	196 MAPBGA	250 MHz	–40 to +85°C
MCF54415CMJ250	MCF54415 Microprocessor	256 MAPBGA		
MCF54416CMJ250	MCF54416 Microprocessor			
MCF54417CMJ250	MCF54417 Microprocessor			
MCF54418CMJ250	MCF54418 Microprocessor			

2 Hardware design considerations

2.1 Power filtering

To further enhance noise isolation, an external filter is strongly recommended for the analog V_{DD} pins (VDDA_PLL and VDDA_DAC_ADC). The filter shown in Figure 1 should be connected between the board 3.3 V (nominal) supply and the analog pins. The resistor and capacitors should be placed as close to the dedicated analog V_{DD} pin as possible. The 10 Ω resistor in the given filter is required.

Figure 5 shows an example for bypassing the FlexBus power supply for the MPU. This bypass should be applied to as many FB_VDD signals as routing allows. Each one should be placed as close to the ball as possible.

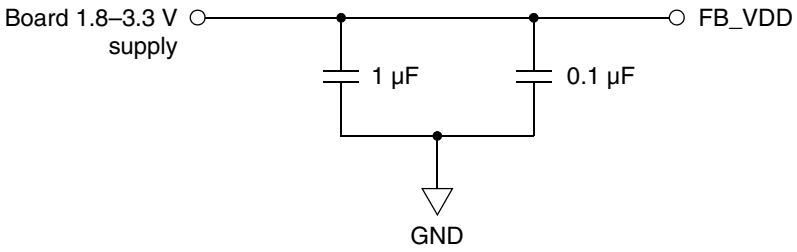
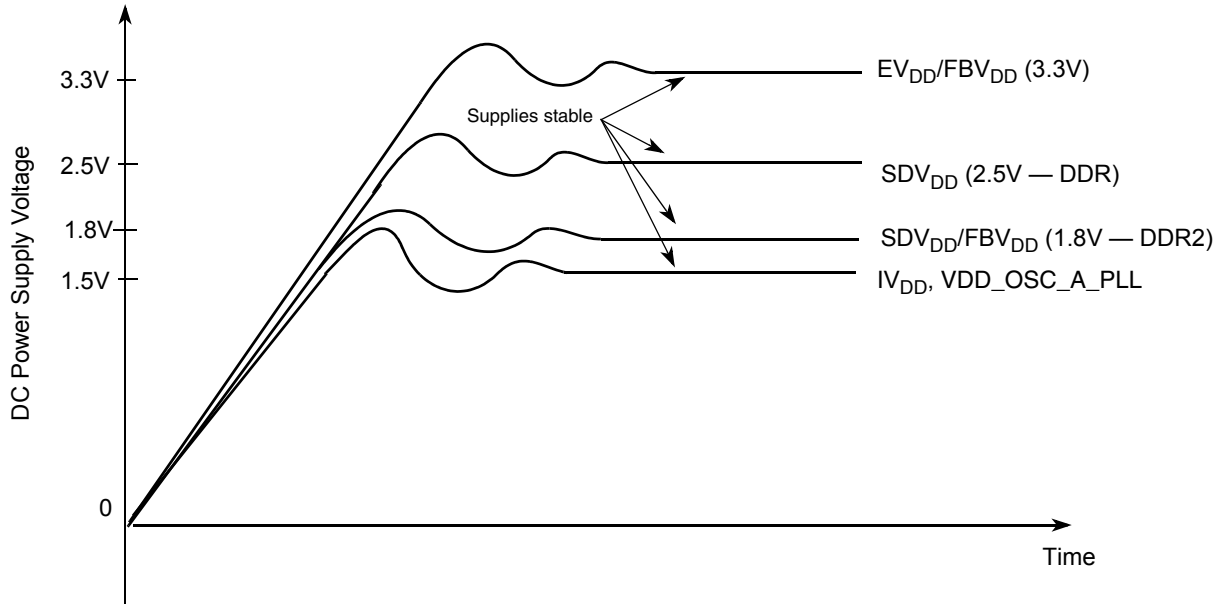


Figure 5. FB_VDD power filter

2.2 Supply voltage sequencing

Figure 6 shows requirements in the sequencing of the I/O V_{DD} (EV_{DD}), FlexBus V_{DD} (FBV_{DD}), SDRAM V_{DD} (SDV_{DD}), PLL V_{DD} (VDD_OSC_A_PLL), and internal logic/core V_{DD} (IV_{DD}).



Notes:
1. Input voltage must not be greater than the supply voltage (EV_{DD}, FBV_{DD}, SDV_{DD}, IV_{DD}, or PV_{DD}) by more than 0.5V at any time, including during power-up.
2. Use 25 V/millisecond or slower rise time for all supplies.

Figure 6. Supply voltage sequencing and separation cautions

The relationships between FBV_{DD}, SDV_{DD} and EV_{DD} are non-critical during power-up and power-down sequences. FBV_{DD} (1.8 – 3.3V), SDV_{DD} (2.5V or 1.8V) and EV_{DD} are specified relative to IV_{DD}.

NOTE

All I/O VDD pins must be powered on when the device is functioning, except when in standby mode.

In standby mode, all I/O VDD pins, except VSTBY_RTC (battery), can be switched off.

2.2.1 Power-up sequence

If EV_{DD}/FBV_{DD}/SDV_{DD} are powered up with the IV_{DD} at 0 V, the sense circuits in the I/O pads cause all pad output drivers connected to the EV_{DD}/FBV_{DD}/SDV_{DD} to be in a high impedance state. There is no limit on how long after EV_{DD}/FBV_{DD}/SDV_{DD} powers up before IV_{DD} must power up. IV_{DD} should not lead the EV_{DD}, FBV_{DD}, or SDV_{DD} by more than 0.4 V during power ramp-up, or there will be high current in the internal ESD protection diodes. The rise times on the power supplies should be slower than 25 V/millisecond to avoid turning on the internal ESD protection clamp diodes.

2.2.2 Power-down sequence

If IV_{DD}/PV_{DD} are powered down first, sense circuits in the I/O pads cause all output drivers to be in a high impedance state. There is no limit on how long after IV_{DD} and PV_{DD} power down before EV_{DD}, FBV_{DD}, or SDV_{DD} must power down. IV_{DD} should not lag EV_{DD}, FBV_{DD}, or SDV_{DD} going low by more than 0.4 V during power down or there will be undesired high current in the ESD protection diodes. There are no requirements for the fall times of the power supplies.

The recommended power down sequence is as follows:

1. Drop IV_{DD}/PV_{DD} to 0 V.
2. Drop EV_{DD}/FBV_{DD}/SDV_{DD} supplies.

2.3 Power consumption specifications

Table 3. Estimated power consumption specifications

Characteristic	Symbol	Typical	Unit
Core operating supply current (nominal 1.2 V)[1]	IVDD		
Run mode		127	mA
Wait mode		33	
Doze mode		32	
Stop00 mode		9.3	
Stop01 mode		9.2	
Stop02 mode		3.6	
Stop03 mode		3.4	
FlexBus operating supply current	FBVDD		
Run mode (application dependent)		80	mA
Wait mode		49	
Doze mode		42	
Stop00 mode		40	
Stop01, Stop02, Stop03 mode		28	
SDRAM operating supply current (DDR2 at 1.8 V)	SDVDD		
Isys(DQ) [×8, 2×DQS]		3	mA
Isys(WR) [×8, 2×DQS]		15	
Isys(RD) [×8, 2×DQS]		15	
SDRAM input reference current	SDVREF		
Isys(REF)		1.3	
SDRAM termination current	SDVTT		
Isys(termRD)		41	
Total SDIDD MPU side[2]		75	
Oscillator/PLL operating supply current (nominal 3.3 V)	VDD_OSC_A_PLL		
Run, Wait, Doze, Stop00, Stop01 mode		10	mA
Stop02 mode		6	
Stop03 mode		1	

Table 4. Special-case default signal functionality

Pin	Default signal
FB_CLK, FB_OE, FB_R/W, FB_BE/BWE[1:0], FB_CS[5:4]	FB_CLK, FB_OE, FB_R/W, FB_BE/BWE[1:0], FB_CS[5:4]
FB_ALE	FB_ALE or FB_TS (depending on RCON[3])
FB_BE/BWE3	Boot from NFC, NF_ALE. Otherwise, FB_BE/BWE3.
FB_BE/BWE2	Boot from NFC, NF_CLE. Otherwise, FB_BE/BWE2.
FB_CS1	Boot from NFC, NFC_CE. Otherwise, GPIO.
FB_CS0	Boot from FlexBus, FB_CS0. Otherwise, GPIO.
FB_TA	Boot from NFC, NFC_R/B. Otherwise, FB_TA.
ALLPST, PST[3:0], DDATA[3:0]	ALLPST, PST[3:0], DDATA[3:0]

NOTE

While most modules and functionalities between the 196 and 256 MAPBGA package are the same, the following modules have been removed from 196 MAPBGA for pin space:

UART2, UART6, UART9, PWM, SSI1, SIM1, USB HOST, IRQ6, IRQ3, IRQ2, FLEXCAN1, I2C1, ADC, DAC.

Other modifications to the 196 MAPBGA package are:

- SDRAMC — One address line, SD_A14, is removed.
- SDHC — Number of data lines for eSDHC have been reduced to 4 instead of 8.
- MAC — Only MAC0_RMII mode is implemented.

Table 5. MCF5441*x* Signal information and muxing

Signal name	GPIO	Alternate 1	Alternate 2	Pullup (U)[1] Pulldown (D)	Direction[2]	Voltage domain	Pad type[3]	196 MAPBGA	256 MAPBGA
Reset									
RESET	—	—	—	U	I	EVDD	ssr	K14	K15
RSTOUT	—	—	—	—	O	EVDD	msr	P12	L16
Clock									
EXTAL/ RMII_REF_CLK	—	—	—	—	I[4]	EVDD	ae	G14	G16

Table 5. MCF5441*x* Signal information and muxing (continued)

Signal name	GPIO	Alternate 1	Alternate 2	Pullup (U)[1] Pulldown (D)	Direction[2]	Voltage domain	Pad type[3]	196 MAPBGA	256 MAPBGA
XTAL	—	—	—	—	O	EVDD	ae	H14	H16
Mode selection									
BOOTMOD[1:0]	—	—	—	—	I	EVDD	msr	G5,H5	K5, L5
FlexBus									
FB_AD[31:24]/ NFC_IO[15:8][5]	—	—	—	—	I/O	FBVDD	fsr	A10, A9, B9, C9, A8, B8, C8, A7	B9, C8, A9, B8, D8, A8, D7, B7
FB_AD[23:16]/ NFC_IO[7:0][5]	—	—	—	—	I/O	FBVDD	fsr	B7, C7, C6, B6, A6, A5, B5, A4	C7, A7, D6, A6, B6, D5, C6, A5
FB_AD[15:10]	—	—	—	—[6]	I/O	FBVDD	fsr	C5, A3, B4, C4, B3, A2	B5, A4, A3, D4, B4, C5
FB_AD[9:8]	—	—	—	U[7]	I/O	FBVDD	fsr	B2, C3	C4, B3
FB_AD[7:0]	—	—	—	—	I/O	FBVDD	fsr	D4, B1, C2, D3, C1, D2, E3, D1	C3, E4, D3, E3, A2, B2, C2, F3
FB_ALE	PA7	$\overline{\text{FB\_TS}}$	—	—	O	FBVDD	fsr	E2	D2
$\overline{\text{FB\_OE}}$/ $\overline{\text{NFC\_RE}}$	PA6	$\overline{\text{FB\_TBST}}$/ $\overline{\text{NFC\_RE}}$	—	—	O	FBVDD	fsr	H1	F1
FB_R/$\overline{\text{W}}$/ $\overline{\text{NFC\_WE}}$	PA5	—	—	—	O	FBVDD	fsr	H2	G2
$\overline{\text{FB\_TA}}$	PA4	—	NFC_R/$\overline{\text{B}}$	U[8]	O	FBVDD	fsr	H3	H3
$\overline{\text{FB\_BE/BWE3}}$	PA3	$\overline{\text{FB\_CS3}}$	FB_A1/ NFC_ALE[9]	—	O	FBVDD	fsr	F3	C1
$\overline{\text{FB\_BE/BWE2}}$	PA2	$\overline{\text{FB\_CS2}}$	FB_A0/ NFC_CLE[10]	—	O	FBVDD	fsr	E1	E2
$\overline{\text{FB\_BE/BWE}}$[1:0]	PA[1:0]	FB_TSIZ[1:0]	—	—	O	FBVDD	fsr	F2, F1	D1, F4
FB_CLK	PB7	—	—	—	O	FBVDD	fsr	G1	G1
$\overline{\text{FB\_CS5}}$	PB6	$\overline{\text{DACK1}}$	—	—	O	FBVDD	fsr	—	F2
$\overline{\text{FB\_CS4}}$	PB5	$\overline{\text{DREQ1}}$	—	—	O	FBVDD	fsr	—	B1
$\overline{\text{FB\_CS1}}$	PB4	—	$\overline{\text{NFC\_CE}}$	—	O	FBVDD	fsr	G3	E1
$\overline{\text{FB\_CS0}}$	PB3	—	—	—	O	FBVDD	fsr	G2	G3
I²C 0									
I2C0_SCL	PB2	UART8_TXD	CAN0_TX	—	I/O	EVDD	ssr	H12	G15
I2C0_SDA	PB1	UART8_RXD	CAN0_RX	—	I/O	EVDD	ssr	G12	G14

Table 5. MCF5441*x* Signal information and muxing (continued)

Signal name	GPIO	Alternate 1	Alternate 2	Pullup (U)[1] Pulldown (D)	Direction[2]	Voltage domain	Pad type[3]	196 MAPBGA	256 MAPBGA
External interrupts port									
$\overline{\text{IRQ7}}$	PC6	—	—	—	I	EVDD	ssr	G10	F12
$\overline{\text{IRQ6}}$	PC5	—	USB_CLKIN[11]	—	I	EVDD	ssr	—	N1
$\overline{\text{IRQ4}}$	PC4	$\overline{\text{DREQ0}}$	—	—	I	EVDD	ssr	E11	F14
$\overline{\text{IRQ3}}$	PC3	DSPI0_PCS3	USBH_VBUS_EN	—	I	EVDD	ssr	—	M1
$\overline{\text{IRQ2}}$	PC2	DSPI0_PCS2	USBH_VBUS_OC	—[12]	I	EVDD	ssr	—	M2
$\overline{\text{IRQ1}}$	PC1	—	—	—	I	EVDD	ssr	E13	F13
USB On-the-Go									
USBO_DM	—	—	—	—	I/O	VDD_USB0	ae	B13	A14
USBO_DP	—	—	—	—	I/O	VDD_USB0	ae	A13	B14
USB host									
USBH_DM	—	—	—	—	I/O	VDD_USBH	ae	—	A15
USBH_DP	—	—	—	—	I/O	VDD_USBH	ae	—	B15
ADC									
ADC_IN7/ DAC1_OUT	—	—	—	—	I	VDDA_DAC_ADC	ae	—	K3
ADC_IN[6:4]	—	—	—	—	I	VDDA_ADC	ae	—	H2, J3, G4
ADC_IN3/ DAC0_OUT	—	—	—	—	I	VDDA_DAC_ADC	ae	—	K4
ADC_IN[2:0]	—	—	—	—	I	VDDA_ADC	ae	—	J2, J1, H1
Real time clock									
RTC_EXTAL	—	—	—	—	I[4]	VSTBY	ae	B14	B16
RTC_XTAL	—	—	—	—	O	VSTBY	ae	C14	C16
DSPI0/SBF[13]									
DSPI0_PCS1/ $\overline{\text{SBF\_CS}}$	PC0	—	—	—	I/O	EVDD	msr	K3	L1

[21] Configurable pull that is enabled and pulled down after reset.

[22] The ALLPST signal is available only on the 196 MAPBGA package and allows limited debug trace functionality compared to the 256 MAPBGA package.

[23] If JTAG_EN is asserted, these pins default to Alternate 1 (JTAG) functionality. The GPIO module is not responsible for assigning these pins.

[24] VSTBY is for optional standby lithium battery. If not used, connect to EVDD.

3.2 Pinout—196 MAPBGA

The pinout for the MCF54410 package is shown below.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	
A	GND	FB_AD10	FB_AD14	FB_AD16	FB_AD18	FB_AD19	FB_AD24	FB_AD27	FB_AD30	FB_AD31	SSI0_TXD	SSI0_MCLK	USB_DPLS	GND	A
B	FB_AD6	FB_AD9	FB_AD11	FB_AD13	FB_AD17	FB_AD20	FB_AD23	FB_AD26	FB_AD29	U1_RXD	U0_TXD	SSI0_RXD	USB_DMNS	RTC_EXTAL	B
C	FB_AD3	FB_AD5	FB_AD8	FB_AD12	FB_AD15	FB_AD21	FB_AD22	FB_AD25	FB_AD28	U1_TXD	U0_RXD	U0RTS_B	SSI0_FS	RTC_XTAL	C
D	FB_AD0	FB_AD2	FB_AD4	FB_AD7	FBVDD	FBVDD	FBVDD	GND	CVDD	CVDD	U1RTS_B	U1CTS_B	SSI0_BCLK	GND	D
E	FB_BE2_B	FB_ALE	FB_AD1	FBVDD	FBVDD	FBVDD	FBVDD	GND	CVDD	CVDD	IRQ4_B	U0CTS_B	IRQ1_B	VSTBY	E
F	FB_BE0_B	FB_BE1_B	FB_BE3_B	EVDD	EVDD	EVDD	EVDD	GND	CVDD	CVDD	VDD_USBO	CVDD	VSS_OSC_A_PLL	VDD_OSC_A_PLL	F
G	FB_CLK	FB_CS0_B	FB_CS1_B	GND	BOOTMOD1	EVDD	EVDD	GND	GND	IRQ7_B	GND	I2C0_SDA	T3IN	EXTAL	G
H	FB_OE_B	FB_RW_B	FB_TA_B	GND	BOOTMOD0	EVDD	EVDD	GND	GND	GND	GND	I2C0_SCL	T1IN	XTAL	H
J	DSPI0_PCS0	DSPI0_SOUT	DSPI0_SCK	SD_BA1	EVDD	EVDD	GND	GND	GND	GND	GND	T2IN	T0IN	GND	J
K	SD_A1	DSPI0_SIN	DSPI0_PCS1	SD_CAS_B	GND	GND	SDVDD	SDVDD	SDVDD	TEST	GND	ALLPST	TMS	RSTIN_B	K
L	SD_A9	SD_A10	SD_A5	SD_A4	SDVDD	SDVDD	SDVDD	SD_VTT	TRST_B	TDI	RM110_TXD0	RM110_TXD1	TDO	TCLK	L
M	SD_A12	SD_A7	SD_A11	SD_RAS_B	SD_CS_B	SD_BA2	SD_D0	SD_D2	SD_D4	SD_D6	OWIO	RMII0_RXER	RMII0_CRS_DV	RMII0_MDIO	M
N	SD_A3	SD_A2	SD_A0	SD_A8	SD_WE_B	SD_CKE	SD_DQM	SD_D1	SD_VREF	SD_D5	JTAG_EN	RMII0_TXEN	RMII0_RXD0	RMII0_MDC	N
P	GND	SD_A6	SD_A13	SD_BA0	SD_ODT	SD_CLK	SD_CLK_B	SD_DQS	SD_DQS_B	SD_D3	SD_D7	RSTOUT_B	RMII0_RXD1	GND	P
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	

Figure 7. MCF54410 Pinout (196 MAPBGA)

4 Electrical characteristics

This document contains electrical specification tables and reference timing diagrams for the MCF5441*x* microprocessor. This section contains detailed information on AC/DC electrical characteristics and AC timing specifications.

NOTE

The specifications for this device in any other document are superseded by the specifications in this document.

4.1 Absolute maximum ratings

Table 6. Absolute maximum ratings[1, 2]

Rating	Symbol	Pin name	Value	Units
External I/O pad supply voltage	EV_{DD}	EVDD	–0.3 to +4.0	V
Internal logic supply voltage	IV_{DD}	IVDD	–0.5 to +2.0	V
FlexBus I/O pad supply voltage	FBV_{DD}	FB_VDD	–0.3 to +4.0	V
SDRAM I/O pad supply voltage	SDV_{DD}	SD_VDD	–0.3 to +4.0	V
PLL supply voltage	PV_{DD}	VDD_OSC_A_PLL	–0.3 to +4.0	V
USB OTG supply voltage	$USBV_{DD}$	VDD_USBO	–0.3 to +4.0	V
USB host supply voltage	$USBV_{DD}$	VDD_USBH	–0.3 to +4.0	V
ADC supply voltage	AV_{DD}	VDDA_ADC	–0.3 to +4.0	V
DAC and ADC supply voltage	—	VDDA_DAC_ADC	–0.3 to +4.0	V
RTC standby supply voltage	$RTCV_{STBY}$	VSTBY_RTC	–0.3 to +4.0	V
Digital input voltage[3]	V_{IN}	—	–0.3 to +3.6	V
Instantaneous maximum current Single pin limit (applies to all pins) [3, 4, 5]	I_{DD}	—	25	mA
Operating temperature range (packaged)	T_A ($T_L - T_H$)	—	–40 to +85	°C
Storage temperature range	T_{stg}	—	–55 to +150	°C

1 Functional operating conditions are given in Table 11. Absolute maximum ratings are stress ratings only, and functional operation at the maximum is not guaranteed. Continued operation at these levels may affect device reliability or cause permanent damage to the device.

2 This device contains circuitry protecting against damage due to high static voltage or electrical fields. However, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Immunity to static and electrical fields is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., V_{SS} or EV_{DD}).

3 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, and then use the larger of the two values.

4 All functional non-supply pins are internally clamped to V_{SS} and EV_{DD} .

5 Power supply must maintain regulation within operating EV_{DD}, FBV_{DD}, and SDV_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{in} > EV_{DD}$, FBV_{DD}, or SDV_{DD}) is greater than I_{DD}, the injection current may flow out of EV_{DD}, FBV_{DD}, or SDV_{DD} and could result in external power supply going out of regulation. Ensure the external EV_{DD}, FBV_{DD}, or SDV_{DD} load shunts current greater than maximum injection current. This is the greatest risk when the MPU is not consuming power (for example, no clock).

Table 12. Output pad slew rates (continued)

Pad type[1]	Slew rate select field value	Drive load (pF)	Rise/fall time (ns)
msr	11	50	1.2
		200	6
	10	50	9
		200	14
	01	50	17
		200	23
	00	50	110
		200	120
fsr	11	50	1.1
		200	2.6
	10	50	2.4
		200	5
	01	50	5
		200	8
	00	50	16
		200	21

[1] The ae pads are used for USB communication and are governed by usb.org specifications. They are not included in this table.

4.7 DDR pad drive strengths

The DDR pins on the MCF5441x devices have programmable drive strengths. Table 13 lists the drive strengths for pins based on the value programmed into the appropriate field of the drive strength control register. Refer to Table 5 for a list of the external signals to pad connections.

NOTE

For a single device drive, this setting should be 00 to enable Half Strength mode. High strength is intended for multiple device drives (DIMM).

Table 13. DDR pad drive strengths

Pad type	Drive strength select field value	Drive strength
st	00	Half strength 1.8V DDR2
	01	Full strength 1.8V DDR2
	10	Reserved
	11	Reserved

4.8 Oscillator and PLL electrical characteristics

Reference Figure 9 for crystal circuits.

Table 14. PLL electrical characteristics

Num	Characteristic	Symbol	Min	Max	Unit
1	PLL Reference Frequency Range[1] Crystal reference External reference	 $f_{ref\_crystal}$ f_{ref_ext}	 14[1] 14[1]	 50[1] 50[1]	 MHz MHz
2	Core frequency FB_CLK frequency[2] (MISCCR2[FBHALF] = 0)	f_{sys} $f_{sys/2}$	120 60	250 100	MHz MHz
3	VCO frequency	f_{vco}	240	500	MHz
4	DCC frequency[3]	f_{DCC}	300	500	MHz
5	Crystal start-up time[4, 5]	t_{cst}	—	10	ms
6	EXTAL input high voltage External and limp modes	V_{IHEXT}	EV_{IH}	EVDD	V
7	EXTAL input low voltage External and limp modes	V_{ILEXT}	0	EV_{IL}	V
8	PLL lock time [4, 6]	t_{lpll}	—	50	ms
9	Duty cycle of reference [4]	t_{dc}	–45%	+45%	%
10	Crystal capacitive load	C_L	—	From crystal spec	pF
11	Feedback resistor	R_F	10	—	MΩ
12	Series resistor	R_S	0	200	Ω
13	Discrete load capacitance for XTAL	C_{L_XTAL}	—	$2 \times C_L - C_{S\_XTAL} - C_{PCB\_XTAL}$[7]	pF
14	Discrete load capacitance for EXTAL	C_{L_EXTAL}	—	$2 \times C_L - C_{S\_EXTAL} - C_{PCB\_EXTAL}$[7]	pF
15	FB_CLK period jitter, [4, 5, 7, 8,] Measured at f_{SYS} Max Peak-to-peak jitter (clock edge to clock edge) Long term jitter	C_{jitter}	 — —	 10 0.1	 % $f_{sys/3}$ % $f_{sys/3}$

1 These reference value ranges are for after a PLL predivider (PREDIV), which can be programmed to 1, 2, 4, 8, or 16. The PREDIV value can be set while booting from serial flash. In parallel reset configuration, the PREDIV value is set to one. In this mode, if the input frequency results in an out of range reference frequency, boot the processor in limp mode, set the proper PREDIV and multiplier settings, and switch to PLL mode.

2 All internal registers retain data at 0 Hz.

3 Required only for DDR2 memory.

4 This parameter is guaranteed by characterization before qualification rather than 100% tested.

5 Proper PC board layout procedures must be followed to achieve specifications.

6 This specification is the PLL lock time only and does not include oscillator start-up time.

7 C_{PCB_EXTAL} and C_{PCB_XTAL} are the measured PCB stray capacitances on EXTAL and XTAL, respectively.

8 Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{sys}. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the PLL circuitry via PLL V_{DD}, EV_{DD}, and V_{SS} and variation in crystal oscillator frequency increase the Cjitter percentage for a given interval.

4.15.1 eSDHC timing specifications

Figure 20 depicts the timing of eSDHC, and Table 20 lists the eSDHC timing characteristics.

Table 20. eSDHC interface timing specifications

ID	Parameter	Symbols	Min	Max	Unit
Card Input Clock					
SD1	Clock frequency (low speed)	f_{PP}[1]	0	400	kHz
	Clock frequency (SD/SDIO full speed)	f_{PP}[2]	0	40	MHz
	Clock frequency (MMC full speed)	f_{PP}[3]	0	20	MHz
	Clock frequency (identification mode)	f_{OD}[4]	100	400	kHz
SD2	Clock low time	t_{WL}	7	—	ns
SD3	Clock high time	t_{WH}	7	—	ns
SD4	Clock rise time	t_{TLH}	—	3	ns
SD5	Clock fall time	t_{THL}	—	3	ns
eSDHC Output / card inputs SDHC_CMD, SDHC_DAT (reference to SDHC_CLK)					
SD6	eSDHC output delay (output valid)	t_{OD}	–5	5	ns
eSDHC Input / card outputs SDHC_CMD, SDHC_DAT (reference to SDHC_CLK)					
SD7	eSDHC input setup time	t_{ISU}	5	—	ns
SD8	eSDHC input hold time	t_{IH}	0	—	ns

1 In low speed mode, card clock must be lower than 400 kHz, voltage ranges from 2.7 to 3.6 V.

2 In normal data transfer mode for SD/SDIO card, clock frequency can be any value from 0 to 25 MHz.

3 In normal data transfer mode for MMC card, clock frequency can be any value from 0 to 20 MHz.

4 In card identification mode, card clock must be 100 kHz– 400 kHz, voltage ranges from 2.7 to 3.6 V.

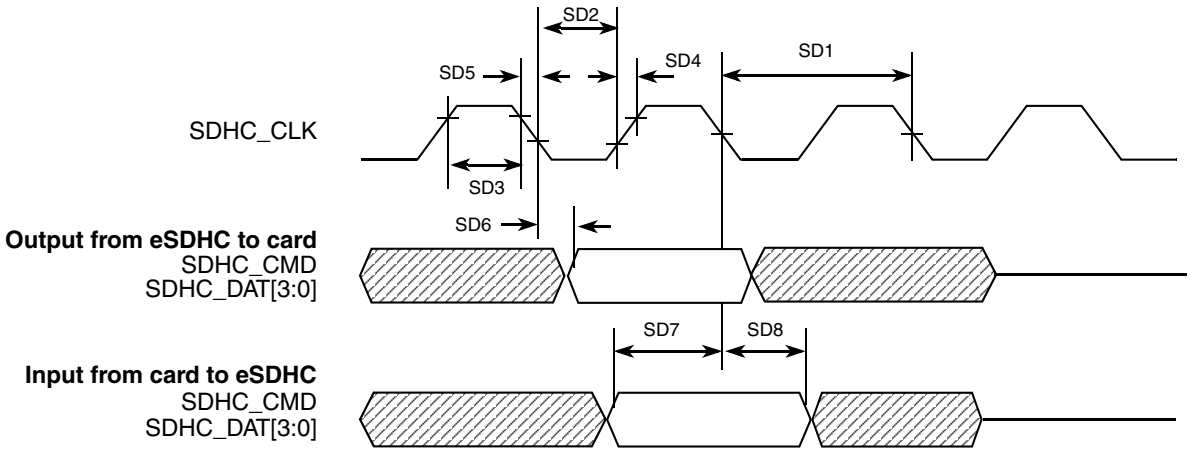


Figure 20. eSDHC timing

4.15.2 eSDHC electrical DC characteristics

Table 21 lists the eSDHC electrical DC characteristics.

Table 21. MMC/SD interface electrical specifications

Num	Parameter	Design value	Min	Max	Unit	Condition/remark
Bus signal line load						
7	Pull-up resistance	47	10	100	kΩ	Internal PU
8	Open drain resistance	NA	NA	NA	kΩ	For MMC cards only
Open drain signal level						For MMC cards only
9	Output high voltage		V_{DD} – 0.2		V	I_{OH} = –100 µA
10	Output low voltage			0.3	V	I_{OL} = 2 mA
Bus signal levels						
11	Output high voltage		0.75 x V_{DD}		V	I_{OH} = –100 µA @V_{DD} min
12	Output low voltage			0.125 x V_{DD}	V	I_{OL} = 100 µA @V_{DD} min
13	Input high voltage		0.625 x V_{DD}	V_{DD} + 3	V	
14	Input low voltage		V_{SS} – 0.3	0.25 x V_{DD}	V	

4.16 SIM timing specifications

Each SIM card interface consist of a total of 12 pins (two separate ports of six pins each. Mostly one port with 5 pins is used).

The interface is meant to be used with synchronous SIM cards. This means that the SIM module provides a clock for the SIM card to use. The frequency of this clock is normally 372 times the data rate on the TX/RX pins, however SIM module can work with CLK equal to 16 times the data rate on TX/RX pins.

There is no timing relationship between the clock and the data. The clock that the SIM module provides to the SIM card is used by the SIM card to recover the clock from the data, like a standard UART. All six (or five when a bidirectional TXRX is used) of the pins for each half of the SIM module are asynchronous to each other. There are no required timing relationships between the signals in normal mode. However, there are some in reset and power down sequences.

All SIM signals use pad type pad_msr. SIM timing is fairly relaxed compared to other interfaces and can be met at 50 pF loading with any slew rate setting other than 00.[1]

1.These timing parameters are specified assuming maximum operating frequency and the fastest pad slew rate setting (11). When operating this interface at lower frequencies, increase the slew rate by using the 10, 01, or 00 setting to increase edge rise and fall times, thus reducing EMI.

Table 24. SSI timing — master modes[1]

Num	Description	Symbol	Min	Max	Units	Notes
S1	SSI_MCLK cycle time	t_{MCLK}	15.15	—	ns	[2]
S2	SSI_MCLK pulse width high / low		45%	55%	t_{MCLK}	
S3	SSI_BCLK cycle time	t_{BCLK}	80	—	ns	[3]
S4	SSI_BCLK pulse width		45%	55%	t_{BCLK}	
S5	SSI_BCLK to SSI_FS output valid		—	15	ns	
S6	SSI_BCLK to SSI_FS output invalid		0	—	ns	
S7	SSI_BCLK to SSI_TXD valid		—	15	ns	
S8	SSI_BCLK to SSI_TXD invalid / high impedance		0	—	ns	
S9	SSI_RXD / SSI_FS input setup before SSI_BCLK		15	—	ns	
S10	SSI_RXD / SSI_FS input hold after SSI_BCLK		0	—	ns	

1 All timings specified with a capacitive load of 25pF.

2 SSI_MCLK can be generated from SSI_CLKIN or a divided version of the internal system clock (f_{sys}).

3 SSI_BCLK can be derived from SSI_CLKIN or a divided version of the internal system clock (f_{sys}).

Table 25. SSI timing — slave modes[1]

Num	Description	Symbol	Min	Max	Units	Notes
S11	SSI_BCLK cycle time	t_{BCLK}	80	—	ns	
S12	SSI_BCLK pulse width high / low		45%	55%	t_{BCLK}	
S13	SSI_FS input setup before SSI_BCLK		10	—	ns	
S14	SSI_FS input hold after SSI_BCLK		2	—	ns	
S15	SSI_BCLK to SSI_TXD / SSI_FS output valid		—	15	ns	
S16	SSI_BCLK to SSI_TXD / SSI_FS output invalid / high impedance		0	—	ns	
S17	SSI_RXD setup before SSI_BCLK		15	—	ns	
S18	SSI_RXD hold after SSI_BCLK		2	—	ns	

1 All timings specified with a capacitive load of 25pF.

4.25 SBF timing specifications

The Serial boot facility (SBF) provides a means to read configuration information and system boot code from a broad array of SPI-compatible EEPROMs, flashes, FRAMs, nVSRAMs, etc. Table 37 provides the AC timing specifications for the SBF.

All SBF signals use pad type pad_msr. The following timing specifications assume a pad slew rate setting of 11 and a load of 50 pF.[1]

Table 37. SBF AC timing specifications

Name	Characteristic	Symbol	Min	Max	Unit	Notes
—	SBF_CK frequency	f_{SBFCK}	—	62.5	MHz	
SB1	SBF_CK cycle time	t_{SBFCK}	16.67	—	ns	1
SB2	SBF_CK high/low time	—	30%	—	t_{SBFCK}	
SB3	$\overline{SBF\_CS}$ to SBF_CK delay	—	$t_{SBFCK} - 2.0$	—	ns	
SB4	SBF_CK to $\overline{SBF\_CS}$ delay	—	$t_{SBFCK} - 2.0$	—	ns	
SB5	SBF_CK to SBF_DO valid	—	—	5	ns	
SB6	SBF_CK to SBF_DO invalid	—	–5	—	ns	
SB7	SBF_DI to SBF_SCK input setup	—	10	—	ns	
SB8	SBF_CK to SBF_DI input hold	—	0	—	ns	

1 At reset, the SBF_CK cycle time is $t_{REF} \times 60$. The first byte of data read from the serial memory contains a divider value that is used to set the SBF_CK cycle time for the duration of the serial boot process.

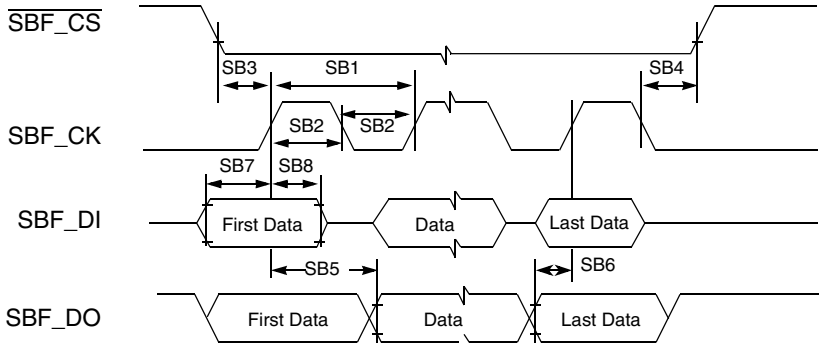


Figure 34. SBF timing

1.These timing parameters are specified assuming maximum operating frequency and the fastest pad slew rate setting (11). When operating this interface at lower frequencies, increase the slew rate by using the 10, 01, or 00 setting to increase edge rise and fall times, thus reducing EMI.

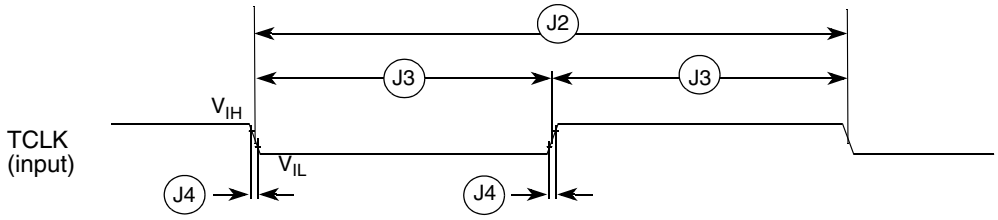


Figure 37. Test clock input timing

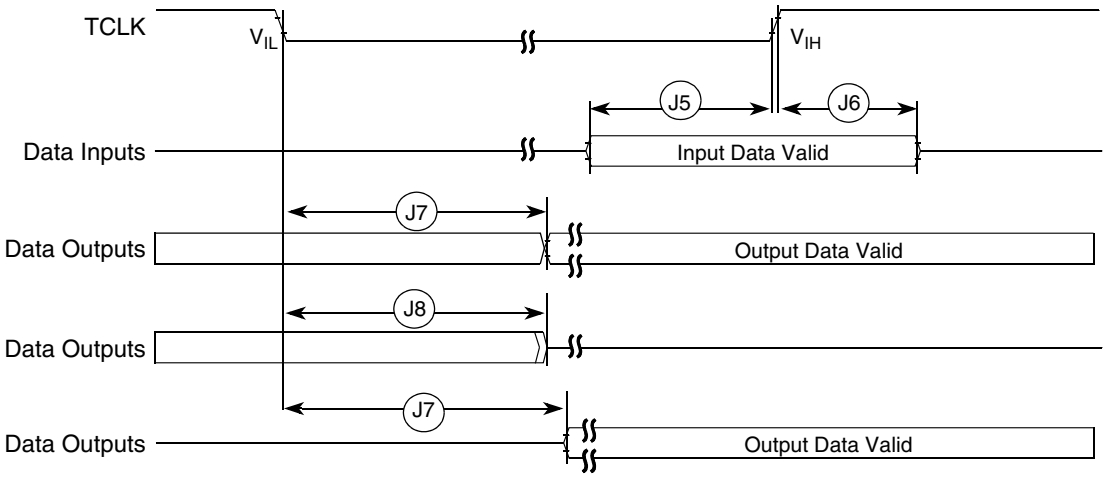


Figure 38. Boundary scan (JTAG) timing

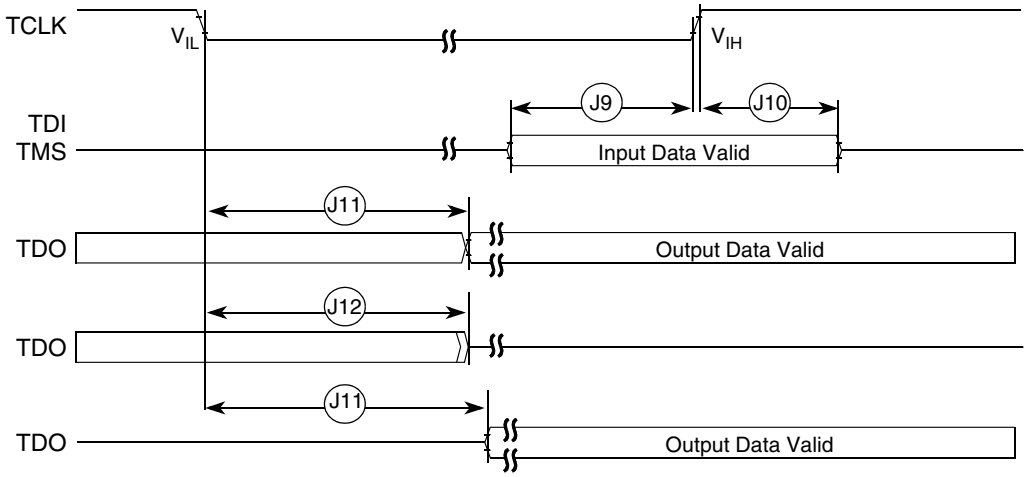


Figure 39. Test access port timing

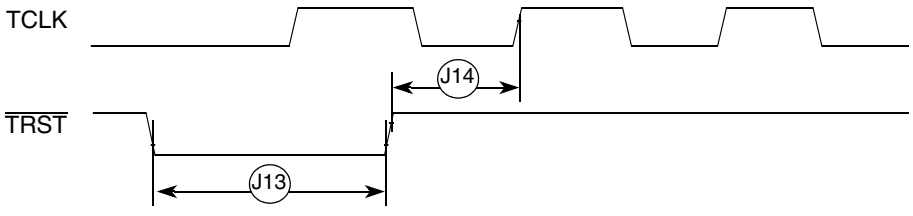


Figure 40. $\overline{\text{TRST}}$ timing

5 Package information

The latest package outline drawings are available on the product summary pages on http://www.freescale.com/coldfire. Table 42 lists the case outline numbers per device. Use these numbers in the web page's keyword search engine to find the latest package outline drawings.

Table 42. Package information

Device	Package type	Case outline numbers
MCF54410	196 MAPBGA	98ASA00321D
MCF54415	256 MAPBGA	98ARH98219A
MCF54416		
MCF54417		
MCF54418		

6 Product documentation

Documentation is available from a local Freescale distributor, a Freescale sales office, the Freescale Literature Distribution Center, or through the Freescale world-wide web address at http://www.freescale.com/coldfire.

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