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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z4d
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, LINbus, SPI, UART/USART
Peripherals	DMA, POR, PWM, WDT
Number of I/O	147
Program Memory Size	1.5MB (1.5M x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 27x10b, 5x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP
Supplier Device Package	176-LQFP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/spc564b64l7c800x

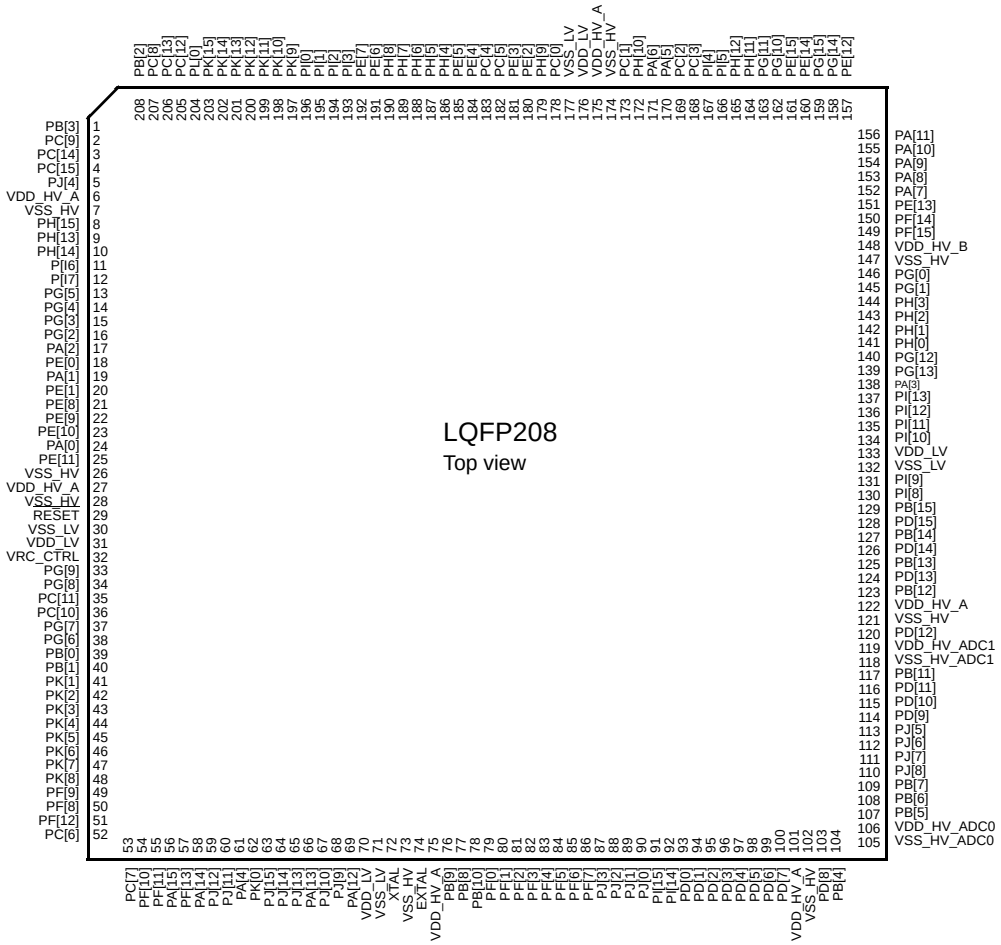
Table 1. Device summary

Package	Part number		
	1.5 MByte	2 MByte	3 MByte
LQFP176	SPC564B64L7 SPC56EC64L7	SPC564B70L7 SPC56EC70L7	SPC564B74L7 SPC56EC74L7
LQFP208	SPC564B64L8 SPC56EC64L8	SPC564B70L8 SPC56EC70L8	SPC564B74L8 SPC56EC74L8
LBGA256	SPC56EC64B3	SPC56EC70B3	SPC56EC74B3

Table 2. SPC564Bxx and SPC56ECxx family comparison[1]

Feature		SPC564B64		SPC56EC64			SPC564B70		SPC56EC70			SPC564B74		SPC56EC74		
Package		LQFP 176	LQFP 208	LQFP 176	LQFP 208	LBGA 256	LQFP 176	LQFP 208	LQFP 176	LQFP 208	LBGA 256	LQFP 176	LQFP 208	LQFP 176	LQFP 208	LBGA 256
CPU		e200z4d		e200z4d + e200z0h			e200z4d		e200z4d + e200z0h			e200z4d		e200z4d + e200z0h		
Execution speed[2]		Up to 120 MHz (e200z4d)		Up to 120 MHz (e200z4d) Up to 80 MHz (e200z0h)[3]			Up to 120 MHz (e200z4d)		Up to 120 MHz (e200z4d) Up to 80 MHz (e200z0h)[3]			Up to 120 MHz (e200z4d)		Up to 120 MHz (e200z4d) Up to 80 MHz (e200z0h)[3]		
Code flash memory		1.5 MB					2 MB					3 MB				
Data flash memory		4 x16 KB														
SRAM		128 KB		192 KB			160 KB		256 KB			192 KB		256 KB		
MPU		16-entry														
eDMA[4]		32 ch														
10-bit ADC		27 ch	33 ch	27 ch	33 ch		27 ch	33 ch	27 ch	33 ch		27 ch	33 ch	27 ch	33 ch	
	dedicated[5], [6]															
	shared with 12-bit ADC[7]	19 ch														
12-bit ADC		5 ch	10 ch	5 ch	10 ch		5 ch	10 ch	5 ch	10 ch		5 ch	10 ch	5 ch	10 ch	
	dedicated[8]															
	shared with 10-bit ADC[7]	19 ch														
CTU		64 ch														
Total timer I/O[9] eMIOS		64 ch, 16-bit														
SCI (LINFlexD)		10														
SPI (DSPI)		8														
CAN (FlexCAN)[10]		6														

Figure 3. 208-pin LQFP configuration



NOTE
1) VDD_HV_B supplies the IO voltage domain for the pins PE[12], PA[11], PA[10], PA[9], PA[8], PA[7], PE[13], PF[14], PF[15], PG[0], PG[1], PH[3], PH[2], PH[1], PH[0], PG[12], PG[13], and PA[3].
2) Availability of port pin alternate functions depends on product selection.

2.1 Pad types

In the device the following types of pads are available for system pins and functional port pins:

S = Slow[a]

M = Medium[a],[b]

F = Fast[a],[b]

I = Input only with analog feature[a]

A = Analog

2.2 System pins

The system pins are listed in *Table 4*.

Table 4. System pin descriptions

Port pin	Function	I/O direction	Pad type	RESET config.	Pin number		
					LQFP 176	LQFP 208	LBGA 256
RESET	Bidirectional reset with Schmitt-Trigger characteristics and noise filter.	I/O	M	Input, weak pull-up only after PHASE2	29	29	K1
EXTAL	Analog input of the oscillator amplifier circuit. Needs to be grounded if oscillator bypass mode is used.	I	A[1]	—	58	74	T8
XTAL	Analog output of the oscillator amplifier circuit, when the oscillator is not in bypass mode. Analog input for the clock generator when the oscillator is in bypass mode.	I/O	A[1]	—	56	72	T7

1. For analog pads, it is not recommended to enable IBE if APC is enabled to avoid extra current in middle range voltage.

a. See the I/O pad electrical characteristics in the device datasheet for details.

b. All medium and fast pads are in slow configuration by default at reset and can be configured as fast or medium. For example, Fast/Medium pad will be Medium by default at reset. Similarly, Slow/Medium pad will be Slow by default. Only exception is PC[1] which is in medium configuration by default (refer to PCR.SRC in the reference manual, Pad Configuration Registers (PCR0—PCR198)).

Table 5. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET config.	Pin number		
								LQFP 176	LQFP 208	LBGA256
PC[14]	PCR[46]	AF0 AF1 AF2 AF3 ALT4 —	GPIO[46] E0UC[14] SCK_2 — FR_DBG[2] EIRQ[8]	SIUL eMIOS_0 DSPI_2 — Flexray SIUL	I/O I/O I/O — O I	M/S	Tristate	3	3	B2
PC[15]	PCR[47]	AF0 AF1 AF2 AF3 ALT4	GPIO[47] E0UC[15] CS0_2 — FR_DBG[3] EIRQ[20]	SIUL eMIOS_0 DSPI_2 — Flexray SIUL	I/O I/O I/O — O I	M/S	Tristate	4	4	A1
PD[0]	PCR[48]	AF0 AF1 AF2 AF3 — — —	GPI[48] — — — ADC0_P[4] ADC1_P[4] WKPU[27]	SIUL — — — ADC_0 ADC_1 WKPU	I — — — I I I	I	Tristate	77	93	R12
PD[1]	PCR[49]	AF0 AF1 AF2 AF3 — — —	GPI[49] — — — ADC0_P[5] ADC1_P[5] WKPU[28]	SIUL — — — ADC_0 ADC_1 WKPU	I — — — I I I	I	Tristate	78	94	T13
PD[2]	PCR[50]	AF0 AF1 AF2 AF3 — —	GPI[50] — — — ADC0_P[6] ADC1_P[6]	SIUL — — — ADC_0 ADC_1	I — — — I I	I	Tristate	79	95	N11

Table 5. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET config.	Pin number		
								LQFP 176	LQFP 208	LBGA256
PF[14]	PCR[94]	AF0 AF1 AF2 AF3 ALT4	GPIO[94] CAN4TX E1UC[27] CAN1TX MDIO	SIUL FlexCAN_4 eMIOS_1 FlexCAN_1 FEC	I/O O I/O O I/O	M/S	Tristate	126	150	D14
PF[15]	PCR[95]	AF0 AF1 AF2 AF3 — — — —	GPIO[95] E1UC[4] — — RX_DV CAN1RX CAN4RX EIRQ[13]	SIUL eMIOS_1 — — FEC FlexCAN_1 FlexCAN_4 SIUL	I/O I/O — — I I I I	M/S	Tristate	125	149	D15
PG[0]	PCR[96]	AF0 AF1 AF2 AF3 ALT4	GPIO[96] CAN5TX E1UC[23] — MDC	SIUL FlexCAN_5 eMIOS_1 — FEC	I/O O I/O — O	F	Tristate	122	146	E13
PG[1]	PCR[97]	AF0 AF1 AF2 AF3 — — —	GPIO[97] — E1UC[24] — TX_CLK CAN5RX EIRQ[14]	SIUL — eMIOS_1 — FEC FlexCAN_5 SIUL	I/O — I/O — I I I	M	Tristate	121	145	E14
PG[2]	PCR[98]	AF0 AF1 AF2 AF3	GPIO[98] E1UC[11] SOUT_3 —	SIUL eMIOS_1 DSPI_3 —	I/O I/O O —	M/S	Tristate	16	16	E4
PG[3]	PCR[99]	AF0 AF1 AF2 AF3 —	GPIO[99] E1UC[12] CS0_3 — WKPU[17]	SIUL eMIOS_1 DSPI_3 — WKPU	I/O I/O I/O — I	S	Tristate	15	15	E1

Table 5. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET config.	Pin number		
								LQFP 176	LQFP 208	LBGA256
PJ[3]	PCR[147]	AF0 AF1 AF2 AF3 —	GPIO[147] CS1_5 CS1_6 CS1_7 ADC0_S[27]	SIUL DSPI_5 DSPI_6 DSPI_7 ADC_0	I/O O O O I	S	Tristate	71	87	P10
PJ[4]	PCR[148]	AF0 AF1 AF2 AF3	GPIO[148] SCK_5 E1UC[18] —	SIUL DSPI_5 eMIOS_1 —	I/O I/O I/O —	M/S	Tristate	5	5	D3
PJ[5]	PCR[149]	AF0 AF1 AF2 AF3 —	GPIO[149] — — — ADC0_S[28]	SIUL — — — ADC_0	I/O — — — I	S	Tristate	—	113	N12
PJ[6]	PCR[150]	AF0 AF1 AF2 AF3 —	GPIO[150] — — — ADC0_S[29]	SIUL — — — ADC_0	I/O — — — I	S	Tristate	—	112	N15
PJ[7]	PCR[151]	AF0 AF1 AF2 AF3 —	GPIO[151] — — — ADC0_S[30]	SIUL — — — ADC_0	I/O — — — I	S	Tristate	—	111	P16
PJ[8]	PCR[152]	AF0 AF1 AF2 AF3 —	GPIO[152] — — — ADC0_S[31]	SIUL — — — ADC_0	I/O — — — I	S	Tristate	—	110	P15
PJ[9]	PCR[153]	AF0 AF1 AF2 AF3 —	GPIO[153] — — — ADC1_S[8]	SIUL — — — ADC_1	I/O — — — I	S	Tristate	—	68	P5

Table 5. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET config.	Pin number		
								LQFP 176	LQFP 208	LBGA256
PM[5]	PCR[197]	AF0 AF1 AF2 AF3	GPIO[197] — — —	SIUL — — —	I/O — — —	M/S	Tristate	—	—	F9
PM[6]	PCR[198]	AF0 AF1 AF2 AF3	GPIO[198] — — —	SIUL — — —	I/O — — —	M/S	Tristate	—	—	F6

1. Alternate functions are chosen by setting the values of the PCR.PA bitfields inside the SIUL module. PCR.PA = 000 → AF0; PCR.PA = 001 → AF1; PCR.PA = 010 → AF2; PCR.PA = 011 → AF3; PCR.PA = 100 → ALT4. This is intended to select the output functions; to use one of the input functions, the PCR.IBE bit must be written to '1', regardless of the values selected in the PCR.PA bitfields. For this reason, the value corresponding to an input only function is reported as "—".
2. Multiple inputs are routed to all respective modules internally. The input of some modules must be configured by setting the values of the PSMIO.PADSELx bitfields inside the SIUL module.
3. NMI[0] and NMI[1] have a higher priority than alternate functions. When NMI is selected, the PCR.PA field is ignored.
4. SXOSC's OSC32k_XTAL and OSC32k_EXTAL pins are shared with GPIO functionality. When used as crystal pins, other functionality of the pin cannot be used and it should be ensured that application never programs OBE and PUE bit of the corresponding PCR to "1".
5. If you want to use OSC32K functionality through PB[8] and PB[9], you must ensure that PB[10] is static in nature as PB[10] can induce coupling on PB[9] and disturb oscillator frequency.
6. Out of reset all the functional pins except PC[0:1] and PH[9:10] are available to the user as GPIO.
   PC[0:1] are available as JTAG pins (TDI and TDO respectively).
   PH[9:10] are available as JTAG pins (TCK and TMS respectively).
   It is up to the user to configure these pins as GPIO when needed.
7. When MBIST is enabled to run (STCU Enable = 1), the application must not drive or tie PAD[178] (MDO[0]) to 0 V before the device exits reset (external reset is removed) as the pad is internally driven to 1 to indicate MBIST operation. When MBIST is not enabled (STCU Enable = 0), there are no restriction as the device does not internally drive the pad.
8. These pins can be configured as Nexus pins during reset by the debugger writing to the Nexus Development Interface "Port Control Register" rather than the SIUL. Specifically, the debugger can enable the MDO[7:0], MSEO, and MCKO ports by programming NDI (PCR[MCKO_EN] or PCR[PSTAT_EN]). MDO[8:11] ports can be enabled by programming NDI ((PCR[MCKO_EN] and PCR[FPM]) or PCR[PSTAT_EN]).

Table 11. Recommended operating conditions (5.0 V) (continued)

Symbol		Parameter	Conditions	Value		Unit
				Min	Max	
$V_{DD\_HV\_ADC0}$ (5)	SR	Voltage on VDD_HV_ADC0 with respect to ground (V_{SS_HV})	—	4.5	5.5	V
			Voltage drop(2)	3.0	5.5	
			Relative to $V_{DD\_HV\_A}$(6)	$V_{DD\_HV\_A}$ – 0.1	$V_{DD\_HV\_A}$ + 0.1	
$V_{DD\_HV\_ADC1}$ (7)	SR	Voltage on VDD_HV_ADC1 with respect to ground (V_{SS_HV})	—	4.5	5.5	V
			Voltage drop(2)	3.0	5.5	
			Relative to $V_{DD\_HV\_A}$(6)	$V_{DD\_HV\_A}$ – 0.1	$V_{DD\_HV\_A}$ + 0.1	
V_{IN}	SR	Voltage on any GPIO pin with respect to ground (V_{SS_HV})	—	V_{SS_HV} –0.1	—	V
			Relative to $V_{DD\_HV\_A/HV\_B}$	—	$V_{DD\_HV\_A/HV\_B}$ + 0.1	
I_{INJPAD}	SR	Injected input current on any pin during overload condition	—	–5	5	mA
I_{INJSUM}	SR	Absolute sum of all injected input currents during overload condition	—	–50	50	
TV_{DD}	SR	$V_{DD\_HV\_A}$ slope to ensure correct power up(8)	—	—	0.5	V/µs
			—	0.5	—	V/min
T_{A} C-Grade Part	SR	Ambient temperature under bias	—	–40	85	°C
T_{J} C-Grade Part	SR	Junction temperature under bias	—	–40	110	
T_{A} V-Grade Part	SR	Ambient temperature under bias	—	–40	105	
T_{J} V-Grade Part	SR	Junction temperature under bias	—	–40	130	
T_{A} M-Grade Part	SR	Ambient temperature under bias	—	–40	125	
T_{J} M-Grade Part	SR	Junction temperature under bias	—	–40	150	

1. 100 nF EMI capacitance need to be provided between each VDD/VSS_HV pair.
2. Full device operation is guaranteed by design from 3.0 V–5.5 V. OSC functionality is guaranteed from the entire range 3.0V–5.5 V, the parametrics measured are at 3.0V and 5.5V (extreme voltage ranges to cover the range of operation). The parametrics might have some variation in the intermediate voltage range, but there is no impact to functionality.
3. 100 nF EMI capacitance needs to be provided between each VDD_LV/VSS_LV supply pair. 10 µF bulk capacitance needs to be provided as CREG on each VDD_LV pin.
4. This voltage is internally generated by the device and no external voltage should be supplied.
5. 100 nF capacitance needs to be provided between $V_{DD\_HV\_(ADC0/ADC1)}$/$V_{SS\_HV\_(ADC0/ADC1)}$ pair.
6. Both the relative and the fixed conditions must be met. For instance: If $V_{DD\_HV\_A}$ is 5.9 V, $V_{DD\_HV\_ADC0}$ maximum value is 6.0 V then, despite the relative condition, the max value is $V_{DD\_HV\_A}$ + 0.3 = 6.2 V.
7. PA3, PA7, PA10, PA11 and PE12 ADC_1 channels are coming from $V_{DD\_HV\_B}$ domain hence VDD_HV_ADC1 should be within ±100 mV of $V_{DD\_HV\_B}$ when these channels are used for ADC_1.

8. Guaranteed by device validation.

Note: SRAM retention guaranteed to LVD levels.

3.5 Thermal characteristics

3.5.1 Package thermal characteristics

Table 12. LQFP thermal characteristics(1)

Symbol		C	Parameter	Conditions(2)	Pin count	Value(3)			Unit
						Min	Typ	Max	
$R_{\theta JA}$	CC	D	Thermal resistance, junction-to-ambient natural convection	Single-layer board—1s	176	—	—	44.4(4)	°C/W
					208	—	—	43	°C/W
$R_{\theta JA}$	CC	D	Thermal resistance, junction-to-ambient natural convection	Four-layer board—2s2p(5)	176	—	—	36.1	°C/W
					208	—	—	33.9	°C/W

1. Thermal characteristics are targets based on simulation that are subject to change per device characterization.
2. V_{DD} = 3.3 V ± 10 % / 5.0 V ± 10 %, T_A = –40 to 125 °C.
3. All values need to be confirmed during device validation.
4. 1s board as per standard JEDEC (JESD51-7) in natural convection.
5. 2s2p board as per standard JEDEC (JESD51-7) in natural convection.

Table 13. LBGA256 thermal characteristics(1)

Symbol		C	Parameter	Conditions	Value	Unit
$R_{\theta JA}$	CC	—	Thermal resistance, junction-to-ambient natural convection	Single-layer board—1s	44.3	°C/W
				Four-layer board—2s2p	31	

1. Thermal characteristics are targets based on simulation that are subject to change per device characterization.

Figure 13. Equivalent circuit of a quartz crystal

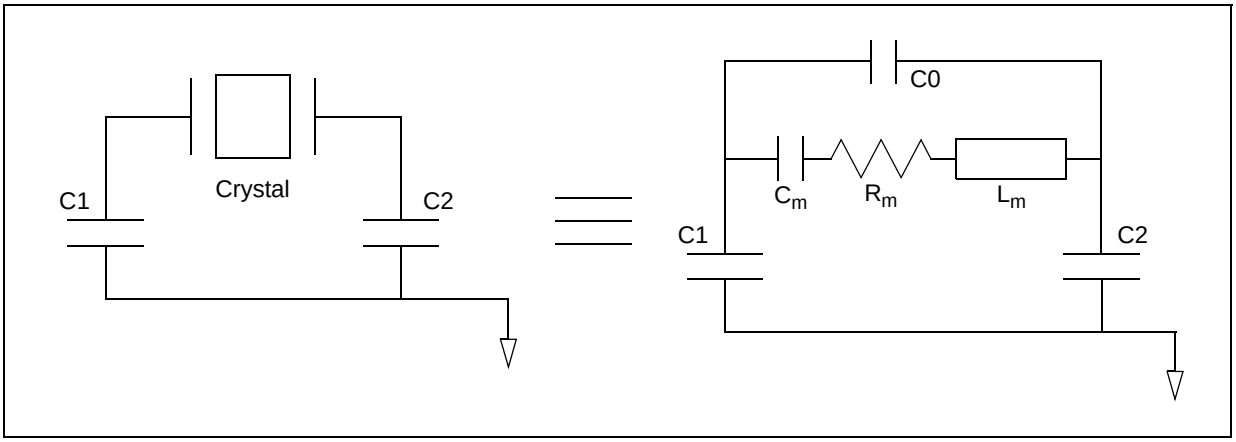


Table 37. Crystal motional characteristics(1)

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
L_m	Motional inductance	—	—	11.796	—	KH
C_m	Motional capacitance	—	—	2	—	fF
C1/C2	Load capacitance at OSC32K_XTAL and OSC32K_EXTAL with respect to ground(2)	—	18	—	28	pF
R_m(3)	Motional resistance	AC coupled @ C0 = 2.85 pF(4)	—	—	65	kW
		AC coupled @ C0 = 4.9 pF(4)	—	—	50	
		AC coupled @ C0 = 7.0 pF(4)	—	—	35	
		AC coupled @ C0 = 9.0 pF(4)	—	—	30	

1. The crystal used is Epson Toyocom MC306.
2. This is the recommended range of load capacitance at OSC32K_XTAL and OSC32K_EXTAL with respect to ground. It includes all the parasitics due to board traces, crystal and package.
3. Maximum ESR (R_m) of the crystal is 50 kΩ.
4. C0 Includes a parasitic capacitance of 2.0 pF between OSC32K_XTAL and OSC32K_EXTAL pins.

Figure 14. Slow external crystal oscillator (32 kHz) electrical characteristics

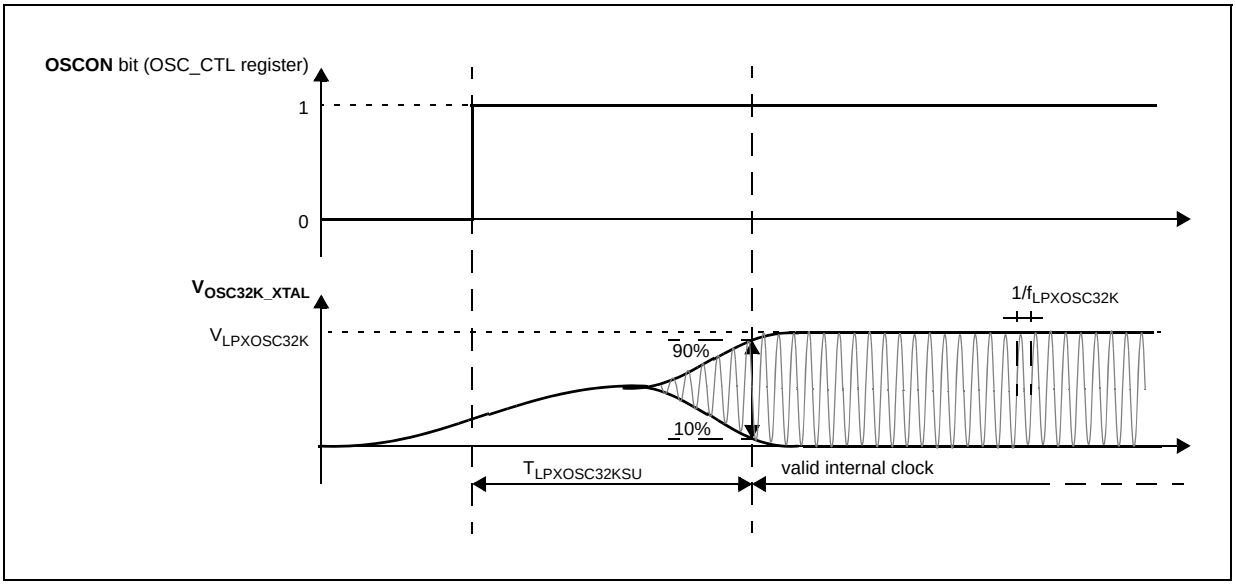
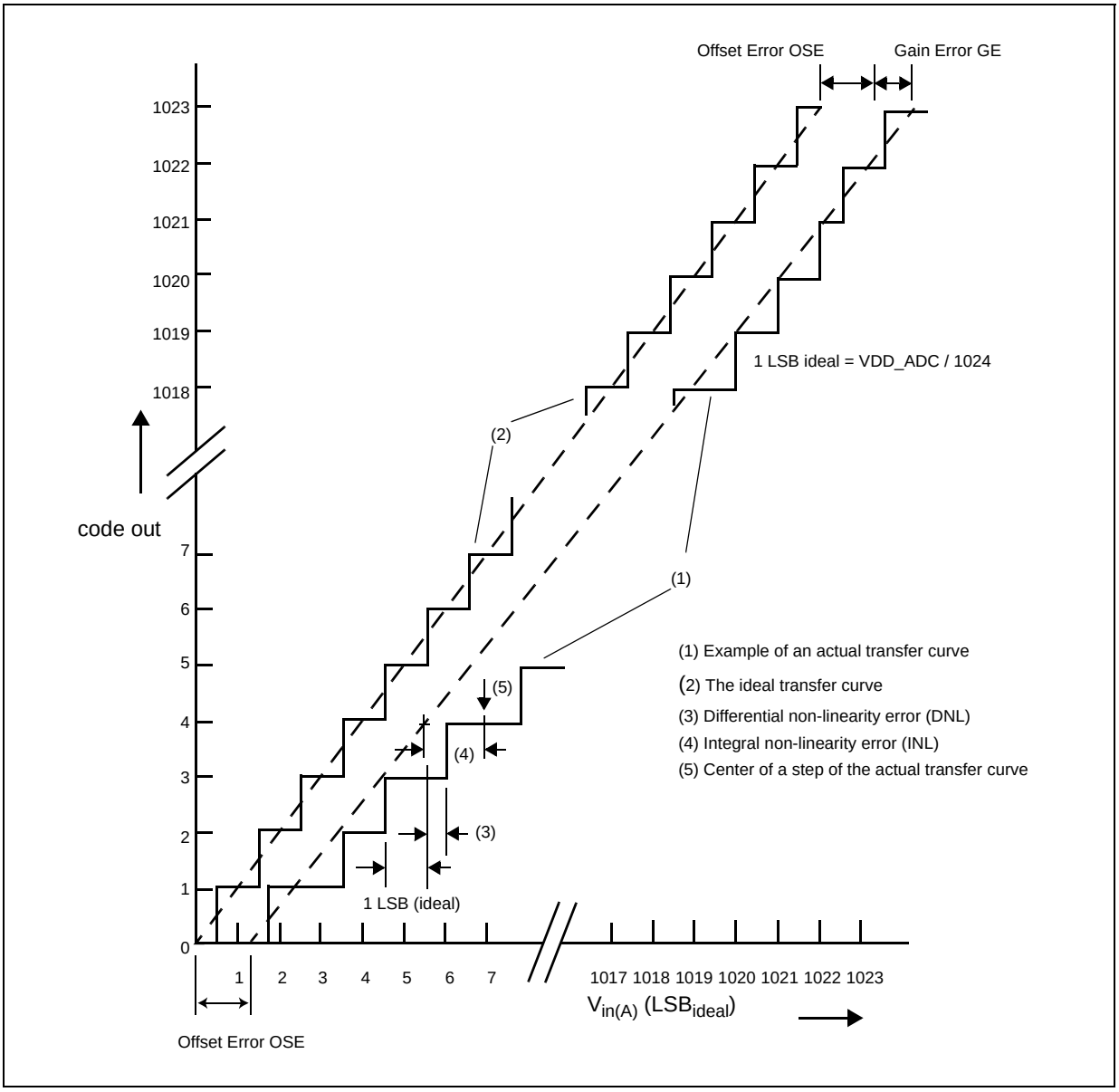


Table 38. Slow external crystal oscillator (32 kHz) electrical characteristics

Symbol		C	Parameter	Conditions[1]	Value[2]			Unit
					Min	Typ	Max	
f_{SXOSC}	SR	—	Slow external crystal oscillator frequency	—	32	32.768	40	kHz
g_{mSXOSC}	CC	—	Slow external crystal oscillator transconductance	V_{DD} = 3.3 V ± 10%,	13[3]	—	33[3]	µA/V
				V_{DD} = 5.0 V ± 10%	15[3]	—	35[3]	
V_{SXOSC}	CC	T	Oscillation amplitude	—	1.2	1.4	1.7	V
$I_{SXOSCBIAS}$	CC	T	Oscillation bias current	—	1.2	—	4.4	µA
I_{SXOSC}	CC	T	Slow external crystal oscillator consumption	—	—	—	7	µA
$T_{SXOSCSU}$	CC	T	Slow external crystal oscillator start-up time	—	—	—	2[4]	s

1. V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified.
2. All values need to be confirmed during device validation.
3. Based on ATE CZ
4. Start-up time has been measured with EPSON TOYOCOM MC306 crystal. Variation may be seen with other crystal.

Figure 15. ADC_0 characteristic and error definitions



3.17.1.1 Input impedance and ADC accuracy

To preserve the accuracy of the A/D converter, it is necessary that analog input pins have low AC impedance. Placing a capacitor with good high frequency characteristics at the input pin of the device, can be effective: the capacitor should be as large as possible, ideally infinite. This capacitor contributes to attenuating the noise present on the input pin; furthermore, it sources charge during the sampling phase, when the analog signal source is a high-impedance source. A real filter, can typically be obtained by using a series resistance with a capacitor on the input pin (simple RC Filter). The RC filtering may be limited according to the value of source impedance of the transducer or circuit supplying the analog signal to be measured. The filter at the input pins must be designed taking into account the dynamic characteristics of the input signal (bandwidth) and the equivalent input impedance of the ADC itself.

Table 49. On-chip peripherals current consumption(1)

Symbol		C	Parameter	Conditions		Value(2) Typ	Unit
IDD_HV_ADC0	CC	D	ADC_0 supply current on $V_{DD\_HV\_ADC0}$	V_{DD} = 5.5 V	Analog static consumption (no conversion)	200	µA
					Analog dynamic consumption (continuous conversion)	4	mA
IDD_HV_ADC1	CC	D	ADC_1 supply current on $V_{DD\_HV\_ADC1}$	V_{DD} = 5.5 V	Analog static consumption (no conversion)	300	µA
				V_{DD} = 5.5 V	Analog dynamic consumption (continuous conversion)	6	mA
$I_{DD\_HV(FLASH)}$	CC	D	CFlash + DFlash supply current on $V_{DD\_HV\_ADC}$	V_{DD} = 5.5 V	—	13.25	mA
$I_{DD\_HV(PLL)}$	CC	D	PLL supply current on V_{DD_HV}	V_{DD} = 5.5 V	—	0.0031 × f_{periph}	

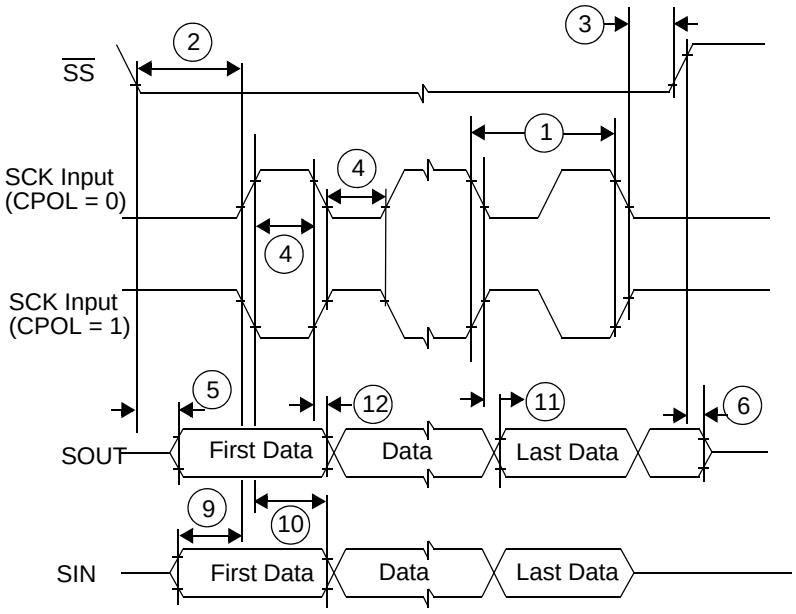
1. Operating conditions: T_A = 25 °C, f_{periph} = 8 MHz to 120 MHz.
2. f_{periph} is in absolute value.

3.19.2 DSPI characteristics

Table 50. DSPI timing

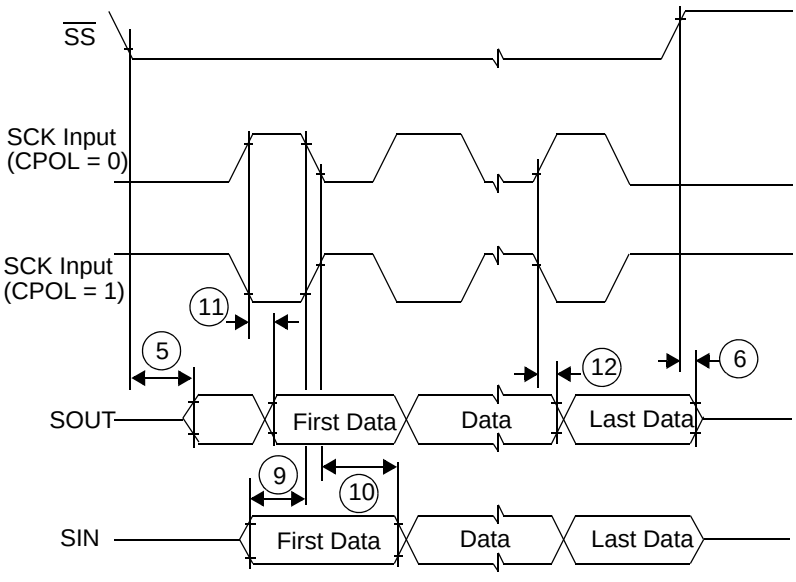
Spec	Characteristic	Symbol	Value Min	Value Max	Unit
1	DSPI Cycle Time	t_{SCK}	Refer note(1)	—	ns
—	Internal delay between pad associated to SCK and pad associated to CSn in master mode for CSn1->0	Δt_{CSC}	—	115	ns
—	Internal delay between pad associated to SCK and pad associated to CSn in master mode for CSn1->1	Δt_{ASC}	15	—	ns
2	CS to SCK Delay(2)	t_{CSC}	7	—	ns
3	After SCK Delay(3)	t_{ASC}	15	—	ns
4	SCK Duty Cycle	t_{SDC}	0.4 × t_{SCK}	0.6 × t_{SCK}	ns

Figure 27. DSPI classic SPI timing–slave, CPHA = 0



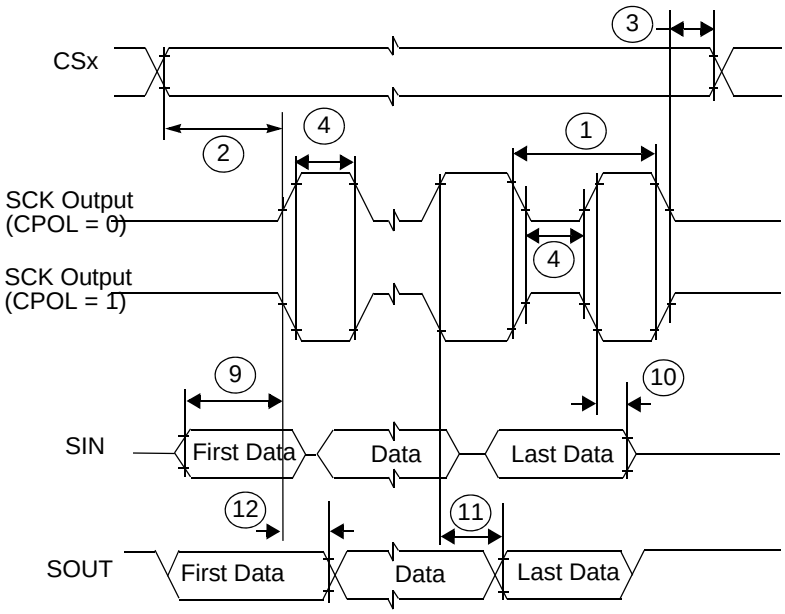
Note: Numbers shown reference *Table 50*.

Figure 28. DSPI classic SPI timing–slave, CPHA = 1



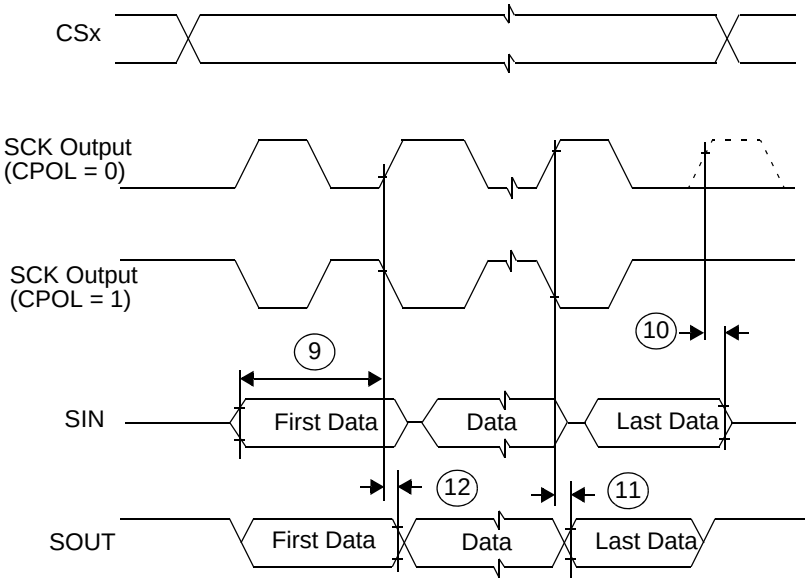
Note: Numbers shown reference *Table 50*.

Figure 29. DSPI modified transfer format timing–master, CPHA = 0



Note: Numbers shown reference *Table 50*.

Figure 30. DSPI modified transfer format timing–master, CPHA = 1



Note: Numbers shown reference *Table 50*.

4 Package characteristics

4.1 ECOPACK®

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

4.2 Package mechanical data

4.2.1 LQFP176 package mechanical drawing

Figure 37. LQFP176 package mechanical drawing

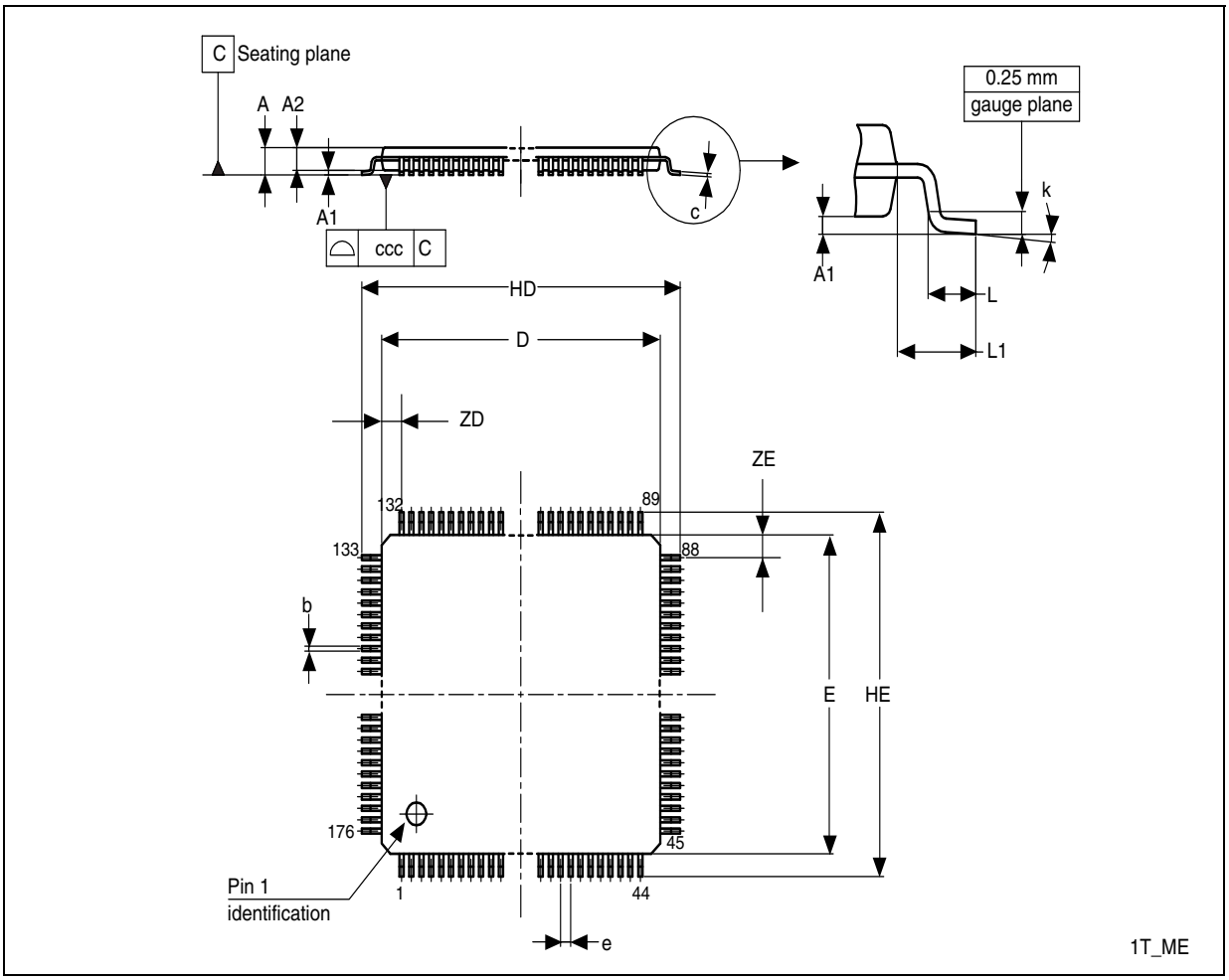


Table 57. Revision history (continued)

Date	Revision	Changes
28-Apr-2011	3	– Replaced VIL min from –0.4 V to –0.3 V in the following tables: - I/O input DC electrical characteristics - Reset electrical characteristics - Fast external crystal oscillator (4 to 40 MHz) electrical characteristics – Updated Crystal oscillator and resonator connection scheme figure – Specified NPN transistor as the recommended BCP68 transistor throughout the document – Code and Data flash memory—Program and erase specifications tables: Renamed the parameter $t_{ESUS\ to}$ T_{eslat} – Revised the footnotes in the “Functional port pin descriptions” table. – In the “System pin descriptions” table, added a footnote to the A pads regarding not using IBE. For ports PB[12–15], changed ANX to ADC0_X. – Revised the presentation of the ADC functions on the following ports: PB[4–7] PD[0–11] – ADC conversion characteristics (10-bit ADC_0) table and Conversion characteristics (12-bit ADC_1) table- Updated footnote 5 and 7 respectively for the definition of the conversion time. – Data flash memory—Program and erase specifications: Updated $T_{wprogram}$ to 500 µs and $T_{16Kpperase}$ to 500 µs. Corrected Teslat classsification from “C” to “D”. – Code flash memory—Program and erase specifications: Corrected Teslat classification from “C” to “D”. – Flash Start-up time/Switch-off time: Changed $T_{FLARSTEXIT}$ classification from “C” to “D”. – Functional port pin description: Added a footnote at the PB [9] port pin. – Absolute maximum ratings table: Added footnote 1. – Low voltage power domain electrical characteristics table: Updated IDDHALT, IDDSTOP, IDDSTBY3, IDDSTDBY2, IDDSTDBY1. – Updated commercial product code structure. – Slow external crystal oscillator (32 kHz) electrical characteristics table: Updated g_{mSXOSC}, V_{SXOSC}, $I_{SXOSCBIAS}$ and I_{SXOSC}. – FMPLL electrical characteristics table: Updated Δt_{LTJIT}. – Fast internal RC oscillator (16 MHz) electrical characteristics table: Updated TFIRCSU and IFIRCPWD. – MII serial management channel timing table: Updated M12 – JTAG characteristics table: Updated t_{TDOV}. – Low voltage monitor electrical characteristics table: Updated VLVDHV3H, VLVDHV3L, VLVDHV5H, VLVDHV5L. – DSPI electricals table: Updated spec 1, 5, 6. Updated footnote 2 and 3. Added Δt_{CSC}, Δt_{ASC}, t_{SUSS}, t_{HSS}. – IO consumption table: Updated all parameter values. – DSPI electricals: Updated Δt_{CSC} max to 115 ns. – Low voltage power domain electrical characteristics table: Added footnote 9. – ADC electrical characteristics: Added 2 notes above 10-bit and 12-bit conversion tables.

Table 57. Revision history (continued)

Date	Revision	Changes
28-Nov-2014	7 (cont.)	– Added Category column in *Table 44: Conversion characteristics (12-bit ADC_1)*. – Added the IDD_HV_ADC0 values in *Table 49: On-chip peripherals current consumption*.
16-Jun-2015	8	Updated *Figure 37: LQFP176 package mechanical drawing* and *Figure 40: Ordering information scheme*.
11-Mar-2016	9	– Added package silhouette on the cover page – Removed *Figure 4: LBGA208 configuration* – Removed LBGA208 column in *Table 4: System pin descriptions* and in *Table 5: Functional port pin descriptions* – *Table 12: LQFP thermal characteristics*: for "$R_{\theta JA}$" row, changed Max value relating to conditions "Single-layer board—1s" and "Four-layer board—2s2p" from "TBD" to "43" and "33.9", respectively – Removed *Table 13: LBGA208 thermal characteristics* – *Table 13: LBGA256 thermal characteristics*: for "$R_{\theta JA}$" row, changed Max value relating to conditions "Single-layer board—1s" and "Four-layer board—2s2p" from "TBD" to "44.3" and "31", respectively – Removed LBGA208 row in *Table 20: I/O supplies* – Removed *Section 4.2.3: LBGA208 package mechanical drawing* – In *Table 25: Low voltage power domain electrical characteristics*, updated notes "Only for the "P" classification: LPreg ON, HPVreg OFF, 96 KB RAM ON, device configured for...", "LPreg ON, HPVreg OFF, 64 KB RAM ON, device configured for...", and "LPreg ON, HPVreg OFF, 8 KB RAM ON, device configured for..." – In *Table 49: On-chip peripherals current consumption*, changed IDD_HV_ADC1 value from "300 × f_{periph}" to "300"

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