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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z4d
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, LINbus, SPI, UART/USART
Peripherals	DMA, POR, PWM, WDT
Number of I/O	147
Program Memory Size	1.5MB (1.5M x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 27x10b, 5x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP
Supplier Device Package	176-LQFP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/spc564b64l7c800y

Table 2. SPC564Bxx and SPC56ECxx family comparison[1] (continued)

Feature	SPC564B64		SPC56EC64			SPC564B70		SPC56EC70			SPC564B74		SPC56EC74		
Package	LQFP 176	LQFP 208	LQFP 176	LQFP 208	LBGA 256	LQFP 176	LQFP 208	LQFP 176	LQFP 208	LBGA 256	LQFP 176	LQFP 208	LQFP 176	LQFP 208	LBGA 256
FlexRay	Yes														
STCU[11]	Yes														
Ethernet	No		Yes			No		Yes			No		Yes		
I^2C	1														
32 kHz oscillator (SXOSC)	Yes														
GPIO[12]	147	177	147	177	199	147	177	147	177	199	147	177	147	177	199
Debug	JTAG				Nexus 3+	JTAG				Nexus 3+	JTAG				Nexus 3+
Cryptographic Services Engine (CSE)	Optional														

1. Feature set dependent on selected peripheral multiplexing; table shows example.
2. Based on 125 °C ambient operating temperature and subject to full device characterization.
3. The e200z0h can run at speeds up to 80 MHz. However, if system frequency is >80 MHz (e.g., e200z4d running at 120 MHz) the e200z0h needs to run at 1/2 system frequency. There is a configurable e200z0 system clock divider for this purpose.
4. DMAMUX also included that allows for software selection of 32 out of a possible 57 sources.
5. Not shared with 12-bit ADC, but possibly shared with other alternate functions.
6. There are 23 dedicated ANS plus 4 dedicated ANX channels on LQPF176. For higher pin count packages, there are 29 dedicated ANS plus 4 dedicated ANX channels.
7. 16x precision channels (ANP) and 3x standard (ANS).
8. Not shared with 10-bit ADC, but possibly shared with other alternate functions.
9. As a minimum, all timer channels can function as PWM or Input Capture and Output Control. Refer to the eMIOS section of the device reference manual for information on the channel configuration and functions.
10. CAN Sampler also included that allows ID of CAN message to be captured when in low power mode.
11. STCU controls MBIST activation and reporting.
12. Estimated I/O count for proposed packages based on multiplexing with peripherals.

2.3 Functional ports

The functional port pins are listed in *Table 5*.

Table 5. Functional port pin descriptions

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET config.	Pin number		
								LQFP 176	LQFP 208	LBGA256
PA[0]	PCR[0]	AF0 AF1 AF2 AF3 — —	GPIO[0] E0UC[0] CLKOUT E0UC[13] WKPU[19] CAN1RX	SIUL eMIOS_0 MC_CGM eMIOS_0 WKPU FlexCAN_1	I/O I/O O I/O I I	M/S	Tristate	24	24	G4
PA[1]	PCR[1]	AF0 AF1 AF2 AF3 — — —	GPIO[1] E0UC[1] — — WKPU[2] CAN3RX NMI[0][3]	SIUL eMIOS_0 — — WKPU FlexCAN_3 WKPU	I/O I/O — — I I I	S	Tristate	19	19	F3
PA[2]	PCR[2]	AF0 AF1 AF2 AF3 — —	GPIO[2] E0UC[2] — MA[2] WKPU[3] NMI[1][3]	SIUL eMIOS_0 — ADC_0 WKPU WKPU	I/O I/O — O I I	S	Tristate	17	17	F1
PA[3]	PCR[3]	AF0 AF1 AF2 AF3 — — —	GPIO[3] E0UC[3] LIN5TX CS4_1 RX_ER_CLK EIRQ[0] ADC1_S[0]	SIUL eMIOS_0 LINFlexD_5 DSPI_1 FEC SIUL ADC_1	I/O I/O O O I I I	M/S	Tristate	114	138	G16
PA[4]	PCR[4]	AF0 AF1 AF2 AF3 — —	GPIO[4] E0UC[4] — CS0_1 LIN5RX WKPU[9]	SIUL eMIOS_0 — DSPI_1 LINFlexD_5 WKPU	I/O I/O — I/O I I	S	Tristate	51	61	T2

Table 5. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET config.	Pin number		
								LQFP 176	LQFP 208	LBGA256
PB[0]	PCR[16]	AF0 AF1 AF2 AF3	GPIO[16] CAN0TX E0UC[30] LIN0TX	SIUL FlexCAN_0 eMIOS_0 LINFlexD_0	I/O O I/O I	M/S	Tristate	39	39	L3
PB[1]	PCR[17]	AF0 AF1 AF2 — — —	GPIO[17] — E0UC[31] LIN0RX WKPU[4] CAN0RX	SIUL — eMIOS_0 LINFlexD_0 WKPU FlexCAN_0	I/O — I/O I I I	S	Tristate	40	40	M2
PB[2]	PCR[18]	AF0 AF1 AF2 AF3	GPIO[18] LIN0TX SDA E0UC[30]	SIUL LINFlexD_0 I^2C eMIOS_0	I/O O I/O I/O	M/S	Tristate	176	208	A2
PB[3]	PCR[19]	AF0 AF1 AF2 AF3 — —	GPIO[19] E0UC[31] SCL — WKPU[11] LIN0RX	SIUL eMIOS_0 I^2C — WKPU LINFlexD_0	I/O I/O I/O — I I	S	Tristate	1	1	D4
PB[4]	PCR[20]	AF0 AF1 AF2 AF3 — —	GPI[20] — — — ADC0_P[0] ADC1_P[0]	SIUL — — — ADC_0 ADC_1	I — — — I I	I	Tristate	88	104	T16
PB[5]	PCR[21]	AF0 AF1 AF2 AF3 — —	GPI[21] — — — ADC0_P[1] ADC1_P[1]	SIUL — — — ADC_0 ADC_1	I — — — I I	I	Tristate	91	107	N13

Table 5. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET config.	Pin number		
								LQFP 176	LQFP 208	LBGA256
PF[1]	PCR[81]	AF0 AF1 AF2 AF3 —	GPIO[81] E0UC[11] CS4_1 — ADC0_S[9]	SIUL eMIOS_0 DSPI_1 — ADC_0	I/O I/O O — I	S	Tristate	64	80	T6
PF[2]	PCR[82]	AF0 AF1 AF2 AF3 —	GPIO[82] E0UC[12] CS0_2 — ADC0_S[10]	SIUL eMIOS_0 DSPI_2 — ADC_0	I/O I/O I/O — I	S	Tristate	65	81	R6
PF[3]	PCR[83]	AF0 AF1 AF2 AF3 —	GPIO[83] E0UC[13] CS1_2 — ADC0_S[11]	SIUL eMIOS_0 DSPI_2 — ADC_0	I/O I/O O — I	S	Tristate	66	82	R7
PF[4]	PCR[84]	AF0 AF1 AF2 AF3 —	GPIO[84] E0UC[14] CS2_2 — ADC0_S[12]	SIUL eMIOS_0 DSPI_2 — ADC_0	I/O I/O O — I	S	Tristate	67	83	R8
PF[5]	PCR[85]	AF0 AF1 AF2 AF3 —	GPIO[85] E0UC[22] CS3_2 — ADC0_S[13]	SIUL eMIOS_0 DSPI_2 — ADC_0	I/O I/O O — I	S	Tristate	68	84	P8
PF[6]	PCR[86]	AF0 AF1 AF2 AF3 —	GPIO[86] E0UC[23] CS1_1 — ADC0_S[14]	SIUL eMIOS_0 DSPI_1 — ADC_0	I/O I/O O — I	S	Tristate	69	85	N8
PF[7]	PCR[87]	AF0 AF1 AF2 AF3 —	GPIO[87] — CS2_1 — ADC0_S[15]	SIUL — DSPI_1 — ADC_0	I/O — O — I	S	Tristate	70	86	P9

Table 5. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET config.	Pin number		
								LQFP 176	LQFP 208	LBGA256
PF[8]	PCR[88]	AF0 AF1 AF2 AF3	GPIO[88] CAN3TX CS4_0 CAN2TX	SIUL FlexCAN_3 DSPI_0 FlexCAN_2	I/O O O O	M/S	Tristate	42	50	N2
PF[9]	PCR[89]	AF0 AF1 AF2 AF3 — — —	GPIO[89] E1UC[1] CS5_0 — CAN2RX CAN3RX WKPU[22]	SIUL eMIOS_1 DSPI_0 — FlexCAN_2 FlexCAN_3 WKPU	I/O I/O O — I I I	S	Tristate	41	49	M4
PF[10]	PCR[90]	AF0 AF1 AF2 AF3	GPIO[90] CS1_0 LIN4TX E1UC[2]	SIUL DSPI_0 LINFlexD_4 eMIOS_1	I/O O O I/O	M/S	Tristate	46	54	P2
PF[11]	PCR[91]	AF0 AF1 AF2 AF3 — —	GPIO[91] CS2_0 E1UC[3] — LIN4RX WKPU[15]	SIUL DSPI_0 eMIOS_1 — LINFlexD_4 WKPU	I/O O I/O — I I	S	Tristate	47	55	R1
PF[12]	PCR[92]	AF0 AF1 AF2 AF3	GPIO[92] E1UC[25] LIN5TX —	SIUL eMIOS_1 LINFlexD_5 —	I/O I/O O —	M/S	Tristate	43	51	P1
PF[13]	PCR[93]	AF0 AF1 AF2 AF3 — —	GPIO[93] E1UC[26] — — LIN5RX WKPU[16]	SIUL eMIOS_1 — — LINFlexD_5 WKPU	I/O I/O — — I I	S	Tristate	49	57	P3

Table 5. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET config.	Pin number		
								LQFP 176	LQFP 208	LBGA256
PK[0]	PCR[160]	AF0 AF1 AF2 AF3	GPIO[160] CAN1TX CS2_6 —	SIUL FlexCAN_1 DSPI_6 —	I/O O O —	M/S	Tristate	—	62	T3
PK[1]	PCR[161]	AF0 AF1 AF2 AF3 —	GPIO[161] CS3_6 — — CAN4RX	SIUL DSPI_6 — — FlexCAN_4	I/O O — — I	M/S	Tristate	—	41	H4
PK[2]	PCR[162]	AF0 AF1 AF2 AF3	GPIO[162] CAN4TX — —	SIUL FlexCAN_4 — —	I/O O — —	M/S	Tristate	—	42	L4
PK[3]	PCR[163]	AF0 AF1 AF2 AF3 — —	GPIO[163] E1UC[0] — — CAN5RX LIN8RX	SIUL eMIOS_1 — — FlexCAN_5 LINFlexD_8	I/O I/O — — I I	M/S	Tristate	—	43	N1
PK[4]	PCR[164]	AF0 AF1 AF2 AF3	GPIO[164] LIN8TX CAN5TX E1UC[1]	SIUL LINFlexD_8 FlexCAN_5 eMIOS_1	I/O O O I/O	M/S	Tristate	—	44	M3
PK[5]	PCR[165]	AF0 AF1 AF2 AF3 — —	GPIO[165] — — — CAN2RX LIN2RX	SIUL — — — FlexCAN_2 LINFlexD_2	I/O — — — I I	M/S	Tristate	—	45	M5
PK[6]	PCR[166]	AF0 AF1 AF2 AF3	GPIO[166] CAN2TX LIN2TX —	SIUL FlexCAN_2 LINFlexD_2 —	I/O O O —	M/S	Tristate	—	46	M6

Table 5. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET config.	Pin number		
								LQFP 176	LQFP 208	LBGA256
PK[7]	PCR[167]	AF0 AF1 AF2 AF3 — —	GPIO[167] — — — CAN3RX LIN3RX	SIUL — — — FlexCAN_3 LINFlexD_3	I/O — — — I I	M/S	Tristate	—	47	M7
PK[8]	PCR[168]	AF0 AF1 AF2 AF3	GPIO[168] CAN3TX LIN3TX —	SIUL FlexCAN_3 LINFlexD_3 —	I/O O O —	M/S	Tristate	—	48	M8
PK[9]	PCR[169]	AF0 AF1 AF2 AF3 —	GPIO[169] — — — SIN_4	SIUL — — — DSPI_4	I/O — — — I	M/S	Tristate	—	197	E8
PK[10]	PCR[170]	AF0 AF1 AF2 AF3	GPIO[170] SOUT_4 — —	SIUL DSPI_4 — —	I/O O — —	M/S	Tristate	—	198	E7
PK[11]	PCR[171]	AF0 AF1 AF2 AF3	GPIO[171] SCK_4 — —	SIUL DSPI_4 — —	I/O I/O — —	M/S	Tristate	—	199	F8
PK[12]	PCR[172]	AF0 AF1 AF2 AF3	GPIO[172] CS0_4 — —	SIUL DSPI_4 — —	I/O I/O — —	M/S	Tristate	—	200	G12
PK[13]	PCR[173]	AF0 AF1 AF2 AF3 —	GPIO[173] CS3_6 CS2_7 SCK_1 CAN3RX	SIUL DSPI_6 DSPI_7 DSPI_1 FlexCAN_3	I/O O O I/O I	M/S	Tristate	—	201	H12

3 Electrical Characteristics

This section contains electrical characteristics of the device as well as temperature and power considerations.

This product contains devices to protect the inputs against damage due to high static voltages. However, it is advisable to take precautions to avoid application of any voltage higher than the specified maximum rated voltages.

To enhance reliability, unused inputs can be driven to an appropriate logic voltage level (V_{DD} or V_{SS_HV}). This could be done by the internal pull-up and pull-down, which is provided by the product for most general purpose pins.

The parameters listed in the following tables represent the characteristics of the device and its demands on the system.

In the tables where the device logic provides signals with their respective timing characteristics, the symbol “CC” for Controller Characteristics is included in the Symbol column.

In the tables where the external system must provide signals with their respective timing characteristics to the device, the symbol “SR” for System Requirement is included in the Symbol column.

3.1 Parameter classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding, the classifications listed in *Table 6* are used and the parameters are tagged accordingly in the tables where appropriate.

Table 6. Parameter classifications

Classification tag	Tag description
P	Those parameters are guaranteed during production testing on each individual device.
C	Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations.
T	Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category.
D	Those parameters are derived mainly from simulations.

Note: The classification is shown in the column labeled “C” in the parameter tables where appropriate.

3.2 NVUSRO register

Portions of the device configuration, such as high voltage supply is controlled via bit values in the Non-Volatile User Options Register (NVUSRO). For a detailed description of the NVUSRO register, see SPC564Bxx and SPC56ECxx Reference Manual.

Table 9. Absolute maximum ratings (continued)

Symbol		Parameter	Conditions	Value		Unit
				Min	Max	
V_{RC_CTRL} (2)		Base control voltage for external BCP68 NPN device	Relative to V_{DD_LV}	0	V_{DD_LV} + 1	V
V_{SS_ADC}	S R	Voltage on VSS_HV_ADC0, VSS_HV_ADC1 (ADC reference) pin with respect to ground (V_{SS_HV})	—	V_{SS_HV} – 0.1	V_{SS_HV} + 0.1	V
$V_{DD\_HV\_ADC0}$	S R	Voltage on VDD_HV_ADC0 with respect to ground (V_{SS_HV})	—	–0.3	6.0	V
			Relative to $V_{DD\_HV\_A}$ (3)	$V_{DD\_HV\_A}$ – 0.3	$V_{DD\_HV\_A}$+0.3	
$V_{DD\_HV\_ADC1}$ (4)	S R	Voltage on VDD_HV_ADC1 with respect to ground (V_{SS_HV})	—	–0.3	6.0	V
			Relative to $V_{DD\_HV\_A}$ 2	$V_{DD\_HV\_A}$–0.3	$V_{DD\_HV\_A}$+0.3	
V_{IN}	S R	Voltage on any GPIO pin with respect to ground (V_{SS_HV})	Relative to $V_{DD\_HV\_A/HV\_B}$	$V_{DD\_HV\_A/HV\_B}$– 0.3	$V_{DD\_HV\_A/HV\_B}$+ 0.3	V
I_{INJPAD}	S R	Injected input current on any pin during overload condition	—	–10	10	mA
I_{INJSUM}	S R	Absolute sum of all injected input currents during overload condition	—	–50	50	
I_{AVGSEG} (5)	S R	Sum of all the static I/O current within a supply segment ($V_{DD\_HV\_A}$ or $V_{DD\_HV\_B}$)	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0		70	mA
			V_{DD} = 3.3 V ± 10%, PAD3V5V = 1		64	
$T_{STORAGE}$	S R	Storage temperature	—	–55 (6)	150	°C

1. $V_{DD\_HV\_B}$ can be independently controlled from $V_{DD\_HV\_A}$. These can ramp up or ramp down in any order. Design is robust against any supply order.
2. This voltage is internally generated by the device and no external voltage should be supplied.
3. Both the relative and the fixed conditions must be met. For instance: If $V_{DD\_HV\_A}$ is 5.9 V, $V_{DD\_HV\_ADC0}$ maximum value is 6.0 V then, despite the relative condition, the max value is $V_{DD\_HV\_A}$ + 0.3 = 6.2 V.
4. PA3, PA7, PA10, PA11 and PE12 ADC_1 channels are coming from $V_{DD\_HV\_B}$ domain hence $V_{DD\_HV\_ADC1}$ should be within ±300 mV of $V_{DD\_HV\_B}$ when these channels are used for ADC_1.
5. Any temperature beyond 125 °C should limit the current to 50 mA (max).
6. This is the storage temperature for the flash memory.

Note: Stresses exceeding the recommended absolute maximum ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. During overload conditions (V_{IN} > $V_{DD\_HV\_A/HV\_B}$ or V_{IN} < V_{SS_HV}), the voltage on pins with respect to ground (V_{SS_HV}) must not exceed the recommended values.

Table 16. SLOW configuration output buffer electrical characteristics (continued)

Symbol		C	Parameter	Conditions[1],[2]		Value			Unit
						Min	Typ	Max	
V_{OL}	CC	P	Output low level SLOW configuration	Push Pull	I_{OL} = 3 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	$0.1V_{DD}$	V
		C			I_{OL} = 3 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 1[3]	—	—	$0.1V_{DD}$	
		P			I_{OL} = 1.5 mA, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	0.5	

1. V_{DD} = 3.3 V ± 10 % / 5.0 V ± 10 %, T_A = –40 to 125 °C, unless otherwise specified.
2. V_{DD} as mentioned in the table is $V_{DD\_HV\_A}$/$V_{DD\_HV\_B}$.
3. The configuration PAD3V5 = 1 when V_{DD} = 5 V is only a transient configuration during power-up. All pads but RESET and Nexus output (MDOx, EVTO, MCKO) are configured in input or in high impedance state.

Table 17. MEDIUM configuration output buffer electrical characteristics

Symbol		C	Parameter	Conditions[1],[2]		Value			Unit
						Min	Typ	Max	
V_{OH}	CC	C	Output high level MEDIUM configuration	Push Pull	I_{OH} = –3 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	$0.8V_{DD}$	—	—	V
		C			I_{OH} = –1.5 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 1[3]	$0.8V_{DD}$	—	—	
		C			I_{OH} = –2 mA, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	V_{DD} – 0.8	—	—	
V_{OL}	CC	C	Output low level MEDIUM configuration	Push Pull	I_{OL} = 3 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	$0.2V_{DD}$	V
		C			I_{OL} = 1.5 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 1[3]	—	—	$0.1V_{DD}$	
		C			I_{OL} = 2 mA, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	0.5	

1. V_{DD} = 3.3 V ± 10 % / 5.0 V ± 10 %, T_A = –40 to 125 °C, unless otherwise specified.
2. V_{DD} as mentioned in the table is $V_{DD\_HV\_A}$/$V_{DD\_HV\_B}$.
3. The configuration PAD3V5 = 1 when V_{DD} = 5 V is only a transient configuration during power-up. All pads but RESET and Nexus output (MDOx, EVTO, MCKO) are configured in input or in high impedance state.

Table 23. Voltage regulator electrical characteristics (continued)

Symbol		C	Parameter	Conditions[1]	Value[2]			Unit
					Min	Typ	Max	
I_{MREG}	SR	—	Main regulator current provided to V_{DD_LV} domain	—	—	—	350	mA
$I_{MREGINT}$	CC	D	Main regulator module current consumption	I_{MREG} = 200 mA	—	—	2	mA
				I_{MREG} = 0 mA	—	—	1	
V_{LPREG}	CC	P	Low power regulator output voltage	After trimming T_A = 25 °C	1.17	1.27	1.32	V
I_{LPREG}	SR	—	Low power regulator current provided to V_{DD_LV} domain	—	—	—	50	mA
$I_{LPREGINT}$	CC	D	Low power regulator module current consumption	I_{LPREG} = 15 mA; T_A = 55 °C	—	—	600	µA
		—		I_{LPREG} = 0 mA; T_A = 55 °C	—	20	—	
$I_{VREGREF}$	CC	D	Main LVDs and reference current consumption (low power and main regulator switched off)	T_A = 55 °C	—	2	—	µA
$I_{VREDLVD12}$	CC	D	Main LVD current consumption (switch-off during standby)	T_A = 55 °C	—	1	—	µA
$I_{DD\_HV\_A}$	CC	D	In-rush current on V_{DD_BV} during power-up	—	—	—	600 (3)	mA

1. $V_{DD\_HV\_A}$ = 3.3 V ± 10 % / 5.0 V ± 10 %, T_A = –40 to 125 °C, unless otherwise specified.
2. All values need to be confirmed during device validation.
3. Inrush current is seen more like steps of 600 mA peak. The startup of the regulator happens in steps of 50 mV in ~25 steps to reach ~1.2 V V_{DD_LV}. Each step peak current is within 600 mA

3.8.3 Voltage monitor electrical characteristics

The device implements a Power-on Reset module to ensure correct power-up initialization, as well as four low voltage detectors to monitor the $V_{DD\_HV\_A}$ and the V_{DD_LV} voltage while device is supplied:

- POR monitors $V_{DD\_HV\_A}$ during the power-up phase to ensure device is maintained in a safe reset state
- LVDHV3 monitors $V_{DD\_HV\_A}$ to ensure device is reset below minimum functional supply
- LVDHV5 monitors $V_{DD\_HV\_A}$ when application uses device in the 5.0 V±10 % range
- LVDLVCOR monitors power domain No. 1 (PD1)
- LVDLVBKP monitors power domain No. 0 (PD0). VDD_LV is same as PD0 supply.

Note: When enabled, PD2 (RAM retention) is monitored through LVD_DIGBKP.

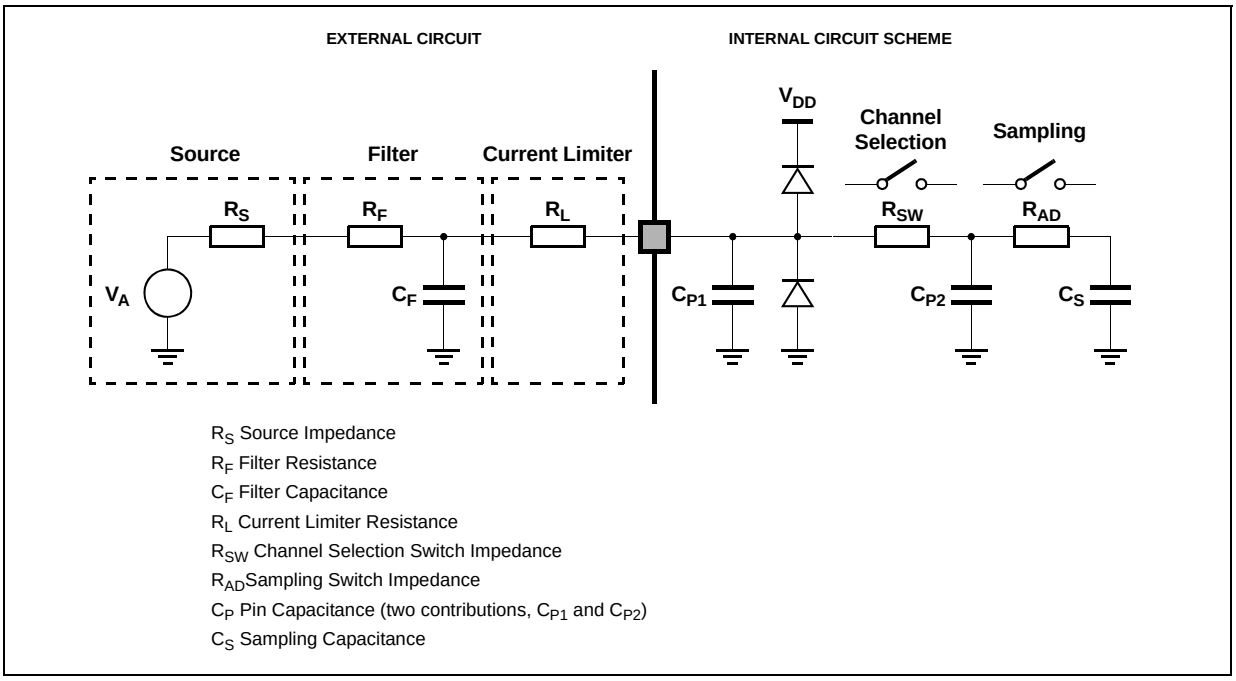
In fact a current sink contributor is represented by the charge sharing effects with the sampling capacitance: being CS and Cp_2 substantially two switched capacitances, with a frequency equal to the conversion rate of the ADC, it can be seen as a resistive path to ground. For instance, assuming a conversion rate of 1MHz, with CS+Cp_2 equal to 3pF, a resistance of 330KΩ is obtained (Reqiv = 1 / (fc*(CS+Cp_2)), where fc represents the conversion rate at the considered channel). To minimize the error induced by the voltage partitioning between this resistance (sampled voltage on CS+Cp_2) and the sum of R_S + R_F, the external circuit must be designed to respect the following relation

Equation 4

$$V_A \bullet \frac{R_S + R_F}{R_{EQ}} < \frac{1}{2} LSB$$

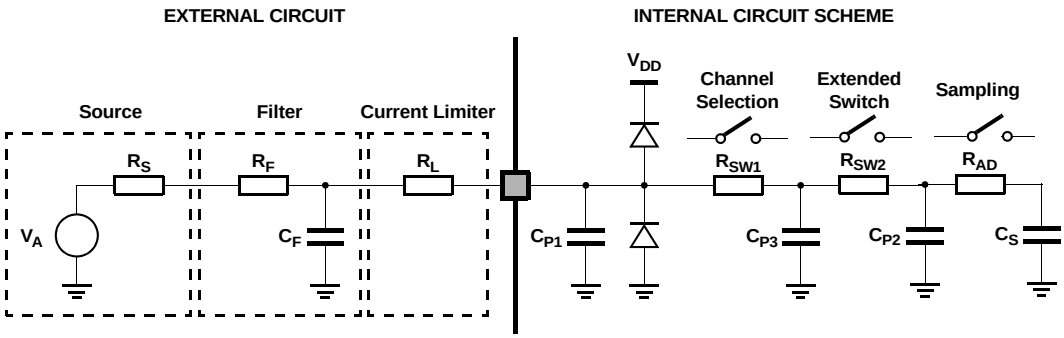
The formula above provides a constraint for external network design, in particular on resistive path.

Figure 16. Input equivalent circuit (precise channels)



R_S Source Impedance
R_F Filter Resistance
C_F Filter Capacitance
R_L Current Limiter Resistance
R_{SW} Channel Selection Switch Impedance
R_{AD}Sampling Switch Impedance
C_P Pin Capacitance (two contributions, C_{P1} and C_{P2})
C_S Sampling Capacitance

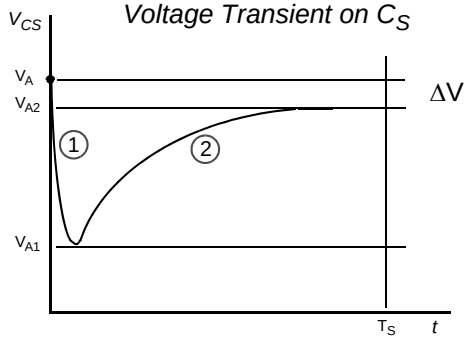
Figure 17. Input equivalent circuit (extended channels)



R_S Source Impedance
R_F Filter Resistance
C_F Filter Capacitance
R_L Current Limiter Resistance
R_{SW} Channel Selection Switch Impedance (two contributions R_{SW1} and R_{SW2})
R_{AD}Sampling Switch Impedance
C_P Pin Capacitance (three contributions, C_{P1}, C_{P2} and C_{P3})
C_S Sampling Capacitance

A second aspect involving the capacitance network shall be considered. Assuming the three capacitances C_F, C_{P1} and C_{P2} initially charged at the source voltage V_A (refer to the equivalent circuit reported in *Figure 16*): when the sampling phase is started (A/D switch close), a charge sharing phenomena is installed.

Figure 18. Transient behavior during sampling phase



$\Delta V < 0.5$ LSB

$\tau_1 < (R_{SW} + R_{AD})\, C_S << T_S$

$\tau_2 = R_L\,(C_S + C_{P1} + C_{P2})$

In particular two different transient periods can be distinguished:

- A first and quick charge transfer from the internal capacitance C_{P1} and C_{P2} to the sampling capacitance C_S occurs (C_S is supposed initially completely discharged): considering a worst case (since the time constant in reality would be faster) in which C_{P2} is reported in parallel to C_{P1} (call $C_P = C_{P1} + C_{P2}$), the two capacitances C_P and C_S are in series, and the time constant is

Equation 5

$$\tau_1 = (R_{SW} + R_{AD}) \bullet \frac{C_P \bullet C_S}{C_P + C_S}$$

Figure 20. ADC_1 characteristic and error definitions

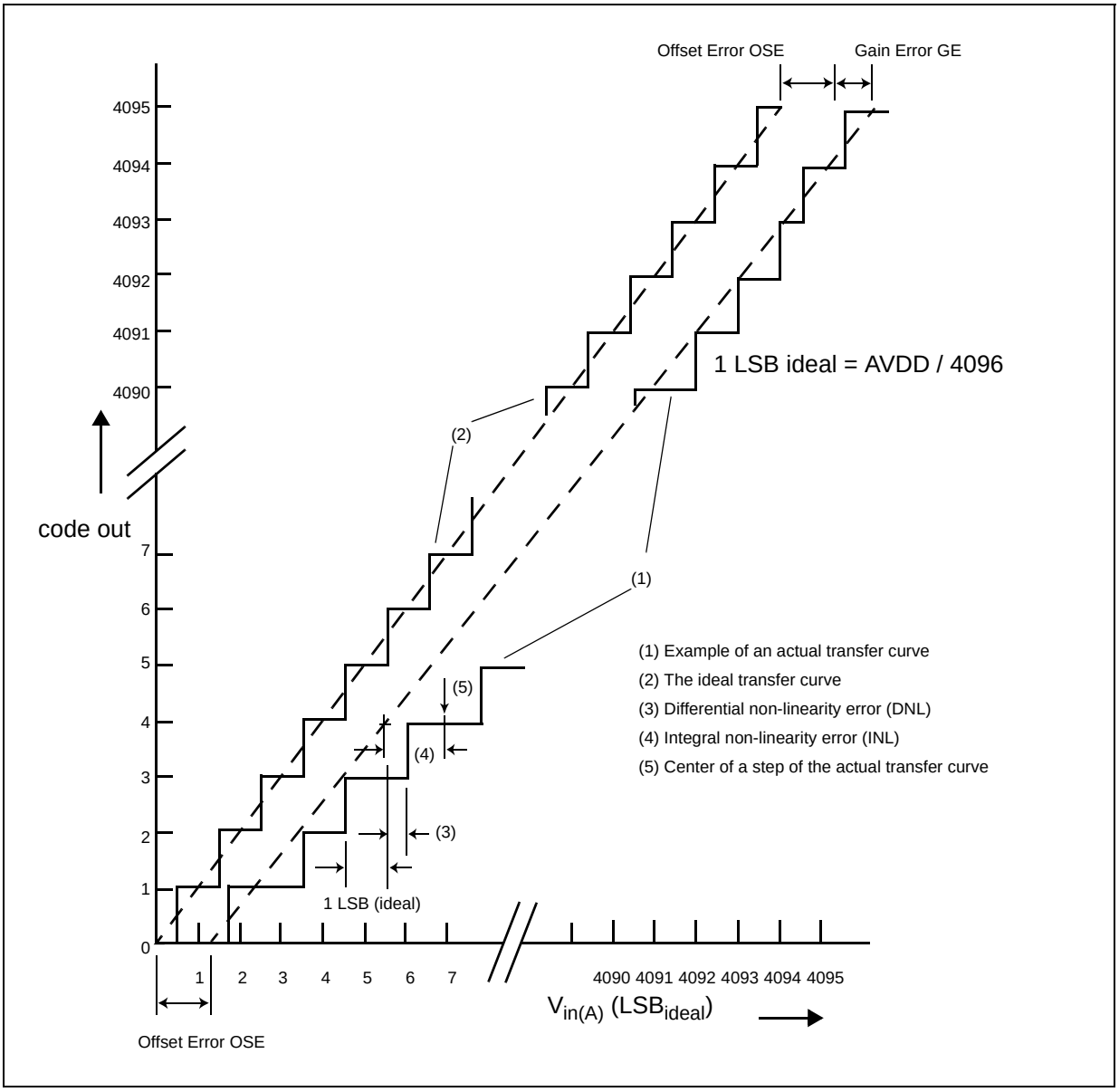
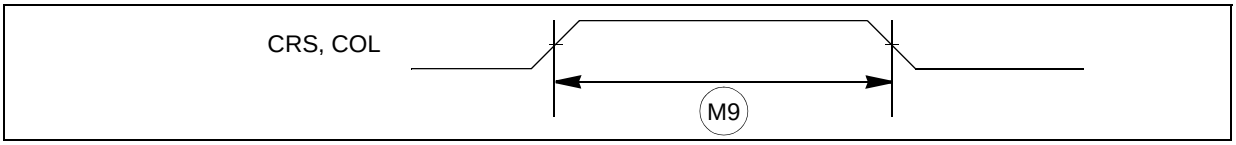


Figure 23. MII async inputs timing diagram



3.18.4 MII Serial Management Channel Timing (MDIO and MDC)

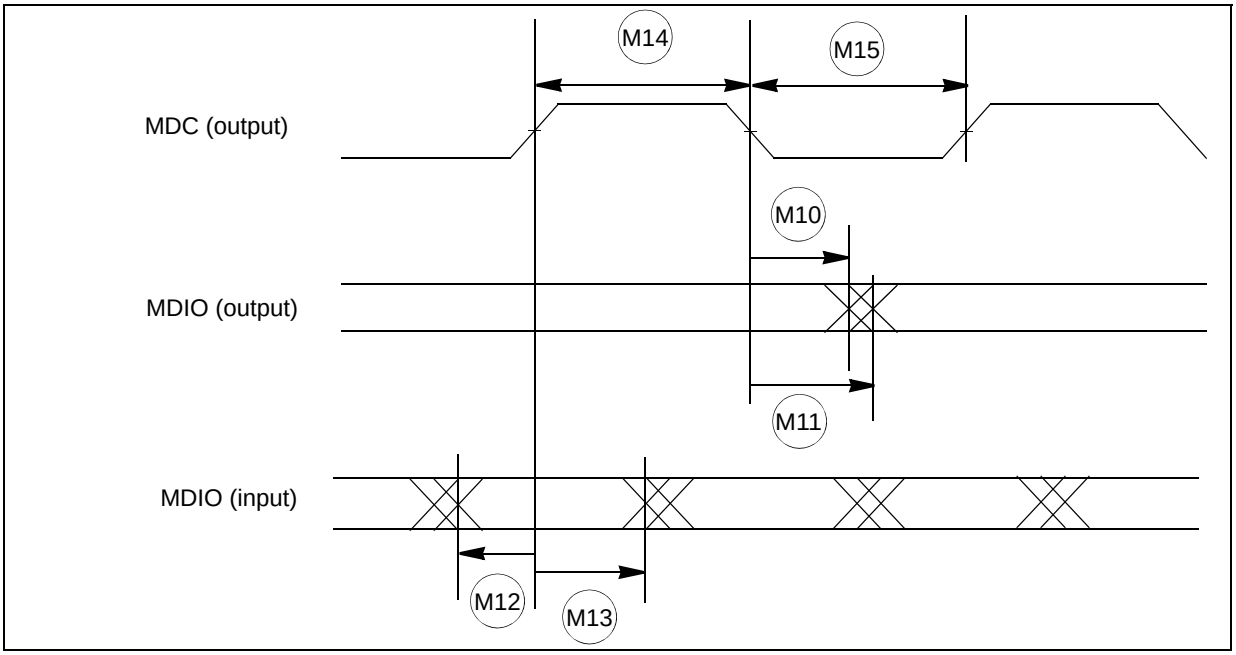
The FEC functions correctly with a maximum MDC frequency of 2.5 MHz.

Table 48. MII serial management channel timing(1)

Spec	Characteristic	Min	Max	Unit
M10	MDC falling edge to MDIO output invalid (minimum propagation delay)	0	—	ns
M11	MDC falling edge to MDIO output valid (max prop delay)	—	25	ns
M12	MDIO (input) to MDC rising edge setup	28	—	ns
M13	MDIO (input) to MDC rising edge hold	0	—	ns
M14	MDC pulse width high	40%	60%	MDC period
M15	MDC pulse width low	40%	60%	MDC period

1. Output pads configured with SRE = 0b11.

Figure 24. MII serial management channel timing diagram



3.19 On-chip peripherals

3.19.1 Current consumption

Table 49. On-chip peripherals current consumption(1)

Symbol		C	Parameter	Conditions		Value(2) Typ	Unit
$I_{DD\_HV\_A(CAN)}$	CC	D	CAN (FlexCAN) supply current on $V_{DD\_HV\_A}$	500 Kbps	Total (static + dynamic) consumption: FlexCAN in loop-back mode XTAL@8 MHz used as CAN engine clock source Message sending period is 580 µs	$7.652 \times f_{periph} + 84.73$	µA
				125 Kbps		$8.0743 \times f_{periph} + 26.757$	
$I_{DD\_HV\_A(eMIOS)}$	CC	D	eMIOS supply current on $V_{DD\_HV\_A}$	Static consumption: eMIOS channel OFF Global prescaler enabled		$28.7 \times f_{periph}$	
				Dynamic consumption: It does not change varying the frequency (0.003 mA)		3	
$I_{DD\_HV\_A(SCI)}$	CC	D	SCI (LINFlex) supply current on $V_{DD\_HV\_A}$	Total (static + dynamic) consumption: LIN mode Baudrate: 20 Kbps		$4.7804 \times f_{periph} + 30.946$	
$I_{DD\_HV\_A(SPI)}$	CC	D	SPI (DSPI) supply current on $V_{DD\_HV\_A}$	Ballast static consumption (only clocked)		1	
				Ballast dynamic consumption (continuous communication): Baudrate: 2 Mbit Transmission every 8 µs Frame: 16 bits		$16.3 \times f_{periph}$	
$I_{DD\_HV\_A(ADC)}$	CC	D	ADC supply current on $V_{DD\_HV\_A}$	V_{DD} = 5.5 V	Ballast static consumption (no conversion)	$0.0409 \times f_{periph}$	mA
				V_{DD} = 5.5 V	Ballast dynamic consumption (continuous conversion)	$0.0049 \times f_{periph}$	

Table 49. On-chip peripherals current consumption(1)

Symbol		C	Parameter	Conditions		Value(2) Typ	Unit
IDD_HV_ADC0	CC	D	ADC_0 supply current on $V_{DD\_HV\_ADC0}$	V_{DD} = 5.5 V	Analog static consumption (no conversion)	200	µA
					Analog dynamic consumption (continuous conversion)	4	mA
IDD_HV_ADC1	CC	D	ADC_1 supply current on $V_{DD\_HV\_ADC1}$	V_{DD} = 5.5 V	Analog static consumption (no conversion)	300	µA
				V_{DD} = 5.5 V	Analog dynamic consumption (continuous conversion)	6	mA
$I_{DD\_HV(FLASH)}$	CC	D	CFlash + DFlash supply current on $V_{DD\_HV\_ADC}$	V_{DD} = 5.5 V	—	13.25	mA
$I_{DD\_HV(PLL)}$	CC	D	PLL supply current on V_{DD_HV}	V_{DD} = 5.5 V	—	0.0031 × f_{periph}	

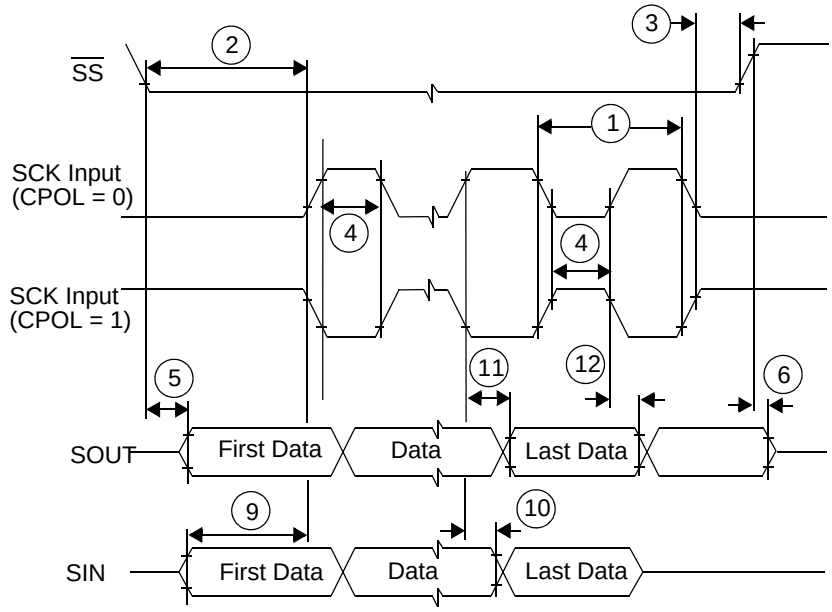
1. Operating conditions: T_A = 25 °C, f_{periph} = 8 MHz to 120 MHz.
2. f_{periph} is in absolute value.

3.19.2 DSPI characteristics

Table 50. DSPI timing

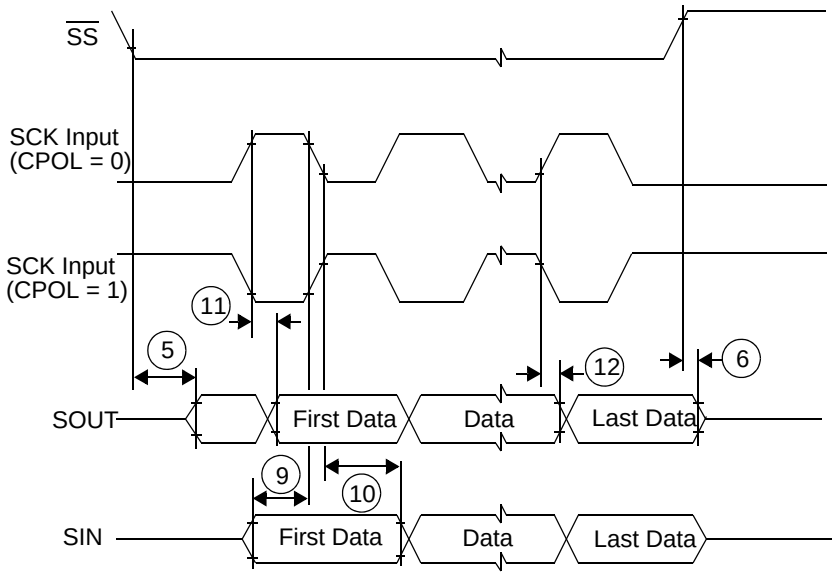
Spec	Characteristic	Symbol	Value Min	Value Max	Unit
1	DSPI Cycle Time	t_{SCK}	Refer note(1)	—	ns
—	Internal delay between pad associated to SCK and pad associated to CSn in master mode for CSn1->0	Δt_{CSC}	—	115	ns
—	Internal delay between pad associated to SCK and pad associated to CSn in master mode for CSn1->1	Δt_{ASC}	15	—	ns
2	CS to SCK Delay(2)	t_{CSC}	7	—	ns
3	After SCK Delay(3)	t_{ASC}	15	—	ns
4	SCK Duty Cycle	t_{SDC}	0.4 × t_{SCK}	0.6 × t_{SCK}	ns

Figure 31. DSPI modified transfer format timing–slave, CPHA = 0



Note: Numbers shown reference *Table 50*.

Figure 32. DSPI modified transfer format timing–slave, CPHA = 1



Note: Numbers shown reference *Table 50*.

Table 55. LBGA256 mechanical data

Ref	mm		
	Min	Typ	Max
A	1.210		1.700
A1	0.300		
A2		0.300	
A4			0.800
b	0.400	0.500	0.600
D	16.800	17.000	17.200
D1		15.000	
E	16.800	17.000	17.200
E1		15.000	
e	0.900	1.000	1.100
Z	0.750	1.000	1.250
ddd			0.200

Note: The package is designed according to the JEDEC standard No 95-1 Section 14 dedicated to Ball Grid Array Package Design Guide.

Revision history

Table 57 summarizes revisions to this document.

Table 57. Revision history

Date	Revision	Changes
01-Jun-2010	1	Initial Release
17-Dec-2010	2	– Editing and formatting updates throughout the document. – Updated Voltage regulator capacitance connection figure. – Added a new sub-section "V_{DD_BV} Options" – Program and erase specifications: Updated Tdwprogram TYP to 22 us Updated T128Kpperase Max to 5000 ms Added t_{ESUS} parameter – Added recommendation in the Voltage regulator electrical characteristics section. – Added Crystal description table in Fast external crystal oscillator (4 to 140 MHz) electrical characteristics section and corrected the cross-reference to the same. – Added new sections - Pad types, System pins and functional ports – Updated TYP numbers in the Flash program and erase specifications table – Added a new table: Program and erase specifications (Data Flash) – Flash read access timing table: Added Data flash memory numbers – Flash power supply DC electrical characteristics table: Updated IDFREAD and IDFMOD values for Data flash, Removed IDFLPW parameter – Updated feature list. – SPC564Bxx and SPC56ECxx family comparison table: Updated ADC channels and added ADC footnotes. – SPC564Bxx and SPC56ECxx block diagram: Updated ADC channels and added legends. – SPC564Bxx and SPC56ECxx series block summary: Added new blocks. – Functional Port Pin Descriptions table: Added OSC32k_XTAL and OSC32k_EXTAL function at PB8 and PB9 port pins. – Electrical Characteristics: Replaced VSS with VSS_HV throughout the section. – Absolute maximum ratings, Recommended operating conditions (3.3 V) and Recommended operating conditions (5.0 V) tables: VRC_CTRL min is updated to "0". – Recommended operating conditions (3.3 V) and Recommended operating conditions (5.0 V) tables: Clarified VIN parameter, clarified footnote 2 in both tables. – LQFP thermal characteristics section: Added numbers for LQFP packages. – Low voltage power domain electrical characteristics table: Clarified footnotes based upon review comments. – Code flash memory—Program and erase specifications: Updated tESRT to 20 ms. – ADC electrical characteristics section: Replace ADC0 with ADC_0 and ADC1 with ADC_1 throughout the document. DSPI characteristics section: Replaced PCSx with CSx in all figures and tables.