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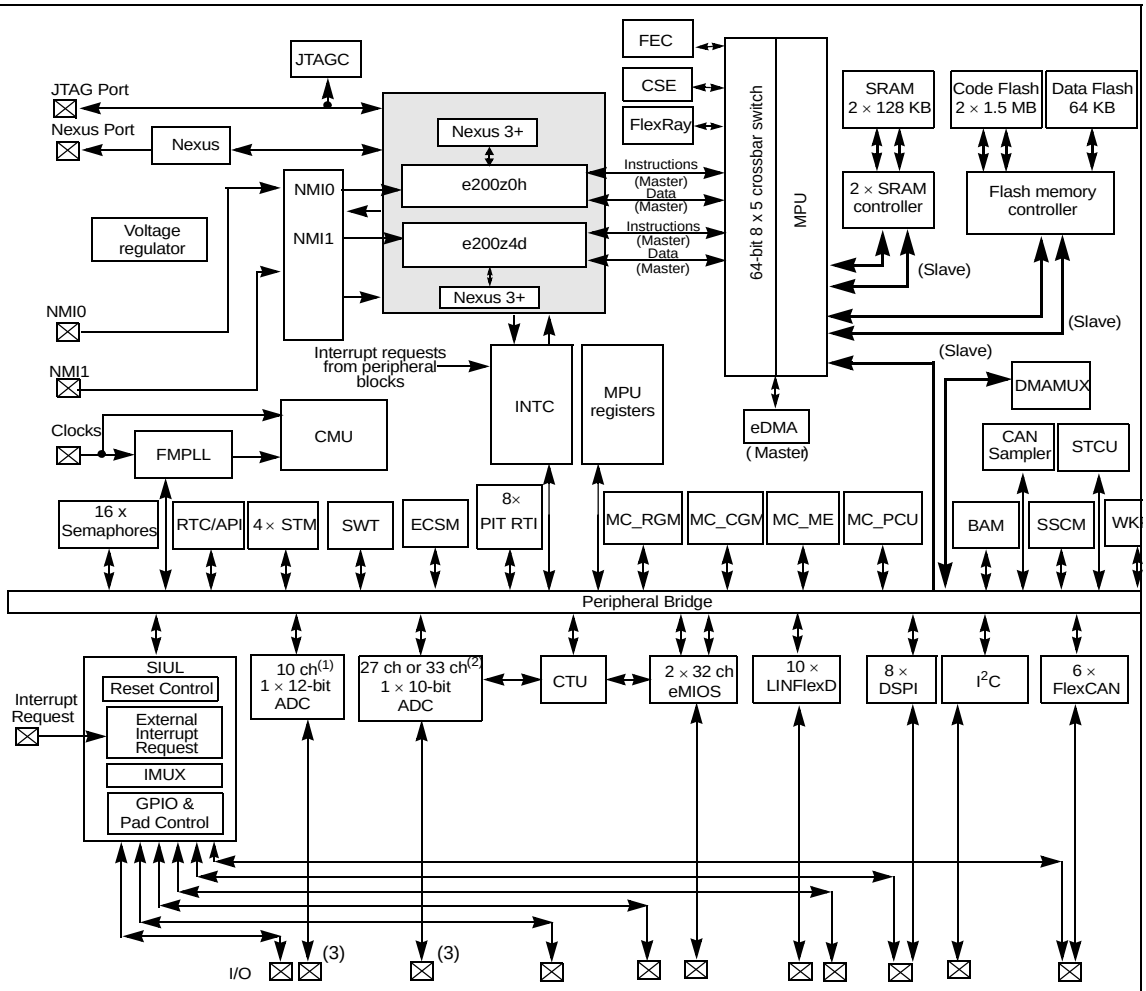
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z4d
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, LINbus, SPI, UART/USART
Peripherals	DMA, POR, PWM, WDT
Number of I/O	147
Program Memory Size	1.5MB (1.5M x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 27x10b, 5x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP
Supplier Device Package	176-LQFP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/spc564b64l7c8ecx

1.3 Block diagram

Figure 1 shows the detailed block diagram of the SPC564Bxx and SPC56ECxx.

Figure 1. SPC564Bxx and SPC56ECxx block diagram



Legend:

ADC	Analog-to-Digital Converter	JTAGC	JTAG controller
BAM	Boot Assist Module	LINFlexD	Local Interconnect Network Flexible with DMA sup
CSE	Cryptographic Services Engine	MC_ME	Mode Entry Module
CAN	Controller Area Network (FlexCAN)	MC_CGM	Clock Generation Module
CMU	Clock Monitor Unit	MC_PCU	Power Control Unit
CTU	Cross Triggering Unit	MC_RGM	Reset Generation Module
DMAMUX	DMA Channel Multiplexer	MPU	Memory Protection Unit
DSPI	Deserial Serial Peripheral Interface	Nexus	Nexus Development Interface
eDMA	enhanced Direct Memory Access	NMI	Non-Maskable Interrupt
FlexCAN	Controller Area Network controller modules	PIT_RTI	Periodic Interrupt Timer with Real-Time Interrupt
FEC	Fast Ethernet Controller	RTC/API	Real-Time Clock/ Autonomous Periodic Interrupt
eMIOS	Enhanced Modular Input Output System	SIUL	System Integration Unit Lite
ECSM	Error Correction Status Module	SRAM	Static Random-Access Memory
FMPLL	Frequency-Modulated Phase-Locked Loop	SSCM	System Status Configuration Module
FlexRay	FlexRay Communication Controller	STM	System Timer Module
I2C	Inter-integrated Circuit Bus	SWT	Software Watchdog Timer
IMUX	Internal Multiplexer	STCU	Self Test Control Unit
INTC	Interrupt Controller	WKPU	Wakeup Unit

Notes:
1) 10 dedicated channels plus up to 19 shared channels. See the device-comparison table.
2) Package dependent. 27 or 33 dedicated channels plus up to 19 shared channels. See the device-comparison table.
3) 16 x precision channels (ANP) are mapped on input only I/O cells.

Table 3 summarizes the functions of the blocks present on the SPC564Bxx and SPC56ECxx.

Table 3. SPC564Bxx and SPC56ECxx series block summary

Block	Function
Analog-to-digital converter (ADC)	Converts analog voltages to digital values
Boot assist module (BAM)	A block of read-only memory containing VLE code which is executed according to the boot mode of the device
Clock monitor unit (CMU)	Monitors clock source (internal and external) integrity
Cross triggering unit (CTU)	Enables synchronization of ADC conversions with a timer event from the eMIOS or from the PIT
Cryptographic Security Engine (CSE)	Supports the encoding and decoding of any kind of data
Crossbar (XBAR) switch	Supports simultaneous connections between two master ports and three slave ports. The crossbar supports a 32-bit address bus width and a 64-bit data bus width
DMA Channel Multiplexer (DMAMUX)	Allows to route DMA sources (called slots) to DMA channels
Deserial serial peripheral interface (DSPI)	Provides a synchronous serial interface for communication with external devices
Error Correction Status Module (ECSM)	Provides a myriad of miscellaneous control functions for the device including program-visible information about configuration and revision levels, a reset status register, wakeup control for exiting sleep modes, and optional features such as information on memory errors reported by error-correcting codes
Enhanced Direct Memory Access (eDMA)	Performs complex data transfers with minimal intervention from a host processor via “n” programmable channels.
Enhanced modular input output system (eMIOS)	Provides the functionality to generate or measure events
Flash memory	Provides non-volatile storage for program code, constants and variables
FlexCAN (controller area network)	Supports the standard CAN communications protocol
FMPLL (frequency-modulated phase-locked loop)	Generates high-speed system clocks and supports programmable frequency modulation
FlexRay (FlexRay communication controller)	Provides high-speed distributed control for advanced automotive applications
Fast Ethernet Controller (FEC)	Ethernet Media Access Controller (MAC) designed to support both 10 and 100 Mbps Ethernet/IEEE 802.3 networks
Internal multiplexer (IMUX) SIUL subblock	Allows flexible mapping of peripheral interface on the different pins of the device
Inter-integrated circuit (I^2C™) bus	A two wire bidirectional serial bus that provides a simple and efficient method of data exchange between devices
Interrupt controller (INTC)	Provides priority-based preemptive scheduling of interrupt requests for both e200z0h and e200z4d cores
JTAG controller	Provides the means to test chip functionality and connectivity while remaining transparent to system logic when not in test mode

2.1 Pad types

In the device the following types of pads are available for system pins and functional port pins:

S = Slow[a]

M = Medium[a],[b]

F = Fast[a],[b]

I = Input only with analog feature[a]

A = Analog

2.2 System pins

The system pins are listed in *Table 4*.

Table 4. System pin descriptions

Port pin	Function	I/O direction	Pad type	RESET config.	Pin number		
					LQFP 176	LQFP 208	LBGA 256
RESET	Bidirectional reset with Schmitt-Trigger characteristics and noise filter.	I/O	M	Input, weak pull-up only after PHASE2	29	29	K1
EXTAL	Analog input of the oscillator amplifier circuit. Needs to be grounded if oscillator bypass mode is used.	I	A[1]	—	58	74	T8
XTAL	Analog output of the oscillator amplifier circuit, when the oscillator is not in bypass mode. Analog input for the clock generator when the oscillator is in bypass mode.	I/O	A[1]	—	56	72	T7

1. For analog pads, it is not recommended to enable IBE if APC is enabled to avoid extra current in middle range voltage.

a. See the I/O pad electrical characteristics in the device datasheet for details.

b. All medium and fast pads are in slow configuration by default at reset and can be configured as fast or medium. For example, Fast/Medium pad will be Medium by default at reset. Similarly, Slow/Medium pad will be Slow by default. Only exception is PC[1] which is in medium configuration by default (refer to PCR.SRC in the reference manual, Pad Configuration Registers (PCR0—PCR198)).

Table 5. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET config.	Pin number		
								LQFP 176	LQFP 208	LBGA256
PA[5]	PCR[5]	AF0 AF1 AF2	GPIO[5] E0UC[5] LIN4TX	SIUL eMIOS_0 LINFlexD_4	I/O I/O O	M/S	Tristate	146	170	C10
PA[6]	PCR[6]	AF0 AF1 AF2 AF3 — —	GPIO[6] E0UC[6] — CS1_1 LIN4RX EIRQ[1]	SIUL eMIOS_0 — DSPI_1 LINFlexD_4 SIUL	I/O I/O — O I I	S	Tristate	147	171	D11
PA[7]	PCR[7]	AF0 AF1 AF2 AF3 — — —	GPIO[7] E0UC[7] LIN3TX — RXD[2] EIRQ[2] ADC1_S[1]	SIUL eMIOS_0 LINFlexD_3 — FEC SIUL ADC_1	I/O I/O O — I I I	M/S	Tristate	128	152	C15
PA[8]	PCR[8]	AF0 AF1 AF2 AF3 — — — —	GPIO[8] E0UC[8] E0UC[14] — RXD[1] EIRQ[3] ABS[0] LIN3RX	SIUL eMIOS_0 eMIOS_0 — FEC SIUL MC_RGM LINFlexD_3	I/O I/O I/O — I I I I	M/S	Input, weak pull-up	129	153	B16
PA[9]	PCR[9]	AF0 AF1 AF2 AF3 — —	GPIO[9] E0UC[9] — CS2_1 RXD[0] FAB	SIUL eMIOS_0 — DSPI1 FEC MC_RGM	I/O I/O — O I I	M/S	Pull-down	130	154	B15

Table 5. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET config.	Pin number		
								LQFP 176	LQFP 208	LBGA256
PC[8]	PCR[40]	AF0 AF1 AF2 AF3	GPIO[40] LIN2TX E0UC[3] —	SIUL LINFlexD_2 eMIOS_0 —	I/O O I/O —	S	Tristate	175	207	B3
PC[9]	PCR[41]	AF0 AF1 AF2 AF3 — —	GPIO[41] — E0UC[7] — LIN2RX WKPU[13]	SIUL — eMIOS_0 — LINFlexD_2 WKPU	I/O — I/O — I I	S	Tristate	2	2	C3
PC[10]	PCR[42]	AF0 AF1 AF2 AF3	GPIO[42] CAN1TX CAN4TX MA[1]	SIUL FlexCAN_1 FlexCAN_4 ADC_0	I/O O O O	M/S	Tristate	36	36	L1
PC[11]	PCR[43]	AF0 AF1 AF2 AF3 — — —	GPIO[43] — — MA[2] CAN1RX CAN4RX WKPU[5]	SIUL — — ADC_0 FlexCAN_1 FlexCAN_4 WKPU	I/O — — O I I I	S	Tristate	35	35	K4
PC[12]	PCR[44]	AF0 AF1 AF2 AF3 ALT4 — —	GPIO[44] E0UC[12] — — FR_DBG[0] SIN_2 EIRQ[19]	SIUL eMIOS_0 — — Flexray DSPI_2 SIUL	I/O I/O — — O I I	M/S	Tristate	173	205	B4
PC[13]	PCR[45]	AF0 AF1 AF2 AF3 ALT4	GPIO[45] E0UC[13] SOUT_2 — FR_DBG[1]	SIUL eMIOS_0 DSPI_2 — Flexray	I/O I/O O — O	M/S	Tristate	174	206	A3

Table 5. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET config.	Pin number		
								LQFP 176	LQFP 208	LBGA256
PH[8]	PCR[120]	AF0 AF1 AF2 AF3	GPIO[120] E1UC[10] CS2_2 MA[0]	SIUL eMIOS_1 DSPI_2 ADC_0	I/O I/O O O	M/S	Tristate	166	190	A6
PH[9][6]	PCR[121]	AF0 AF1 AF2 AF3 —	GPIO[121] — — — TCK	SIUL — — — JTAGC	I/O — — — I	S	Input, weak pull-up	155	179	A11
PH[10][6]	PCR[122]	AF0 AF1 AF2 AF3 —	GPIO[122] — — — TMS	SIUL — — — JTAGC	I/O — — — I	M/S	Input, weak pull-up	148	172	D10
PH[11]	PCR[123]	AF0 AF1 AF2 AF3	GPIO[123] SOUT_3 CS0_4 E1UC[5]	SIUL DSPI_3 DSPI_4 eMIOS_1	I/O O I/O I/O	M/S	Tristate	140	164	A13
PH[12]	PCR[124]	AF0 AF1 AF2 AF3	GPIO[124] SCK_3 CS1_4 E1UC[25]	SIUL DSPI_3 DSPI_4 eMIOS_1	I/O I/O O I/O	M/S	Tristate	141	165	B12
PH[13]	PCR[125]	AF0 AF1 AF2 AF3	GPIO[125] SOUT_4 CS0_3 E1UC[26]	SIUL DSPI_4 DSPI_3 eMIOS_1	I/O O I/O I/O	M/S	Tristate	9	9	B1
PH[14]	PCR[126]	AF0 AF1 AF2 AF3	GPIO[126] SCK_4 CS1_3 E1UC[27]	SIUL DSPI_4 DSPI_3 eMIOS_1	I/O I/O O I/O	M/S	Tristate	10	10	C1
PH[15]	PCR[127]	AF0 AF1 AF2 AF3	GPIO[127] SOUT_5 — E1UC[17]	SIUL DSPI_5 — eMIOS_1	I/O O — I/O	M/S	Tristate	8	8	E3

Table 5. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET config.	Pin number		
								LQFP 176	LQFP 208	LBGA256
PK[14]	PCR[174]	AF0 AF1 AF2 AF3	GPIO[174] CAN3TX CS3_7 CS0_1	SIUL FlexCAN_3 DSPI_7 DSPI_1	I/O O O I/O	M/S	Tristate	—	202	J12
PK[15]	PCR[175]	AF0 AF1 AF2 AF3 — —	GPIO[175] — — — SIN_1 SIN_7	SIUL — — — DSPI_1 DSPI_7	I/O — — — I I	M/S	Tristate	—	203	D5
PL[0]	PCR[176]	AF0 AF1 AF2 AF3	GPIO[176] SOUT_1 SOUT_7 —	SIUL DSPI_1 DSPI_7 —	I/O O O —	M/S	Tristate	—	204	C4
PL[1]	PCR[177]	AF0 AF1 AF2 AF3	GPIO[177] — — —	SIUL — — —	I/O — — —	M/S	Tristate	—	—	F7
PL[2]	PCR[178][7]	AF0 AF1 AF2 AF3	GPIO[178] — MDO0[8] —	SIUL — Nexus —	I/O — O —	M/S	Tristate	—	—	F5
PL[3]	PCR[179]	AF0 AF1 AF2 AF3	GPIO[179] — MDO1 —	SIUL — Nexus —	I/O — O —	M/S	Tristate	—	—	G5
PL[4]	PCR[180]	AF0 AF1 AF2 AF3	GPIO[180] — MDO2 —	SIUL — Nexus —	I/O — O —	M/S	Tristate	—	—	H5
PL[5]	PCR[181]	AF0 AF1 AF2 AF3	GPIO[181] — MDO3 —	SIUL — Nexus —	I/O — O —	M/S	Tristate	—	—	J5

4. The width of input pulse in between 40 ns to 1000 ns is indeterminate. It may pass the noise or may not depending on silicon sample to sample variation.

3.6.3 I/O output DC characteristics

The following tables provide DC characteristics for bidirectional pads:

- *Table 15* provides weak pull figures. Both pull-up and pull-down resistances are supported.
- *Table 16* provides output driver characteristics for I/O pads when in SLOW configuration.
- *Table 17* provides output driver characteristics for I/O pads when in MEDIUM configuration.
- *Table 18* provides output driver characteristics for I/O pads when in FAST configuration.

Table 15. I/O pull-up/pull-down DC electrical characteristics

Symbol		C	Parameter	Conditions(1),(2)		Value			Unit
						Min	Typ	Max	
$\|I_{WPU}\|$	CC	P	Weak pull-up current absolute value	$V_{IN} = V_{IL}$, V_{DD} = 5.0 V ± 10%	PAD3V5V = 0	10	—	150	µA
		C			PAD3V5V = 1(3)	10	—	250	
		P		$V_{IN} = V_{IL}$, V_{DD} = 3.3 V ± 10%	PAD3V5V = 1	10	—	150	
$\|I_{WPD}\|$	CC	P	Weak pull-down current absolute value	$V_{IN} = V_{IH}$, V_{DD} = 5.0 V ± 10%	PAD3V5V = 0	10	—	150	µA
		C			PAD3V5V = 1	10	—	250	
		P		$V_{IN} = V_{IH}$, V_{DD} = 3.3 V ± 10%	PAD3V5V = 1	10	—	150	

1. V_{DD} = 3.3 V ± 10 % / 5.0 V ± 10 %, T_A = –40 to 125 °C, unless otherwise specified.
2. V_{DD} as mentioned in the table is $V_{DD\_HV\_A}$/$V_{DD\_HV\_B}$.
3. The configuration PAD3V5 = 1 when V_{DD} = 5 V is only a transient configuration during power-up. All pads but RESET and Nexus output (MDOx, EVTO, MCKO) are configured in input or in high impedance state.

Table 16. SLOW configuration output buffer electrical characteristics

Symbol		C	Parameter	Conditions(1),(2)		Value			Unit
						Min	Typ	Max	
V_{OH}	CC	P	Output high level SLOW configuration	Push Pull	I_{OH} = –3 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	0.8V_{DD}	—	—	V
		C			I_{OH} = –3 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 1(3)	0.8V_{DD}	—	—	
		P			I_{OH} = –1.5 mA, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	V_{DD} – 0.8	—	—	

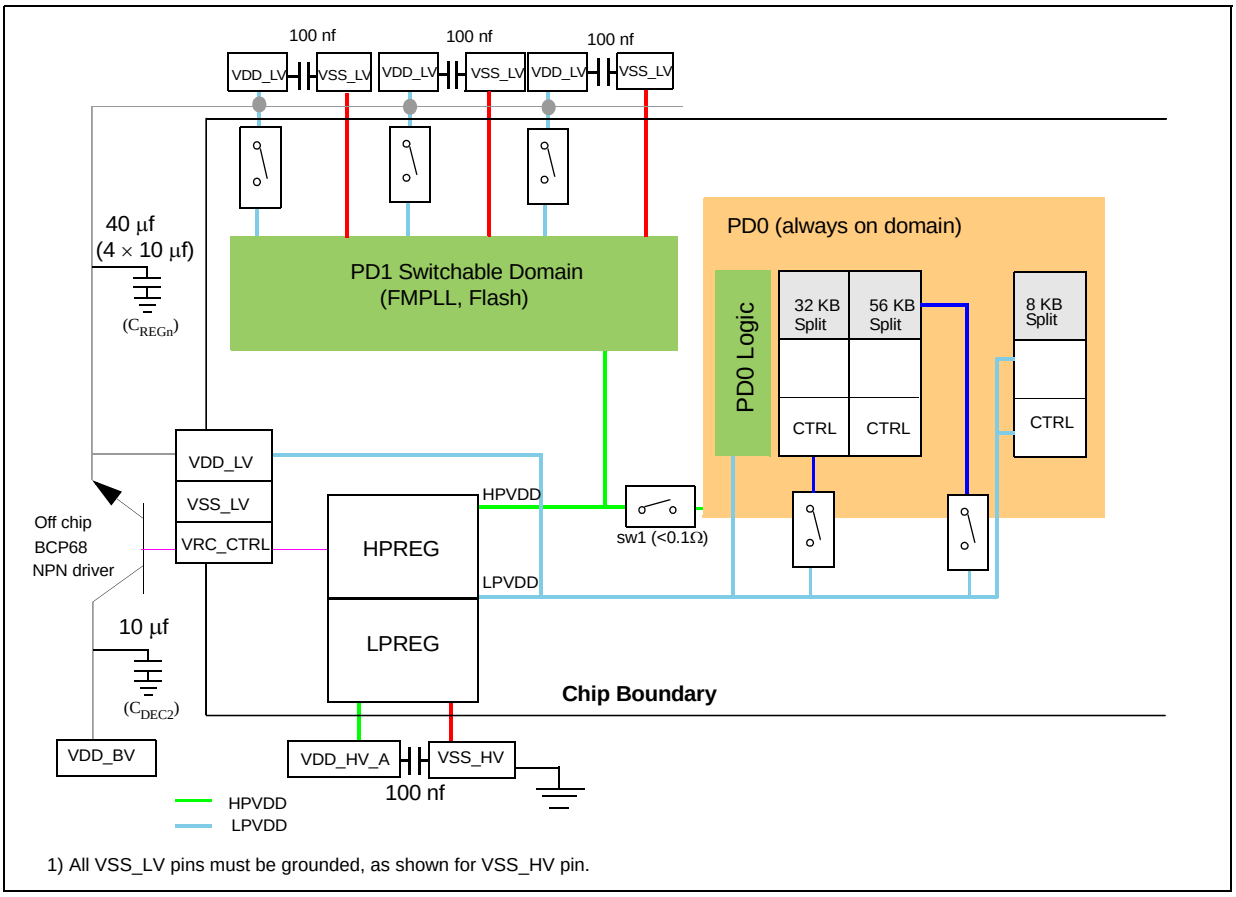
3.8 Power management electrical characteristics

3.8.1 Voltage regulator electrical characteristics

The device implements an internal voltage regulator to generate the low voltage core supply V_{DD_LV} from the high voltage supply $V_{DD\_HV\_A}$. The following supplies are involved:

- HV: High voltage external power supply for voltage regulator module. This must be provided externally through $V_{DD\_HV\_A}$ power pin.
- LV: Low voltage internal power supply for core, FMPLL and Flash digital logic. This is generated by the on-chip VREG with an external ballast (BCP68 NPN device). It is further split into four main domains to ensure noise isolation between critical LV modules within the device:
  - LV_COR: Low voltage supply for the core. It is also used to provide supply for FMPLL through double bonding.
  - LV_CFLA0/CFLA1: Low voltage supply for the two code Flash modules. It is shorted with LV_COR through double bonding.
  - LV_DFLA: Low voltage supply for data Flash module. It is shorted with LV_COR through double bonding.
  - LV_PLL: Low voltage supply for FMPLL. It is shorted to LV_COR through double bonding.

Figure 8. Voltage regulator capacitance connection



1) All VSS_LV pins must be grounded, as shown for VSS_HV pin.

Table 23. Voltage regulator electrical characteristics (continued)

Symbol		C	Parameter	Conditions[1]	Value[2]			Unit
					Min	Typ	Max	
I_{MREG}	SR	—	Main regulator current provided to V_{DD_LV} domain	—	—	—	350	mA
$I_{MREGINT}$	CC	D	Main regulator module current consumption	I_{MREG} = 200 mA	—	—	2	mA
				I_{MREG} = 0 mA	—	—	1	
V_{LPREG}	CC	P	Low power regulator output voltage	After trimming T_A = 25 °C	1.17	1.27	1.32	V
I_{LPREG}	SR	—	Low power regulator current provided to V_{DD_LV} domain	—	—	—	50	mA
$I_{LPREGINT}$	CC	D	Low power regulator module current consumption	I_{LPREG} = 15 mA; T_A = 55 °C	—	—	600	µA
		—		I_{LPREG} = 0 mA; T_A = 55 °C	—	20	—	
$I_{VREGREF}$	CC	D	Main LVDs and reference current consumption (low power and main regulator switched off)	T_A = 55 °C	—	2	—	µA
$I_{VREDLVD12}$	CC	D	Main LVD current consumption (switch-off during standby)	T_A = 55 °C	—	1	—	µA
$I_{DD\_HV\_A}$	CC	D	In-rush current on V_{DD_BV} during power-up	—	—	—	600 (3)	mA

1. $V_{DD\_HV\_A}$ = 3.3 V ± 10 % / 5.0 V ± 10 %, T_A = –40 to 125 °C, unless otherwise specified.
2. All values need to be confirmed during device validation.
3. Inrush current is seen more like steps of 600 mA peak. The startup of the regulator happens in steps of 50 mV in ~25 steps to reach ~1.2 V V_{DD_LV}. Each step peak current is within 600 mA

3.8.3 Voltage monitor electrical characteristics

The device implements a Power-on Reset module to ensure correct power-up initialization, as well as four low voltage detectors to monitor the $V_{DD\_HV\_A}$ and the V_{DD_LV} voltage while device is supplied:

- POR monitors $V_{DD\_HV\_A}$ during the power-up phase to ensure device is maintained in a safe reset state
- LVDHV3 monitors $V_{DD\_HV\_A}$ to ensure device is reset below minimum functional supply
- LVDHV5 monitors $V_{DD\_HV\_A}$ when application uses device in the 5.0 V±10 % range
- LVDLVCOR monitors power domain No. 1 (PD1)
- LVDLVBKP monitors power domain No. 0 (PD0). VDD_LV is same as PD0 supply.

Note: When enabled, PD2 (RAM retention) is monitored through LVD_DIGBKP.

Figure 9. Low voltage monitor vs. Reset

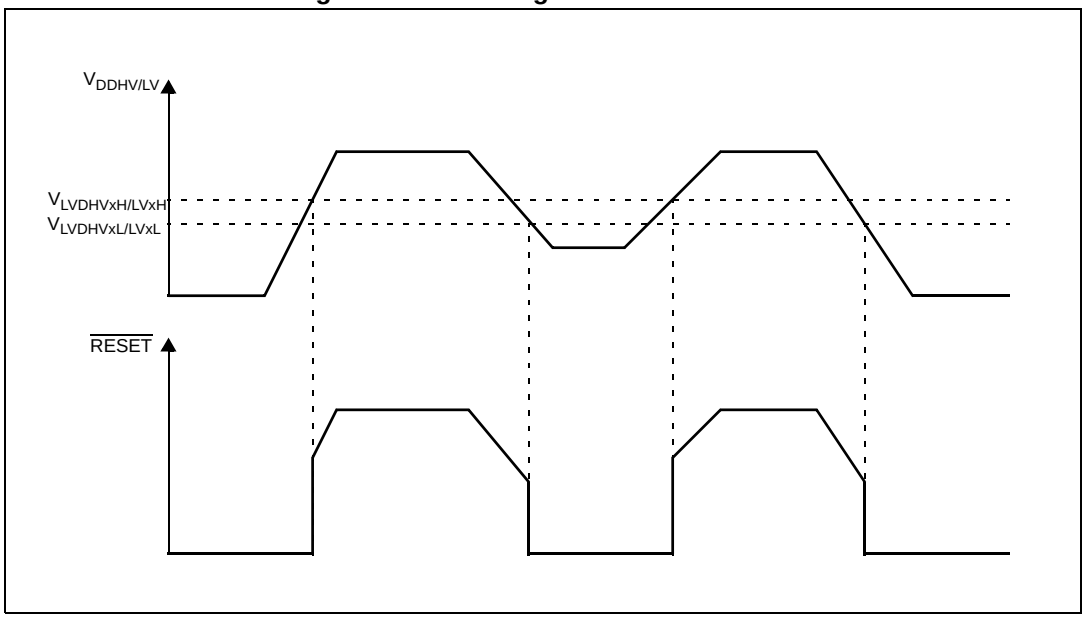


Table 24. Low voltage monitor electrical characteristics

Symbol		C	Parameter	Conditions[1]	Value[2]			Unit
					Min	Typ	Max	
V_{PORUP}	SR	P	Supply for functional POR module	—	1.0	—	5.5	V
V_{PORH}	CC	P	Power-on reset threshold	—	1.5	—	2.6	
$V_{LVDHV3H}$	CC	T	LVDHV3 low voltage detector high threshold	—	2.7	—	2.85	
$V_{LVDHV3L}$	CC	T	LVDHV3 low voltage detector low threshold	—	2.6	—	2.74	
$V_{LVDHV5H}$	CC	T	LVDHV5 low voltage detector high threshold	—	4.3	—	4.5	
$V_{LVDHV5L}$	CC	T	LVDHV5 low voltage detector low threshold	—	4.2	—	4.4	
$V_{LVDLVCORL}$	CC	P	LVDLVCOR low voltage detector low threshold	T_A = 25 °C, after trimming	1.08	—	1.17	
$V_{LVDLVBKPL}$	CC	P	LVDLVBKP low voltage detector low threshold		1.08	—	1.17	

1. V_{DD} = 3.3 V ± 10 % / 5.0 V ± 10 %, T_A = –40 to 125 °C, unless otherwise specified.
2. All values need to be confirmed during device validation.

3.9 Low voltage domain power consumption

Table 25 provides DC electrical characteristics for significant application modes. These values are indicative values; actual consumption depends on the application.

ECC circuitry provides correction of single bit faults and is used to improve further automotive reliability results. Some units will experience single bit corrections throughout the life of the product with no impact to product reliability.

Table 29. Flash memory read access timing(1)

Symbol		C	Parameter	Conditions(2)		Frequency range	Unit
				Code flash memory	Data flash memory		
f_{READ}	CC	P	Maximum frequency for Flash reading	5 wait states	13 wait states	120 —100	MHz
		C		4 wait states	11 wait states	100—80	
		D		3 wait states	9 wait states	80—64	
		C		2 wait states	7 wait states	64—40	
		C		1 wait states	4 wait states	40—20	
		C		0 wait states	2 wait states	20—0	

1. Max speed is the maximum speed allowed including PLL frequency modulation (FM).
2. V_{DD} = 3.3 V ± 10 % / 5.0 V ± 10 %, T_A = –40 to 125 °C, unless otherwise specified.

3.10.2 Flash memory power supply DC characteristics

Table 30 shows the flash memory power supply DC characteristics on external supply.

Table 30. Flash memory power supply DC electrical characteristics

Symbol		Parameter	Conditions(1)		Value(2)			Unit
					Min	Typ	Max	
I_{CFREAD}(3)	CC	Sum of the current consumption on $V_{DD\_HV\_A}$ on read access	Flash memory module read f_{CPU} = 120 MHz + 2%(4)	Code flash memory			33	mA
I_{DFREAD}(3)				Data flash memory			13	
I_{CFMOD}(3)	CC	Sum of the current consumption on $V_{DD\_HV\_A}$ (program/erase)	Program/Erase on-going while reading flash memory registers f_{CPU} = 120 MHz + 2% (4)	Code flash memory			52	mA
I_{DFMOD}(3)				Data flash memory			13	
I_{CFLPW}(3)	CC	Sum of the current consumption on $V_{DD\_HV\_A}$ during flash memory low power mode		Code flash memory			1.1	mA
I_{CFPWD}(3)	CC	Sum of the current consumption on $V_{DD\_HV\_A}$ during flash memory power down mode		Code flash memory			150	µA
I_{DFPWD}(3)				Data flash memory			150	

1. V_{DD} = 3.3 V ± 10 % / 5.0 V ± 10 %, T_A = –40 to 125 °C, unless otherwise specified.
2. All values need to be confirmed during device validation.
3. Data based on characterization results, not tested in production.
4. f_{CPU} 120 MHz + 2 % can be achieved over full temperature 125 °C ambient, 150 °C junction temperature.

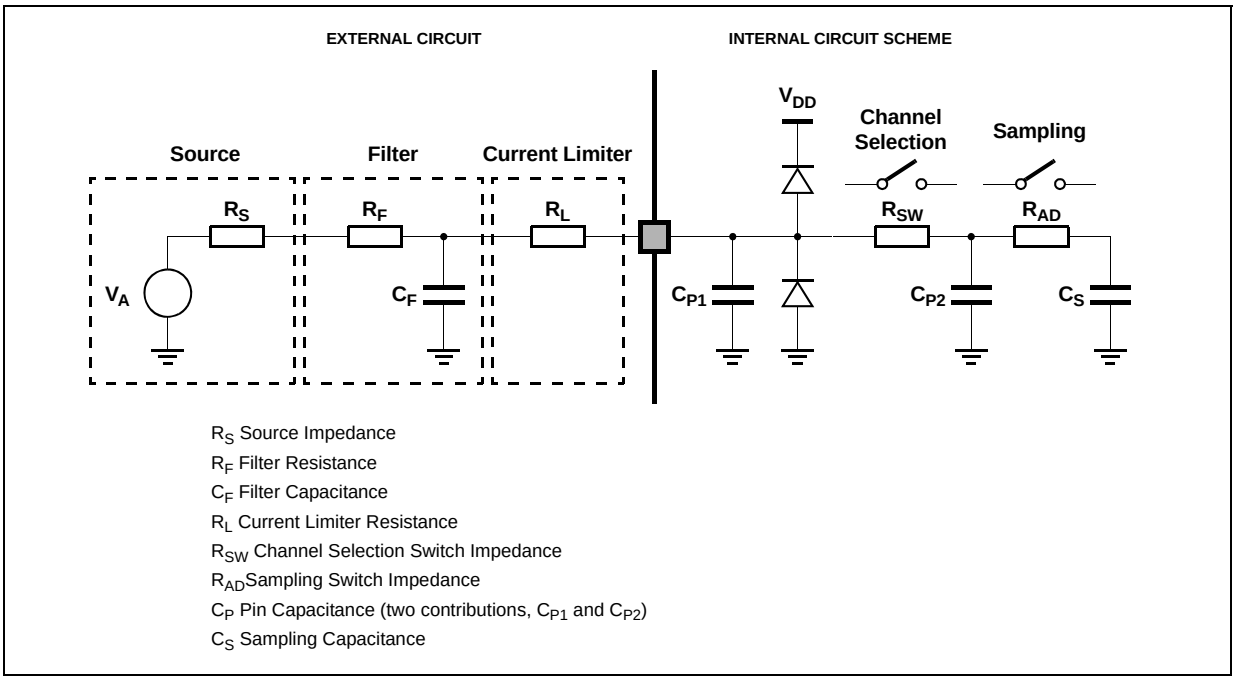
In fact a current sink contributor is represented by the charge sharing effects with the sampling capacitance: being CS and Cp_2 substantially two switched capacitances, with a frequency equal to the conversion rate of the ADC, it can be seen as a resistive path to ground. For instance, assuming a conversion rate of 1MHz, with CS+Cp_2 equal to 3pF, a resistance of 330KΩ is obtained (Reqiv = 1 / (fc*(CS+Cp_2)), where fc represents the conversion rate at the considered channel). To minimize the error induced by the voltage partitioning between this resistance (sampled voltage on CS+Cp_2) and the sum of R_S + R_F, the external circuit must be designed to respect the following relation

Equation 4

$$V_A \bullet \frac{R_S + R_F}{R_{EQ}} < \frac{1}{2} LSB$$

The formula above provides a constraint for external network design, in particular on resistive path.

Figure 16. Input equivalent circuit (precise channels)



R_S Source Impedance
R_F Filter Resistance
C_F Filter Capacitance
R_L Current Limiter Resistance
R_{SW} Channel Selection Switch Impedance
R_{AD}Sampling Switch Impedance
C_P Pin Capacitance (two contributions, C_{P1} and C_{P2})
C_S Sampling Capacitance

3.18.2 MII Transmit Signal Timing (TXD[3:0], TX_EN, TX_ER, TX_CLK)

The transmitter functions correctly up to a TX_CLK maximum frequency of 25 MHz +1%. There is no minimum frequency requirement. In addition, the system clock frequency must exceed four times the TX_CLK frequency in 2:1 mode and two times the TX_CLK frequency in 1:1 mode.

The transmit outputs (TXD[3:0], TX_EN, TX_ER) can be programmed to transition from either the rising or falling edge of TX_CLK, and the timing is the same in either case. This options allows the use of non-compliant MII PHYs.

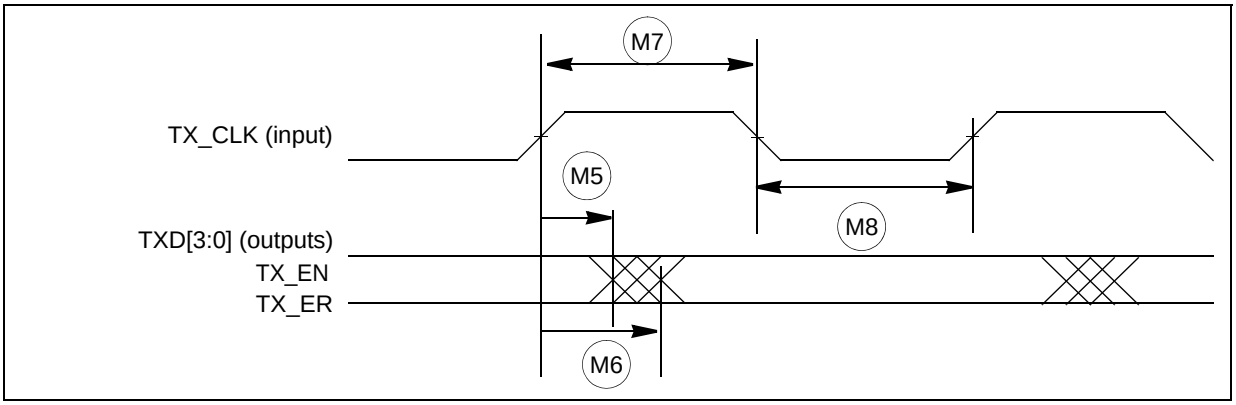
Refer to the Fast Ethernet Controller (FEC) chapter of the SPC564B74 and SPC56EC74 Reference Manual for details of this option and how to enable it.

Table 46. MII transmit signal timing(1)

Spec	Characteristic	Min	Max	Unit
M5	TX_CLK to TXD[3:0], TX_EN, TX_ER invalid	5	—	ns
M6	TX_CLK to TXD[3:0], TX_EN, TX_ER valid	—	25	ns
M7	TX_CLK pulse width high	35%	65%	TX_CLK period
M8	TX_CLK pulse width low	35%	65%	TX_CLK period

1. Output pads configured with SRE = 0b11.

Figure 22. MII transmit signal timing diagram



3.18.3 MII Async Inputs Signal Timing (CRS and COL)

Table 47. MII Async Inputs Signal Timing(1)

Spec	Characteristic	Min	Max	Unit
M9	CRS, COL minimum pulse width	1.5	—	TX_CLK period

1. Output pads configured with SRE = 0b11.

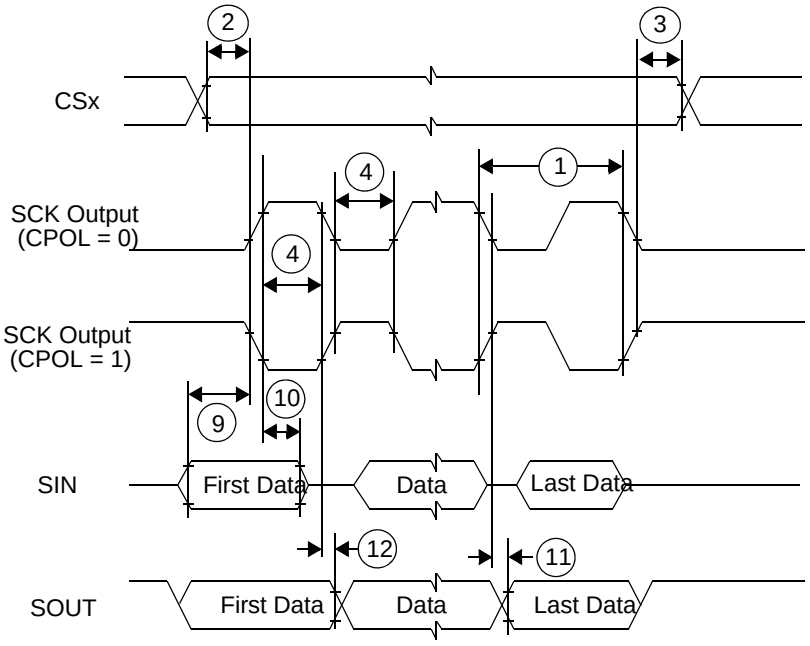
3.19 On-chip peripherals

3.19.1 Current consumption

Table 49. On-chip peripherals current consumption(1)

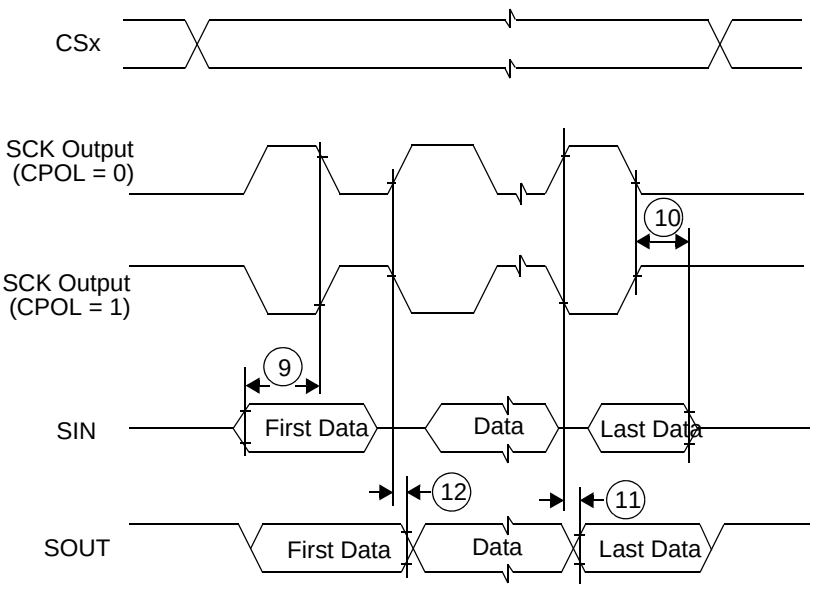
Symbol		C	Parameter	Conditions		Value(2) Typ	Unit
$I_{DD\_HV\_A(CAN)}$	CC	D	CAN (FlexCAN) supply current on $V_{DD\_HV\_A}$	500 Kbps	Total (static + dynamic) consumption: FlexCAN in loop-back mode XTAL@8 MHz used as CAN engine clock source Message sending period is 580 µs	$7.652 \times f_{periph} + 84.73$	µA
				125 Kbps		$8.0743 \times f_{periph} + 26.757$	
$I_{DD\_HV\_A(eMIOS)}$	CC	D	eMIOS supply current on $V_{DD\_HV\_A}$	Static consumption: eMIOS channel OFF Global prescaler enabled		$28.7 \times f_{periph}$	
				Dynamic consumption: It does not change varying the frequency (0.003 mA)		3	
$I_{DD\_HV\_A(SCI)}$	CC	D	SCI (LINFlex) supply current on $V_{DD\_HV\_A}$	Total (static + dynamic) consumption: LIN mode Baudrate: 20 Kbps		$4.7804 \times f_{periph} + 30.946$	
$I_{DD\_HV\_A(SPI)}$	CC	D	SPI (DSPI) supply current on $V_{DD\_HV\_A}$	Ballast static consumption (only clocked)		1	
				Ballast dynamic consumption (continuous communication): Baudrate: 2 Mbit Transmission every 8 µs Frame: 16 bits		$16.3 \times f_{periph}$	
$I_{DD\_HV\_A(ADC)}$	CC	D	ADC supply current on $V_{DD\_HV\_A}$	V_{DD} = 5.5 V	Ballast static consumption (no conversion)	$0.0409 \times f_{periph}$	mA
				V_{DD} = 5.5 V	Ballast dynamic consumption (continuous conversion)	$0.0049 \times f_{periph}$	

Figure 25. DSPI classic SPI timing–master, CPHA = 0



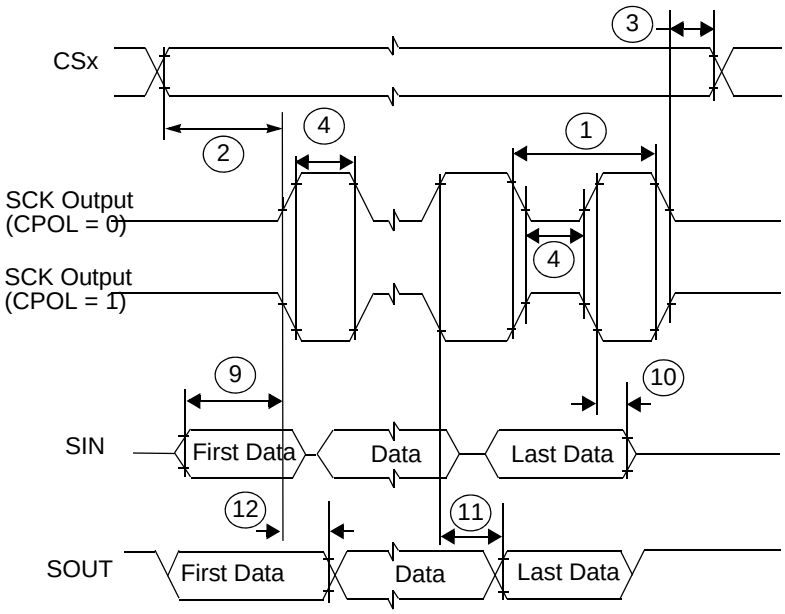
Note: Numbers shown reference *Table 50*.

Figure 26. DSPI classic SPI timing–master, CPHA = 1



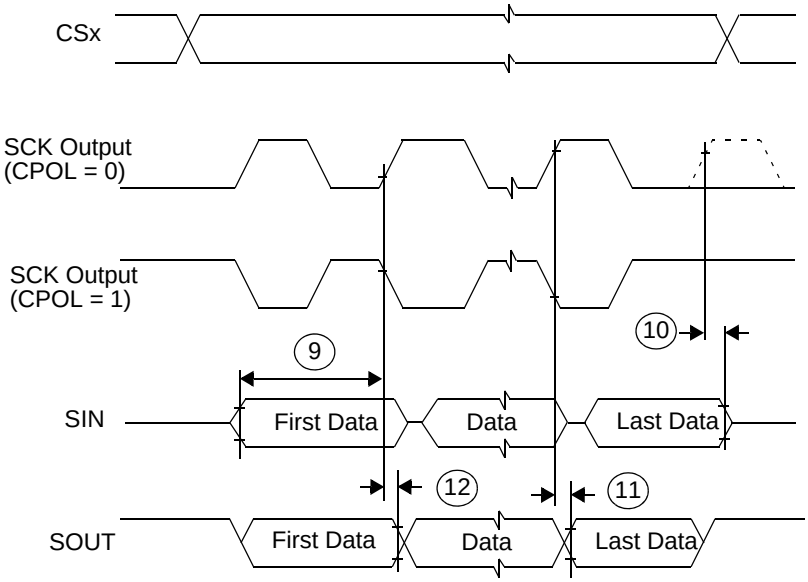
Note: Numbers shown reference *Table 50*.

Figure 29. DSPI modified transfer format timing–master, CPHA = 0



Note: Numbers shown reference *Table 50*.

Figure 30. DSPI modified transfer format timing–master, CPHA = 1



Note: Numbers shown reference *Table 50*.

4 Package characteristics

4.1 ECOPACK®

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

4.2 Package mechanical data

4.2.1 LQFP176 package mechanical drawing

Figure 37. LQFP176 package mechanical drawing

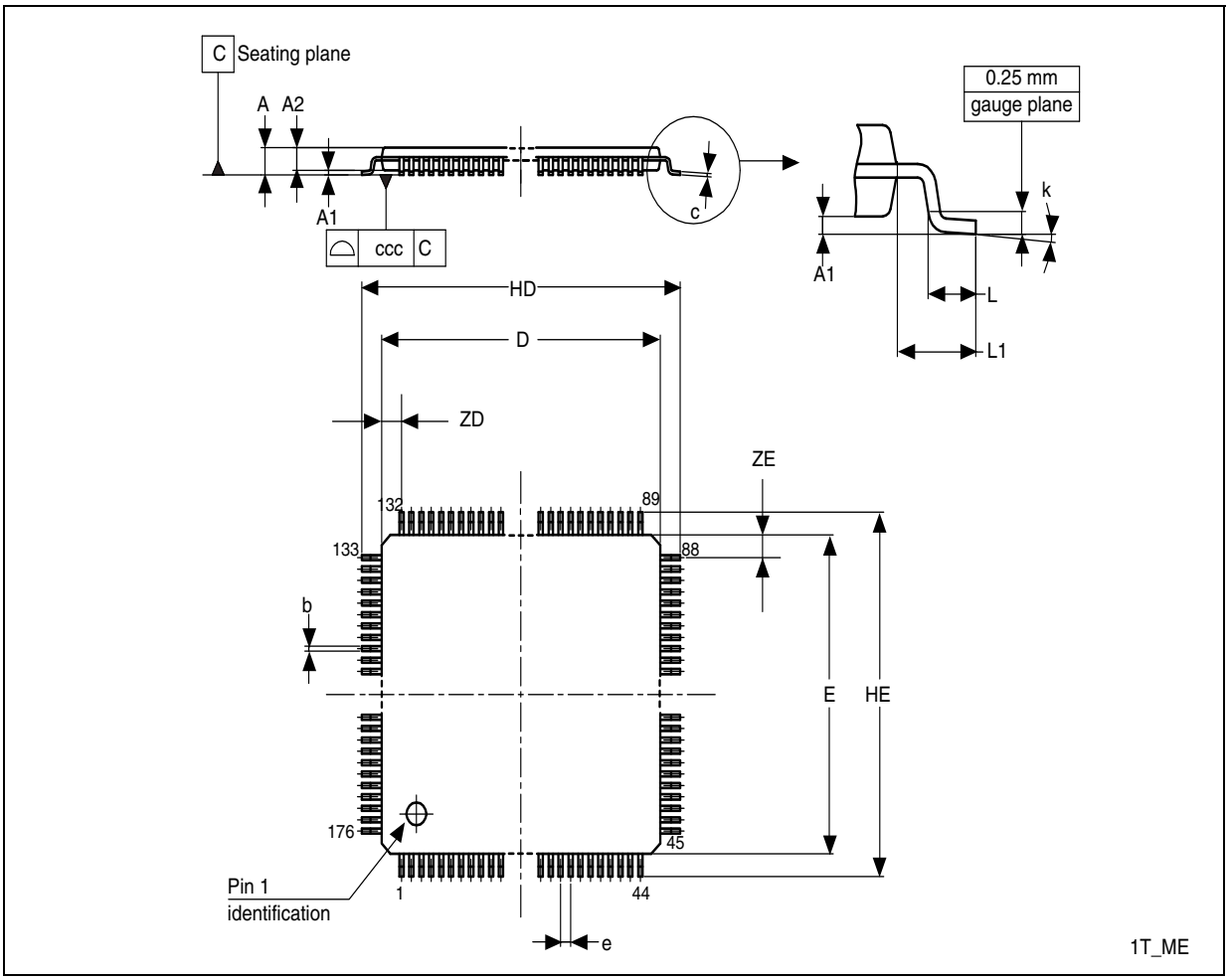


Table 55. LBGA256 mechanical data

Ref	mm		
	Min	Typ	Max
A	1.210		1.700
A1	0.300		
A2		0.300	
A4			0.800
b	0.400	0.500	0.600
D	16.800	17.000	17.200
D1		15.000	
E	16.800	17.000	17.200
E1		15.000	
e	0.900	1.000	1.100
Z	0.750	1.000	1.250
ddd			0.200

Note: The package is designed according to the JEDEC standard No 95-1 Section 14 dedicated to Ball Grid Array Package Design Guide.

Revision history

Table 57 summarizes revisions to this document.

Table 57. Revision history

Date	Revision	Changes
01-Jun-2010	1	Initial Release
17-Dec-2010	2	– Editing and formatting updates throughout the document. – Updated Voltage regulator capacitance connection figure. – Added a new sub-section "V_{DD_BV} Options" – Program and erase specifications: Updated Tdwprogram TYP to 22 us Updated T128Kpperase Max to 5000 ms Added t_{ESUS} parameter – Added recommendation in the Voltage regulator electrical characteristics section. – Added Crystal description table in Fast external crystal oscillator (4 to 140 MHz) electrical characteristics section and corrected the cross-reference to the same. – Added new sections - Pad types, System pins and functional ports – Updated TYP numbers in the Flash program and erase specifications table – Added a new table: Program and erase specifications (Data Flash) – Flash read access timing table: Added Data flash memory numbers – Flash power supply DC electrical characteristics table: Updated IDFREAD and IDFMOD values for Data flash, Removed IDFLPW parameter – Updated feature list. – SPC564Bxx and SPC56ECxx family comparison table: Updated ADC channels and added ADC footnotes. – SPC564Bxx and SPC56ECxx block diagram: Updated ADC channels and added legends. – SPC564Bxx and SPC56ECxx series block summary: Added new blocks. – Functional Port Pin Descriptions table: Added OSC32k_XTAL and OSC32k_EXTAL function at PB8 and PB9 port pins. – Electrical Characteristics: Replaced VSS with VSS_HV throughout the section. – Absolute maximum ratings, Recommended operating conditions (3.3 V) and Recommended operating conditions (5.0 V) tables: VRC_CTRL min is updated to "0". – Recommended operating conditions (3.3 V) and Recommended operating conditions (5.0 V) tables: Clarified VIN parameter, clarified footnote 2 in both tables. – LQFP thermal characteristics section: Added numbers for LQFP packages. – Low voltage power domain electrical characteristics table: Clarified footnotes based upon review comments. – Code flash memory—Program and erase specifications: Updated tESRT to 20 ms. – ADC electrical characteristics section: Replace ADC0 with ADC_0 and ADC1 with ADC_1 throughout the document. DSPI characteristics section: Replaced PCSx with CSx in all figures and tables.