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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z4d
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, LINbus, SPI, UART/USART
Peripherals	DMA, POR, PWM, WDT
Number of I/O	147
Program Memory Size	1.5MB (1.5M x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 27x10b, 5x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP
Supplier Device Package	176-LQFP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/spc564b64l7c9e0x

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Table 5. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET config.	Pin number		
								LQFP 176	LQFP 208	LBGA256
PA[10]	PCR[10]	AF0 AF1 AF2 AF3 — — —	GPIO[10] E0UC[10] SDA LIN2TX COL ADC1_S[2] SIN_1	SIUL eMIOS_0 I^2C LINFlexD_2 FEC ADC_1 DSPI_1	I/O I/O I/O O I I I	M/S	Tristate	131	155	A15
PA[11]	PCR[11]	AF0 AF1 AF2 AF3 — — — —	GPIO[11] E0UC[11] SCL — RX_ER EIRQ[16] LIN2RX ADC1_S[3]	SIUL eMIOS_0 I^2C — FEC SIUL LINFlexD_2 ADC_1	I/O I/O I/O — I I I I	M/S	Tristate	132	156	B14
PA[12]	PCR[12]	AF0 AF1 AF2 AF3 — —	GPIO[12] — E0UC[28] CS3_1 EIRQ[17] SIN_0	SIUL — eMIOS_0 DSPI1 SIUL DSPI_0	I/O — I/O O I I	S	Tristate	53	69	P6
PA[13]	PCR[13]	AF0 AF1 AF2 AF3	GPIO[13] SOUT_0 E0UC[29] —	SIUL DSPI_0 eMIOS_0 —	I/O O I/O —	M/S	Tristate	52	66	R5
PA[14]	PCR[14]	AF0 AF1 AF2 AF3 —	GPIO[14] SCK_0 CS0_0 E0UC[0] EIRQ[4]	SIUL DSPI_0 DSPI_0 eMIOS_0 SIUL	I/O I/O I/O I/O I	M/S	Tristate	50	58	P4
PA[15]	PCR[15]	AF0 AF1 AF2 AF3 —	GPIO[15] CS0_0 SCK_0 E0UC[1] WKPU[10]	SIUL DSPI_0 DSPI_0 eMIOS_0 WKPU	I/O I/O I/O I/O I	M/S	Tristate	48	56	R2

Table 5. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET config.	Pin number		
								LQFP 176	LQFP 208	LBGA256
PD[15]	PCR[63]	AF0 AF1 AF2 AF3 ALT4 —	GPIO[63] CS2_1 E0UC[27] — FR_DBG[1] ADC0_S[7]	SIUL DSPI_1 eMIOS_0 — Flexray ADC_0	I/O O I/O — O I	S	Tristate	106	128	J13
PE[0]	PCR[64]	AF0 AF1 AF2 AF3 — —	GPIO[64] E0UC[16] — — CAN5RX WKPU[6]	SIUL eMIOS_0 — — FlexCAN_5 WKPU	I/O I/O — — I I	S	Tristate	18	18	G2
PE[1]	PCR[65]	AF0 AF1 AF2 AF3	GPIO[65] E0UC[17] CAN5TX —	SIUL eMIOS_0 FlexCAN_5 —	I/O I/O O —	M/S	Tristate	20	20	F4
PE[2]	PCR[66]	AF0 AF1 AF2 AF3 ALT4 — —	GPIO[66] E0UC[18] — — FR_A_TX_EN SIN_1 EIRQ[21]	SIUL eMIOS_0 — — Flexray DSPI_1 SIUL	I/O I/O — — O I I	M/S	Tristate	156	180	A7
PE[3]	PCR[67]	AF0 AF1 AF2 AF3 — —	GPIO[67] E0UC[19] SOUT_1 — FR_A_RX WKPU[29]	SIUL eMIOS_0 DSPI_1 — Flexray WKPU	I/O I/O O — I I	M/S	Tristate	157	181	A10
PE[4]	PCR[68]	AF0 AF1 AF2 AF3 ALT4 —	GPIO[68] E0UC[20] SCK_1 — FR_B_TX EIRQ[9]	SIUL eMIOS_0 DSPI_1 — Flexray SIUL	I/O I/O I/O — O I	M/S	Tristate	160	184	A8

Table 5. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET config.	Pin number		
								LQFP 176	LQFP 208	LBGA256
PE[11]	PCR[75]	AF0 AF1 AF2 AF3 — —	GPIO[75] E0UC[24] CS4_1 — LIN3RX WKPU[14]	SIUL eMIOS_0 DSPI_1 — LINFlexD_3 WKPU	I/O I/O O — I I	S	Tristate	25	25	H3
PE[12]	PCR[76]	AF0 AF1 AF2 AF3 — — — —	GPIO[76] — E1UC[19] — CRS SIN_2 EIRQ[11] ADC1_S[7]	SIUL — eMIOS_1 — FEC DSPI_2 SIUL ADC_1	I/O — I/O — I I I I	M/S	Tristate	133	157	C14
PE[13]	PCR[77]	AF0 AF1 AF2 AF3 —	GPIO[77] SOUT_2 E1UC[20] — RXD[3]	SIUL DSPI_2 eMIOS_1 — FEC	I/O O I/O — I	M/S	Tristate	127	151	C16
PE[14]	PCR[78]	AF0 AF1 AF2 AF3 —	GPIO[78] SCK_2 E1UC[21] — EIRQ[12]	SIUL DSPI_2 eMIOS_1 — SIUL	I/O I/O I/O — I	M/S	Tristate	136	160	A14
PE[15]	PCR[79]	AF0 AF1 AF2 AF3	GPIO[79] CS0_2 E1UC[22] SCK_6	SIUL DSPI_2 eMIOS_1 DSPI_6	I/O I/O I/O I/O	M/S	Tristate	137	161	C12
PF[0]	PCR[80]	AF0 AF1 AF2 AF3 —	GPIO[80] E0UC[10] CS3_1 — ADC0_S[8]	SIUL eMIOS_0 DSPI_1 — ADC_0	I/O I/O O — I	S	Tristate	63	79	P7

Table 5. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET config.	Pin number		
								LQFP 176	LQFP 208	LBGA256
PF[1]	PCR[81]	AF0 AF1 AF2 AF3 —	GPIO[81] E0UC[11] CS4_1 — ADC0_S[9]	SIUL eMIOS_0 DSPI_1 — ADC_0	I/O I/O O — I	S	Tristate	64	80	T6
PF[2]	PCR[82]	AF0 AF1 AF2 AF3 —	GPIO[82] E0UC[12] CS0_2 — ADC0_S[10]	SIUL eMIOS_0 DSPI_2 — ADC_0	I/O I/O I/O — I	S	Tristate	65	81	R6
PF[3]	PCR[83]	AF0 AF1 AF2 AF3 —	GPIO[83] E0UC[13] CS1_2 — ADC0_S[11]	SIUL eMIOS_0 DSPI_2 — ADC_0	I/O I/O O — I	S	Tristate	66	82	R7
PF[4]	PCR[84]	AF0 AF1 AF2 AF3 —	GPIO[84] E0UC[14] CS2_2 — ADC0_S[12]	SIUL eMIOS_0 DSPI_2 — ADC_0	I/O I/O O — I	S	Tristate	67	83	R8
PF[5]	PCR[85]	AF0 AF1 AF2 AF3 —	GPIO[85] E0UC[22] CS3_2 — ADC0_S[13]	SIUL eMIOS_0 DSPI_2 — ADC_0	I/O I/O O — I	S	Tristate	68	84	P8
PF[6]	PCR[86]	AF0 AF1 AF2 AF3 —	GPIO[86] E0UC[23] CS1_1 — ADC0_S[14]	SIUL eMIOS_0 DSPI_1 — ADC_0	I/O I/O O — I	S	Tristate	69	85	N8
PF[7]	PCR[87]	AF0 AF1 AF2 AF3 —	GPIO[87] — CS2_1 — ADC0_S[15]	SIUL — DSPI_1 — ADC_0	I/O — O — I	S	Tristate	70	86	P9

Table 5. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET config.	Pin number		
								LQFP 176	LQFP 208	LBGA256
PH[8]	PCR[120]	AF0 AF1 AF2 AF3	GPIO[120] E1UC[10] CS2_2 MA[0]	SIUL eMIOS_1 DSPI_2 ADC_0	I/O I/O O O	M/S	Tristate	166	190	A6
PH[9][6]	PCR[121]	AF0 AF1 AF2 AF3 —	GPIO[121] — — — TCK	SIUL — — — JTAGC	I/O — — — I	S	Input, weak pull-up	155	179	A11
PH[10][6]	PCR[122]	AF0 AF1 AF2 AF3 —	GPIO[122] — — — TMS	SIUL — — — JTAGC	I/O — — — I	M/S	Input, weak pull-up	148	172	D10
PH[11]	PCR[123]	AF0 AF1 AF2 AF3	GPIO[123] SOUT_3 CS0_4 E1UC[5]	SIUL DSPI_3 DSPI_4 eMIOS_1	I/O O I/O I/O	M/S	Tristate	140	164	A13
PH[12]	PCR[124]	AF0 AF1 AF2 AF3	GPIO[124] SCK_3 CS1_4 E1UC[25]	SIUL DSPI_3 DSPI_4 eMIOS_1	I/O I/O O I/O	M/S	Tristate	141	165	B12
PH[13]	PCR[125]	AF0 AF1 AF2 AF3	GPIO[125] SOUT_4 CS0_3 E1UC[26]	SIUL DSPI_4 DSPI_3 eMIOS_1	I/O O I/O I/O	M/S	Tristate	9	9	B1
PH[14]	PCR[126]	AF0 AF1 AF2 AF3	GPIO[126] SCK_4 CS1_3 E1UC[27]	SIUL DSPI_4 DSPI_3 eMIOS_1	I/O I/O O I/O	M/S	Tristate	10	10	C1
PH[15]	PCR[127]	AF0 AF1 AF2 AF3	GPIO[127] SOUT_5 — E1UC[17]	SIUL DSPI_5 — eMIOS_1	I/O O — I/O	M/S	Tristate	8	8	E3

Table 5. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET config.	Pin number		
								LQFP 176	LQFP 208	LBGA256
PK[0]	PCR[160]	AF0 AF1 AF2 AF3	GPIO[160] CAN1TX CS2_6 —	SIUL FlexCAN_1 DSPI_6 —	I/O O O —	M/S	Tristate	—	62	T3
PK[1]	PCR[161]	AF0 AF1 AF2 AF3 —	GPIO[161] CS3_6 — — CAN4RX	SIUL DSPI_6 — — FlexCAN_4	I/O O — — I	M/S	Tristate	—	41	H4
PK[2]	PCR[162]	AF0 AF1 AF2 AF3	GPIO[162] CAN4TX — —	SIUL FlexCAN_4 — —	I/O O — —	M/S	Tristate	—	42	L4
PK[3]	PCR[163]	AF0 AF1 AF2 AF3 — —	GPIO[163] E1UC[0] — — CAN5RX LIN8RX	SIUL eMIOS_1 — — FlexCAN_5 LINFlexD_8	I/O I/O — — I I	M/S	Tristate	—	43	N1
PK[4]	PCR[164]	AF0 AF1 AF2 AF3	GPIO[164] LIN8TX CAN5TX E1UC[1]	SIUL LINFlexD_8 FlexCAN_5 eMIOS_1	I/O O O I/O	M/S	Tristate	—	44	M3
PK[5]	PCR[165]	AF0 AF1 AF2 AF3 — —	GPIO[165] — — — CAN2RX LIN2RX	SIUL — — — FlexCAN_2 LINFlexD_2	I/O — — — I I	M/S	Tristate	—	45	M5
PK[6]	PCR[166]	AF0 AF1 AF2 AF3	GPIO[166] CAN2TX LIN2TX —	SIUL FlexCAN_2 LINFlexD_2 —	I/O O O —	M/S	Tristate	—	46	M6

Table 5. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET config.	Pin number		
								LQFP 176	LQFP 208	LBGA256
PM[5]	PCR[197]	AF0 AF1 AF2 AF3	GPIO[197] — — —	SIUL — — —	I/O — — —	M/S	Tristate	—	—	F9
PM[6]	PCR[198]	AF0 AF1 AF2 AF3	GPIO[198] — — —	SIUL — — —	I/O — — —	M/S	Tristate	—	—	F6

1. Alternate functions are chosen by setting the values of the PCR.PA bitfields inside the SIUL module. PCR.PA = 000 → AF0; PCR.PA = 001 → AF1; PCR.PA = 010 → AF2; PCR.PA = 011 → AF3; PCR.PA = 100 → ALT4. This is intended to select the output functions; to use one of the input functions, the PCR.IBE bit must be written to '1', regardless of the values selected in the PCR.PA bitfields. For this reason, the value corresponding to an input only function is reported as "—".
2. Multiple inputs are routed to all respective modules internally. The input of some modules must be configured by setting the values of the PSMIO.PADSELx bitfields inside the SIUL module.
3. NMI[0] and NMI[1] have a higher priority than alternate functions. When NMI is selected, the PCR.PA field is ignored.
4. SXOSC's OSC32k_XTAL and OSC32k_EXTAL pins are shared with GPIO functionality. When used as crystal pins, other functionality of the pin cannot be used and it should be ensured that application never programs OBE and PUE bit of the corresponding PCR to "1".
5. If you want to use OSC32K functionality through PB[8] and PB[9], you must ensure that PB[10] is static in nature as PB[10] can induce coupling on PB[9] and disturb oscillator frequency.
6. Out of reset all the functional pins except PC[0:1] and PH[9:10] are available to the user as GPIO.
   PC[0:1] are available as JTAG pins (TDI and TDO respectively).
   PH[9:10] are available as JTAG pins (TCK and TMS respectively).
   It is up to the user to configure these pins as GPIO when needed.
7. When MBIST is enabled to run (STCU Enable = 1), the application must not drive or tie PAD[178] (MDO[0]) to 0 V before the device exits reset (external reset is removed) as the pad is internally driven to 1 to indicate MBIST operation. When MBIST is not enabled (STCU Enable = 0), there are no restriction as the device does not internally drive the pad.
8. These pins can be configured as Nexus pins during reset by the debugger writing to the Nexus Development Interface "Port Control Register" rather than the SIUL. Specifically, the debugger can enable the MDO[7:0], MSEO, and MCKO ports by programming NDI (PCR[MCKO_EN] or PCR[PSTAT_EN]). MDO[8:11] ports can be enabled by programming NDI ((PCR[MCKO_EN] and PCR[FPM]) or PCR[PSTAT_EN]).

4. The width of input pulse in between 40 ns to 1000 ns is indeterminate. It may pass the noise or may not depending on silicon sample to sample variation.

3.6.3 I/O output DC characteristics

The following tables provide DC characteristics for bidirectional pads:

- *Table 15* provides weak pull figures. Both pull-up and pull-down resistances are supported.
- *Table 16* provides output driver characteristics for I/O pads when in SLOW configuration.
- *Table 17* provides output driver characteristics for I/O pads when in MEDIUM configuration.
- *Table 18* provides output driver characteristics for I/O pads when in FAST configuration.

Table 15. I/O pull-up/pull-down DC electrical characteristics

Symbol		C	Parameter	Conditions(1),(2)		Value			Unit
						Min	Typ	Max	
$\|I_{WPU}\|$	CC	P	Weak pull-up current absolute value	$V_{IN} = V_{IL}$, V_{DD} = 5.0 V ± 10%	PAD3V5V = 0	10	—	150	µA
		C			PAD3V5V = 1(3)	10	—	250	
		P		$V_{IN} = V_{IL}$, V_{DD} = 3.3 V ± 10%	PAD3V5V = 1	10	—	150	
$\|I_{WPD}\|$	CC	P	Weak pull-down current absolute value	$V_{IN} = V_{IH}$, V_{DD} = 5.0 V ± 10%	PAD3V5V = 0	10	—	150	µA
		C			PAD3V5V = 1	10	—	250	
		P		$V_{IN} = V_{IH}$, V_{DD} = 3.3 V ± 10%	PAD3V5V = 1	10	—	150	

1. V_{DD} = 3.3 V ± 10 % / 5.0 V ± 10 %, T_A = –40 to 125 °C, unless otherwise specified.
2. V_{DD} as mentioned in the table is $V_{DD\_HV\_A}$/$V_{DD\_HV\_B}$.
3. The configuration PAD3V5 = 1 when V_{DD} = 5 V is only a transient configuration during power-up. All pads but RESET and Nexus output (MDOx, EVTO, MCKO) are configured in input or in high impedance state.

Table 16. SLOW configuration output buffer electrical characteristics

Symbol		C	Parameter	Conditions(1),(2)		Value			Unit
						Min	Typ	Max	
V_{OH}	CC	P	Output high level SLOW configuration	Push Pull	I_{OH} = –3 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	0.8V_{DD}	—	—	V
		C			I_{OH} = –3 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 1(3)	0.8V_{DD}	—	—	
		P			I_{OH} = –1.5 mA, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	V_{DD} – 0.8	—	—	

Table 23. Voltage regulator electrical characteristics (continued)

Symbol		C	Parameter	Conditions[1]	Value[2]			Unit
					Min	Typ	Max	
I_{MREG}	SR	—	Main regulator current provided to V_{DD_LV} domain	—	—	—	350	mA
$I_{MREGINT}$	CC	D	Main regulator module current consumption	I_{MREG} = 200 mA	—	—	2	mA
				I_{MREG} = 0 mA	—	—	1	
V_{LPREG}	CC	P	Low power regulator output voltage	After trimming T_A = 25 °C	1.17	1.27	1.32	V
I_{LPREG}	SR	—	Low power regulator current provided to V_{DD_LV} domain	—	—	—	50	mA
$I_{LPREGINT}$	CC	D	Low power regulator module current consumption	I_{LPREG} = 15 mA; T_A = 55 °C	—	—	600	µA
		—		I_{LPREG} = 0 mA; T_A = 55 °C	—	20	—	
$I_{VREGREF}$	CC	D	Main LVDs and reference current consumption (low power and main regulator switched off)	T_A = 55 °C	—	2	—	µA
$I_{VREDLVD12}$	CC	D	Main LVD current consumption (switch-off during standby)	T_A = 55 °C	—	1	—	µA
$I_{DD\_HV\_A}$	CC	D	In-rush current on V_{DD_BV} during power-up	—	—	—	600 (3)	mA

1. $V_{DD\_HV\_A}$ = 3.3 V ± 10 % / 5.0 V ± 10 %, T_A = –40 to 125 °C, unless otherwise specified.
2. All values need to be confirmed during device validation.
3. Inrush current is seen more like steps of 600 mA peak. The startup of the regulator happens in steps of 50 mV in ~25 steps to reach ~1.2 V V_{DD_LV}. Each step peak current is within 600 mA

3.8.3 Voltage monitor electrical characteristics

The device implements a Power-on Reset module to ensure correct power-up initialization, as well as four low voltage detectors to monitor the $V_{DD\_HV\_A}$ and the V_{DD_LV} voltage while device is supplied:

- POR monitors $V_{DD\_HV\_A}$ during the power-up phase to ensure device is maintained in a safe reset state
- LVDHV3 monitors $V_{DD\_HV\_A}$ to ensure device is reset below minimum functional supply
- LVDHV5 monitors $V_{DD\_HV\_A}$ when application uses device in the 5.0 V±10 % range
- LVDLVCOR monitors power domain No. 1 (PD1)
- LVDLVBKP monitors power domain No. 0 (PD0). VDD_LV is same as PD0 supply.

Note: When enabled, PD2 (RAM retention) is monitored through LVD_DIGBKP.

ECC circuitry provides correction of single bit faults and is used to improve further automotive reliability results. Some units will experience single bit corrections throughout the life of the product with no impact to product reliability.

Table 29. Flash memory read access timing(1)

Symbol		C	Parameter	Conditions(2)		Frequency range	Unit
				Code flash memory	Data flash memory		
f_{READ}	CC	P	Maximum frequency for Flash reading	5 wait states	13 wait states	120 —100	MHz
		C		4 wait states	11 wait states	100—80	
		D		3 wait states	9 wait states	80—64	
		C		2 wait states	7 wait states	64—40	
		C		1 wait states	4 wait states	40—20	
		C		0 wait states	2 wait states	20—0	

1. Max speed is the maximum speed allowed including PLL frequency modulation (FM).
2. V_{DD} = 3.3 V ± 10 % / 5.0 V ± 10 %, T_A = –40 to 125 °C, unless otherwise specified.

3.10.2 Flash memory power supply DC characteristics

Table 30 shows the flash memory power supply DC characteristics on external supply.

Table 30. Flash memory power supply DC electrical characteristics

Symbol		Parameter	Conditions(1)		Value(2)			Unit
					Min	Typ	Max	
I_{CFREAD}(3)	CC	Sum of the current consumption on $V_{DD\_HV\_A}$ on read access	Flash memory module read f_{CPU} = 120 MHz + 2%(4)	Code flash memory			33	mA
I_{DFREAD}(3)				Data flash memory			13	
I_{CFMOD}(3)	CC	Sum of the current consumption on $V_{DD\_HV\_A}$ (program/erase)	Program/Erase on-going while reading flash memory registers f_{CPU} = 120 MHz + 2% (4)	Code flash memory			52	mA
I_{DFMOD}(3)				Data flash memory			13	
I_{CFLPW}(3)	CC	Sum of the current consumption on $V_{DD\_HV\_A}$ during flash memory low power mode		Code flash memory			1.1	mA
I_{CFPWD}(3)	CC	Sum of the current consumption on $V_{DD\_HV\_A}$ during flash memory power down mode		Code flash memory			150	µA
I_{DFPWD}(3)				Data flash memory			150	

1. V_{DD} = 3.3 V ± 10 % / 5.0 V ± 10 %, T_A = –40 to 125 °C, unless otherwise specified.
2. All values need to be confirmed during device validation.
3. Data based on characterization results, not tested in production.
4. f_{CPU} 120 MHz + 2 % can be achieved over full temperature 125 °C ambient, 150 °C junction temperature.

3.10.3 Flash memory start-up/switch-off timings

Table 31. Start-up time/Switch-off time

Symbol		C	Parameter		Conditions (1)	Value			Unit
						Min	Typ	Max	
$T_{FLARSTEXIT}$	CC	D	Delay for flash memory module to exit reset mode	Code flash memory	—	—	—	125	µs
				Data flash memory		—	—		
$T_{FLALPEXIT}$	CC	T	Delay for flash memory module to exit low-power mode	Code flash memory	—	—	—	0.5	
$T_{FLAPDEXIT}$	CC	T	Delay for flash memory module to exit power-down mode	Code flash memory	—	—	—	30	
				Data flash memory		—	—		
$T_{FLALPENTRY}$	CC	T	Delay for flash memory module to enter low-power mode	Code flash memory	—	—	—	0.5	

1. V_{DD} = 3.3 V ± 10 % / 5.0 V ± 10 %, T_A = –40 to 125 °C, unless otherwise specified.

3.11 Electromagnetic compatibility (EMC) characteristics

Susceptibility tests are performed on a sample basis during product characterization.

3.11.1 Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user apply EMC software optimization and pre-qualification tests in relation with the EMC level requested for the application.

- Software recommendations – The software flowchart must include the management of runaway conditions such as:
  - Corrupted program counter
  - Unexpected reset
  - Critical data corruption (control registers)
- Pre-qualification trials – Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the reset pin or the oscillator pins for 1 second.

  To complete these trials, ESD stress can be applied directly on the device. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note *Software Techniques For Improving Microcontroller EMC Performance* (AN1015)).

Figure 14. Slow external crystal oscillator (32 kHz) electrical characteristics

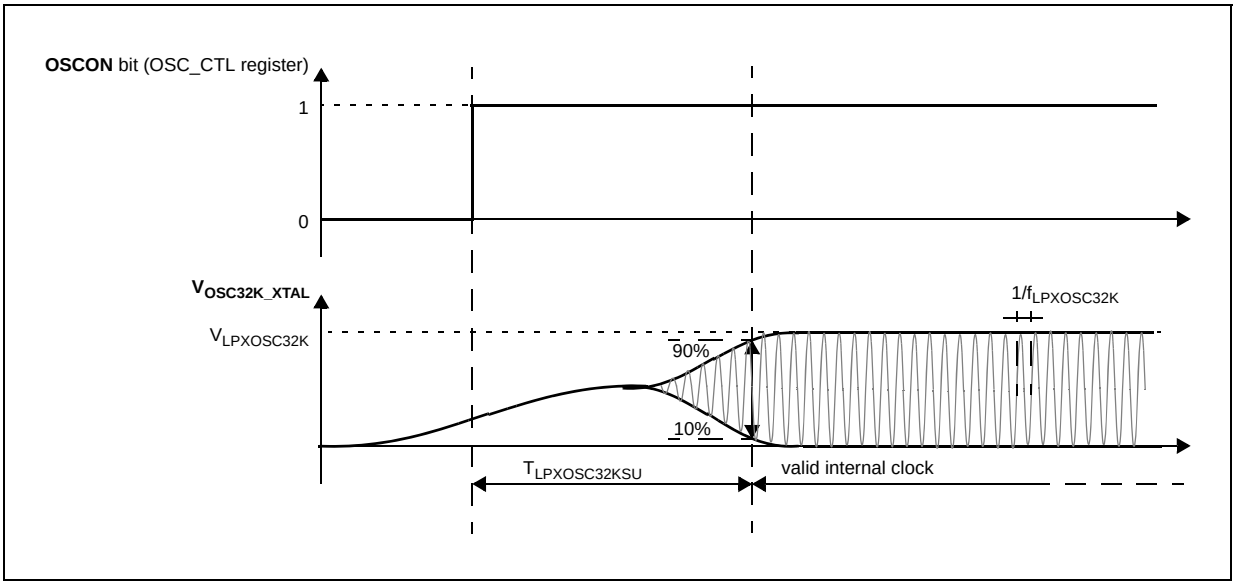


Table 38. Slow external crystal oscillator (32 kHz) electrical characteristics

Symbol		C	Parameter	Conditions[1]	Value[2]			Unit
					Min	Typ	Max	
f_{SXOSC}	SR	—	Slow external crystal oscillator frequency	—	32	32.768	40	kHz
g_{mSXOSC}	CC	—	Slow external crystal oscillator transconductance	V_{DD} = 3.3 V ± 10%,	13[3]	—	33[3]	µA/V
				V_{DD} = 5.0 V ± 10%	15[3]	—	35[3]	
V_{SXOSC}	CC	T	Oscillation amplitude	—	1.2	1.4	1.7	V
$I_{SXOSCBIAS}$	CC	T	Oscillation bias current	—	1.2	—	4.4	µA
I_{SXOSC}	CC	T	Slow external crystal oscillator consumption	—	—	—	7	µA
$T_{SXOSCSU}$	CC	T	Slow external crystal oscillator start-up time	—	—	—	2[4]	s

1. V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified.
2. All values need to be confirmed during device validation.
3. Based on ATE CZ
4. Start-up time has been measured with EPSON TOYOCOM MC306 crystal. Variation may be seen with other crystal.

3.14 FMPLL electrical characteristics

The device provides a frequency-modulated phase-locked loop (FMPLL) module to generate a fast system clock from the main oscillator driver.

Table 39. FMPLL electrical characteristics

Symbol		C	Parameter	Conditions[1]	Value[2]			Unit
					Min	Typ	Max	
f_{PLLIN}	SR	—	FMPLL reference clock[3]	—	4	—	64	MHz
Δ_{PLLIN}	SR	—	FMPLL reference clock duty cycle[3]	—	40	—	60	%
f_{PLLOUT}	CC	P	FMPLL output clock frequency	—	16	—	120	MHz
f_{CPU}	SR	—	System clock frequency	—	—	—	120 + 2%[4]	MHz
f_{FREE}	CC	P	Free-running frequency	—	20	—	150	MHz
t_{LOCK}	CC	P	FMPLL lock time	Stable oscillator (f_{PLLIN} = 16 MHz)		40	100	µs
Δt_{LTJIT}	CC	—	FMPLL long term jitter	f_{PLLIN} = 40 MHz (resonator), f_{PLLCLK} @ 120 MHz, 4000 cycles	—	—	6 (for < 1ppm)	ns
I_{PLL}	CC	C	FMPLL consumption	T_A = 25 °C	—	—	3	mA

1. V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified.
2. All values need to be confirmed during device validation.
3. PLLIN clock retrieved directly from 4-40 MHz XOSC or 16 MIRC. Input characteristics are granted when oscillator is used in functional mode. When bypass mode is used, oscillator input clock should verify f_{PLLIN} and Δ_{PLLIN}.
4. f_{CPU} 120 + 2% MHz can be achieved at 125 °C.

3.15 Fast internal RC oscillator (16 MHz) electrical characteristics

The device provides a 16 MHz main internal RC oscillator. This is used as the default clock at the power-up of the device and can also be used as input to PLL.

Table 40. Fast internal RC oscillator (16 MHz) electrical characteristics

Symbol		C	Parameter	Conditions[1]	Value[2]			Unit
					Min	Typ	Max	
f_{FIRC}	CC	P	Fast internal RC oscillator high frequency	T_A = 25 °C, trimmed	—	16	—	MHz
	SR	—		—	12		20	

Table 40. Fast internal RC oscillator (16 MHz) electrical characteristics (continued)

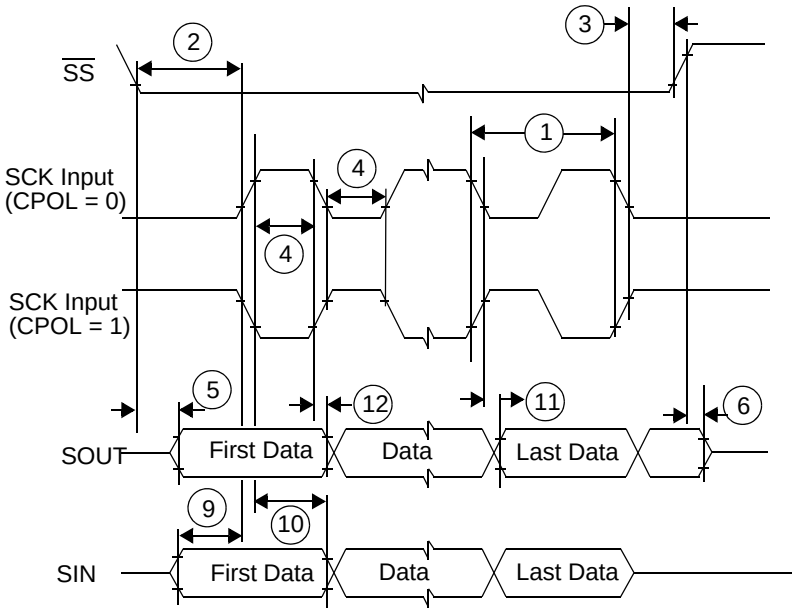
Symbol		C	Parameter	Conditions[1]		Value[2]			Unit
						Min	Typ	Max	
$I_{FIRCRUN}$[3]	CC	T	Fast internal RC oscillator high frequency current in running mode	T_A = 25 °C, trimmed		—	—	200	µA
$I_{FIRCPWD}$	CC	D	Fast internal RC oscillator high frequency current in power down mode	T_A = 25 °C		—	—	100	nA
		D		T_A = 55 °C		—	—	200	nA
		D		T_A = 125 °C		—	—	1	µA
$I_{FIRCSTOP}$	CC	T	Fast internal RC oscillator high frequency and system clock current in stop mode	T_A = 25 °C	sysclk = off	—	500	—	µA
					sysclk = 2 MHz	—	600	—	
					sysclk = 4 MHz	—	700	—	
					sysclk = 8 MHz	—	900	—	
					sysclk = 16 MHz	—	1250	—	
T_{FIRCSU}	CC	C	Fast internal RC oscillator start-up time	T_A = 55 °C	V_{DD} = 5.0 V ± 10%	—	—	2.0	µs
		—			V_{DD} = 3.3 V ± 10%	—	—	5	
		—		T_A = 125 °C	V_{DD} = 5.0 V ± 10%	—	—	2.0	
		—			V_{DD} = 3.3 V ± 10%	—	—	5	
$\Delta_{FIRCPRE}$	CC	C	Fast internal RC oscillator precision after software trimming of f_{FIRC}	T_A = 25 °C		–1	—	+1	%
$\Delta_{FIRCTRIM}$	CC	C	Fast internal RC oscillator trimming step	T_A = 25 °C		—	1.6		%
$\Delta_{FIRCVAR}$	CC	C	Fast internal RC oscillator variation over temperature and supply with respect to f_{FIRC} at T_A = 25 °C in high-frequency configuration	—		–5	—	+5	%

1. V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified.
2. All values need to be confirmed during device validation.
3. This does not include consumption linked to clock tree toggling and peripherals consumption when RC oscillator is ON.

Table 44. Conversion characteristics (12-bit ADC_1)

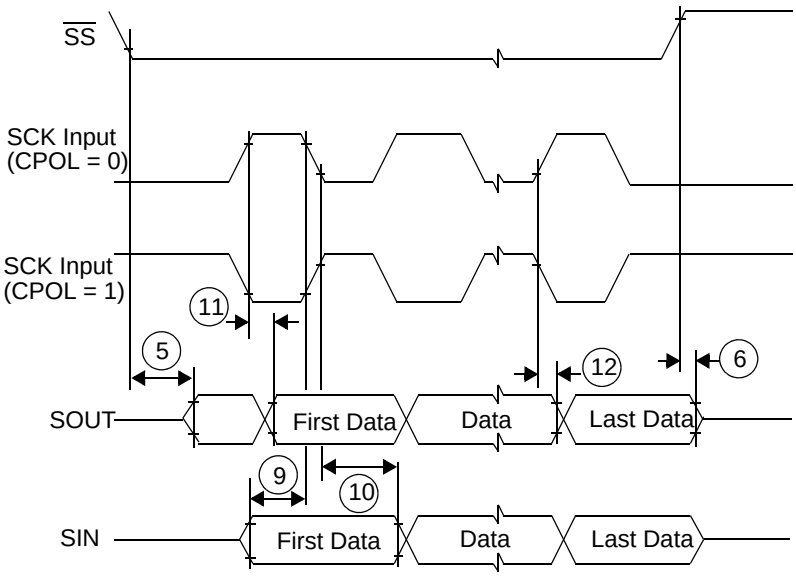
Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
V_{SS_ADC1}	SR	—	Voltage on VSS_HV_ADC1 (ADC_1 reference) pin with respect to ground (V_{SS_HV})[2]	—	–0.1		0.1	V
V_{DD_ADC1}	SR	—	Voltage on VDD_HV_ADC1 pin (ADC_1 reference) with respect to ground (V_{SS_HV})	—	$V_{DD\_HV\_A}$ – 0.1		$V_{DD\_HV\_A}$ + 0.1	V
V_{AINx}[3], [4]	SR	—	Analog input voltage[5]	—	V_{SS_ADC1} – 0.1		V_{DD_ADC1} + 0.1	V
f_{ADC1}	SR	—	ADC_1 analog frequency	—	8 + 2%		32 + 2%	MHz
t_{ADC1_PU}	SR	—	ADC_1 power up delay	—	1.5			µs
t_{ADC1_S}	CC	T	Sample time[6] VDD=5.0 V	—	440			ns
			Sample time[6] VDD=3.3 V	—	530			
t_{ADC1_C}	CC	P	Conversion time[7], [8] VDD=5.0 V	f_{ADC1} = 32 MHz	2			µs
			Conversion time[7], [6] VDD =5.0 V	$f_{ADC\ 1}$= 30 MHz	2.1			
			Conversion time[7], [6] VDD=3.3 V	$f_{ADC\ 1}$= 20 MHz	3			
			Conversion time[7], [6] VDD =3.3 V	f_{ADC1} = 15 MHz	3.01			
C_S	CC	D	ADC_1 input sampling capacitance	—	5			pF
C_{P1}	CC	D	ADC_1 input pin capacitance 1	—	3			pF
C_{P2}	CC	D	ADC_1 input pin capacitance 2	—	1			pF

Figure 27. DSPI classic SPI timing–slave, CPHA = 0



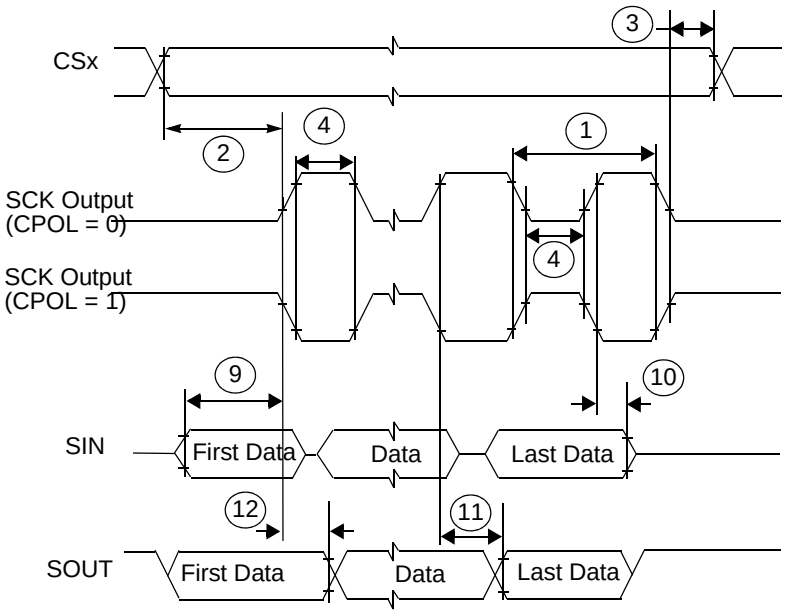
Note: Numbers shown reference *Table 50*.

Figure 28. DSPI classic SPI timing–slave, CPHA = 1



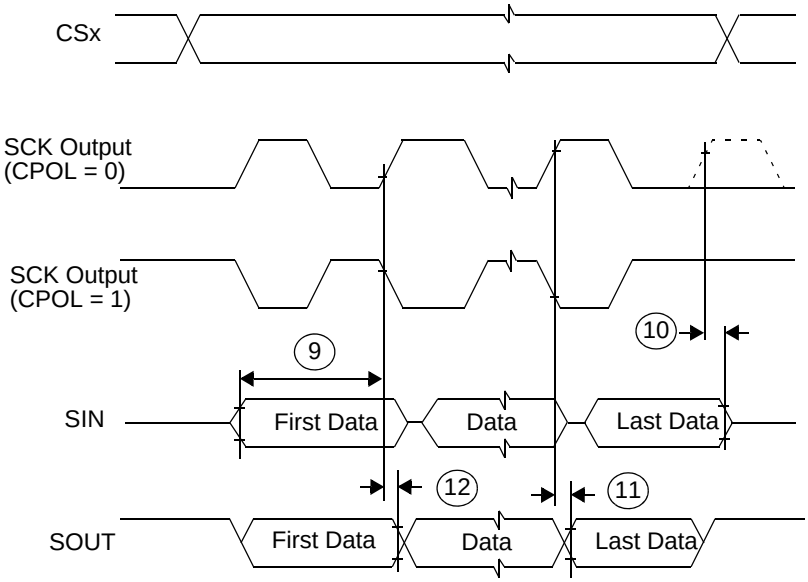
Note: Numbers shown reference *Table 50*.

Figure 29. DSPI modified transfer format timing–master, CPHA = 0



Note: Numbers shown reference *Table 50*.

Figure 30. DSPI modified transfer format timing–master, CPHA = 1



Note: Numbers shown reference *Table 50*.

Table 57. Revision history (continued)

Date	Revision	Changes
28-Apr-2011	3	– Replaced VIL min from –0.4 V to –0.3 V in the following tables: - I/O input DC electrical characteristics - Reset electrical characteristics - Fast external crystal oscillator (4 to 40 MHz) electrical characteristics – Updated Crystal oscillator and resonator connection scheme figure – Specified NPN transistor as the recommended BCP68 transistor throughout the document – Code and Data flash memory—Program and erase specifications tables: Renamed the parameter $t_{ESUS\ to}$ T_{eslat} – Revised the footnotes in the “Functional port pin descriptions” table. – In the “System pin descriptions” table, added a footnote to the A pads regarding not using IBE. For ports PB[12–15], changed ANX to ADC0_X. – Revised the presentation of the ADC functions on the following ports: PB[4–7] PD[0–11] – ADC conversion characteristics (10-bit ADC_0) table and Conversion characteristics (12-bit ADC_1) table- Updated footnote 5 and 7 respectively for the definition of the conversion time. – Data flash memory—Program and erase specifications: Updated $T_{wprogram}$ to 500 µs and $T_{16Kpperase}$ to 500 µs. Corrected Teslat classsification from “C” to “D”. – Code flash memory—Program and erase specifications: Corrected Teslat classification from “C” to “D”. – Flash Start-up time/Switch-off time: Changed $T_{FLARSTEXIT}$ classification from “C” to “D”. – Functional port pin description: Added a footnote at the PB [9] port pin. – Absolute maximum ratings table: Added footnote 1. – Low voltage power domain electrical characteristics table: Updated IDDHALT, IDDSTOP, IDDSTBY3, IDDSTDBY2, IDDSTDBY1. – Updated commercial product code structure. – Slow external crystal oscillator (32 kHz) electrical characteristics table: Updated g_{mSXOSC}, V_{SXOSC}, $I_{SXOSCBIAS}$ and I_{SXOSC}. – FMPLL electrical characteristics table: Updated Δt_{LTJIT}. – Fast internal RC oscillator (16 MHz) electrical characteristics table: Updated TFIRCSU and IFIRCPWD. – MII serial management channel timing table: Updated M12 – JTAG characteristics table: Updated t_{TDOV}. – Low voltage monitor electrical characteristics table: Updated VLVDHV3H, VLVDHV3L, VLVDHV5H, VLVDHV5L. – DSPI electricals table: Updated spec 1, 5, 6. Updated footnote 2 and 3. Added Δt_{CSC}, Δt_{ASC}, t_{SUSS}, t_{HSS}. – IO consumption table: Updated all parameter values. – DSPI electricals: Updated Δt_{CSC} max to 115 ns. – Low voltage power domain electrical characteristics table: Added footnote 9. – ADC electrical characteristics: Added 2 notes above 10-bit and 12-bit conversion tables.