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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z4d
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, LINbus, SPI, UART/USART
Peripherals	DMA, POR, PWM, WDT
Number of I/O	177
Program Memory Size	1.5MB (1.5M x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 33x10b, 10x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	208-LQFP
Supplier Device Package	208-LQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/spc564b64l8c9e0x

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Table 5. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET config.	Pin number		
								LQFP 176	LQFP 208	LBGA256
PA[5]	PCR[5]	AF0 AF1 AF2	GPIO[5] E0UC[5] LIN4TX	SIUL eMIOS_0 LINFlexD_4	I/O I/O O	M/S	Tristate	146	170	C10
PA[6]	PCR[6]	AF0 AF1 AF2 AF3 — —	GPIO[6] E0UC[6] — CS1_1 LIN4RX EIRQ[1]	SIUL eMIOS_0 — DSPI_1 LINFlexD_4 SIUL	I/O I/O — O I I	S	Tristate	147	171	D11
PA[7]	PCR[7]	AF0 AF1 AF2 AF3 — — —	GPIO[7] E0UC[7] LIN3TX — RXD[2] EIRQ[2] ADC1_S[1]	SIUL eMIOS_0 LINFlexD_3 — FEC SIUL ADC_1	I/O I/O O — I I I	M/S	Tristate	128	152	C15
PA[8]	PCR[8]	AF0 AF1 AF2 AF3 — — — —	GPIO[8] E0UC[8] E0UC[14] — RXD[1] EIRQ[3] ABS[0] LIN3RX	SIUL eMIOS_0 eMIOS_0 — FEC SIUL MC_RGM LINFlexD_3	I/O I/O I/O — I I I I	M/S	Input, weak pull-up	129	153	B16
PA[9]	PCR[9]	AF0 AF1 AF2 AF3 — —	GPIO[9] E0UC[9] — CS2_1 RXD[0] FAB	SIUL eMIOS_0 — DSPI1 FEC MC_RGM	I/O I/O — O I I	M/S	Pull-down	130	154	B15

Table 5. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET config.	Pin number		
								LQFP 176	LQFP 208	LBGA256
PA[10]	PCR[10]	AF0 AF1 AF2 AF3 — — —	GPIO[10] E0UC[10] SDA LIN2TX COL ADC1_S[2] SIN_1	SIUL eMIOS_0 I^2C LINFlexD_2 FEC ADC_1 DSPI_1	I/O I/O I/O O I I I	M/S	Tristate	131	155	A15
PA[11]	PCR[11]	AF0 AF1 AF2 AF3 — — — —	GPIO[11] E0UC[11] SCL — RX_ER EIRQ[16] LIN2RX ADC1_S[3]	SIUL eMIOS_0 I^2C — FEC SIUL LINFlexD_2 ADC_1	I/O I/O I/O — I I I I	M/S	Tristate	132	156	B14
PA[12]	PCR[12]	AF0 AF1 AF2 AF3 — —	GPIO[12] — E0UC[28] CS3_1 EIRQ[17] SIN_0	SIUL — eMIOS_0 DSPI1 SIUL DSPI_0	I/O — I/O O I I	S	Tristate	53	69	P6
PA[13]	PCR[13]	AF0 AF1 AF2 AF3	GPIO[13] SOUT_0 E0UC[29] —	SIUL DSPI_0 eMIOS_0 —	I/O O I/O —	M/S	Tristate	52	66	R5
PA[14]	PCR[14]	AF0 AF1 AF2 AF3 —	GPIO[14] SCK_0 CS0_0 E0UC[0] EIRQ[4]	SIUL DSPI_0 DSPI_0 eMIOS_0 SIUL	I/O I/O I/O I/O I	M/S	Tristate	50	58	P4
PA[15]	PCR[15]	AF0 AF1 AF2 AF3 —	GPIO[15] CS0_0 SCK_0 E0UC[1] WKPU[10]	SIUL DSPI_0 DSPI_0 eMIOS_0 WKPU	I/O I/O I/O I/O I	M/S	Tristate	48	56	R2

Table 5. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET config.	Pin number		
								LQFP 176	LQFP 208	LBGA256
PD[3]	PCR[51]	AF0 AF1 AF2 AF3 — —	GPI[51] — — — ADC0_P[7] ADC1_P[7]	SIUL — — — ADC_0 ADC_1	I — — — I I	I	Tristate	80	96	R13
PD[4]	PCR[52]	AF0 AF1 AF2 AF3 — —	GPI[52] — — — ADC0_P[8] ADC1_P[8]	SIUL — — — ADC_0 ADC_1	I — — — I I	I	Tristate	81	97	P12
PD[5]	PCR[53]	AF0 AF1 AF2 AF3 — —	GPI[53] — — — ADC0_P[9] ADC1_P[9]	SIUL — — — ADC_0 ADC_1	I — — — I I	I	Tristate	82	98	T14
PD[6]	PCR[54]	AF0 AF1 AF2 AF3 — —	GPI[54] — — — ADC0_P[10] ADC1_P[10]	SIUL — — — ADC_0 ADC_1	I — — — I I	I	Tristate	83	99	R14
PD[7]	PCR[55]	AF0 AF1 AF2 AF3 — —	GPI[55] — — — ADC0_P[11] ADC1_P[11]	SIUL — — — ADC_0 ADC_1	I — — — I I	I	Tristate	84	100	P13
PD[8]	PCR[56]	AF0 AF1 AF2 AF3 — —	GPI[56] — — — ADC0_P[12] ADC1_P[12]	SIUL — — — ADC_0 ADC_1	I — — — I I	I	Tristate	87	103	P14

8. Guaranteed by device validation.

Note: SRAM retention guaranteed to LVD levels.

3.5 Thermal characteristics

3.5.1 Package thermal characteristics

Table 12. LQFP thermal characteristics(1)

Symbol		C	Parameter	Conditions(2)	Pin count	Value(3)			Unit
						Min	Typ	Max	
$R_{\theta JA}$	CC	D	Thermal resistance, junction-to-ambient natural convection	Single-layer board—1s	176	—	—	44.4(4)	°C/W
					208	—	—	43	°C/W
$R_{\theta JA}$	CC	D	Thermal resistance, junction-to-ambient natural convection	Four-layer board—2s2p(5)	176	—	—	36.1	°C/W
					208	—	—	33.9	°C/W

1. Thermal characteristics are targets based on simulation that are subject to change per device characterization.
2. V_{DD} = 3.3 V ± 10 % / 5.0 V ± 10 %, T_A = –40 to 125 °C.
3. All values need to be confirmed during device validation.
4. 1s board as per standard JEDEC (JESD51-7) in natural convection.
5. 2s2p board as per standard JEDEC (JESD51-7) in natural convection.

Table 13. LBGA256 thermal characteristics(1)

Symbol		C	Parameter	Conditions	Value	Unit
$R_{\theta JA}$	CC	—	Thermal resistance, junction-to-ambient natural convection	Single-layer board—1s	44.3	°C/W
				Four-layer board—2s2p	31	

1. Thermal characteristics are targets based on simulation that are subject to change per device characterization.

Medium and fast pads can use slow configuration to reduce electromagnetic emission, at the cost of reducing AC performance.

3.6.2 I/O input DC characteristics

Table 14 provides input DC electrical characteristics as described in *Figure 5*.

Figure 5. I/O input DC electrical characteristics definition

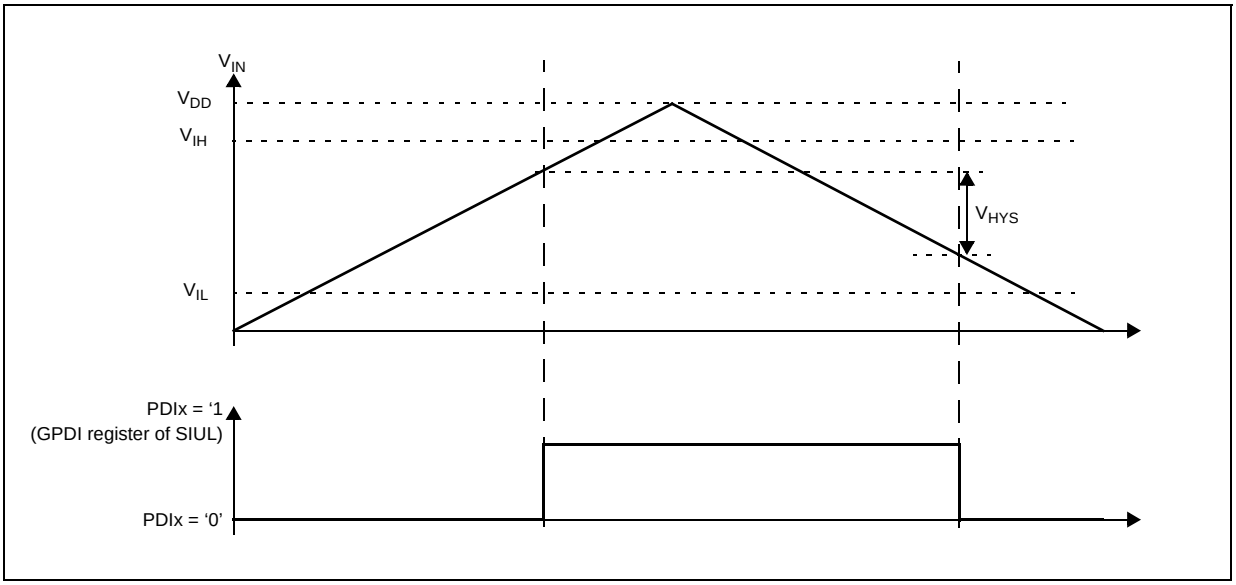


Table 14. I/O input DC electrical characteristics

Symbol		C	Parameter	Conditions[1]		Value[2] Min	Value[2] Typ	Value[2] Max	Unit
V_{IH}	SR	P	Input high level CMOS (Schmitt Trigger)	—		0.65 V_{DD}	—	V_{DD} + 0.4	V
V_{IL}	SR	P	Input low level CMOS (Schmitt Trigger)	—		–0.3	—	0.35V_{DD}	
V_{HYS}	CC	C	Input hysteresis CMOS (Schmitt Trigger)	—		0.1V_{DD}	—	—	
I_{LKG}	CC	P	Digital input leakage	No injection on adjacent pin	T_A = –40 °C	—	2	—	nA
		P			T_A = 25 °C	—	2	—	
		D			T_A = 105 °C	—	12	500	
		P			T_A = 125 °C	—	70	1000	
W_{FI}	SR	P	Width of input pulse rejected by analog filter[3]	—		—	—	40[4]	ns
W_{NFI}	SR	P	Width of input pulse accepted by analog filter[3]	—		1000[4]	—	—	ns

1. V_{DD} = 3.3 V ± 10 % / 5.0 V ± 10 %, T_A = –40 to 125 °C, unless otherwise specified.
2. V_{DD} as mentioned in the table is $V_{DD\_HV\_A}$/$V_{DD\_HV\_B}$. All values need to be confirmed during device validation.
3. Analog filters are available on all wakeup lines.

Table 16. SLOW configuration output buffer electrical characteristics (continued)

Symbol		C	Parameter	Conditions[1],[2]		Value			Unit
						Min	Typ	Max	
V_{OL}	CC	P	Output low level SLOW configuration	Push Pull	I_{OL} = 3 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	$0.1V_{DD}$	V
		C			I_{OL} = 3 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 1[3]	—	—	$0.1V_{DD}$	
		P			I_{OL} = 1.5 mA, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	0.5	

1. V_{DD} = 3.3 V ± 10 % / 5.0 V ± 10 %, T_A = –40 to 125 °C, unless otherwise specified.
2. V_{DD} as mentioned in the table is $V_{DD\_HV\_A}$/$V_{DD\_HV\_B}$.
3. The configuration PAD3V5 = 1 when V_{DD} = 5 V is only a transient configuration during power-up. All pads but RESET and Nexus output (MDOx, EVTO, MCKO) are configured in input or in high impedance state.

Table 17. MEDIUM configuration output buffer electrical characteristics

Symbol		C	Parameter	Conditions[1],[2]		Value			Unit
						Min	Typ	Max	
V_{OH}	CC	C	Output high level MEDIUM configuration	Push Pull	I_{OH} = –3 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	$0.8V_{DD}$	—	—	V
		C			I_{OH} = –1.5 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 1[3]	$0.8V_{DD}$	—	—	
		C			I_{OH} = –2 mA, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	V_{DD} – 0.8	—	—	
V_{OL}	CC	C	Output low level MEDIUM configuration	Push Pull	I_{OL} = 3 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	$0.2V_{DD}$	V
		C			I_{OL} = 1.5 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 1[3]	—	—	$0.1V_{DD}$	
		C			I_{OL} = 2 mA, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	0.5	

1. V_{DD} = 3.3 V ± 10 % / 5.0 V ± 10 %, T_A = –40 to 125 °C, unless otherwise specified.
2. V_{DD} as mentioned in the table is $V_{DD\_HV\_A}$/$V_{DD\_HV\_B}$.
3. The configuration PAD3V5 = 1 when V_{DD} = 5 V is only a transient configuration during power-up. All pads but RESET and Nexus output (MDOx, EVTO, MCKO) are configured in input or in high impedance state.

Figure 9. Low voltage monitor vs. Reset

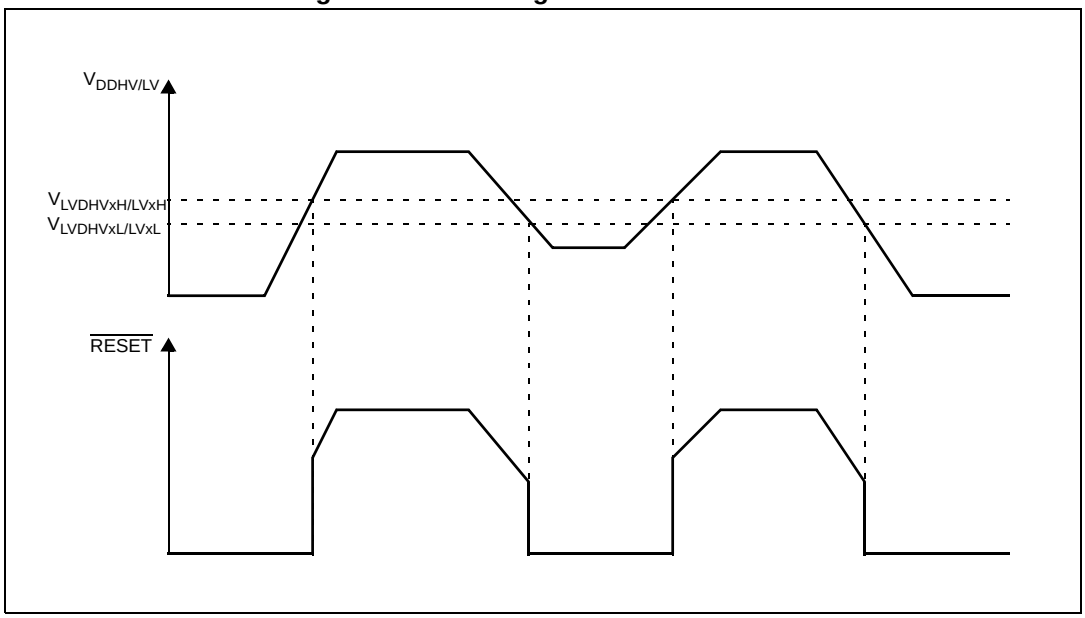


Table 24. Low voltage monitor electrical characteristics

Symbol		C	Parameter	Conditions[1]	Value[2]			Unit
					Min	Typ	Max	
V_{PORUP}	SR	P	Supply for functional POR module	—	1.0	—	5.5	V
V_{PORH}	CC	P	Power-on reset threshold	—	1.5	—	2.6	
$V_{LVDHV3H}$	CC	T	LVDHV3 low voltage detector high threshold	—	2.7	—	2.85	
$V_{LVDHV3L}$	CC	T	LVDHV3 low voltage detector low threshold	—	2.6	—	2.74	
$V_{LVDHV5H}$	CC	T	LVDHV5 low voltage detector high threshold	—	4.3	—	4.5	
$V_{LVDHV5L}$	CC	T	LVDHV5 low voltage detector low threshold	—	4.2	—	4.4	
$V_{LVDLVCORL}$	CC	P	LVDLVCOR low voltage detector low threshold	T_A = 25 °C, after trimming	1.08	—	1.17	
$V_{LVDLVBKPL}$	CC	P	LVDLVBKP low voltage detector low threshold		1.08	—	1.17	

1. V_{DD} = 3.3 V ± 10 % / 5.0 V ± 10 %, T_A = –40 to 125 °C, unless otherwise specified.
2. All values need to be confirmed during device validation.

3.9 Low voltage domain power consumption

Table 25 provides DC electrical characteristics for significant application modes. These values are indicative values; actual consumption depends on the application.

Table 25. Low voltage power domain electrical characteristics(1)

Symbol		C	Parameter	Conditions(2)		Value			Unit
						Min	Typ(3)	Max(4)	
I_{DDMAX}(5)	CC	D	RUN mode maximum average current	—		—	210	300(6), (7)	mA
I_{DDRUN}	CC	P	RUN mode typical average current(8)	at 120 MHz	T_A = 25 °C	—	150	208(9)	mA
		D		at 80 MHz	T_A = 25 °C	—	110(8)	150(10)	mA
		C		at 120 MHz	T_A = 125 °C	—	180	280	mA
I_{DDHALT}	CC	P	HALT mode current(11)	at 120 MHz	T_A = 25 °C	—	20	27	mA
		C		at 120 MHz	T_A = 125 °C	—	35	100	mA
I_{DDSTOP}	CC	P	STOP mode current(12)	No clocks active	T_A = 25 °C	—	0.4	5	mA
		C			T_A = 125 °C	—	16	72	mA
$I_{DDSTDBY3}$ (96 KB RAM retained)	CC	P	STANDBY3 mode current(13)	No clocks active	T_A = 25 °C	—	50	96	µA
		C			T_A = 125 °C	—	630	2400	µA
$I_{DDSTDBY2}$ (64 KB RAM retained)	CC	C	STANDBY2 mode current(14)	No clocks active	T_A = 25 °C	—	40	92	µA
		C			T_A = 125 °C	—	500	2000	µA
$I_{DDSTDBY1}$ (8 KB RAM retained)	CC	C	STANDBY1 mode current(15)	No clocks active	T_A = 25 °C	—	25	85	µA
		C			T_A = 125 °C	—	230	1100	µA
Adders in LP mode	CC	T	32 KHz OSC	—	T_A = 25 °C	—	—	5	µA
			4–40 MHz OSC	—	T_A = 25 °C	—	—	3	mA
			16 MHz IRC	—	T_A = 25 °C	—	—	500	µA
			128 KHz IRC	—	T_A = 25 °C	—	—	5	µA

1. Except for I_{DDMAX}, all the current values are total current drawn from $V_{DD\_HV\_A}$.
2. V_{DD} = 3.3 V ± 10 % / 5.0 V ± 10 %, T_A = –40 to 125 °C, unless otherwise specified All temperatures are based on an ambient temperature.
3. Target typical current consumption for the following typical operating conditions and configuration. Process = typical, Voltage = 1.2 V.
4. Target maximum current consumption for mode observed under typical operating conditions. Process = Fast, Voltage = 1.32 V.
5. Running consumption is given on voltage regulator supply (V_{DDREG}). It does not include consumption linked to I/Os toggling. This value is highly dependent on the application. The given value is thought to be a worst case value with all cores and peripherals running, and code fetched from code flash while modify operation on-going on data flash. It is to be noticed that this value can be significantly reduced by application: switch-off not used peripherals (default), reduce peripheral frequency through internal prescaler, fetch from RAM most used functions, use low power mode when possible.
6. Higher current may sunk by device during power-up and standby exit. Please refer to in rush current in *Table 23*.
7. Maximum “allowed” current is package dependent.
8. Only for the “P” classification: Code fetched from RAM: Serial IPs CAN and LIN in loop back mode, DSPI as Master, PLL as system Clock (4 x Multiplier) peripherals on (eMIOS/CTU/ADC) and running at max frequency, periodic SW/WDG timer reset enabled. RUN current measured with typical application with accesses on both code flash and RAM.

9. Subject to change, Configuration: 1 × e200z4d + 4 kbit/s Cache, 1 × e200z0h (1/2 system frequency), CSE, 1 × eDMA (10 ch.), 6 × FlexCAN (4 × 500 kbit/s, 2 × 125 kbit/s), 4 × LINFlexD (20 kbit/s), 6 × DSPI (2 × 2 Mbit/s, 3 × 4 Mbit/s, 1 × 10 Mbit/s), 16 × Timed I/O, 16 × ADC Input, 1 × FlexRay (2 ch., 10 Mbit/s), 1 × FEC (100 Mbit/s), 1 × RTC, 4 PIT channels, 1 × SWT, 1 × STM. For lower pin count packages reduce the amount of timed I/O's and ADC channels. RUN current measured with typical application with accesses on both code flash and RAM.
10. This value is obtained from limited sample set.
11. Data Flash Power Down. Code Flash in Low Power. SIRC 128 kHz and FIRC 16 MHz ON. 16 MHz XTAL clock. FlexCAN: instances: 0, 1, 2 ON (clocked but no reception or transmission), instances: 4, 5, 6 clocks gated. LINFlex: instances: 0, 1, 2 ON (clocked but no reception or transmission), instance: 3-9 clocks gated. eMIOS: instance: 0 ON (16 channels on PA[0]-PA[11] and PC[12]-PC[15]) with PWM 20 kHz, instance: 1 clock gated. DSPI: instance: 0 (clocked but no communication, instance: 1-7 clocks gated). RTC/API ON. PIT ON. STM ON. ADC ON but no conversion except 2 analog watchdogs.
12. Only for the "P" classification: No clock, FIRC 16 MHz OFF, SIRC128 kHz ON, PLL OFF, HPvreg OFF, LPVreg ON. All possible peripherals off and clock gated. Flash in power down mode.
13. Only for the "P" classification: LPreg ON, HPVreg OFF, 96 KB RAM ON, device configured for minimum consumption, all possible modules switched-off. Measurement condition assumes T_j = Ta.
14. LPreg ON, HPVreg OFF, 64 KB RAM ON, device configured for minimum consumption, all possible modules switched-off. Measurement condition assumes T_j = Ta.
15. LPreg ON, HPVreg OFF, 8 KB RAM ON, device configured for minimum consumption, all possible modules switched OFF. Measurement condition assumes T_j = Ta.

3.10 Flash memory electrical characteristics

3.10.1 Program/Erase characteristics

Table 26 shows the code flash memory program and erase characteristics.

Table 26. Code flash memory—Program and erase specifications

Symbol		C	Parameter	Value				Unit
				Min	Typ(1)	Initial max(2)	Max(3)	
$T_{dwprogram}$	CC	C	Double word (64 bits) program time(4)	—	18	50	500	µs
$T_{16Kpperase}$			16 KB block pre-program and erase time	—	200	500	5000	ms
$T_{32Kpperase}$			32 KB block pre-program and erase time	—	300	600	5000	ms
$T_{128Kpperase}$			128 KB block pre-program and erase time	—	600	1300	5000	ms
T_{eslat}		D	Erase Suspend Latency	—	—	30	30	µs
t_{ESRT}(5)		C	Erase Suspend Request Rate	20	—	—	—	ms
t_{PABT}		D	Program Abort Latency	—	—	10	10	µs
t_{EAPT}		D	Erase Abort Latency	—	—	30	30	µs

1. Typical program and erase times assume nominal supply values and operation at 25 °C. All times are subject to change pending device characterization.
2. Initial factory condition: < 100 program/erase cycles, 25 °C, typical supply voltage.
3. The maximum program and erase times occur after the specified number of program/erase cycles. These maximum values are characterized but not guaranteed.
4. Actual hardware programming times. This does not include software overhead.
5. It is Time between erase suspend resume and the next erase suspend request.

Table 27 shows the data flash memory program and erase characteristics.

3.10.3 Flash memory start-up/switch-off timings

Table 31. Start-up time/Switch-off time

Symbol		C	Parameter		Conditions (1)	Value			Unit
						Min	Typ	Max	
$T_{FLARSTEXIT}$	CC	D	Delay for flash memory module to exit reset mode	Code flash memory	—	—	—	125	µs
				Data flash memory		—	—		
$T_{FLALPEXIT}$	CC	T	Delay for flash memory module to exit low-power mode	Code flash memory	—	—	—	0.5	
$T_{FLAPDEXIT}$	CC	T	Delay for flash memory module to exit power-down mode	Code flash memory	—	—	—	30	
				Data flash memory		—	—		
$T_{FLALPENTRY}$	CC	T	Delay for flash memory module to enter low-power mode	Code flash memory	—	—	—	0.5	

1. V_{DD} = 3.3 V ± 10 % / 5.0 V ± 10 %, T_A = –40 to 125 °C, unless otherwise specified.

3.11 Electromagnetic compatibility (EMC) characteristics

Susceptibility tests are performed on a sample basis during product characterization.

3.11.1 Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user apply EMC software optimization and pre-qualification tests in relation with the EMC level requested for the application.

- Software recommendations – The software flowchart must include the management of runaway conditions such as:
  - Corrupted program counter
  - Unexpected reset
  - Critical data corruption (control registers)
- Pre-qualification trials – Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the reset pin or the oscillator pins for 1 second.

  To complete these trials, ESD stress can be applied directly on the device. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note *Software Techniques For Improving Microcontroller EMC Performance* (AN1015)).

Figure 14. Slow external crystal oscillator (32 kHz) electrical characteristics

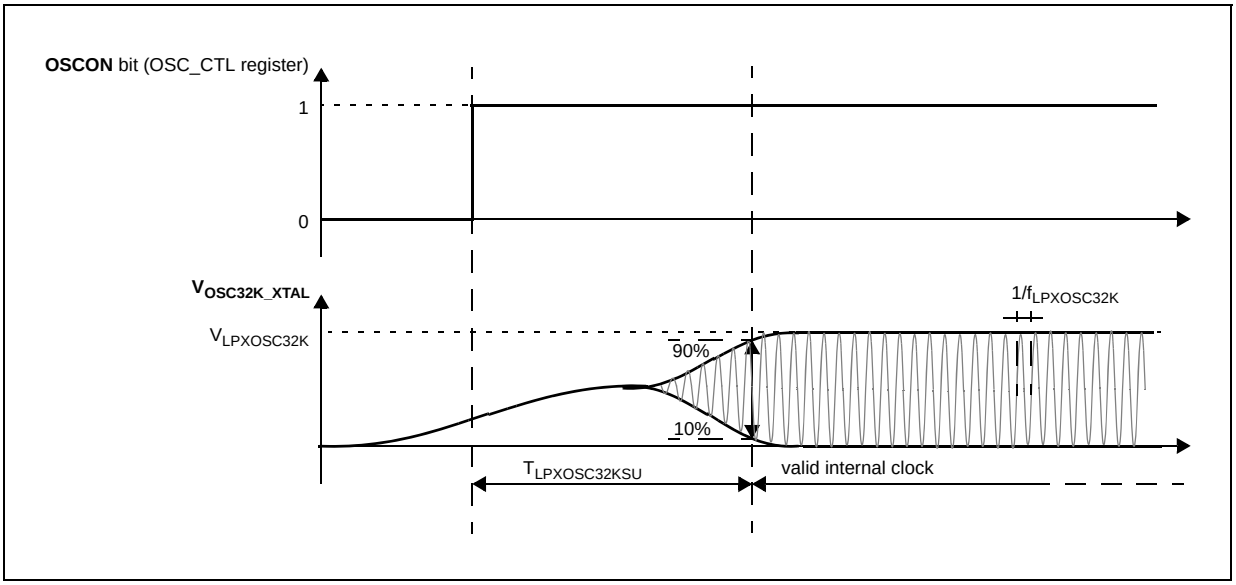
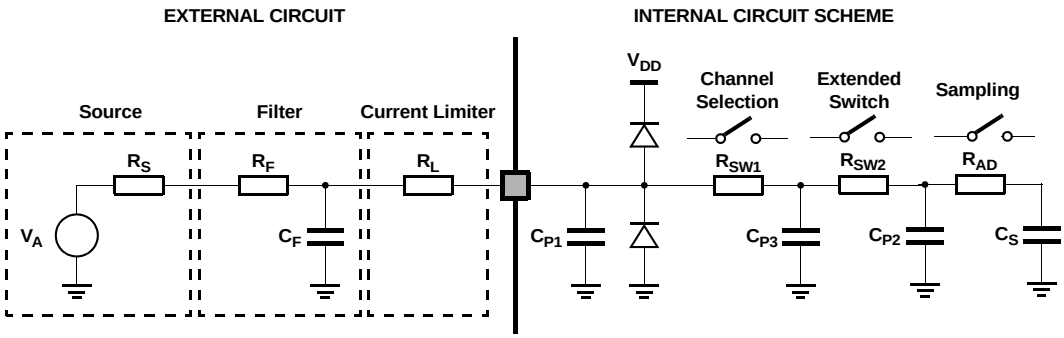


Table 38. Slow external crystal oscillator (32 kHz) electrical characteristics

Symbol		C	Parameter	Conditions[1]	Value[2]			Unit
					Min	Typ	Max	
f_{SXOSC}	SR	—	Slow external crystal oscillator frequency	—	32	32.768	40	kHz
g_{mSXOSC}	CC	—	Slow external crystal oscillator transconductance	V_{DD} = 3.3 V ± 10%,	13[3]	—	33[3]	µA/V
				V_{DD} = 5.0 V ± 10%	15[3]	—	35[3]	
V_{SXOSC}	CC	T	Oscillation amplitude	—	1.2	1.4	1.7	V
$I_{SXOSCBIAS}$	CC	T	Oscillation bias current	—	1.2	—	4.4	µA
I_{SXOSC}	CC	T	Slow external crystal oscillator consumption	—	—	—	7	µA
$T_{SXOSCSU}$	CC	T	Slow external crystal oscillator start-up time	—	—	—	2[4]	s

1. V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified.
2. All values need to be confirmed during device validation.
3. Based on ATE CZ
4. Start-up time has been measured with EPSON TOYOCOM MC306 crystal. Variation may be seen with other crystal.

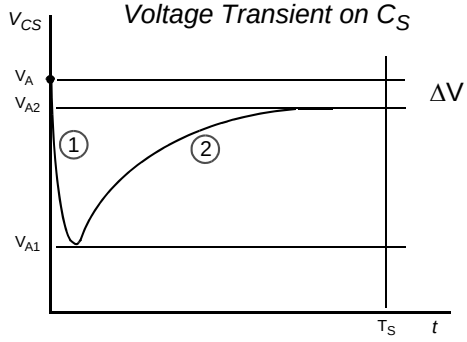
Figure 17. Input equivalent circuit (extended channels)



R_S Source Impedance
R_F Filter Resistance
C_F Filter Capacitance
R_L Current Limiter Resistance
R_{SW} Channel Selection Switch Impedance (two contributions R_{SW1} and R_{SW2})
R_{AD}Sampling Switch Impedance
C_P Pin Capacitance (three contributions, C_{P1}, C_{P2} and C_{P3})
C_S Sampling Capacitance

A second aspect involving the capacitance network shall be considered. Assuming the three capacitances C_F, C_{P1} and C_{P2} initially charged at the source voltage V_A (refer to the equivalent circuit reported in *Figure 16*): when the sampling phase is started (A/D switch close), a charge sharing phenomena is installed.

Figure 18. Transient behavior during sampling phase



$\Delta V < 0.5$ LSB

$\tau_1 < (R_{SW} + R_{AD})\, C_S << T_S$

$\tau_2 = R_L\,(C_S + C_{P1} + C_{P2})$

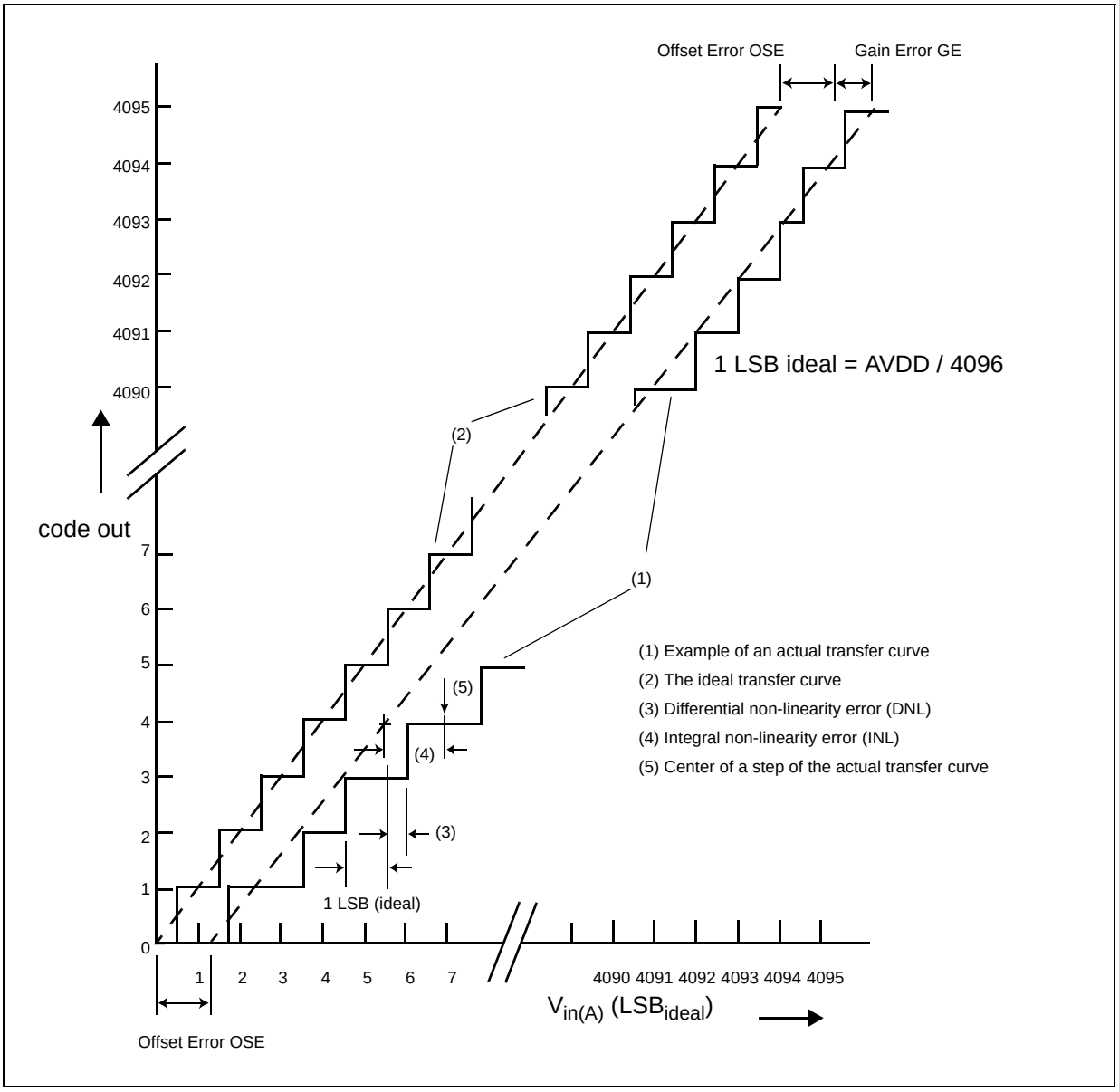
In particular two different transient periods can be distinguished:

- A first and quick charge transfer from the internal capacitance C_{P1} and C_{P2} to the sampling capacitance C_S occurs (C_S is supposed initially completely discharged): considering a worst case (since the time constant in reality would be faster) in which C_{P2} is reported in parallel to C_{P1} (call $C_P = C_{P1} + C_{P2}$), the two capacitances C_P and C_S are in series, and the time constant is

Equation 5

$$\tau_1 = (R_{SW} + R_{AD}) \bullet \frac{C_P \bullet C_S}{C_P + C_S}$$

Figure 20. ADC_1 characteristic and error definitions



3. PA3, PA7, PA10, PA11 and PE12 ADC_1 channels are coming from $V_{DD\_HV\_B}$ domain hence VDD_HV_ADC1 should be within ±100 mV of VDD_HV_B when these channels are used for ADC_1.
4. VDD_HV_ADC1 can operate at 5V condition while $V_{DD\_HV\_B}$ can operate at 3.3V provided that ADC_1 channels coming from $V_{DD\_HV\_B}$ domain are limited in max swing as $V_{DD\_HV\_B}$.
5. V_{AINx} may exceed V_{SS_ADC1} and V_{DD_ADC1} limits, remaining on absolute maximum ratings, but the results of the conversion will be clamped respectively to 0x000 or 0xFFF.
6. During the sample time the input capacitance C_S can be charged/discharged by the external source. The internal resistance of the analog source must allow the capacitance to reach its final voltage level within t_{ADC1_S}. After the end of the sample time t_{ADC1_S}, changes of the analog input voltage have no effect on the conversion result. Values for the sample clock t_{ADC1_S} depend on programming.
7. Conversion time = Bit evaluation time + Sampling time + 1 Clock cycle delay.
8. Refer to ADC conversion table for detailed calculations.
9. Total Unadjusted Error: The maximum error that occurs without adjusting Offset and Gain errors. This error is a combination of Offset, Gain and Integral Linearity errors.

3.18 Fast Ethernet Controller

MII signals use CMOS signal levels compatible with devices operating at 3.3 V. Signals are not TTL compatible. They follow the CMOS electrical characteristics.

3.18.1 MII Receive Signal Timing (RXD[3:0], RX_DV, RX_ER, and RX_CLK)

The receiver functions correctly up to a RX_CLK maximum frequency of 25 MHz +1%. There is no minimum frequency requirement. In addition, the system clock frequency must exceed four times the RX_CLK frequency in 2:1 mode and two times the RX_CLK frequency in 1:1 mode.

Table 45. MII Receive Signal Timing

Spec	Characteristic	Min	Max	Unit
M1	RXD[3:0], RX_DV, RX_ER to RX_CLK setup	5	—	ns
M2	RX_CLK to RXD[3:0], RX_DV, RX_ER hold	5	—	ns
M3	RX_CLK pulse width high	35%	65%	RX_CLK period
M4	RX_CLK pulse width low	35%	65%	RX_CLK period

Figure 21. MII receive signal timing diagram

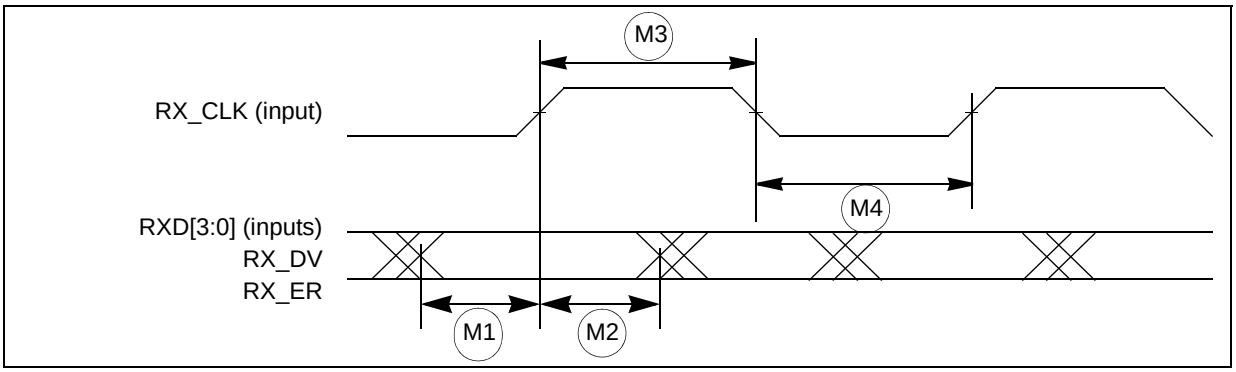
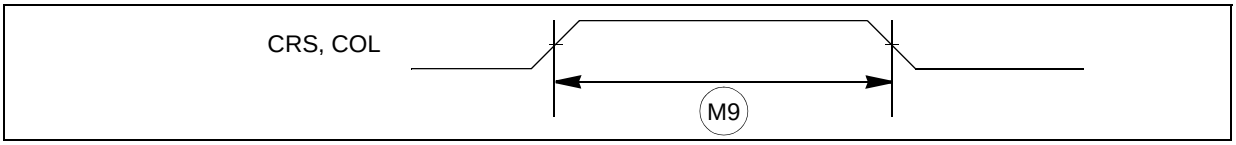


Figure 23. MII async inputs timing diagram



3.18.4 MII Serial Management Channel Timing (MDIO and MDC)

The FEC functions correctly with a maximum MDC frequency of 2.5 MHz.

Table 48. MII serial management channel timing(1)

Spec	Characteristic	Min	Max	Unit
M10	MDC falling edge to MDIO output invalid (minimum propagation delay)	0	—	ns
M11	MDC falling edge to MDIO output valid (max prop delay)	—	25	ns
M12	MDIO (input) to MDC rising edge setup	28	—	ns
M13	MDIO (input) to MDC rising edge hold	0	—	ns
M14	MDC pulse width high	40%	60%	MDC period
M15	MDC pulse width low	40%	60%	MDC period

1. Output pads configured with SRE = 0b11.

Figure 24. MII serial management channel timing diagram

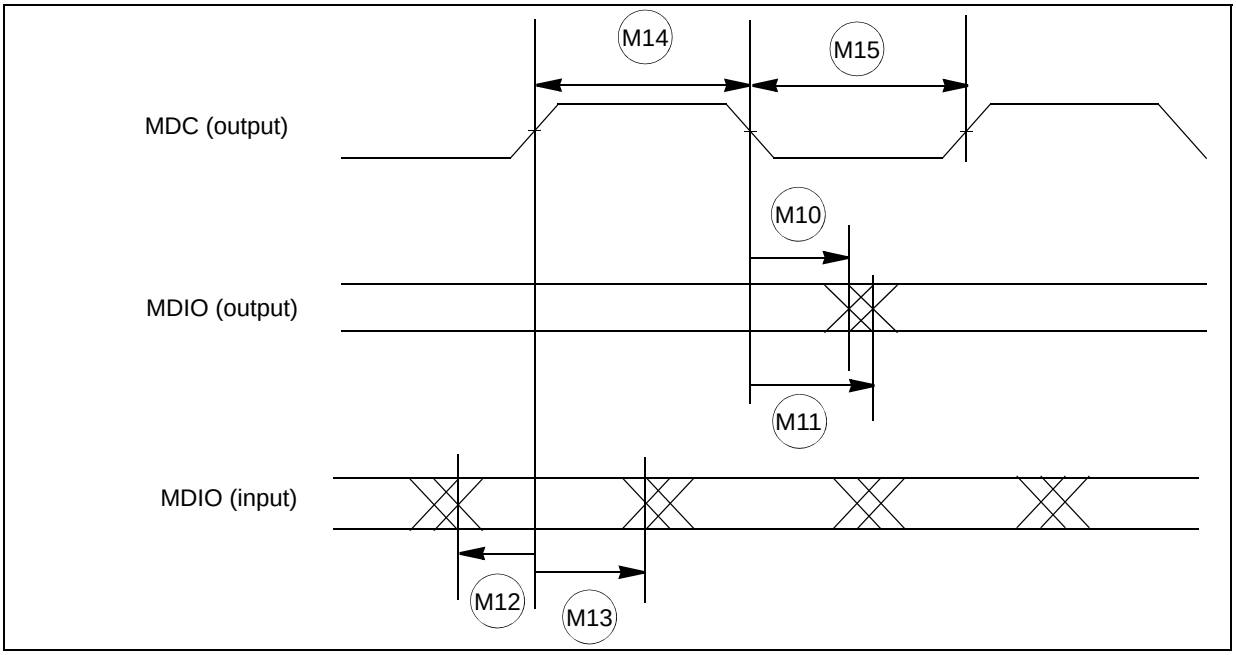
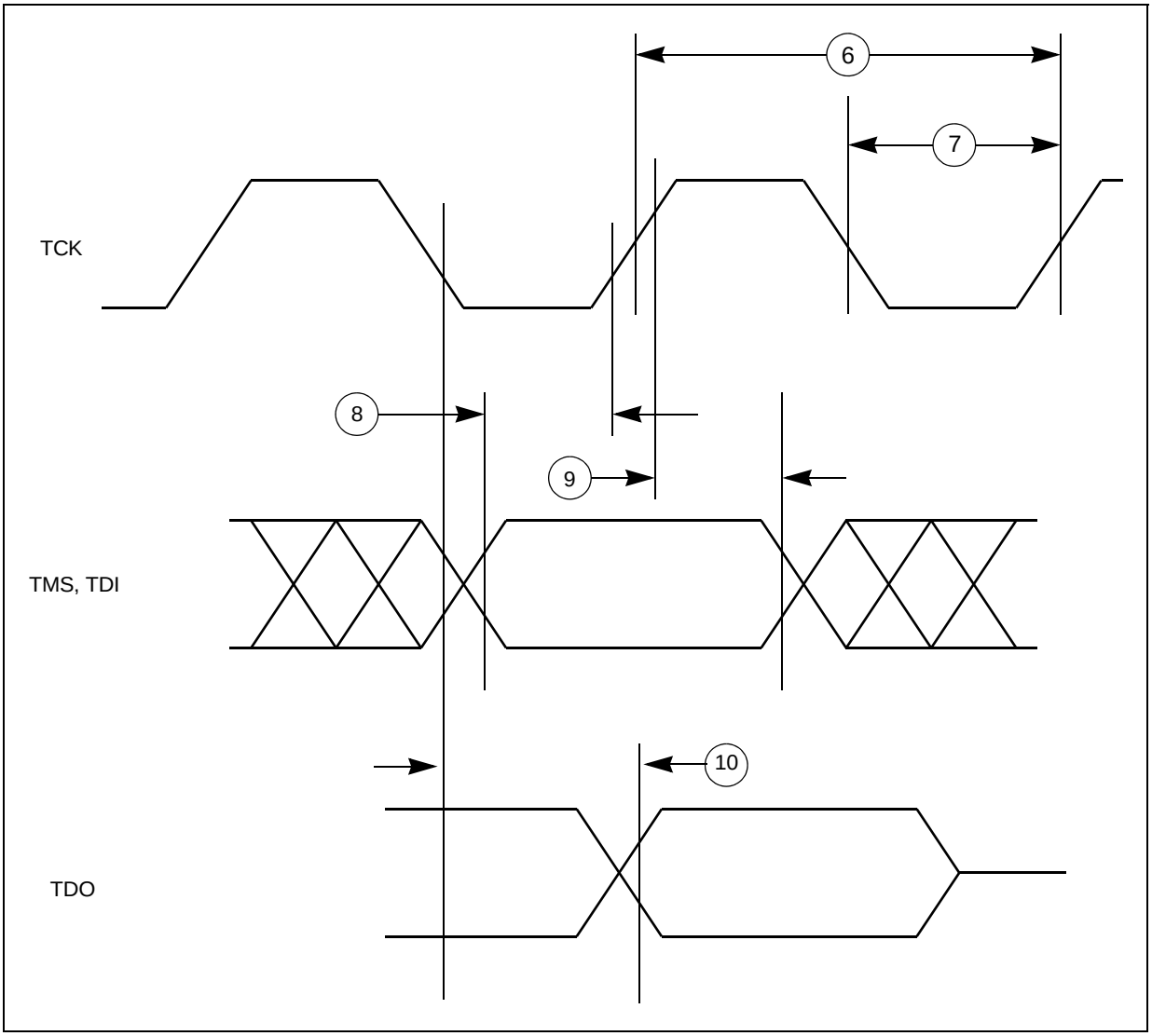


Figure 35. Nexus TDI, TMS, TDO timing



3.19.4 JTAG characteristics

Table 52. JTAG characteristics

No.	Symbol		C	Parameter	Value			Unit
					Min	Typ	Max	
1	t_{JCYC}	CC	D	TCK cycle time	64	—	—	ns
2	t_{TDIS}	CC	D	TDI setup time	10	—	—	ns
3	t_{TDIH}	CC	D	TDI hold time	5	—	—	ns
4	t_{TMSS}	CC	D	TMS setup time	10	—	—	ns
5	t_{TMSH}	CC	D	TMS hold time	5	—	—	ns
6	t_{TDOV}	CC	D	TCK low to TDO valid	—	—	33	ns

Table 55. LBGA256 mechanical data

Ref	mm		
	Min	Typ	Max
A	1.210		1.700
A1	0.300		
A2		0.300	
A4			0.800
b	0.400	0.500	0.600
D	16.800	17.000	17.200
D1		15.000	
E	16.800	17.000	17.200
E1		15.000	
e	0.900	1.000	1.100
Z	0.750	1.000	1.250
ddd			0.200

Note: The package is designed according to the JEDEC standard No 95-1 Section 14 dedicated to Ball Grid Array Package Design Guide.