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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z4d
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, LINbus, SPI, UART/USART
Peripherals	DMA, POR, PWM, WDT
Number of I/O	177
Program Memory Size	1.5MB (1.5M x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 33x10b, 10x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	208-LQFP
Supplier Device Package	208-LQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/spc564b64l8c9e0y

Table 5. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET config.	Pin number		
								LQFP 176	LQFP 208	LBGA256
PA[10]	PCR[10]	AF0 AF1 AF2 AF3 — — —	GPIO[10] E0UC[10] SDA LIN2TX COL ADC1_S[2] SIN_1	SIUL eMIOS_0 I^2C LINFlexD_2 FEC ADC_1 DSPI_1	I/O I/O I/O O I I I	M/S	Tristate	131	155	A15
PA[11]	PCR[11]	AF0 AF1 AF2 AF3 — — — —	GPIO[11] E0UC[11] SCL — RX_ER EIRQ[16] LIN2RX ADC1_S[3]	SIUL eMIOS_0 I^2C — FEC SIUL LINFlexD_2 ADC_1	I/O I/O I/O — I I I I	M/S	Tristate	132	156	B14
PA[12]	PCR[12]	AF0 AF1 AF2 AF3 — —	GPIO[12] — E0UC[28] CS3_1 EIRQ[17] SIN_0	SIUL — eMIOS_0 DSPI1 SIUL DSPI_0	I/O — I/O O I I	S	Tristate	53	69	P6
PA[13]	PCR[13]	AF0 AF1 AF2 AF3	GPIO[13] SOUT_0 E0UC[29] —	SIUL DSPI_0 eMIOS_0 —	I/O O I/O —	M/S	Tristate	52	66	R5
PA[14]	PCR[14]	AF0 AF1 AF2 AF3 —	GPIO[14] SCK_0 CS0_0 E0UC[0] EIRQ[4]	SIUL DSPI_0 DSPI_0 eMIOS_0 SIUL	I/O I/O I/O I/O I	M/S	Tristate	50	58	P4
PA[15]	PCR[15]	AF0 AF1 AF2 AF3 —	GPIO[15] CS0_0 SCK_0 E0UC[1] WKPU[10]	SIUL DSPI_0 DSPI_0 eMIOS_0 WKPU	I/O I/O I/O I/O I	M/S	Tristate	48	56	R2

Table 5. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET config.	Pin number		
								LQFP 176	LQFP 208	LBGA256
PC[8]	PCR[40]	AF0 AF1 AF2 AF3	GPIO[40] LIN2TX E0UC[3] —	SIUL LINFlexD_2 eMIOS_0 —	I/O O I/O —	S	Tristate	175	207	B3
PC[9]	PCR[41]	AF0 AF1 AF2 AF3 — —	GPIO[41] — E0UC[7] — LIN2RX WKPU[13]	SIUL — eMIOS_0 — LINFlexD_2 WKPU	I/O — I/O — I I	S	Tristate	2	2	C3
PC[10]	PCR[42]	AF0 AF1 AF2 AF3	GPIO[42] CAN1TX CAN4TX MA[1]	SIUL FlexCAN_1 FlexCAN_4 ADC_0	I/O O O O	M/S	Tristate	36	36	L1
PC[11]	PCR[43]	AF0 AF1 AF2 AF3 — — —	GPIO[43] — — MA[2] CAN1RX CAN4RX WKPU[5]	SIUL — — ADC_0 FlexCAN_1 FlexCAN_4 WKPU	I/O — — O I I I	S	Tristate	35	35	K4
PC[12]	PCR[44]	AF0 AF1 AF2 AF3 ALT4 — —	GPIO[44] E0UC[12] — — FR_DBG[0] SIN_2 EIRQ[19]	SIUL eMIOS_0 — — Flexray DSPI_2 SIUL	I/O I/O — — O I I	M/S	Tristate	173	205	B4
PC[13]	PCR[45]	AF0 AF1 AF2 AF3 ALT4	GPIO[45] E0UC[13] SOUT_2 — FR_DBG[1]	SIUL eMIOS_0 DSPI_2 — Flexray	I/O I/O O — O	M/S	Tristate	174	206	A3

Table 5. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET config.	Pin number		
								LQFP 176	LQFP 208	LBGA256
PD[9]	PCR[57]	AF0 AF1 AF2 AF3 — —	GPI[57] — — — ADC0_P[13] ADC1_P[13]	SIUL — — — ADC_0 ADC_1	I — — — I I	I	Tristate	94	114	N16
PD[10]	PCR[58]	AF0 AF1 AF2 AF3 — —	GPI[58] — — — ADC0_P[14] ADC1_P[14]	SIUL — — — ADC_0 ADC_1	I — — — I I	I	Tristate	95	115	M14
PD[11]	PCR[59]	AF0 AF1 AF2 AF3 — —	GPI[59] — — — ADC0_P[15] ADC1_P[15]	SIUL — — — ADC_0 ADC_1	I — — — I I	I	Tristate	96	116	M15
PD[12]	PCR[60]	AF0 AF1 AF2 AF3 —	GPIO[60] CS5_0 E0UC[24] — ADC0_S[4]	SIUL DSPI_0 eMIOS_0 — ADC_0	I/O O I/O — I	S	Tristate	100	120	L13
PD[13]	PCR[61]	AF0 AF1 AF2 AF3 —	GPIO[61] CS0_1 E0UC[25] — ADC0_S[5]	SIUL DSPI_1 eMIOS_0 — ADC_0	I/O I/O I/O — I	S	Tristate	102	124	K14
PD[14]	PCR[62]	AF0 AF1 AF2 AF3 ALT4 —	GPIO[62] CS1_1 E0UC[26] — FR_DBG[0] ADC0_S[6]	SIUL DSPI_1 eMIOS_0 — Flexray ADC_0	I/O O I/O — O I	S	Tristate	104	126	K13

Table 5. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET config.	Pin number		
								LQFP 176	LQFP 208	LBGA256
PF[8]	PCR[88]	AF0 AF1 AF2 AF3	GPIO[88] CAN3TX CS4_0 CAN2TX	SIUL FlexCAN_3 DSPI_0 FlexCAN_2	I/O O O O	M/S	Tristate	42	50	N2
PF[9]	PCR[89]	AF0 AF1 AF2 AF3 — — —	GPIO[89] E1UC[1] CS5_0 — CAN2RX CAN3RX WKPU[22]	SIUL eMIOS_1 DSPI_0 — FlexCAN_2 FlexCAN_3 WKPU	I/O I/O O — I I I	S	Tristate	41	49	M4
PF[10]	PCR[90]	AF0 AF1 AF2 AF3	GPIO[90] CS1_0 LIN4TX E1UC[2]	SIUL DSPI_0 LINFlexD_4 eMIOS_1	I/O O O I/O	M/S	Tristate	46	54	P2
PF[11]	PCR[91]	AF0 AF1 AF2 AF3 — —	GPIO[91] CS2_0 E1UC[3] — LIN4RX WKPU[15]	SIUL DSPI_0 eMIOS_1 — LINFlexD_4 WKPU	I/O O I/O — I I	S	Tristate	47	55	R1
PF[12]	PCR[92]	AF0 AF1 AF2 AF3	GPIO[92] E1UC[25] LIN5TX —	SIUL eMIOS_1 LINFlexD_5 —	I/O I/O O —	M/S	Tristate	43	51	P1
PF[13]	PCR[93]	AF0 AF1 AF2 AF3 — —	GPIO[93] E1UC[26] — — LIN5RX WKPU[16]	SIUL eMIOS_1 — — LINFlexD_5 WKPU	I/O I/O — — I I	S	Tristate	49	57	P3

Table 5. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET config.	Pin number		
								LQFP 176	LQFP 208	LBGA256
PJ[10]	PCR[154]	AF0 AF1 AF2 AF3 —	GPIO[154] — — — ADC1_S[9]	SIUL — — — ADC_1	I/O — — — I	S	Tristate	—	67	T5
PJ[11]	PCR[155]	AF0 AF1 AF2 AF3 —	GPIO[155] — — — ADC1_S[10]	SIUL — — — ADC_1	I/O — — — I	S	Tristate	—	60	R3
PJ[12]	PCR[156]	AF0 AF1 AF2 AF3 —	GPIO[156] — — — ADC1_S[11]	SIUL — — — ADC_1	I/O — — — I	S	Tristate	—	59	T1
PJ[13]	PCR[157]	AF0 AF1 AF2 AF3 — — — —	GPIO[157] — CS1_7 — CAN4RX ADC1_S[12] CAN1RX WKPU[31]	SIUL — DSPI_7 — FlexCAN_4 ADC_1 FlexCAN_1 WKPU	I/O — O — I I I I	S	Tristate	—	65	N5
PJ[14]	PCR[158]	AF0 AF1 AF2 AF3	GPIO[158] CAN1TX CAN4TX CS2_7	SIUL FlexCAN_1 FlexCAN_4 DSPI_7	I/O O O O	M/S	Tristate	—	64	T4
PJ[15]	PCR[159]	AF0 AF1 AF2 AF3 —	GPIO[159] — CS1_6 — CAN1RX	SIUL — DSPI_6 — FlexCAN_1	I/O — O — I	M/S	Tristate	—	63	R4

Table 5. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET config.	Pin number		
								LQFP 176	LQFP 208	LBGA256
PK[14]	PCR[174]	AF0 AF1 AF2 AF3	GPIO[174] CAN3TX CS3_7 CS0_1	SIUL FlexCAN_3 DSPI_7 DSPI_1	I/O O O I/O	M/S	Tristate	—	202	J12
PK[15]	PCR[175]	AF0 AF1 AF2 AF3 — —	GPIO[175] — — — SIN_1 SIN_7	SIUL — — — DSPI_1 DSPI_7	I/O — — — I I	M/S	Tristate	—	203	D5
PL[0]	PCR[176]	AF0 AF1 AF2 AF3	GPIO[176] SOUT_1 SOUT_7 —	SIUL DSPI_1 DSPI_7 —	I/O O O —	M/S	Tristate	—	204	C4
PL[1]	PCR[177]	AF0 AF1 AF2 AF3	GPIO[177] — — —	SIUL — — —	I/O — — —	M/S	Tristate	—	—	F7
PL[2]	PCR[178][7]	AF0 AF1 AF2 AF3	GPIO[178] — MDO0[8] —	SIUL — Nexus —	I/O — O —	M/S	Tristate	—	—	F5
PL[3]	PCR[179]	AF0 AF1 AF2 AF3	GPIO[179] — MDO1 —	SIUL — Nexus —	I/O — O —	M/S	Tristate	—	—	G5
PL[4]	PCR[180]	AF0 AF1 AF2 AF3	GPIO[180] — MDO2 —	SIUL — Nexus —	I/O — O —	M/S	Tristate	—	—	H5
PL[5]	PCR[181]	AF0 AF1 AF2 AF3	GPIO[181] — MDO3 —	SIUL — Nexus —	I/O — O —	M/S	Tristate	—	—	J5

Table 5. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET config.	Pin number		
								LQFP 176	LQFP 208	LBGA256
PL[14]	PCR[190]	AF0 AF1 AF2 AF3	GPIO[190] — MDO7 —	SIUL — Nexus —	I/O — O —	M/S	Tristate	—	—	E12
PL[15]	PCR[191]	AF0 AF1 AF2 AF3	GPIO[191] — MDO8 —	SIUL — Nexus —	I/O — O —	M/S	Tristate	—	—	E11
PM[0]	PCR[192]	AF0 AF1 AF2 AF3	GPIO[192] — MDO9 —	SIUL — Nexus —	I/O — O —	M/S	Tristate	—	—	E10
PM[1]	PCR[193]	AF0 AF1 AF2 AF3	GPIO[193] — MDO10 —	SIUL — Nexus —	I/O — O —	M/S	Tristate	—	—	E9
PM[2]	PCR[194]	AF0 AF1 AF2 AF3	GPIO[194] — MDO11 —	SIUL — Nexus —	I/O — O —	M/S	Tristate	—	—	F12
PM[3]	PCR[195]	AF0 AF1 AF2 AF3	GPIO[195] — — —	SIUL — — —	I/O — — —	M/S	Tristate	—	—	K12
PM[4]	PCR[196]	AF0 AF1 AF2 AF3	GPIO[196] — — —	SIUL — — —	I/O — — —	M/S	Tristate	—	—	L12

3.5.2 Power considerations

The average chip-junction temperature, T_J, in degrees Celsius, may be calculated using *Equation 1*:

Equation 1 $T_J = T_A + (P_D \times R_{\theta JA})$

Where:

T_A is the ambient temperature in °C.

$R_{\theta JA}$ is the package junction-to-ambient thermal resistance, in °C/W.

P_D is the sum of P_{INT} and $P_{I/O}$ ($P_D = P_{INT} + P_{I/O}$).

P_{INT} is the product of I_{DD} and V_{DD}, expressed in watts. This is the chip internal power.

$P_{I/O}$ represents the power dissipation on input and output pins; user determined.

Most of the time for the applications, $P_{I/O} < P_{INT}$ and may be neglected. On the other hand, $P_{I/O}$ may be significant, if the device is configured to continuously drive external modules and/or memories.

An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is given by:

Equation 2 $P_D = K / (T_J + 273\ °C)$

Therefore, solving equations *Equation 1* and *Equation 2*:

Equation 3 $K = P_D \times (T_A + 273\ °C) + R_{\theta JA} \times P_D^2$

Where:

K is a constant for the particular part, which may be determined from *Equation 3* by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J may be obtained by solving equations *Equation 1* and *Equation 2* iteratively for any value of T_A.

3.6 I/O pad electrical characteristics

3.6.1 I/O pad types

The device provides four main I/O pad types depending on the associated alternate functions:

- Slow pads—These pads are the most common pads, providing a good compromise between transition time and low electromagnetic emission.
- Medium pads—These pads provide transition fast enough for the serial communication channels with controlled current to reduce electromagnetic emission.
- Fast pads—These pads provide maximum speed. These are used for improved Nexus debugging capability.
- Input only pads—These pads are associated to ADC channels and 32 kHz low power external crystal oscillator providing low input leakage.
- Low power pads—These pads are active in standby mode for wakeup source.

Also, medium/slow and fast/medium pads are available in design which can be configured to behave like a slow/medium and medium/fast pads depending upon the slew-rate control.

Table 18. FAST configuration output buffer electrical characteristics

Symbol		C	Parameter	Conditions[1],[2]		Value			Unit
						Min	Typ	Max	
V_{OH}	CC	P	Output high level FAST configuration	Push Pull	I_{OH} = –14 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	$0.8V_{DD}$	—	—	V
		C			I_{OH} = –7 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 1[3]	$0.8V_{DD}$	—	—	
		C			I_{OH} = –11 mA, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	V_{DD} – 0.8	—	—	
V_{OL}	CC	P	Output low level FAST configuration	Push Pull	I_{OL} = 14 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	$0.1V_{DD}$	V
		C			I_{OL} = 7 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 1[3]	—	—	$0.1V_{DD}$	
		C			I_{OL} = 11 mA, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	0.5	

1. V_{DD} = 3.3 V ± 10 % / 5.0 V ± 10 %, T_A = –40 to 125 °C, unless otherwise specified.
2. V_{DD} as mentioned in the table is $V_{DD\_HV\_A}$/$V_{DD\_HV\_B}$.
3. The configuration PAD3V5 = 1 when V_{DD} = 5 V is only a transient configuration during power-up. All pads but RESET and Nexus outputs (MDOx, EVTO, MCKO) are configured in input or in high impedance state.

3.6.4 Output pin transition times

Table 19. Output pin transition times

Symbol		C	Parameter	Conditions[1],[2]		Value[3]			Unit
						Min	Typ	Max	
T_{tr}	CC	D	Output transition time output pin[4] SLOW configuration	C_L = 25 pF	V_{DD} = 5.0 V ± 10 %, PAD3V5V = 0	—	—	50	ns
		T		C_L = 50 pF		—	—	100	
		D		C_L = 100 pF		—	—	125	
		D		C_L = 25 pF	V_{DD} = 3.3 V ± 10 %, PAD3V5V = 1	—	—	40	
		T		C_L = 50 pF		—	—	50	
		D		C_L = 100 pF		—	—	75	
T_{tr}	CC	D	Output transition time output pin[4] MEDIUM configuration	C_L = 25 pF	V_{DD} = 5.0 V ± 10 %, PAD3V5V = 0 SIUL.PCRx.SRC = 1	—	—	10	ns
		T		C_L = 50 pF		—	—	20	
		D		C_L = 100 pF		—	—	40	
		D		C_L = 25 pF	V_{DD} = 3.3 V ± 10 %, PAD3V5V = 1 SIUL.PCRx.SRC = 1	—	—	12	
		T		C_L = 50 pF		—	—	25	
		D		C_L = 100 pF		—	—	40	

Table 22. Reset electrical characteristics

Symbol		C	Parameter	Conditions[1]	Value[2]			Unit
					Min	Typ	Max	
V_{IH}	SR	P	Input High Level CMOS (Schmitt Trigger)	—	$0.65V_{DD}$	—	V_{DD} + 0.4	V
V_{IL}	SR	P	Input low Level CMOS (Schmitt Trigger)	—	–0.3	—	$0.35V_{DD}$	V
V_{HYS}	CC	C	Input hysteresis CMOS (Schmitt Trigger)	—	$0.1V_{DD}$	—	—	V
V_{OL}	CC	P	Output low level	Push Pull, I_{OL} = 2 mA, V_{DD} = 5.0 V ± 10 %, PAD3V5V = 0 (recommended)	—	—	$0.1V_{DD}$	V
				Push Pull, I_{OL} = 1 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 1[3]	—	—	$0.1V_{DD}$	
				Push Pull, I_{OL} = 1 mA, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1 (recommended)	—	—	0.5	
T_{tr}	CC	D	Output transition time output pin[4] MEDIUM configuration	C_L = 25 pF, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	10	ns
				C_L = 50 pF, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	20	
				C_L = 100 pF, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	40	
				C_L = 25 pF, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	12	
				C_L = 50 pF, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	25	
				C_L = 100 pF, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	40	
W_{FRST}	SR	P	Reset input filtered pulse	—	—	—	40	ns
W_{NFRST}	SR	P	Reset input not filtered pulse	—	1000	—	—	ns
$\|I_{WPU}\|$	CC	P	Weak pull-up current absolute value	V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	10	—	150	µA
				V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	10	—	150	
				V_{DD} = 5.0 V ± 10%, PAD3V5V = 1[5]	10	—	250	

1. V_{DD} = 3.3 V ± 10 % / 5.0 V ± 10 %, T_A = –40 to 125 °C, unless otherwise specified.
2. V_{DD} as mentioned in the table is $V_{DD\_HV\_A}$/$V_{DD\_HV\_B}$. All values need to be confirmed during device validation.
3. This is a transient configuration during power-up, up to the end of reset PHASE2 (refer to the RGM module section of the device Reference Manual).
4. C_L includes device and package capacitance (C_{PKG} < 5 pF).
5. The configuration PAD3V5 = 1 when V_{DD} = 5 V is only transient configuration during power-up. All pads but RESET and Nexus output (MDOx, EVTO, MCKO) are configured in input or in high impedance state.

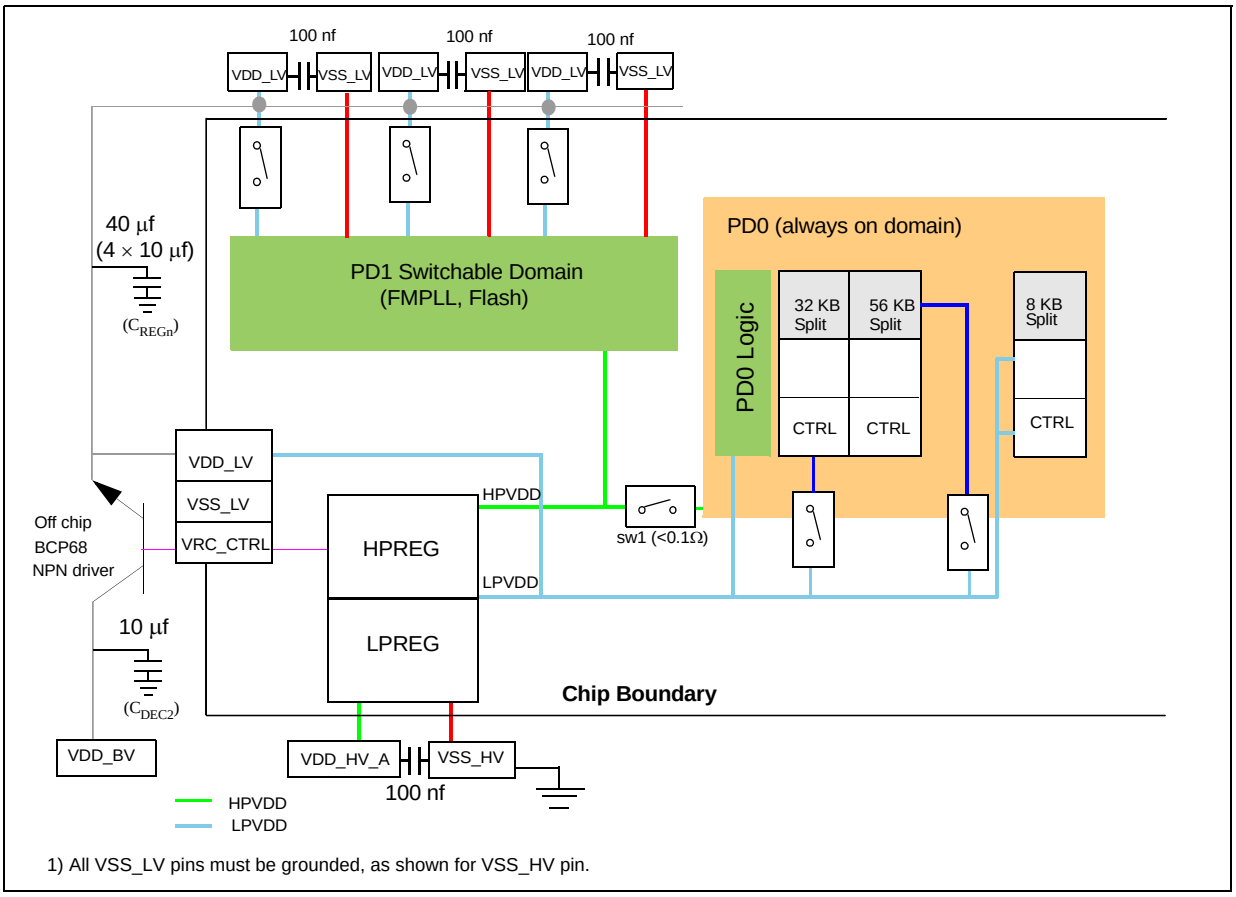
3.8 Power management electrical characteristics

3.8.1 Voltage regulator electrical characteristics

The device implements an internal voltage regulator to generate the low voltage core supply V_{DD_LV} from the high voltage supply $V_{DD\_HV\_A}$. The following supplies are involved:

- HV: High voltage external power supply for voltage regulator module. This must be provided externally through $V_{DD\_HV\_A}$ power pin.
- LV: Low voltage internal power supply for core, FMPLL and Flash digital logic. This is generated by the on-chip VREG with an external ballast (BCP68 NPN device). It is further split into four main domains to ensure noise isolation between critical LV modules within the device:
  - LV_COR: Low voltage supply for the core. It is also used to provide supply for FMPLL through double bonding.
  - LV_CFLA0/CFLA1: Low voltage supply for the two code Flash modules. It is shorted with LV_COR through double bonding.
  - LV_DFLA: Low voltage supply for data Flash module. It is shorted with LV_COR through double bonding.
  - LV_PLL: Low voltage supply for FMPLL. It is shorted to LV_COR through double bonding.

Figure 8. Voltage regulator capacitance connection



1) All VSS_LV pins must be grounded, as shown for VSS_HV pin.

Table 25. Low voltage power domain electrical characteristics(1)

Symbol		C	Parameter	Conditions(2)		Value			Unit
						Min	Typ(3)	Max(4)	
I_{DDMAX}(5)	CC	D	RUN mode maximum average current	—		—	210	300(6), (7)	mA
I_{DDRUN}	CC	P	RUN mode typical average current(8)	at 120 MHz	T_A = 25 °C	—	150	208(9)	mA
		D		at 80 MHz	T_A = 25 °C	—	110(8)	150(10)	mA
		C		at 120 MHz	T_A = 125 °C	—	180	280	mA
I_{DDHALT}	CC	P	HALT mode current(11)	at 120 MHz	T_A = 25 °C	—	20	27	mA
		C		at 120 MHz	T_A = 125 °C	—	35	100	mA
I_{DDSTOP}	CC	P	STOP mode current(12)	No clocks active	T_A = 25 °C	—	0.4	5	mA
		C			T_A = 125 °C	—	16	72	mA
$I_{DDSTDBY3}$ (96 KB RAM retained)	CC	P	STANDBY3 mode current(13)	No clocks active	T_A = 25 °C	—	50	96	µA
		C			T_A = 125 °C	—	630	2400	µA
$I_{DDSTDBY2}$ (64 KB RAM retained)	CC	C	STANDBY2 mode current(14)	No clocks active	T_A = 25 °C	—	40	92	µA
		C			T_A = 125 °C	—	500	2000	µA
$I_{DDSTDBY1}$ (8 KB RAM retained)	CC	C	STANDBY1 mode current(15)	No clocks active	T_A = 25 °C	—	25	85	µA
		C			T_A = 125 °C	—	230	1100	µA
Adders in LP mode	CC	T	32 KHz OSC	—	T_A = 25 °C	—	—	5	µA
			4–40 MHz OSC	—	T_A = 25 °C	—	—	3	mA
			16 MHz IRC	—	T_A = 25 °C	—	—	500	µA
			128 KHz IRC	—	T_A = 25 °C	—	—	5	µA

1. Except for I_{DDMAX}, all the current values are total current drawn from $V_{DD\_HV\_A}$.
2. V_{DD} = 3.3 V ± 10 % / 5.0 V ± 10 %, T_A = –40 to 125 °C, unless otherwise specified All temperatures are based on an ambient temperature.
3. Target typical current consumption for the following typical operating conditions and configuration. Process = typical, Voltage = 1.2 V.
4. Target maximum current consumption for mode observed under typical operating conditions. Process = Fast, Voltage = 1.32 V.
5. Running consumption is given on voltage regulator supply (V_{DDREG}). It does not include consumption linked to I/Os toggling. This value is highly dependent on the application. The given value is thought to be a worst case value with all cores and peripherals running, and code fetched from code flash while modify operation on-going on data flash. It is to be noticed that this value can be significantly reduced by application: switch-off not used peripherals (default), reduce peripheral frequency through internal prescaler, fetch from RAM most used functions, use low power mode when possible.
6. Higher current may sunk by device during power-up and standby exit. Please refer to in rush current in *Table 23*.
7. Maximum “allowed” current is package dependent.
8. Only for the “P” classification: Code fetched from RAM: Serial IPs CAN and LIN in loop back mode, DSPI as Master, PLL as system Clock (4 x Multiplier) peripherals on (eMIOS/CTU/ADC) and running at max frequency, periodic SW/WDG timer reset enabled. RUN current measured with typical application with accesses on both code flash and RAM.

3.11.2 Electromagnetic interference (EMI)

The product is monitored in terms of emission based on a typical application. This emission test conforms to the IEC61967-1 standard, which specifies the general conditions for EMI measurements.

Table 32. EMI radiated emission measurement(1)(2)

Symbol		C	Parameter	Conditions		Value			Unit
						Min	Typ	Max	
—	SR	—	Scan range	—		0.150		1000	MHz
f_{CPU}	SR	—	Operating frequency	—		—	120	—	MHz
V_{DD_LV}	SR	—	LV operating voltages	—		—	1.28	—	V
S_{EMI}	CC	T	Peak level	V_{DD} = 5 V, T_A = 25 °C, LQFP176 package Test conforming to IEC 61967-2, f_{OSC} = 40 MHz/f_{CPU} = 120 MHz	No PLL frequency modulation	—	—	18	dBµV
					± 2% PLL frequency modulation	—	—	14(3)	dBµV

1. EMI testing and I/O port waveforms per IEC 61967-1, -2, -4.
2. For information on conducted emission and susceptibility measurement (norm IEC 61967-4), please contact your local marketing representative.
3. All values need to be confirmed during device validation.

3.11.3 Absolute maximum ratings (electrical sensitivity)

Based on two different tests (ESD and LU) using specific measurement methods, the product is stressed in order to determine its performance in terms of electrical sensitivity.

3.11.3.1 Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n+1) supply pin). This test conforms to the AEC-Q100-002/-003/-011 standard. For more details, refer to the application note *Electrostatic Discharge Sensitivity Measurement* (AN1181).

Table 33. ESD absolute maximum ratings(1)(2)

Symbol	Ratings	Conditions	Class	Max value(3)	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (Human Body Model)	T_A = 25 °C conforming to AEC-Q100-002	H1C	2000	V
$V_{ESD(MM)}$	Electrostatic discharge voltage (Machine Model)	T_A = 25 °C conforming to AEC-Q100-003	M2	200	
$V_{ESD(CDM)}$	Electrostatic discharge voltage (Charged Device Model)	T_A = 25 °C conforming to AEC-Q100-011	C3A	500	
				750 (corners)	

Table 36. Fast external crystal oscillator (4 to 40 MHz) electrical characteristics (continued)

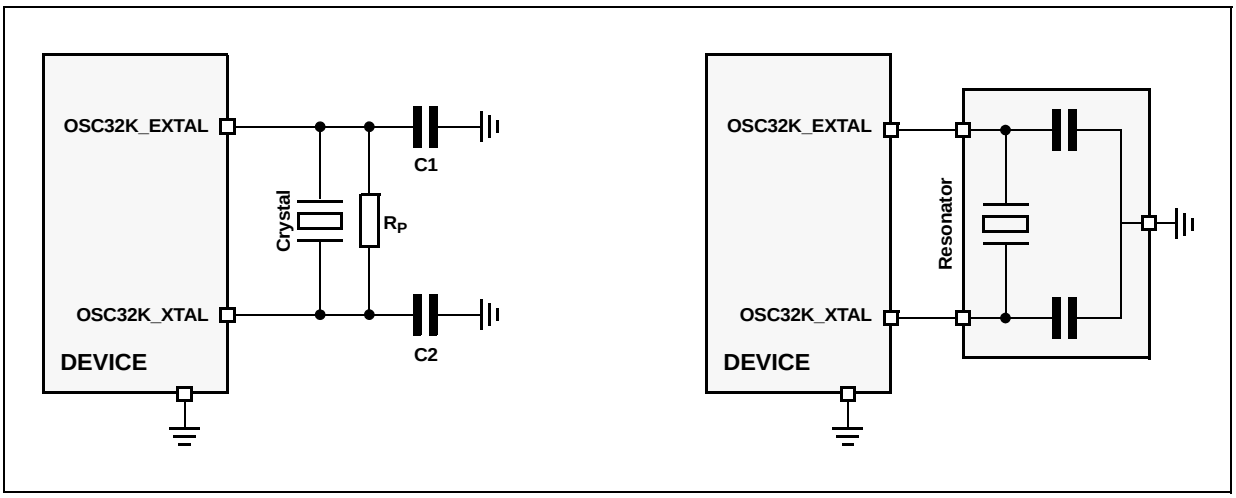
Symbol		C	Parameter	Conditions[1]	Value[2]			Unit
					Min	Typ	Max	
V_{IH}	SR	P	Input high level CMOS (Schmitt Trigger)	Oscillator bypass mode	$0.65V_{DD\_HV\_A}$	—	$V_{DD\_HV\_A}$ + 0.4	V
V_{IL}	SR	P	Input low level CMOS (Schmitt Trigger)	Oscillator bypass mode	–0.3	—	$0.35V_{DD\_HV\_A}$	V

1. V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified.
2. All values need to be confirmed during device validation.
3. Based on ATE Cz
4. Stated values take into account only analog module consumption but not the digital contributor (clock tree and enabled peripherals).

3.13 Slow external crystal oscillator (32 kHz) electrical characteristics

The device provides a low power oscillator/resonator driver.

Figure 12. Crystal oscillator and resonator connection scheme



Note: OSC32K_XTAL/OSC32K_EXTAL must not be directly used to drive external circuits.

3.14 FMPLL electrical characteristics

The device provides a frequency-modulated phase-locked loop (FMPLL) module to generate a fast system clock from the main oscillator driver.

Table 39. FMPLL electrical characteristics

Symbol		C	Parameter	Conditions[1]	Value[2]			Unit
					Min	Typ	Max	
f_{PLLIN}	SR	—	FMPLL reference clock[3]	—	4	—	64	MHz
Δ_{PLLIN}	SR	—	FMPLL reference clock duty cycle[3]	—	40	—	60	%
f_{PLLOUT}	CC	P	FMPLL output clock frequency	—	16	—	120	MHz
f_{CPU}	SR	—	System clock frequency	—	—	—	120 + 2%[4]	MHz
f_{FREE}	CC	P	Free-running frequency	—	20	—	150	MHz
t_{LOCK}	CC	P	FMPLL lock time	Stable oscillator (f_{PLLIN} = 16 MHz)		40	100	µs
Δt_{LTJIT}	CC	—	FMPLL long term jitter	f_{PLLIN} = 40 MHz (resonator), f_{PLLCLK} @ 120 MHz, 4000 cycles	—	—	6 (for < 1ppm)	ns
I_{PLL}	CC	C	FMPLL consumption	T_A = 25 °C	—	—	3	mA

1. V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified.
2. All values need to be confirmed during device validation.
3. PLLIN clock retrieved directly from 4-40 MHz XOSC or 16 MIRC. Input characteristics are granted when oscillator is used in functional mode. When bypass mode is used, oscillator input clock should verify f_{PLLIN} and Δ_{PLLIN}.
4. f_{CPU} 120 + 2% MHz can be achieved at 125 °C.

3.15 Fast internal RC oscillator (16 MHz) electrical characteristics

The device provides a 16 MHz main internal RC oscillator. This is used as the default clock at the power-up of the device and can also be used as input to PLL.

Table 40. Fast internal RC oscillator (16 MHz) electrical characteristics

Symbol		C	Parameter	Conditions[1]	Value[2]			Unit
					Min	Typ	Max	
f_{FIRC}	CC	P	Fast internal RC oscillator high frequency	T_A = 25 °C, trimmed	—	16	—	MHz
	SR	—		—	12		20	

Table 43. ADC conversion characteristics (10-bit ADC_0) (continued)

Symbol		C	Parameter	Conditions[1]		Value			Unit
						Min	Typ	Max	
R_{SW2}	CC	D	Internal resistance of analog source	—		—	—	2	kΩ
R_{AD}	CC	D	Internal resistance of analog source	—		—	—	2	kΩ
I_{INJ}[7]	SR	—	Input current Injection	Current injection on one ADC_0 input, different from the converted one	V_{DD} = 3.3 V ± 10%	–5	—	5	mA
					V_{DD} = 5.0 V ± 10%	–5	—	5	
| INL |	CC	T	Absolute value for integral non-linearity	No overload		—	0.5	1.5	LSB
| DNL |	CC	T	Absolute differential non-linearity	No overload		—	0.5	1.0	LSB
| OFS |	CC	T	Absolute offset error	—		—	0.5	—	LSB
| GNE |	CC	T	Absolute gain error	—		—	0.6	—	LSB
TUEP	CC	P	Total unadjusted error[8] for precise channels, input only pins	Without current injection		–2	0.6	2	LSB
		T		With current injection		–3		3	
TUEX	CC	T	Total unadjusted error[8] for extended channel	Without current injection		–3	1	3	LSB
		T		With current injection		–4		4	

1. V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified.
2. Analog and digital V_{SS_HV} must be common (to be tied together externally).
3. V_{AINx} may exceed V_{SS_ADC0} and V_{DD_ADC0} limits, remaining on absolute maximum ratings, but the results of the conversion will be clamped respectively to 0x000 or 0x3FF.
4. During the sample time the input capacitance C_S can be charged/discharged by the external source. The internal resistance of the analog source must allow the capacitance to reach its final voltage level within t_{ADC0_S}. After the end of the sample time t_{ADC0_S}, changes of the analog input voltage have no effect on the conversion result. Values for the sample clock t_{ADC0_S} depend on programming.
5. This parameter does not include the sample time t_{ADC0_S}, but only the time for determining the digital result and the time to load the result's register with the conversion result.
6. Refer to ADC conversion table for detailed calculations.
7. PB10 should not have any current injected. It can disturb accuracy on other ADC_0 pins.
8. Total Unadjusted Error: The maximum error that occurs without adjusting Offset and Gain errors. This error is a combination of Offset, Gain and Integral Linearity errors.

Table 44. Conversion characteristics (12-bit ADC_1) (continued)

Symbol		C	Parameter	Conditions[1]		Value			Unit
						Min	Typ	Max	
C_{P3}	CC	D	ADC_1 input pin capacitance 3	—			1.5		pF
R_{SW1}	CC	D	Internal resistance of analog source	—				1	kΩ
R_{SW2}	CC	D	Internal resistance of analog source	—				2	kΩ
R_{AD}	CC	D	Internal resistance of analog source	—				0.3	kΩ
I_{INJ}	SR	—	Input current Injection	Current injection on one ADC_1 input, different from the converted one	V_{DD} = 3.3 V ± 10%	–5	—	5	mA
					V_{DD} = 5.0 V ± 10%	–5	—	5	
INLP	CC	T	Absolute Integral non-linearity-Precise channels	No overload			1	3	LSB
INLS	CC	T	Absolute Integral non-linearity-Standard channels	No overload			1.5	5	LSB
DNL	CC	T	Absolute Differential non-linearity	No overload			0.5	1	LSB
OFS	CC	T	Absolute Offset error	—			2		LSB
GNE	CC	T	Absolute Gain error	—			2		LSB
TUEP[9]	CC	P	Total Unadjusted Error for precise channels, input only pins	Without current injection		–6		6	LSB
		T		With current injection		–8		8	LSB
TUES[9]	CC	T	Total Unadjusted Error for standard channel	Without current injection		–10		10	LSB
		T		With current injection		–12		12	LSB

1. V_{DD} = 3.3 V ± 10 % / 5.0 V ± 10 %, T_A = –40 to 125 °C, unless otherwise specified.
2. Analog and digital V_{SS_HV} must be common (to be tied together externally).

3.19 On-chip peripherals

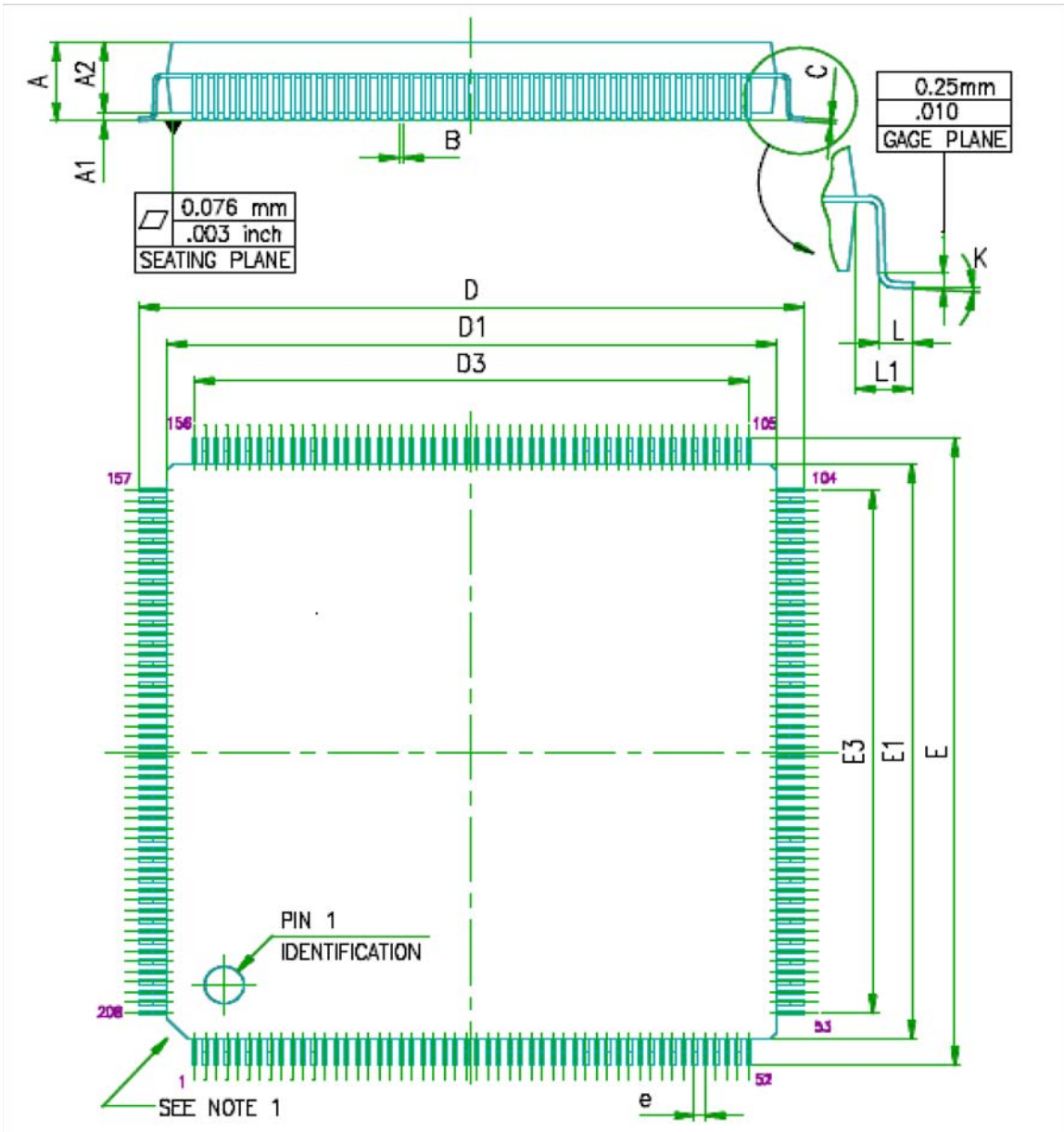
3.19.1 Current consumption

Table 49. On-chip peripherals current consumption(1)

Symbol		C	Parameter	Conditions		Value(2) Typ	Unit
$I_{DD\_HV\_A(CAN)}$	CC	D	CAN (FlexCAN) supply current on $V_{DD\_HV\_A}$	500 Kbps	Total (static + dynamic) consumption: FlexCAN in loop-back mode XTAL@8 MHz used as CAN engine clock source Message sending period is 580 µs	$7.652 \times f_{periph} + 84.73$	µA
				125 Kbps		$8.0743 \times f_{periph} + 26.757$	
$I_{DD\_HV\_A(eMIOS)}$	CC	D	eMIOS supply current on $V_{DD\_HV\_A}$	Static consumption: eMIOS channel OFF Global prescaler enabled		$28.7 \times f_{periph}$	
				Dynamic consumption: It does not change varying the frequency (0.003 mA)		3	
$I_{DD\_HV\_A(SCI)}$	CC	D	SCI (LINFlex) supply current on $V_{DD\_HV\_A}$	Total (static + dynamic) consumption: LIN mode Baudrate: 20 Kbps		$4.7804 \times f_{periph} + 30.946$	
$I_{DD\_HV\_A(SPI)}$	CC	D	SPI (DSPI) supply current on $V_{DD\_HV\_A}$	Ballast static consumption (only clocked)		1	
				Ballast dynamic consumption (continuous communication): Baudrate: 2 Mbit Transmission every 8 µs Frame: 16 bits		$16.3 \times f_{periph}$	
$I_{DD\_HV\_A(ADC)}$	CC	D	ADC supply current on $V_{DD\_HV\_A}$	V_{DD} = 5.5 V	Ballast static consumption (no conversion)	$0.0409 \times f_{periph}$	mA
				V_{DD} = 5.5 V	Ballast dynamic consumption (continuous conversion)	$0.0049 \times f_{periph}$	

4.2.2 LQFP208 package mechanical drawing

Figure 38. LQFP208 mechanical drawing



Note: Exact shape of each corner is optional.

Appendix A Abbreviations

Table 56 lists abbreviations used but not defined elsewhere in this document.

Table 56. Abbreviations

Abbreviation	Meaning
CS	Chip select
EVTO	Event out
MCKO	Message clock out
MDO	Message data out
MSEO	Message start/end out
MTFE	Modified timing format enable
SCK	Serial communications clock
SOUT	Serial data out
TBD	To be defined
TCK	Test clock input
TDI	Test data input
TDO	Test data output
TMS	Test mode select