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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z4d
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, LINbus, SPI, UART/USART
Peripherals	DMA, POR, PWM, WDT
Number of I/O	147
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	160K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 27x10b, 5x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP
Supplier Device Package	176-LQFP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/spc564b70l7b9e0x

Table 3 summarizes the functions of the blocks present on the SPC564Bxx and SPC56ECxx.

Table 3. SPC564Bxx and SPC56ECxx series block summary

Block	Function
Analog-to-digital converter (ADC)	Converts analog voltages to digital values
Boot assist module (BAM)	A block of read-only memory containing VLE code which is executed according to the boot mode of the device
Clock monitor unit (CMU)	Monitors clock source (internal and external) integrity
Cross triggering unit (CTU)	Enables synchronization of ADC conversions with a timer event from the eMIOS or from the PIT
Cryptographic Security Engine (CSE)	Supports the encoding and decoding of any kind of data
Crossbar (XBAR) switch	Supports simultaneous connections between two master ports and three slave ports. The crossbar supports a 32-bit address bus width and a 64-bit data bus width
DMA Channel Multiplexer (DMAMUX)	Allows to route DMA sources (called slots) to DMA channels
Deserial serial peripheral interface (DSPI)	Provides a synchronous serial interface for communication with external devices
Error Correction Status Module (ECSM)	Provides a myriad of miscellaneous control functions for the device including program-visible information about configuration and revision levels, a reset status register, wakeup control for exiting sleep modes, and optional features such as information on memory errors reported by error-correcting codes
Enhanced Direct Memory Access (eDMA)	Performs complex data transfers with minimal intervention from a host processor via “n” programmable channels.
Enhanced modular input output system (eMIOS)	Provides the functionality to generate or measure events
Flash memory	Provides non-volatile storage for program code, constants and variables
FlexCAN (controller area network)	Supports the standard CAN communications protocol
FMPLL (frequency-modulated phase-locked loop)	Generates high-speed system clocks and supports programmable frequency modulation
FlexRay (FlexRay communication controller)	Provides high-speed distributed control for advanced automotive applications
Fast Ethernet Controller (FEC)	Ethernet Media Access Controller (MAC) designed to support both 10 and 100 Mbps Ethernet/IEEE 802.3 networks
Internal multiplexer (IMUX) SIUL subblock	Allows flexible mapping of peripheral interface on the different pins of the device
Inter-integrated circuit (I^2C™) bus	A two wire bidirectional serial bus that provides a simple and efficient method of data exchange between devices
Interrupt controller (INTC)	Provides priority-based preemptive scheduling of interrupt requests for both e200z0h and e200z4d cores
JTAG controller	Provides the means to test chip functionality and connectivity while remaining transparent to system logic when not in test mode

Table 5. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET config.	Pin number		
								LQFP 176	LQFP 208	LBGA256
PC[2]	PCR[34]	AF0 AF1 AF2 AF3 —	GPIO[34] SCK_1 CAN4TX — EIRQ[5]	SIUL DSPI_1 FlexCAN_4 — SIUL	I/O I/O O — I	M/S	Tristate	145	169	B11
PC[3]	PCR[35]	AF0 AF1 AF2 AF3 — — —	GPIO[35] CS0_1 MA[0] — CAN1RX CAN4RX EIRQ[6]	SIUL DSPI_1 ADC_0 — FlexCAN_1 FlexCAN_4 SIUL	I/O I/O O I I I	S	Tristate	144	168	C11
PC[4]	PCR[36]	AF0 AF1 AF2 AF3 ALT4 — — —	GPIO[36] E1UC[31] — FR_B_TX_EN SIN_1 CAN3RX EIRQ[18]	SIUL eMIOS_1 — Flexray DSPI_1 FlexCAN_3 SIUL	I/O I/O — O I I I	M/S	Tristate	159	183	A9
PC[5]	PCR[37]	AF0 AF1 AF2 AF3 ALT4 —	GPIO[37] SOUT_1 CAN3TX — FR_A_TX EIRQ[7]	SIUL DSPI_1 FlexCAN_3 — Flexray SIUL	I/O O O — O I	M/S	Tristate	158	182	B9
PC[6]	PCR[38]	AF0 AF1 AF2 AF3	GPIO[38] LIN1TX E1UC[28] —	SIUL LINFlexD_1 eMIOS_1 —	I/O O I/O —	S	Tristate	44	52	N3
PC[7]	PCR[39]	AF0 AF1 AF2 AF3 — —	GPIO[39] — E1UC[29] — LIN1RX WKPU[12]	SIUL — eMIOS_1 — LINFlexD_1 WKPU	I/O — I/O — I I	S	Tristate	45	53	N4

Table 5. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET config.	Pin number		
								LQFP 176	LQFP 208	LBGA256
PF[1]	PCR[81]	AF0 AF1 AF2 AF3 —	GPIO[81] E0UC[11] CS4_1 — ADC0_S[9]	SIUL eMIOS_0 DSPI_1 — ADC_0	I/O I/O O — I	S	Tristate	64	80	T6
PF[2]	PCR[82]	AF0 AF1 AF2 AF3 —	GPIO[82] E0UC[12] CS0_2 — ADC0_S[10]	SIUL eMIOS_0 DSPI_2 — ADC_0	I/O I/O I/O — I	S	Tristate	65	81	R6
PF[3]	PCR[83]	AF0 AF1 AF2 AF3 —	GPIO[83] E0UC[13] CS1_2 — ADC0_S[11]	SIUL eMIOS_0 DSPI_2 — ADC_0	I/O I/O O — I	S	Tristate	66	82	R7
PF[4]	PCR[84]	AF0 AF1 AF2 AF3 —	GPIO[84] E0UC[14] CS2_2 — ADC0_S[12]	SIUL eMIOS_0 DSPI_2 — ADC_0	I/O I/O O — I	S	Tristate	67	83	R8
PF[5]	PCR[85]	AF0 AF1 AF2 AF3 —	GPIO[85] E0UC[22] CS3_2 — ADC0_S[13]	SIUL eMIOS_0 DSPI_2 — ADC_0	I/O I/O O — I	S	Tristate	68	84	P8
PF[6]	PCR[86]	AF0 AF1 AF2 AF3 —	GPIO[86] E0UC[23] CS1_1 — ADC0_S[14]	SIUL eMIOS_0 DSPI_1 — ADC_0	I/O I/O O — I	S	Tristate	69	85	N8
PF[7]	PCR[87]	AF0 AF1 AF2 AF3 —	GPIO[87] — CS2_1 — ADC0_S[15]	SIUL — DSPI_1 — ADC_0	I/O — O — I	S	Tristate	70	86	P9

Table 5. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET config.	Pin number		
								LQFP 176	LQFP 208	LBGA256
PH[8]	PCR[120]	AF0 AF1 AF2 AF3	GPIO[120] E1UC[10] CS2_2 MA[0]	SIUL eMIOS_1 DSPI_2 ADC_0	I/O I/O O O	M/S	Tristate	166	190	A6
PH[9][6]	PCR[121]	AF0 AF1 AF2 AF3 —	GPIO[121] — — — TCK	SIUL — — — JTAGC	I/O — — — I	S	Input, weak pull-up	155	179	A11
PH[10][6]	PCR[122]	AF0 AF1 AF2 AF3 —	GPIO[122] — — — TMS	SIUL — — — JTAGC	I/O — — — I	M/S	Input, weak pull-up	148	172	D10
PH[11]	PCR[123]	AF0 AF1 AF2 AF3	GPIO[123] SOUT_3 CS0_4 E1UC[5]	SIUL DSPI_3 DSPI_4 eMIOS_1	I/O O I/O I/O	M/S	Tristate	140	164	A13
PH[12]	PCR[124]	AF0 AF1 AF2 AF3	GPIO[124] SCK_3 CS1_4 E1UC[25]	SIUL DSPI_3 DSPI_4 eMIOS_1	I/O I/O O I/O	M/S	Tristate	141	165	B12
PH[13]	PCR[125]	AF0 AF1 AF2 AF3	GPIO[125] SOUT_4 CS0_3 E1UC[26]	SIUL DSPI_4 DSPI_3 eMIOS_1	I/O O I/O I/O	M/S	Tristate	9	9	B1
PH[14]	PCR[126]	AF0 AF1 AF2 AF3	GPIO[126] SCK_4 CS1_3 E1UC[27]	SIUL DSPI_4 DSPI_3 eMIOS_1	I/O I/O O I/O	M/S	Tristate	10	10	C1
PH[15]	PCR[127]	AF0 AF1 AF2 AF3	GPIO[127] SOUT_5 — E1UC[17]	SIUL DSPI_5 — eMIOS_1	I/O O — I/O	M/S	Tristate	8	8	E3

Table 5. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET config.	Pin number		
								LQFP 176	LQFP 208	LBGA256
PK[0]	PCR[160]	AF0 AF1 AF2 AF3	GPIO[160] CAN1TX CS2_6 —	SIUL FlexCAN_1 DSPI_6 —	I/O O O —	M/S	Tristate	—	62	T3
PK[1]	PCR[161]	AF0 AF1 AF2 AF3 —	GPIO[161] CS3_6 — — CAN4RX	SIUL DSPI_6 — — FlexCAN_4	I/O O — — I	M/S	Tristate	—	41	H4
PK[2]	PCR[162]	AF0 AF1 AF2 AF3	GPIO[162] CAN4TX — —	SIUL FlexCAN_4 — —	I/O O — —	M/S	Tristate	—	42	L4
PK[3]	PCR[163]	AF0 AF1 AF2 AF3 — —	GPIO[163] E1UC[0] — — CAN5RX LIN8RX	SIUL eMIOS_1 — — FlexCAN_5 LINFlexD_8	I/O I/O — — I I	M/S	Tristate	—	43	N1
PK[4]	PCR[164]	AF0 AF1 AF2 AF3	GPIO[164] LIN8TX CAN5TX E1UC[1]	SIUL LINFlexD_8 FlexCAN_5 eMIOS_1	I/O O O I/O	M/S	Tristate	—	44	M3
PK[5]	PCR[165]	AF0 AF1 AF2 AF3 — —	GPIO[165] — — — CAN2RX LIN2RX	SIUL — — — FlexCAN_2 LINFlexD_2	I/O — — — I I	M/S	Tristate	—	45	M5
PK[6]	PCR[166]	AF0 AF1 AF2 AF3	GPIO[166] CAN2TX LIN2TX —	SIUL FlexCAN_2 LINFlexD_2 —	I/O O O —	M/S	Tristate	—	46	M6

3 Electrical Characteristics

This section contains electrical characteristics of the device as well as temperature and power considerations.

This product contains devices to protect the inputs against damage due to high static voltages. However, it is advisable to take precautions to avoid application of any voltage higher than the specified maximum rated voltages.

To enhance reliability, unused inputs can be driven to an appropriate logic voltage level (V_{DD} or V_{SS_HV}). This could be done by the internal pull-up and pull-down, which is provided by the product for most general purpose pins.

The parameters listed in the following tables represent the characteristics of the device and its demands on the system.

In the tables where the device logic provides signals with their respective timing characteristics, the symbol “CC” for Controller Characteristics is included in the Symbol column.

In the tables where the external system must provide signals with their respective timing characteristics to the device, the symbol “SR” for System Requirement is included in the Symbol column.

3.1 Parameter classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding, the classifications listed in *Table 6* are used and the parameters are tagged accordingly in the tables where appropriate.

Table 6. Parameter classifications

Classification tag	Tag description
P	Those parameters are guaranteed during production testing on each individual device.
C	Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations.
T	Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category.
D	Those parameters are derived mainly from simulations.

Note: The classification is shown in the column labeled “C” in the parameter tables where appropriate.

3.2 NVUSRO register

Portions of the device configuration, such as high voltage supply is controlled via bit values in the Non-Volatile User Options Register (NVUSRO). For a detailed description of the NVUSRO register, see SPC564Bxx and SPC56ECxx Reference Manual.

Table 11. Recommended operating conditions (5.0 V) (continued)

Symbol		Parameter	Conditions	Value		Unit
				Min	Max	
$V_{DD\_HV\_ADC0}$ (5)	SR	Voltage on VDD_HV_ADC0 with respect to ground (V_{SS_HV})	—	4.5	5.5	V
			Voltage drop(2)	3.0	5.5	
			Relative to $V_{DD\_HV\_A}$(6)	$V_{DD\_HV\_A}$ – 0.1	$V_{DD\_HV\_A}$ + 0.1	
$V_{DD\_HV\_ADC1}$ (7)	SR	Voltage on VDD_HV_ADC1 with respect to ground (V_{SS_HV})	—	4.5	5.5	V
			Voltage drop(2)	3.0	5.5	
			Relative to $V_{DD\_HV\_A}$(6)	$V_{DD\_HV\_A}$ – 0.1	$V_{DD\_HV\_A}$ + 0.1	
V_{IN}	SR	Voltage on any GPIO pin with respect to ground (V_{SS_HV})	—	V_{SS_HV} –0.1	—	V
			Relative to $V_{DD\_HV\_A/HV\_B}$	—	$V_{DD\_HV\_A/HV\_B}$ + 0.1	
I_{INJPAD}	SR	Injected input current on any pin during overload condition	—	–5	5	mA
I_{INJSUM}	SR	Absolute sum of all injected input currents during overload condition	—	–50	50	
TV_{DD}	SR	$V_{DD\_HV\_A}$ slope to ensure correct power up(8)	—	—	0.5	V/µs
			—	0.5	—	V/min
T_{A} C-Grade Part	SR	Ambient temperature under bias	—	–40	85	°C
T_{J} C-Grade Part	SR	Junction temperature under bias	—	–40	110	
T_{A} V-Grade Part	SR	Ambient temperature under bias	—	–40	105	
T_{J} V-Grade Part	SR	Junction temperature under bias	—	–40	130	
T_{A} M-Grade Part	SR	Ambient temperature under bias	—	–40	125	
T_{J} M-Grade Part	SR	Junction temperature under bias	—	–40	150	

1. 100 nF EMI capacitance need to be provided between each VDD/VSS_HV pair.
2. Full device operation is guaranteed by design from 3.0 V–5.5 V. OSC functionality is guaranteed from the entire range 3.0V–5.5 V, the parametrics measured are at 3.0V and 5.5V (extreme voltage ranges to cover the range of operation). The parametrics might have some variation in the intermediate voltage range, but there is no impact to functionality.
3. 100 nF EMI capacitance needs to be provided between each VDD_LV/VSS_LV supply pair. 10 µF bulk capacitance needs to be provided as CREG on each VDD_LV pin.
4. This voltage is internally generated by the device and no external voltage should be supplied.
5. 100 nF capacitance needs to be provided between $V_{DD\_HV\_(ADC0/ADC1)}$/$V_{SS\_HV\_(ADC0/ADC1)}$ pair.
6. Both the relative and the fixed conditions must be met. For instance: If $V_{DD\_HV\_A}$ is 5.9 V, $V_{DD\_HV\_ADC0}$ maximum value is 6.0 V then, despite the relative condition, the max value is $V_{DD\_HV\_A}$ + 0.3 = 6.2 V.
7. PA3, PA7, PA10, PA11 and PE12 ADC_1 channels are coming from $V_{DD\_HV\_B}$ domain hence VDD_HV_ADC1 should be within ±100 mV of $V_{DD\_HV\_B}$ when these channels are used for ADC_1.

Table 16. SLOW configuration output buffer electrical characteristics (continued)

Symbol		C	Parameter	Conditions[1],[2]		Value			Unit
						Min	Typ	Max	
V_{OL}	CC	P	Output low level SLOW configuration	Push Pull	I_{OL} = 3 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	$0.1V_{DD}$	V
		C			I_{OL} = 3 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 1[3]	—	—	$0.1V_{DD}$	
		P			I_{OL} = 1.5 mA, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	0.5	

1. V_{DD} = 3.3 V ± 10 % / 5.0 V ± 10 %, T_A = –40 to 125 °C, unless otherwise specified.
2. V_{DD} as mentioned in the table is $V_{DD\_HV\_A}$/$V_{DD\_HV\_B}$.
3. The configuration PAD3V5 = 1 when V_{DD} = 5 V is only a transient configuration during power-up. All pads but RESET and Nexus output (MDOx, EVTO, MCKO) are configured in input or in high impedance state.

Table 17. MEDIUM configuration output buffer electrical characteristics

Symbol		C	Parameter	Conditions[1],[2]		Value			Unit
						Min	Typ	Max	
V_{OH}	CC	C	Output high level MEDIUM configuration	Push Pull	I_{OH} = –3 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	$0.8V_{DD}$	—	—	V
		C			I_{OH} = –1.5 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 1[3]	$0.8V_{DD}$	—	—	
		C			I_{OH} = –2 mA, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	V_{DD} – 0.8	—	—	
V_{OL}	CC	C	Output low level MEDIUM configuration	Push Pull	I_{OL} = 3 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	$0.2V_{DD}$	V
		C			I_{OL} = 1.5 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 1[3]	—	—	$0.1V_{DD}$	
		C			I_{OL} = 2 mA, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	0.5	

1. V_{DD} = 3.3 V ± 10 % / 5.0 V ± 10 %, T_A = –40 to 125 °C, unless otherwise specified.
2. V_{DD} as mentioned in the table is $V_{DD\_HV\_A}$/$V_{DD\_HV\_B}$.
3. The configuration PAD3V5 = 1 when V_{DD} = 5 V is only a transient configuration during power-up. All pads but RESET and Nexus output (MDOx, EVTO, MCKO) are configured in input or in high impedance state.

Table 19. Output pin transition times (continued)

Symbol		C	Parameter	Conditions[1],[2]		Value[3]			Unit
						Min	Typ	Max	
T_{tr}	CC	D	Output transition time output pin[4] FAST configuration	C_L = 25 pF	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	4	ns
				C_L = 50 pF		—	—	6	
				C_L = 100 pF		—	—	12	
				C_L = 25 pF	V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	4	
				C_L = 50 pF		—	—	7	
				C_L = 100 pF		—	—	12	

1. V_{DD} = 3.3 V ± 10 % / 5.0 V ± 10 %, T_A = –40 to 125 °C, unless otherwise specified.
2. V_{DD} as mentioned in the table is $V_{DD\_HV\_A}$/$V_{DD\_HV\_B}$.
3. All values need to be confirmed during device validation.
4. C_L includes device and package capacitances (C_{PKG} < 5 pF).

3.6.5 I/O pad current specification

The I/O pads are distributed across the I/O supply segment. Each I/O supply is associated to a V_{DD}/V_{SS_HV} supply pair as described in *Table 20*.

Table 21 provides I/O consumption figures.

In order to ensure device reliability, the average current of the I/O on a single segment should remain below the I_{AVGSEG} maximum value.

In order to ensure device functionality, the sum of the dynamic and static current of the I/O on a single segment should remain below the I_{DYNSEG} maximum value.

Table 20. I/O supplies

Package	I/O Supplies							
LBGA256[1]	Equivalent to 208-pin LQFP segment pad distribution + G6, G11, H11, J11							
LQFP208	pin6 ($V_{DD\_HV\_A}$) pin7 (V_{SS_HV})	pin27 ($V_{DD\_HV\_A}$)pin28 (V_{SS_HV})	pin73 (V_{SS_HV}) pin75 ($V_{DD\_HV\_A}$)	pin101 ($V_{DD\_HV\_A}$) pin102 (V_{SS_HV})	pin132 (V_{SS_HV}) pin133 ($V_{DD\_HV\_A}$)	pin147 (V_{SS_HV}) pin148 ($V_{DD\_HV\_B}$)	pin174 (V_{SS_HV}) pin175 ($V_{DD\_HV\_A}$)	—
LQFP176	pin6 ($V_{DD\_HV\_A}$) pin7 (V_{SS_HV})	pin27 ($V_{DD\_HV\_A}$)pin28 (V_{SS_HV})	pin57 (V_{SS_HV}) pin59 ($V_{DD\_HV\_A}$)	pin85 ($V_{DD\_HV\_A}$) pin86 (V_{SS_HV})	pin123 (V_{SS_HV}) pin124 ($V_{DD\_HV\_B}$)	pin150 (V_{SS_HV}) pin151 ($V_{DD\_HV\_A}$)	—	—

1. VDD_HV_B supplies the IO voltage domain for the pins PE[12], PA[11], PA[10], PA[9], PA[8], PA[7], PE[13], PF[14], PF[15], PG[0], PG[1], PH[3], PH[2], PH[1], PH[0], PG[12], PG[13], and PA[3].

Table 23. Voltage regulator electrical characteristics (continued)

Symbol		C	Parameter	Conditions[1]	Value[2]			Unit
					Min	Typ	Max	
I_{MREG}	SR	—	Main regulator current provided to V_{DD_LV} domain	—	—	—	350	mA
$I_{MREGINT}$	CC	D	Main regulator module current consumption	I_{MREG} = 200 mA	—	—	2	mA
				I_{MREG} = 0 mA	—	—	1	
V_{LPREG}	CC	P	Low power regulator output voltage	After trimming T_A = 25 °C	1.17	1.27	1.32	V
I_{LPREG}	SR	—	Low power regulator current provided to V_{DD_LV} domain	—	—	—	50	mA
$I_{LPREGINT}$	CC	D	Low power regulator module current consumption	I_{LPREG} = 15 mA; T_A = 55 °C	—	—	600	µA
		—		I_{LPREG} = 0 mA; T_A = 55 °C	—	20	—	
$I_{VREGREF}$	CC	D	Main LVDs and reference current consumption (low power and main regulator switched off)	T_A = 55 °C	—	2	—	µA
$I_{VREDLVD12}$	CC	D	Main LVD current consumption (switch-off during standby)	T_A = 55 °C	—	1	—	µA
$I_{DD\_HV\_A}$	CC	D	In-rush current on V_{DD_BV} during power-up	—	—	—	600 (3)	mA

1. $V_{DD\_HV\_A}$ = 3.3 V ± 10 % / 5.0 V ± 10 %, T_A = –40 to 125 °C, unless otherwise specified.
2. All values need to be confirmed during device validation.
3. Inrush current is seen more like steps of 600 mA peak. The startup of the regulator happens in steps of 50 mV in ~25 steps to reach ~1.2 V V_{DD_LV}. Each step peak current is within 600 mA

3.8.3 Voltage monitor electrical characteristics

The device implements a Power-on Reset module to ensure correct power-up initialization, as well as four low voltage detectors to monitor the $V_{DD\_HV\_A}$ and the V_{DD_LV} voltage while device is supplied:

- POR monitors $V_{DD\_HV\_A}$ during the power-up phase to ensure device is maintained in a safe reset state
- LVDHV3 monitors $V_{DD\_HV\_A}$ to ensure device is reset below minimum functional supply
- LVDHV5 monitors $V_{DD\_HV\_A}$ when application uses device in the 5.0 V±10 % range
- LVDLVCOR monitors power domain No. 1 (PD1)
- LVDLVBKP monitors power domain No. 0 (PD0). VDD_LV is same as PD0 supply.

Note: When enabled, PD2 (RAM retention) is monitored through LVD_DIGBKP.

1. All ESD testing is in conformity with CDF-AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits.
2. A device will be defined as a failure if after exposure to ESD pulses the device no longer meets the device specification requirements. Complete DC parametric and functional testing shall be performed per applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.
3. Data based on characterization results, not tested in production.

3.11.3.2 Static latch-up (LU)

Two complementary static tests are required on six parts to assess the latch-up performance:

- A supply over-voltage is applied to each power supply pin.
- A current injection is applied to each input, output and configurable I/O pin.

These tests are compliant with the EIA/JESD 78 IC latch-up standard.

Table 34. Latch-up results

Symbol	Parameter	Conditions	Class
LU	Static latch-up class	T_A = 125 °C conforming to JESD 78	II level A

3.12 Fast external crystal oscillator (4–40 MHz) electrical characteristics

The device provides an oscillator/resonator driver. *Figure 10* describes a simple model of the internal oscillator driver and provides an example of a connection for an oscillator or a resonator.

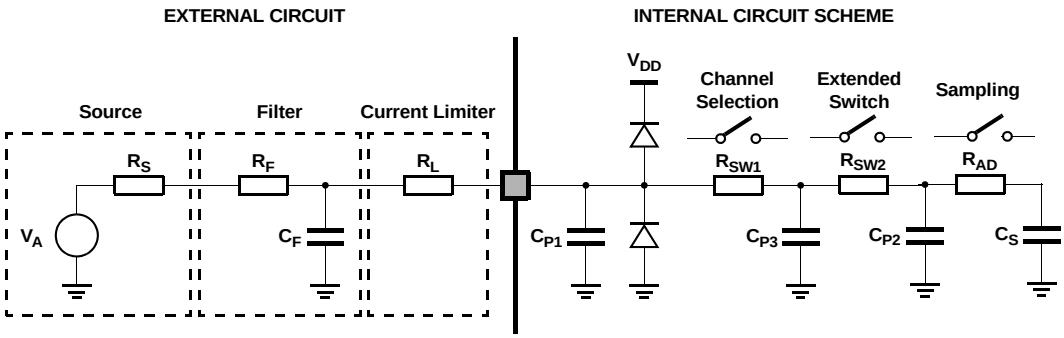
Table 35 provides the parameter description of 4 MHz to 40 MHz crystals used for the design simulations.

Table 40. Fast internal RC oscillator (16 MHz) electrical characteristics (continued)

Symbol		C	Parameter	Conditions[1]		Value[2]			Unit
						Min	Typ	Max	
$I_{FIRCRUN}$[3]	CC	T	Fast internal RC oscillator high frequency current in running mode	T_A = 25 °C, trimmed		—	—	200	µA
$I_{FIRCPWD}$	CC	D	Fast internal RC oscillator high frequency current in power down mode	T_A = 25 °C		—	—	100	nA
		D		T_A = 55 °C		—	—	200	nA
		D		T_A = 125 °C		—	—	1	µA
$I_{FIRCSTOP}$	CC	T	Fast internal RC oscillator high frequency and system clock current in stop mode	T_A = 25 °C	sysclk = off	—	500	—	µA
					sysclk = 2 MHz	—	600	—	
					sysclk = 4 MHz	—	700	—	
					sysclk = 8 MHz	—	900	—	
					sysclk = 16 MHz	—	1250	—	
T_{FIRCSU}	CC	C	Fast internal RC oscillator start-up time	T_A = 55 °C	V_{DD} = 5.0 V ± 10%	—	—	2.0	µs
		—			V_{DD} = 3.3 V ± 10%	—	—	5	
		—		T_A = 125 °C	V_{DD} = 5.0 V ± 10%	—	—	2.0	
		—			V_{DD} = 3.3 V ± 10%	—	—	5	
$\Delta_{FIRCPRE}$	CC	C	Fast internal RC oscillator precision after software trimming of f_{FIRC}	T_A = 25 °C		–1	—	+1	%
$\Delta_{FIRCTRIM}$	CC	C	Fast internal RC oscillator trimming step	T_A = 25 °C		—	1.6		%
$\Delta_{FIRCVAR}$	CC	C	Fast internal RC oscillator variation over temperature and supply with respect to f_{FIRC} at T_A = 25 °C in high-frequency configuration	—		–5	—	+5	%

1. V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified.
2. All values need to be confirmed during device validation.
3. This does not include consumption linked to clock tree toggling and peripherals consumption when RC oscillator is ON.

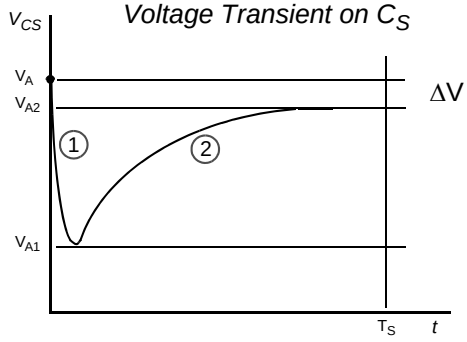
Figure 17. Input equivalent circuit (extended channels)



R_S Source Impedance
R_F Filter Resistance
C_F Filter Capacitance
R_L Current Limiter Resistance
R_{SW} Channel Selection Switch Impedance (two contributions R_{SW1} and R_{SW2})
R_{AD}Sampling Switch Impedance
C_P Pin Capacitance (three contributions, C_{P1}, C_{P2} and C_{P3})
C_S Sampling Capacitance

A second aspect involving the capacitance network shall be considered. Assuming the three capacitances C_F, C_{P1} and C_{P2} initially charged at the source voltage V_A (refer to the equivalent circuit reported in *Figure 16*): when the sampling phase is started (A/D switch close), a charge sharing phenomena is installed.

Figure 18. Transient behavior during sampling phase



$\Delta V < 0.5$ LSB

$\tau_1 < (R_{SW} + R_{AD})\, C_S << T_S$

$\tau_2 = R_L\,(C_S + C_{P1} + C_{P2})$

In particular two different transient periods can be distinguished:

- A first and quick charge transfer from the internal capacitance C_{P1} and C_{P2} to the sampling capacitance C_S occurs (C_S is supposed initially completely discharged): considering a worst case (since the time constant in reality would be faster) in which C_{P2} is reported in parallel to C_{P1} (call $C_P = C_{P1} + C_{P2}$), the two capacitances C_P and C_S are in series, and the time constant is

Equation 5

$$\tau_1 = (R_{SW} + R_{AD}) \bullet \frac{C_P \bullet C_S}{C_P + C_S}$$

This relation can again be simplified considering C_S as an additional worst condition. In reality, transient is faster, but the A/D converter circuitry has been designed to be robust also in very worst case: the sampling time T_s is always much longer than the internal time constant.

Equation 6

$$\tau_1 < (R_{SW} + R_{AD}) \bullet C_S \ll T_S$$

The charge of C_{P1} and C_{P2} is redistributed on C_S,determining a new value of the voltage V_{A1} on the capacitance according to the following equation

Equation 7

$$V_{A1} \bullet (C_S + C_{P1} + C_{P2}) = V_A \bullet (C_{P1} + C_{P2})$$

A second charge transfer involves also C_F (that is typically bigger than the on-chip capacitance) through the resistance RL: again considering the worst case in which C_{P2} and C_S were in parallel to C_{P1} (since the time constant in reality would be faster), the time constant is:

Equation 8

$$\tau_2 < R_L \bullet (C_S + C_{P1} + C_{P2})$$

In this case, the time constant depends on the external circuit: in particular imposing that the transient is completed well before the end of sampling time T_S, a constraints on R_L sizing is obtained:

Equation 9

$$8.5 \bullet \tau_2 = 8.5 \bullet R_L \bullet (C_S + C_{P1} + C_{P2}) < T_S$$

Of course, R_L shall be sized also according to the current limitation constraints, in combination with R_S (source impedance) and R_F (filter resistance). Being C_F definitively bigger than C_{P1}, C_{P2} and C_S, then the final voltage V_{A2} (at the end of the charge transfer transient) will be much higher than V_{A1}. The following equation must be respected (charge balance assuming now C_S already charged at V_{A1}):

Equation 10

$$V_{A2} \bullet (C_S + C_{P1} + C_{P2} + C_F) = V_A \bullet C_F + V_{A1} \bullet (C_{P1} + C_{P2} + C_S)$$

The two transients above are not influenced by the voltage source that, due to the presence of the R_FC_F filter, is not able to provide the extra charge to compensate the voltage drop on C_S with respect to the ideal source V_A; the time constant R_FC_F of the filter is very high with respect to the sampling time (T_S). The filter is typically designed to act as anti-aliasing

Table 43. ADC conversion characteristics (10-bit ADC_0) (continued)

Symbol		C	Parameter	Conditions[1]		Value			Unit
						Min	Typ	Max	
R_{SW2}	CC	D	Internal resistance of analog source	—		—	—	2	kΩ
R_{AD}	CC	D	Internal resistance of analog source	—		—	—	2	kΩ
I_{INJ}[7]	SR	—	Input current Injection	Current injection on one ADC_0 input, different from the converted one	V_{DD} = 3.3 V ± 10%	–5	—	5	mA
					V_{DD} = 5.0 V ± 10%	–5	—	5	
| INL |	CC	T	Absolute value for integral non-linearity	No overload		—	0.5	1.5	LSB
| DNL |	CC	T	Absolute differential non-linearity	No overload		—	0.5	1.0	LSB
| OFS |	CC	T	Absolute offset error	—		—	0.5	—	LSB
| GNE |	CC	T	Absolute gain error	—		—	0.6	—	LSB
TUEP	CC	P	Total unadjusted error[8] for precise channels, input only pins	Without current injection		–2	0.6	2	LSB
		T		With current injection		–3		3	
TUEX	CC	T	Total unadjusted error[8] for extended channel	Without current injection		–3	1	3	LSB
		T		With current injection		–4		4	

1. V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified.
2. Analog and digital V_{SS_HV} must be common (to be tied together externally).
3. V_{AINx} may exceed V_{SS_ADC0} and V_{DD_ADC0} limits, remaining on absolute maximum ratings, but the results of the conversion will be clamped respectively to 0x000 or 0x3FF.
4. During the sample time the input capacitance C_S can be charged/discharged by the external source. The internal resistance of the analog source must allow the capacitance to reach its final voltage level within t_{ADC0_S}. After the end of the sample time t_{ADC0_S}, changes of the analog input voltage have no effect on the conversion result. Values for the sample clock t_{ADC0_S} depend on programming.
5. This parameter does not include the sample time t_{ADC0_S}, but only the time for determining the digital result and the time to load the result's register with the conversion result.
6. Refer to ADC conversion table for detailed calculations.
7. PB10 should not have any current injected. It can disturb accuracy on other ADC_0 pins.
8. Total Unadjusted Error: The maximum error that occurs without adjusting Offset and Gain errors. This error is a combination of Offset, Gain and Integral Linearity errors.

Figure 20. ADC_1 characteristic and error definitions

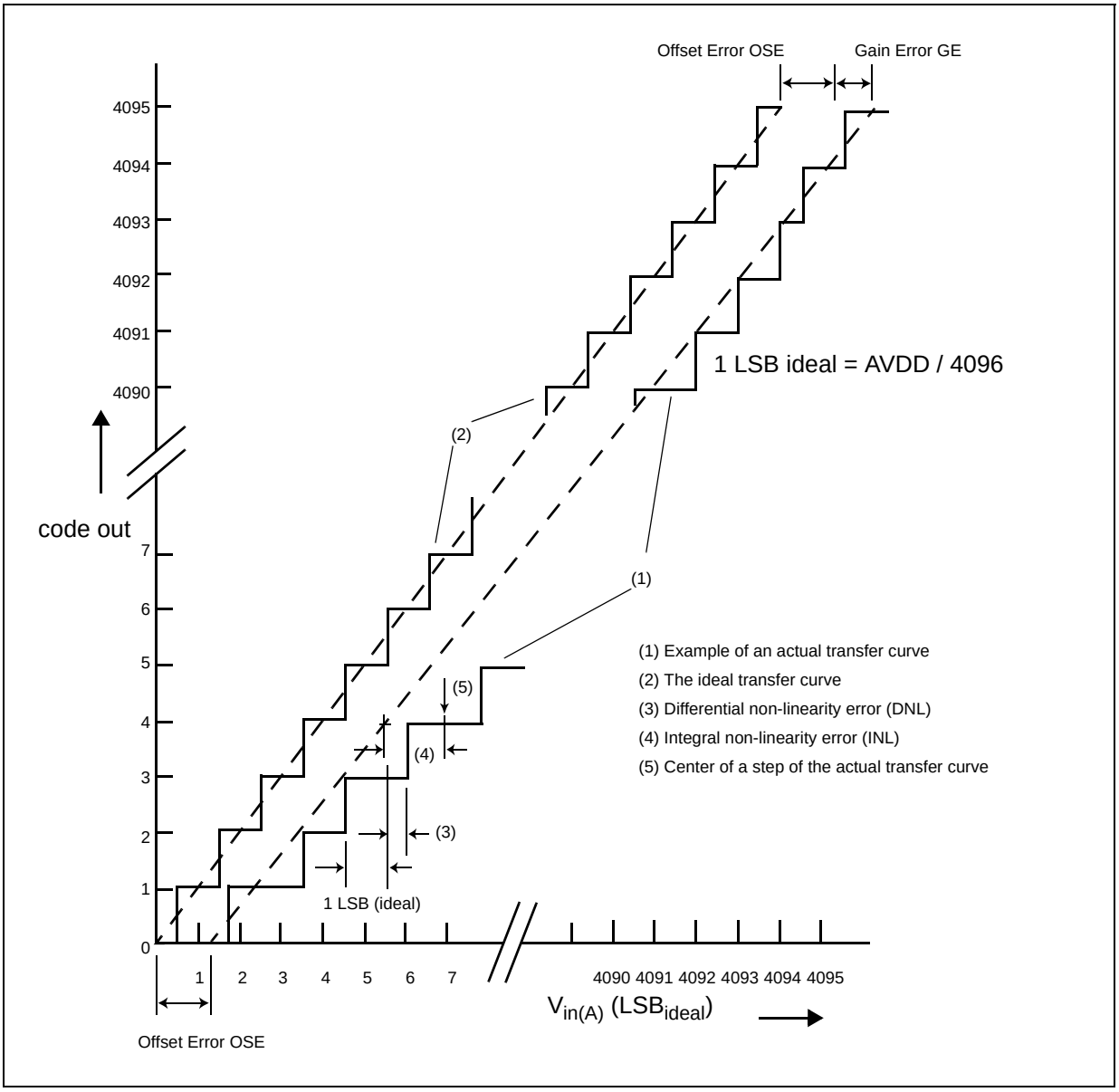
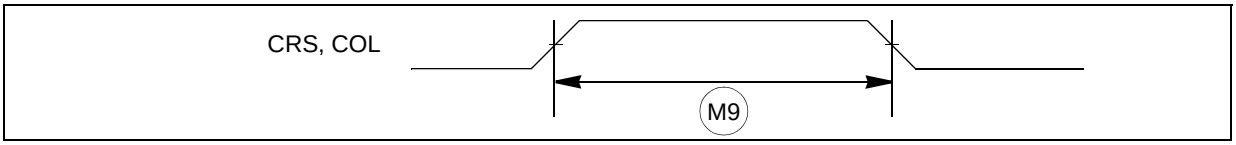


Table 44. Conversion characteristics (12-bit ADC_1) (continued)

Symbol		C	Parameter	Conditions[1]		Value			Unit
						Min	Typ	Max	
C_{P3}	CC	D	ADC_1 input pin capacitance 3	—			1.5		pF
R_{SW1}	CC	D	Internal resistance of analog source	—				1	kΩ
R_{SW2}	CC	D	Internal resistance of analog source	—				2	kΩ
R_{AD}	CC	D	Internal resistance of analog source	—				0.3	kΩ
I_{INJ}	SR	—	Input current Injection	Current injection on one ADC_1 input, different from the converted one	V_{DD} = 3.3 V ± 10%	–5	—	5	mA
					V_{DD} = 5.0 V ± 10%	–5	—	5	
INLP	CC	T	Absolute Integral non-linearity-Precise channels	No overload			1	3	LSB
INLS	CC	T	Absolute Integral non-linearity-Standard channels	No overload			1.5	5	LSB
DNL	CC	T	Absolute Differential non-linearity	No overload			0.5	1	LSB
OFS	CC	T	Absolute Offset error	—			2		LSB
GNE	CC	T	Absolute Gain error	—			2		LSB
TUEP[9]	CC	P	Total Unadjusted Error for precise channels, input only pins	Without current injection		–6		6	LSB
		T		With current injection		–8		8	LSB
TUES[9]	CC	T	Total Unadjusted Error for standard channel	Without current injection		–10		10	LSB
		T		With current injection		–12		12	LSB

1. V_{DD} = 3.3 V ± 10 % / 5.0 V ± 10 %, T_A = –40 to 125 °C, unless otherwise specified.
2. Analog and digital V_{SS_HV} must be common (to be tied together externally).

Figure 23. MII async inputs timing diagram



3.18.4 MII Serial Management Channel Timing (MDIO and MDC)

The FEC functions correctly with a maximum MDC frequency of 2.5 MHz.

Table 48. MII serial management channel timing(1)

Spec	Characteristic	Min	Max	Unit
M10	MDC falling edge to MDIO output invalid (minimum propagation delay)	0	—	ns
M11	MDC falling edge to MDIO output valid (max prop delay)	—	25	ns
M12	MDIO (input) to MDC rising edge setup	28	—	ns
M13	MDIO (input) to MDC rising edge hold	0	—	ns
M14	MDC pulse width high	40%	60%	MDC period
M15	MDC pulse width low	40%	60%	MDC period

1. Output pads configured with SRE = 0b11.

Figure 24. MII serial management channel timing diagram

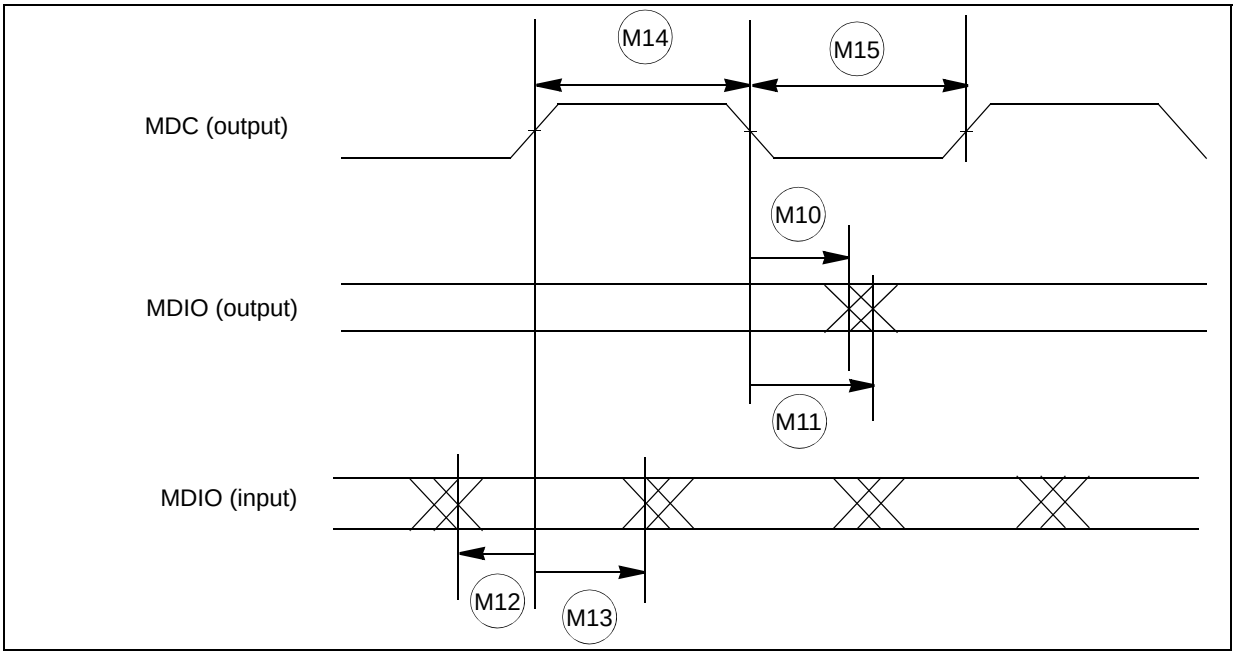
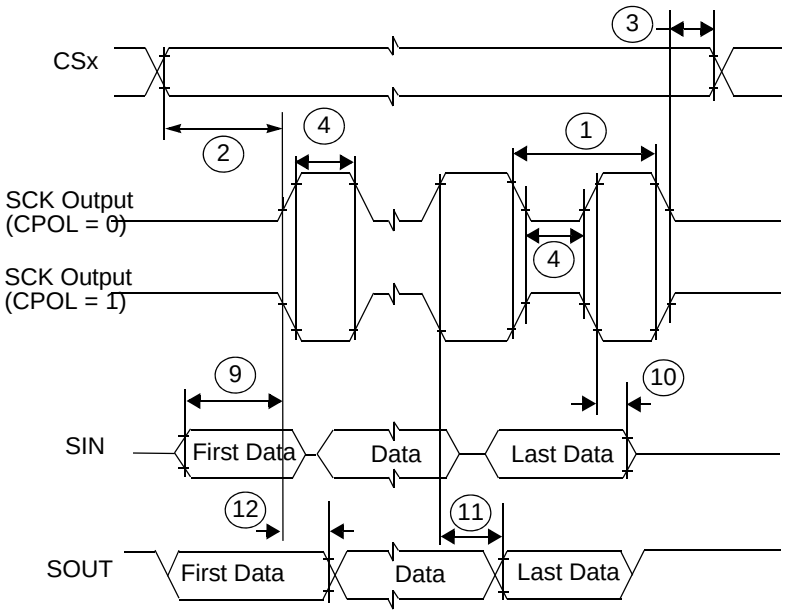
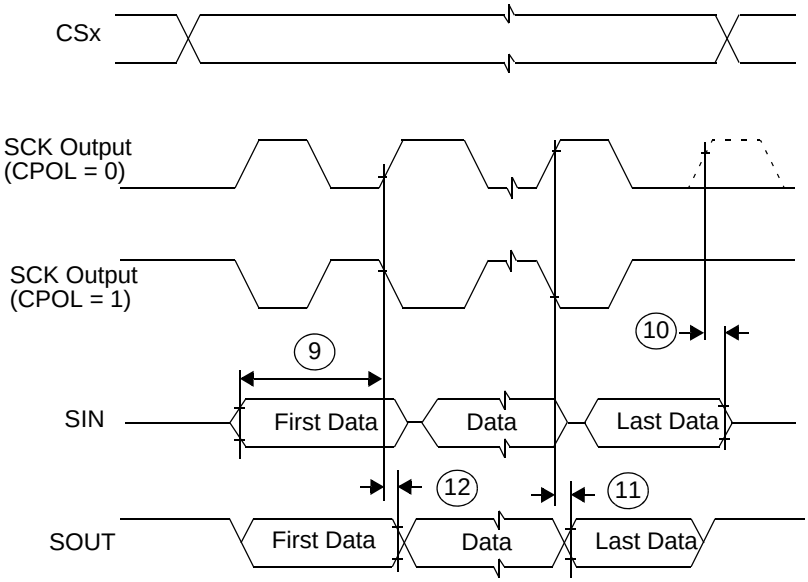


Figure 29. DSPI modified transfer format timing–master, CPHA = 0



Note: Numbers shown reference *Table 50*.

Figure 30. DSPI modified transfer format timing–master, CPHA = 1



Note: Numbers shown reference *Table 50*.

Table 57. Revision history (continued)

Date	Revision	Changes
04-Mar-2013	5 (cont.)	– Updated the min, max and typical values of $V_{LVDLVCORL}$ and $V_{LVDLVBKPL}$ in *Table 24: Low voltage monitor electrical characteristics* – Updated values of gmFXOSC in *Table 36: Fast external crystal oscillator (4 to 40 MHz) electrical characteristics* – Updated values of gmSXOSC in *Table 38: Slow external crystal oscillator (32 kHz) electrical characteristics* – Updated the footnote 5 for T_{ADC0_C} in *Table 43: ADC conversion characteristics (10-bit ADC_0)* – Updated the footnotes of *Table 25: Low voltage power domain electrical characteristics*
17-Sep-2013	6	– Updated Disclaimer
28-Nov-2014	7	– Removed occurrences of 208BGA from *Table 2: SPC564Bxx and SPC56ECxx family comparison*. – Added PM[3] and PM[4] in the figure note 1 of *Figure 4: 256-pin BGA configuration*. – Added a table note in*Table 20: I/O supplies*. – Updated *Figure 8: Voltage regulator capacitance connection* and added a note in this figure. – Removed before trimming value for V_{MREG}, updated after trimming min value of V_{MREG} from 1.24 V to 1.20 V, updated after trimming min value of V_{LPREG} from 1.225 V to 1.17 V, updated after trimming typical value of V_{LPREG} from 1.25 V to 1.27 V and updated after trimming max value of V_{LPREG} from 1.275 V to 1.32 V in *Table 23: Voltage regulator electrical characteristics*. – Changed min value of $V_{LVDLVCORL}$ and $V_{LVDLVBKPL}$ from 1.12 V to 1.08 V, and removed typical value of $V_{LVDLVCORL}$ and $V_{LVDLVBKPL}$ in *Table 24: Low voltage monitor electrical characteristics* – Updated max values at 120 MHz for I_{DDRUN} from 200 mA to 208 mA and from 270 mA to 280 mA; updated max value at T_A = 125 °C for I_{DDHALT} from 80 mA to 100 mA; updated max value at T_A = 25 °C for I_{DDSTOP} from 1.2 mA to 5 mA and at T_A = 125 °C from 60 mA to 72 mA; updated max value at T_A = 25 °C for $I_{DDSTDBY3}$ from 75 µA to 96 µA and at T_A = 125 °C from 1200 µA to 2400 µA; updated max value at T_A = 25 °C for $I_{DDSTDBY2}$ from 70 µA to 92 µA and at T_A = 125 °C from 1100 µA to 2000 µA; updated max value at T_A = 25 °C for $I_{DDSTDBY1}$ from 65 µA to 85 µA and at T_A = 125 °C from 650 µA to 1100 µA; updated 1st footnote in *Table 25: Low voltage power domain electrical characteristics*. – Added a footnote below *Table 29: Flash memory read access timing*. – Updated the formula in Eq. 11 in *Section 3.17.1.1: Input impedance and ADC accuracy*. – Updated legend in *Figure 16: Input equivalent circuit (precise channels)* – Updated min and max values for g_{mFXOSC} at V_{DD} = 5.0 V ± 10% from 4 mA/V to 6.5 mA/V and from 20 mA/V to 25 mA/V in *Table 36: Fast external crystal oscillator (4 to 40 MHz) electrical characteristics* – Added *Figure 17: Input equivalent circuit (extended channels)*. – Updated t_{ADC0_PU} value to 1.5 as max and added footnote for I_{INJ} in *Table 43: ADC conversion characteristics (10-bit ADC_0)*.